CyberPro2010

Data Sheet

"The Internet Multimedia Company!"

Revision 1.A1F

CyberPro2010

Data Sheet

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IGS Technologies, Inc.
4001 Burton Drive
Santa Clara, CA 95054
Phone (408) 982-8588
FAX (408) 982-8591
http://www.igst.com

Table of Contents

Table of Contents

1. Features Overview

1.1 World's First TV Direct™ Output

- Integrated TV Encoder for Direct NTSC/PAL
- Only requires a single crystal for NTSC/PAL
- NTSC(640x480,60Hz), PAL(800x600/640x480,50Hz)
- Simultaneous S-video, composite & AMD SCART TV
- Simultaneous VGA & TV

1.2 VL Bus Interface

- Direct Interface to 486 Embedded Processors via VL bus, including AMD Elan 400/410

1.3 DuoVision™ Dual Display Support

- DuoVision provides simultaneous display of graphics on VGA while playing MPEG movies on TV

1.4 64-bit GUI, 128/64/32-bit EDO Interface

- 64-bit GUI engine, 200mhz RAMDAC, dual clock
- Supports EDO DRAM from 1MB up to 4MB

1.5 Flexible Video Inputs

- VBI data including Intercast, teletext, CC support
- CCIR656/8-bit video input interface

1.6 Support for Video Games on TV

- Shadow registers provide complete compatibility for popular DOS, Windows, and other video games on TV

1.7 RGB/Composite/S-video/AMD SCART TV

- Six DAC's on-chip to support TV RGB, Composite, S-video and AMD SCART outputs
- Best Text, Video quality for composite underscan TV output using 3-line buffers, Interpolation, 9-bit DAC for 8/16/24-bit colors
- Flicker control bypass for best video quality on TV
- Higher precision PLL to work with any TV world wide

1.8 MPEG Movie Playback on TV

- MPEG-2 movie playback on TV using H/W MPEG-2 decoders/players
- DirectDraw MPEG-1 playback on TV with S/W
- High quality horizontal and vertical interpolation with jagged edge smoothing

1.9 Video Editing/Phone/Video Conferencing on TV

- Three scaleable video windows plus PIP
- Direct input from TV tuner, analog & digital camera via IGS video port and decoder ASIC
- High quality multitap filtering during video capture
- Mirror/upside down support for video conferencing

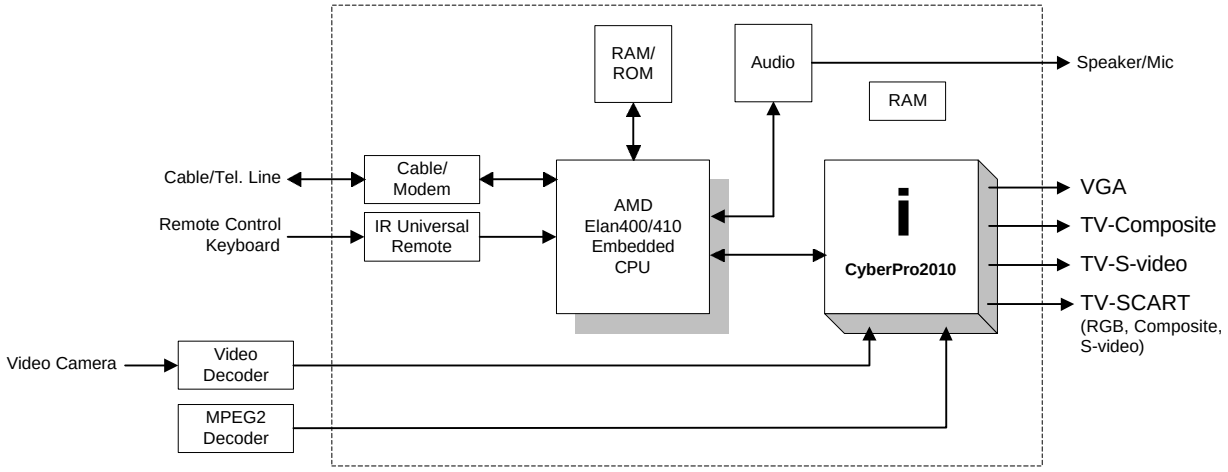

Figure 1-1. System Block Diagram Example

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2. Features Description

2.1 Integrated Bridge, GUI & Encoder

The CyberPro2010 is the FIRST and ONLY multimedia accelerator that integrates three major components of an NC/SetTop/Internet Appliance/TV design; namely, CPU Bridge, GUI and video Accelerator, and NTSC/PAL TV Encoder.

In addition, the CyberPro2010 integrates high speed 200 MHz RAMDAC and clock.

The CyberPro2010 has a 64-bit GUI multimedia accelerator which interfaces to true single cycle SDRAM, SGRAM and EDO DRAM frame buffer sizes from 1MB to 4MB. It provides VGA output up to 1600x1200 resolutions for enterprise NC applications.

2.2 Flicker-Free TVDirect™ Output

The TVDirect™ feature incorporates an on-chip NTSC/PAL TV encoder which has a proprietary flicker free technology with a 3-line buffer. It provides the best TV quality for the majority of TV's worldwide, where composite input is the norm with its underscan interpolation techniques, high precision PLL and 9-bit DAC.

Also, SetTops can be designed with several glueless connectors directly from the CyberPro2010 for simultaneous connections, including VGA, RGB at TV frequency, SCART, S-video and Composite TV outputs.

2.3 World's First FlexiBus™ Interface

The flexuous feature incorporates the CPU bridge functions for most of the embedded CPU's which are designed into NC's, SetTops and Internet appliances. As indicated in Table 2-1, the CyberPro2010 has a glueless CPU bus interface to all PCI, VL bus and RISC CPU's, like IBM and Motorola PowerPC, NEC V83X, Hitachi SHX and ESS ES3208.

In addition, any other RISC CPU can be interfaced through the non-multiplexed linear VL bus interfaced on-chip. This lowers the total BOM for an Internet appliance to a cost lower than any competitive solution on the market.

2.4 DuoVision™ Dual Display Support

The DuoVision™ feature, unique to the CyberPro2010, enables simultaneous display on TV of video (DVD, MPEG, karaoke or video conferencing) and VGA graphics.

2.5 Video Capture and Playback Output

The CyberPro2010 provides the best quality video capture and playback output on TV of any single chip solution, by using its multi-tap filters, interpolation techniques and multiple hardware windows capability. These features are very important for SetTop designs which require DVD or MPEG output on TV or video conferencing capability where the CyberPro2010 can interface directly to DVD decoders (connected to DVD drives, players or satellite equipment) or video decoders (connected to analog or digital cameras, or a VCR).

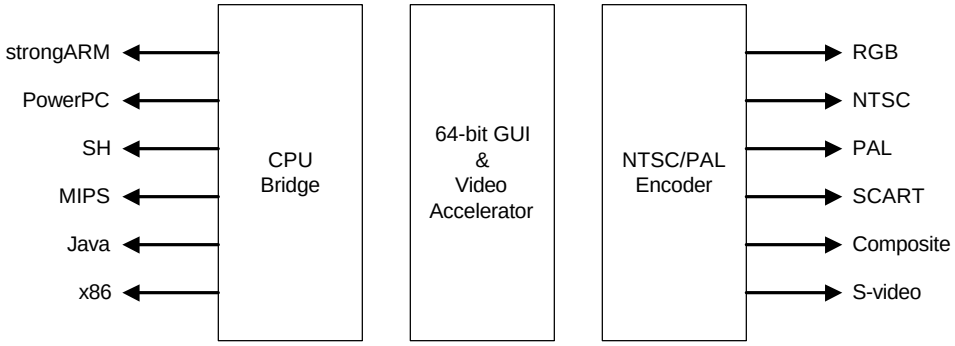

Figure 2-1: Block Diagram

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3. VL Bus Information

- Faster memory means higher performance for the CyberPro2010, allowing use of EDO and FPM DRAM of 35-60ns.
- For VL bus configuration, the memory bus bandwidth is always 32-bit for 1MB and 2MB.

3.1 AMD Elan4XX CPU Interfaces

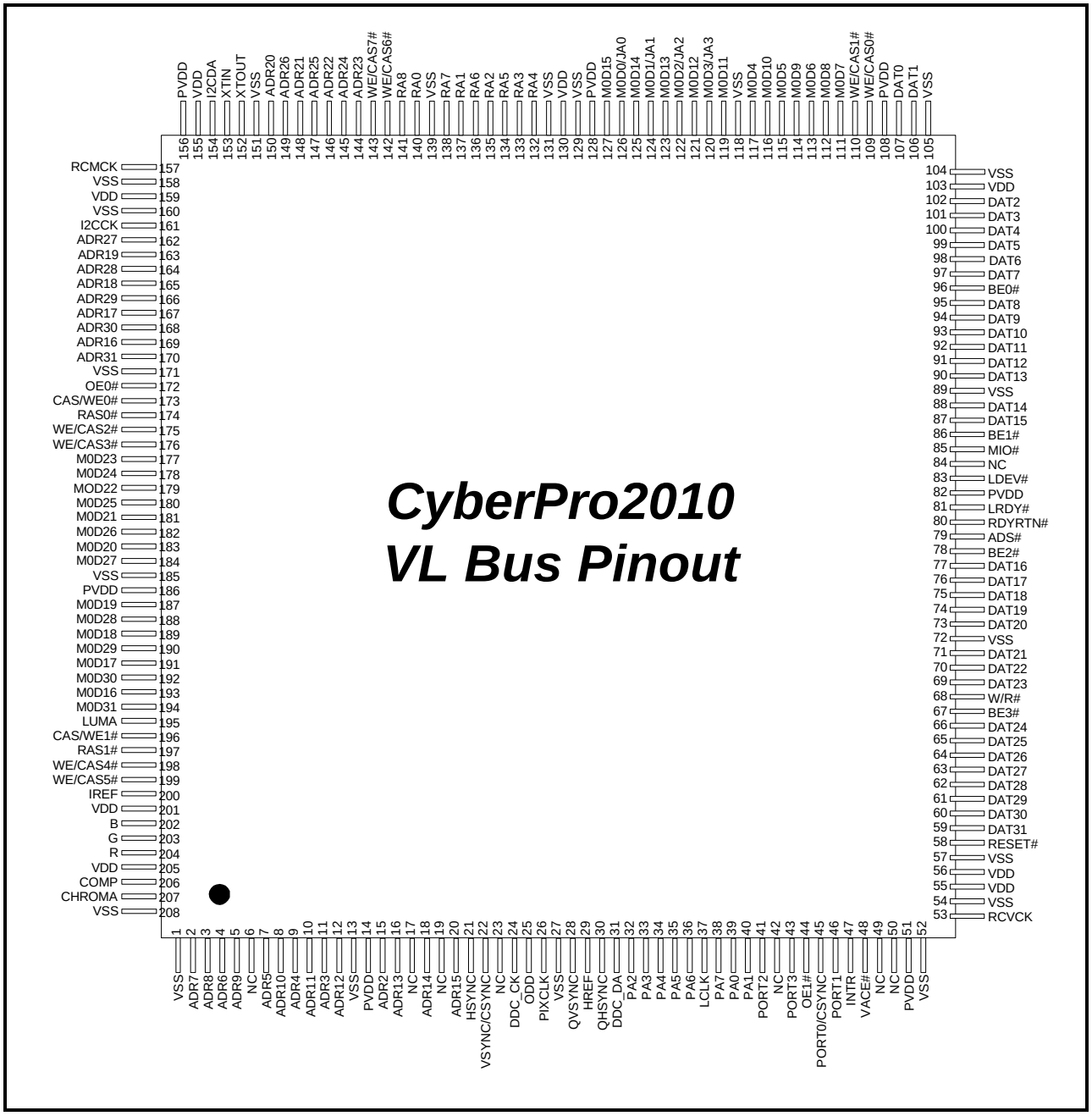
ADR[31:2]	ADS#	W/R#	LRDY#
CS#/AUX[1:0]	LDEV#	RDYTRN#	INTR
DAT[31:0]	LCLK	MIO#	RESET#
BE[3:0]#			

3.2 Power-up Bus Type Configuration

All memory addresses from RA8 to RA0 have an internal power-down.

RA2	RA1	RA0	Bus Type
1	0	0	VL Standard
1	0	1	VL Linear Address

3.3 VL Pin Description



3.4 VL Pin Description Tables

3.4.1 Host Interface (VL)

Name	Type	Pin No.	Description
ADR[31:2]	I/O	170,168,166,164, 162,149,147,145, 144,146,148,150, 163,165,167,169, 20,18,16,12,10,8, 5,3,2,4,7,9,11,15	The address bus furnishes the physical memory or I/O port addresses to the VL bus target.
LCLK	I	37	The system input clock signal.
INTR	O	47	Used to request an interrupt to the system.
RESET#	I	58	System reset. During power-up or a hardware reset, this signal must be at a logic low for at least 1ms. When this signal is low, the CyberPro2010 is in a reset state, all the pins are inactive, and the memory data bus is tri-state.
DAT[31:0]	I/O	59,60,61,62,63, 64,65,66,69,70, 71,73,74,75,76, 77,87,88,90,91, 92,93,94,95,97, 98,99,100,101, 102,106,107	Data bus. This is a bi-directional data path between VL bus devices and the CPU.
BE[3:0]#	I/O	67,78,86,96	Byte enable. The byte enables indicate which byte lanes of the 32-bit data bus are involved with the current VL bus transfer.
W/R#	I/O	68	Writer or read status. This CPU output indicates the type of access currently executing on the VL bus.
ADS#	I/O	79	Address data strobe. ADS# indicates the start of the VL bus cycle.
RDYRTN#	I/O	80	Ready return. RDYRTN# establishes a handshake so the VL bus target knows when the cycle has ended.
LRDY#	I/O	81	Local ready. LRDY# begins the handshake that terminates the current active bus cycle when the target is not bursting.
LDEV#	I/O	83	Device select. LDEV# is an active low output signal that responds to the current access, which means it is a valid cycle for the CyberPro2010.
MIO#	I/O	85	Memory or I/O status. This CPU output indicates the type of access currently executing on the VL bus.

3.4.2 Memory Interface (VL)

Name	Type	Pin No.	Description
OE1#	O	44	Output enable.
WE/CAS[7:0]#	O	143,142,199,198, 176,175,110,109	Used to control different banks of memory.
M0D[31:0]	I/O	194,192,190,188, 184,182,180,178, 177,179,181,183, 187,189,191,193, 127,125,123,121, 119,116,114,112, 111,113,115,117, 120,122,124,126	Used to transfer data between DRAM and the CyberPro2010.
RA[8:0]	O	141,138,136, 134,132,133, 135,137,140,	Output address pins to DRAM.
OE0#	O	172	Output enable. Used to control output enable to the DRAM.
CAS/WE[1:0]#	O	196,173	Each of these signals is used to control one bank of DRAM.
RAS[1:0]#	O	197,174	ROW ADDRESS STROBE[1:0]# is used to control the DRAM RAS# signal.

3.4.3 Miscellaneous (VL)

Name	Type	Pin No.	Description
NC		6,17,19,23,42,49,50, 84	No connection.
PORT2	I/O	41	Port I/O programmable pin.
PORT3	I/O	43	Port I/O programmable pin.
PORT0/ CSYNC	I/O	45	Port I/O programmable pin/composite sync for TV.
PORT1	I/O	46	Port I/O programmable pin.
RCVCK	I	53	RC filter for internal DOT clock.
XTOUT	O	152	An output loop back pin for a crystal.
XTIN	I	153	An input pin for a crystal.
I2CDA	I/O	154	I^2C bus serial data input/output.
RCMCK	I	157	RC memory clock. An input from the memory clock RC network to control the memory frequency.
I2CCK	I/O	161	I^2C bus serial clock input/output.
IREF	O	200	DAC reference current.

3.4.4 Power (VL)

Name	Type	Pin No.	Description
VSS	I	1,13,27,52,54,57,72, 89,104,105,118, 129,131,139,151, 158,160,171,185, 208	0.0V
PVDD	I	14,51,82,108,128, 156,186	I/O pad power, 3.3/5.0V.
VDD	I	55,56,103,130,155, 159,201,205	+5.0V.

3.4.5 Video Port Interface (VL)

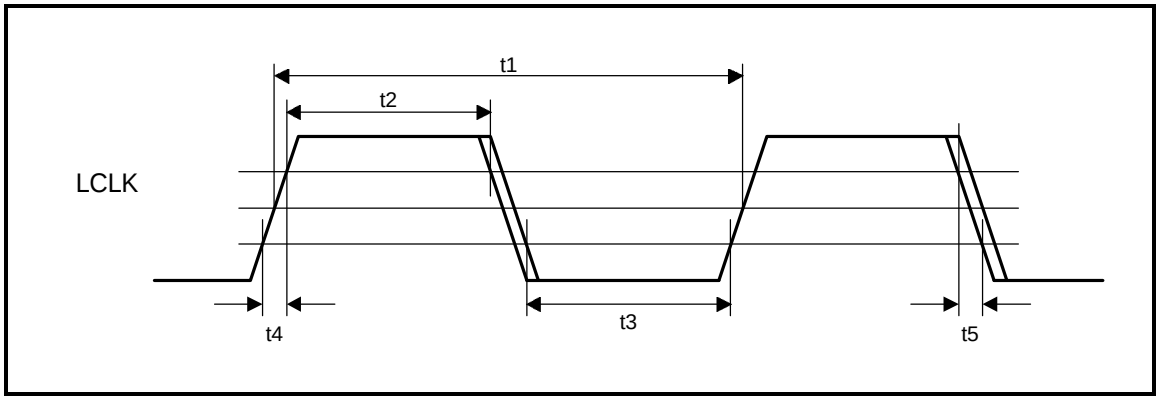
Name	Type	Pin No.	Description
ODD	I/O	25	Odd/even field ID.
PIXCLK	I/O	26	Video port clock.
QVSYNC	I/O	28	Vertical sync for video port.
QHSYNC	I/O	30	Video port horizontal reference or sync.
HREF	I/O	29	Horizontal Reference.
PA[7:0]	I/O	38,36-32,40,39	Video port data.
VACE#	O	48	Video port enable.

3.4.6 CRT & TV Interface (VL)

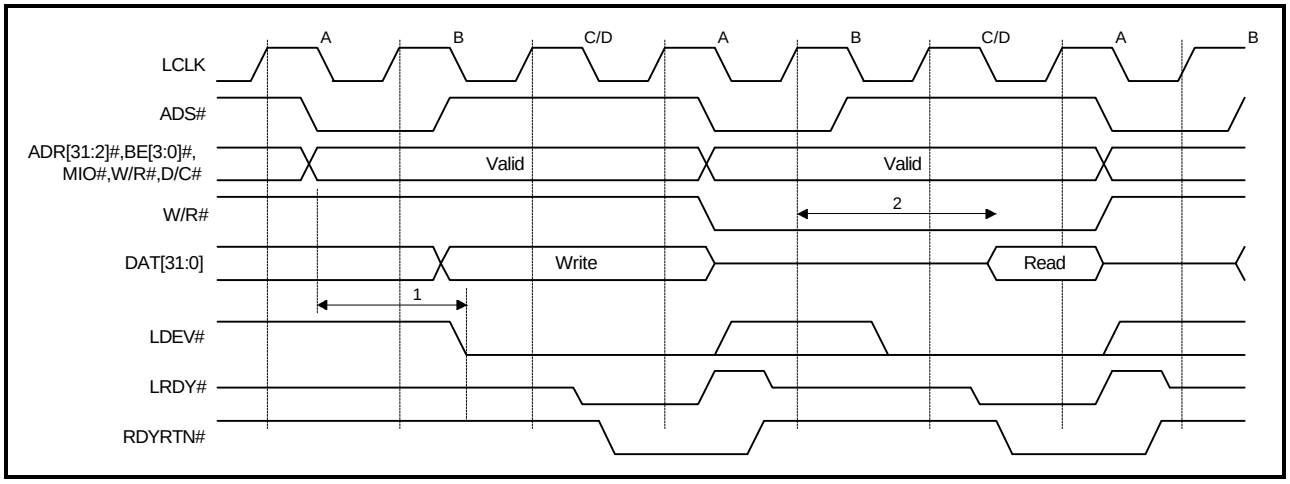
Name	Type	Pin No.	Description
HSYNC	O	21	HSYNC to CRT/fast switch (SCART).
VSYNC/ CSYNC	O	22	VSYNC to CRT; composite sync to TV.
DDC_CK	I/O	24	DDC2B clock.
DDC_DA	I/O	31	DDC2B data.
LUMA	O	195	Luminance output/TV blue.
B	O	202	Blue analog output connected to the monitor/TV blue.
G	O	203	Green analog output connected to the monitor/TV green.
R	O	204	Red analog output connected to the monitor/TV red.
COMP	O	206	Composite video output/TV red.
CHROMA	O	207	Chrominance output//TV green.

3.5 VL Timing Diagrams

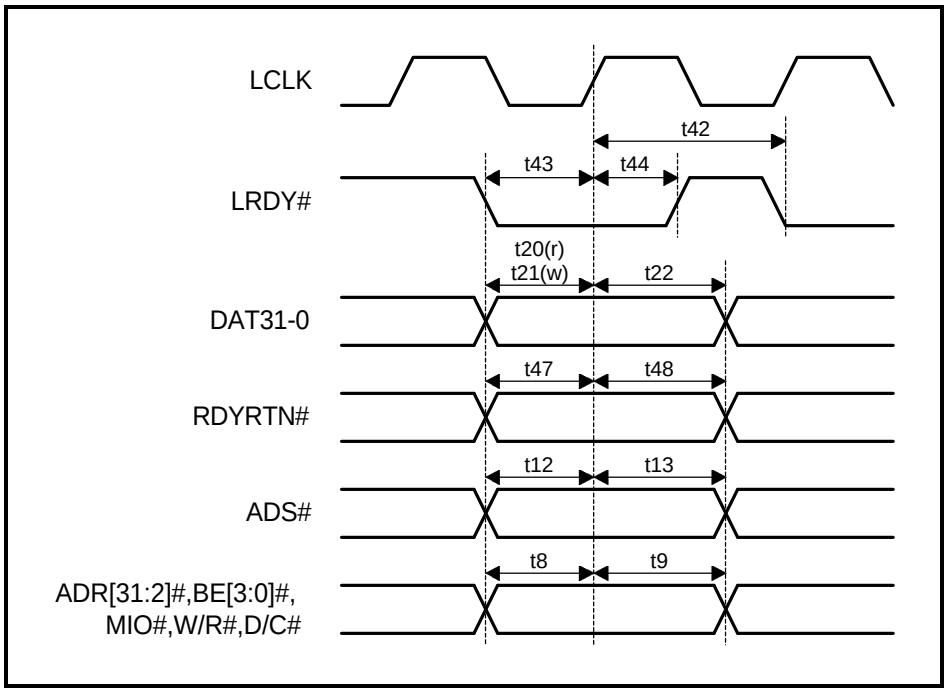
3.5.1 VL Bus LCLK Timing



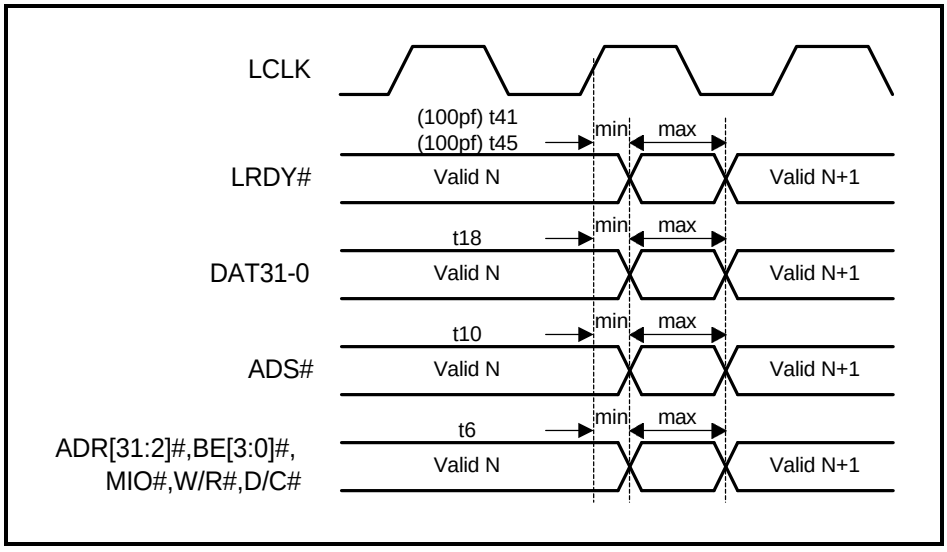
3.5.2 VL Bus Write and Read Cycle



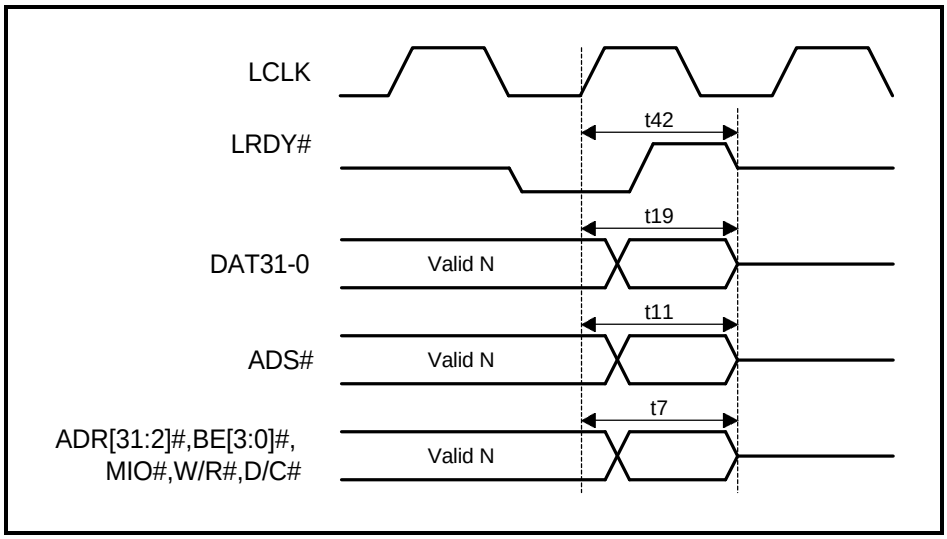
3.5.3 VL Bus Input Setup and Hold Timing



3.5.4 VL Bus Output Valid Delay Timing



3.5.5 VL Bus Output Float Delay Timing



4. Addressing Modes

4.1 Legend for Decode Tables

#	0 or one range
x	Don't Care
C	RISC processor chip select (active low)
$	Binary range ($$$: from 0 to 7)
J	Jumper setting at power-up (JJJJ : M0D[3:0]

4.2 VL Linear Information

ADR[23:0]	ADR[31:24]
1st 1MB Memory	00JJ JJ00
2nd 1MB Memory	00JJ JJ00
Map I/O Write	00JJ JJ00
Map I/O Read BE0	00JJ JJ00
Map I/O Read BE1	00JJ JJ00
Map I/O Read BE2	00JJ JJ00
Map I/O Read BE3	00JJ JJ00
R/W Port [7:0]	00JJ JJ00
R/W TV 2K Byte	00JJ JJ00
COPREG R/W	00JJ JJ00
EPROM Read (R=0)	00JJ JJ00
COP Memory (R=1)	00JJ JJ00

4.2.1 Address Map

1. M0D[3:0] has internal pull-down.
2. At power-up, M0D[3:0] to decode the linear address.
3. M0D[3:0] is mapped to linear address A[29:26].
4. Process addresses A[31:30] and A[25:24] are always zero.
5. Example:
   At power-up, M0D[3:0] = 0101; then, linear address will be 0001,0100 or 14H.

4.2.2 VL Linear Address Decodes

ADR[23:0]	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1st 1MB Memory	0	0	0	0	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#	x	x
2nd 1MB Memory	0	0	0	1	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#	x	x
Map I/O Write	1	0	0	0	0	0	0	0	#	#	x	x	#	#	#	#	#	#	#	#	#	#	x	x
Map I/O Read BE0	1	0	0	0	0	0	0	0	#	#	0	0	#	#	#	#	#	#	#	#	#	#	x	x
Map I/O Read BE1	1	0	0	0	0	0	0	0	#	#	0	1	#	#	#	#	#	#	#	#	#	#	x	x
Map I/O Read BE2	1	0	0	0	0	0	0	0	#	#	1	0	#	#	#	#	#	#	#	#	#	#	x	x
Map I/O Read BE3	1	0	0	0	0	0	0	0	#	#	1	1	#	#	#	#	#	#	#	#	#	#	x	x
R/W Port [7:0]	1	0	0	0	1	0	1	%	1	1	0	$	$	$	#	#	#	#	#	#	#	#	0	0
R/W TV 2K Byte	1	0	0	0	1	0	1	%	1	1	1	0	x	#	#	#	#	#	#	#	#	#	0	0
COPREG R/W	1	0	0	0	1	0	1	%	1	1	1	1	#	#	#	#	#	#	#	#	#	#	0	0

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5. Frame Buffer Memory Timing

For memory timing parameters, refer to the manufacturer's data manual.

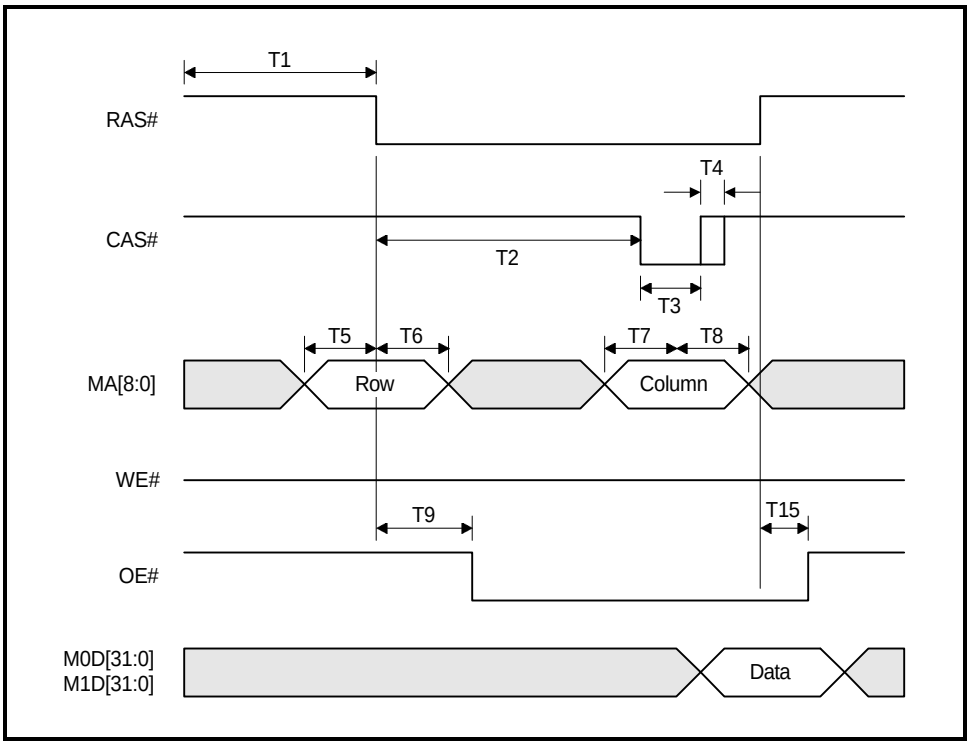
5.1 EDO/Fast Page Mode

All timing is relative to the memory clock (MCLK).

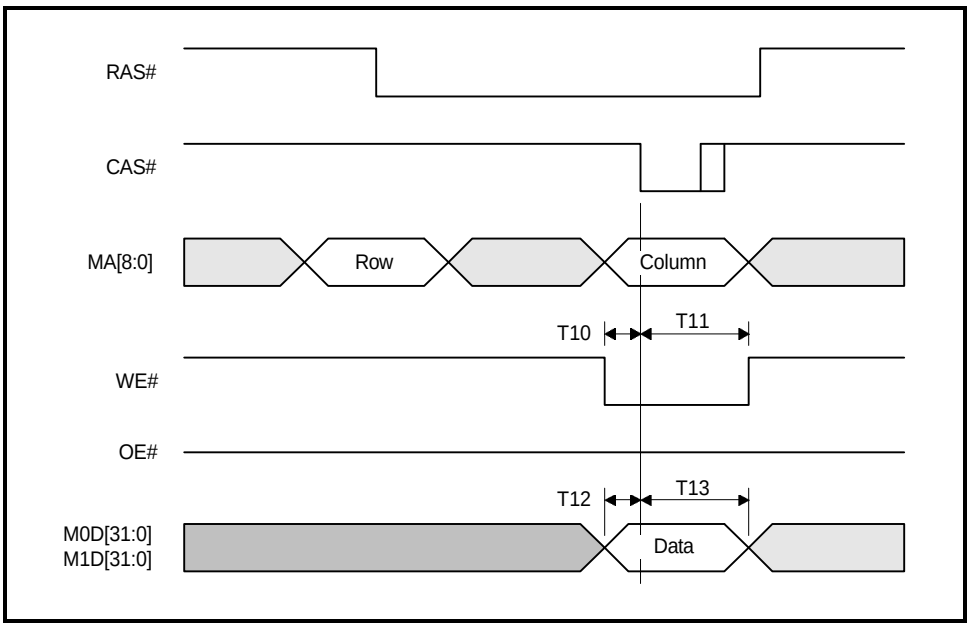
5.1.1 Read Cycle

Read data latch position relationship (small vertical rectangle in the diagram under T4):

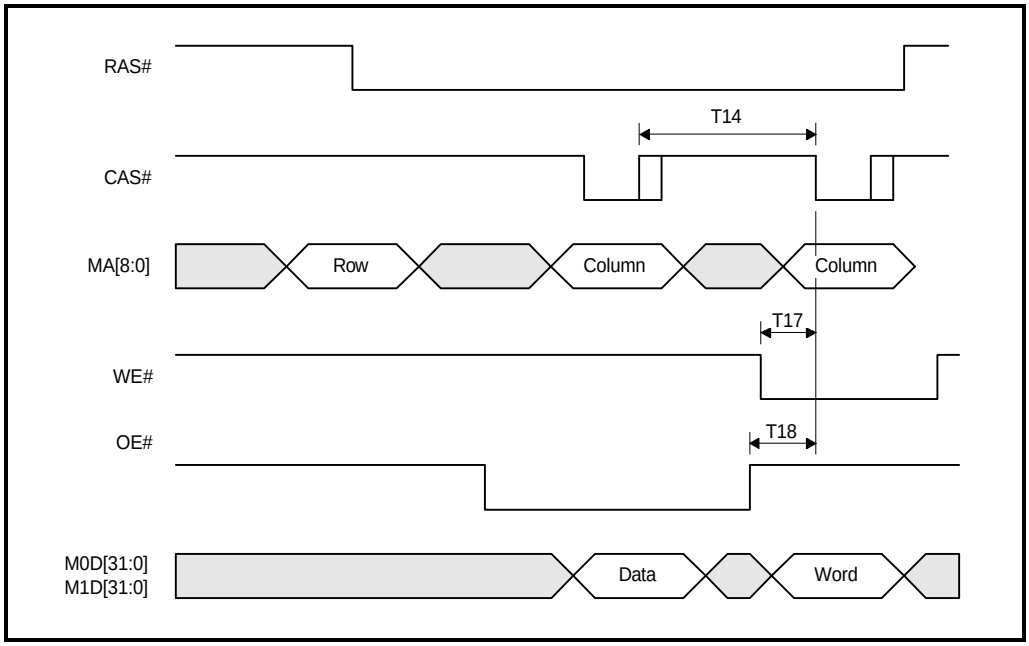
1. Coprocessor read (3CE.7A[7:6]): If the CAS wave form has been used for the memory read data latch, then 3CE.7A[6:5] controls the edge to latch the memory read data.
2. Other reads (3CE.79[5:4]): If the CAS wave form has been used for the memory read data latch, then 3CE.79[3:2] controls the edge to latch the memory read data.



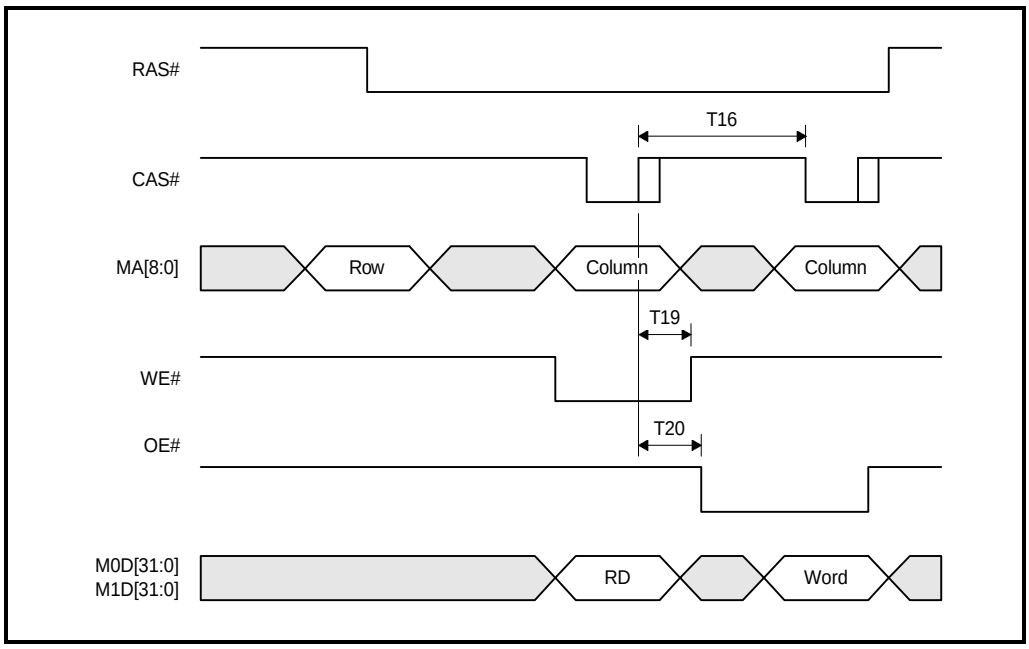
5.1.2 Write Cycle



5.1.3 Read-to-Write Cycle



5.1.4 Write-to-Read Cycle

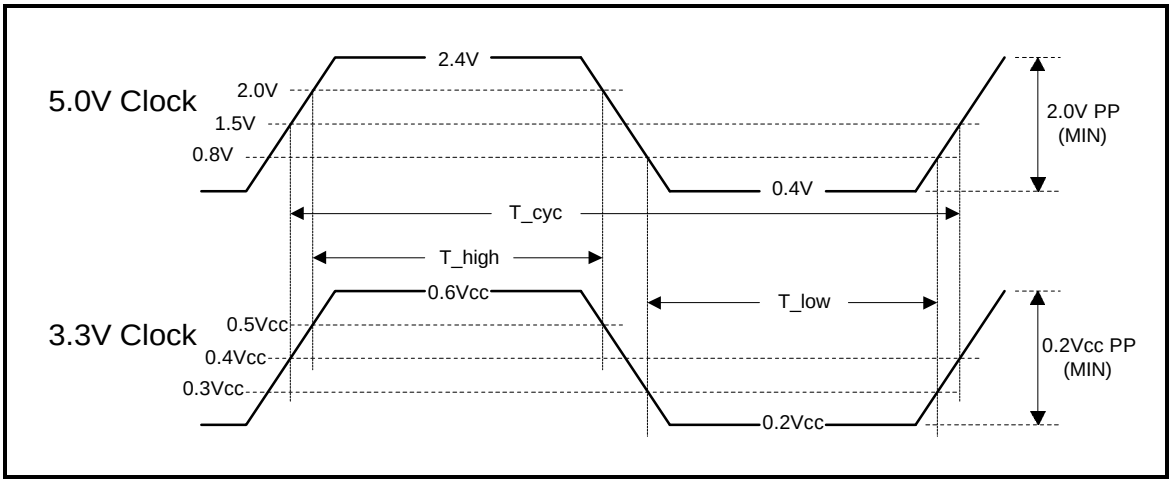


5.1.5 Timing Parameters

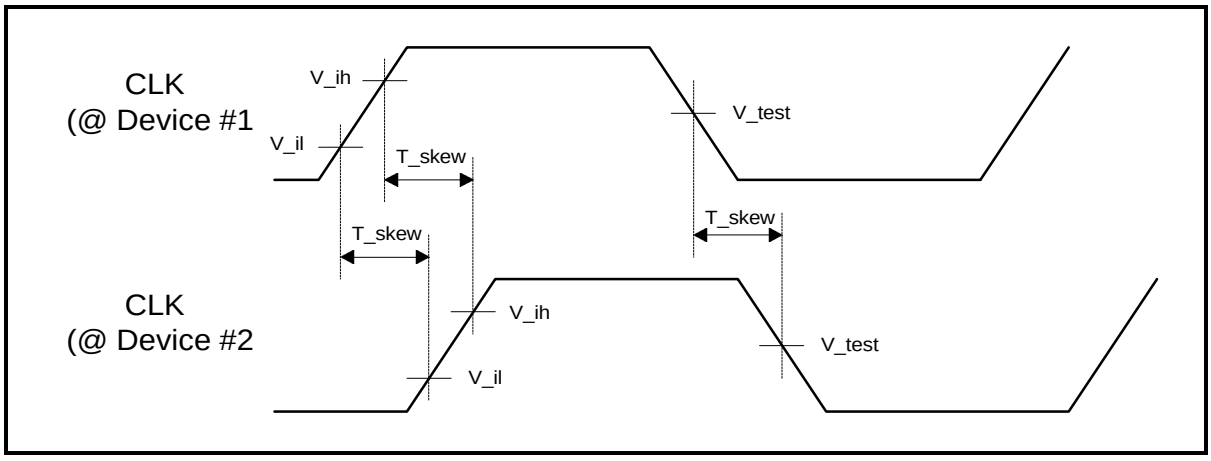
Symbol	T Periods (T = 1xMCLK)	Register[Bits]
T1	2.5-4T	3CE.70[0]; 3CE.70[1]
T2	2.5-4T	3CE.70[0]; 3CE.70[2]
T3	1T	Fixed
T4	0,2,4,6 ns	3CE.79[1:0]
T5	2.5-3T	3CE.70[0]
T6	2T	Fixed
T7	0.5-1T	3CE.F4[0]
T8	1-1.5T	3CE.F4[0]
T9	2-2.5T	3CE.70[0]
T10	0.5T	Fixed
T11	1.5T	Fixed
T12	0.5-1T	3CE.73[5]
T13	1-1.5T	Fixed
T14	1-3T	3CE.73[1]; 3CE.7A[0]
T15	1T	Fixed
T16	1-2T	3CE.7A[1]
T17	0.5-2.5T	3CE.F8[1:0]
T18	1-3T	3CE.F8[3:2]
T19	0.5T	Fixed
T20	1T	Fixed

5.2 Memory Timing Specifications

5.2.1 Clock Waveforms



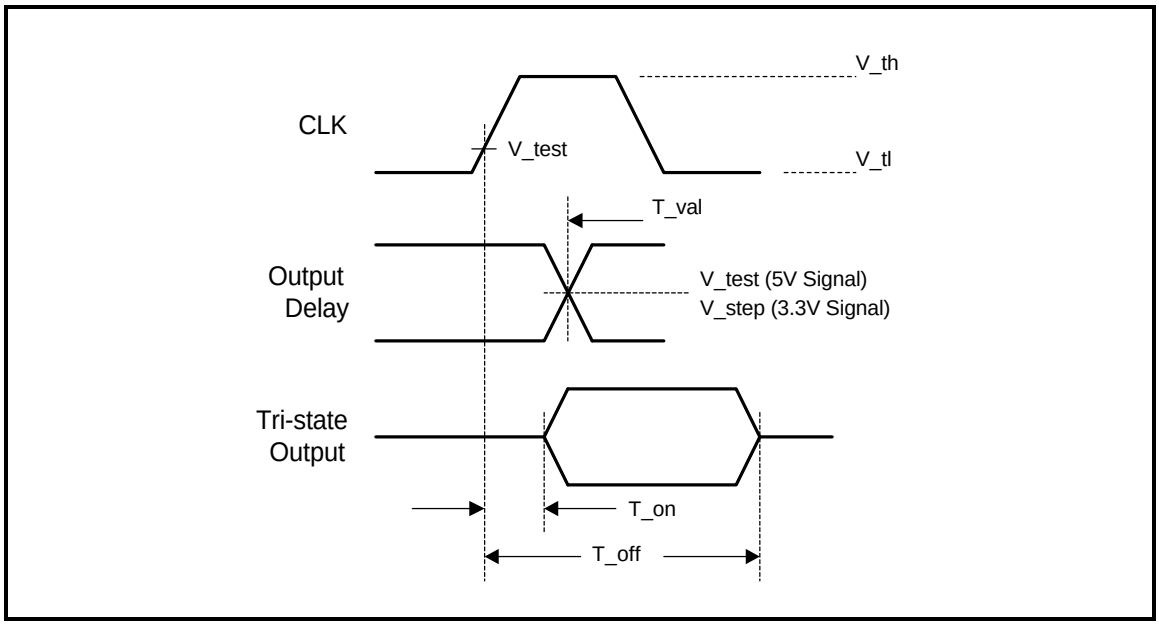
5.2.2 Clock Skew



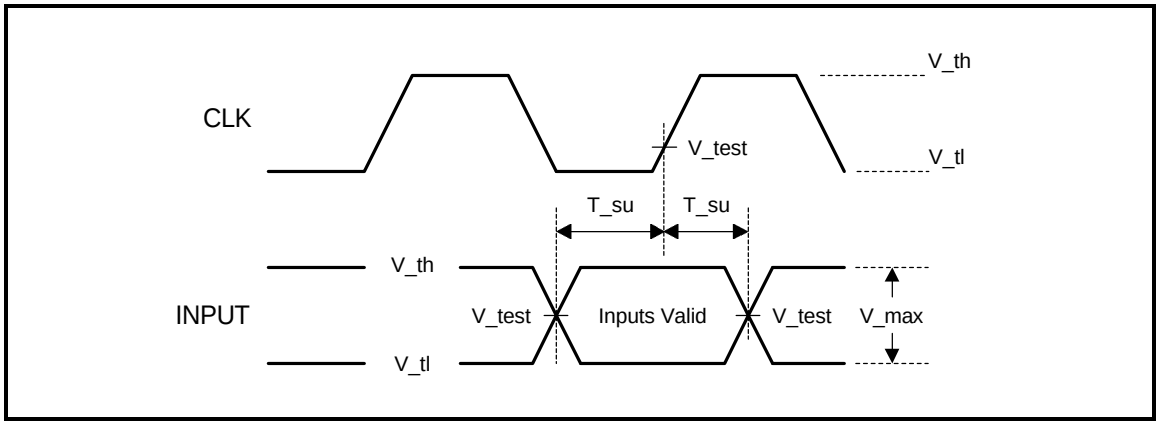
5.2.3 Clock Skew Parameters

Symbol	5.0V Signaling	3.3V Signaling	Units
V_test	1.5	0.4Vcc	V
T_skew	2 (max)	2 (max)	ns

5.2.4 Output Timing



5.2.5 Input Timing



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6. Electrical Characteristics

6.1 Absolute Maximum Ratings

Ambient temperature ..... 0°C to 55°C

Storage temperature..... -65°C to 150°C

Voltage on any digital pin..... -0.5V to Vcc + 0.5V

Power supply voltage..... -0.5V to 7.0V

Injection current (latch-up testing) 100mA

Note:

Stresses above those listed may cause permanent damage to the device. These are absolute stress ratings only. Functional operation at these or any conditions above those indicated in the operational ratings of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

6.2 DC Specifications (Digital)

(Vcc = 5V ± 5%, T_A = 0° to 70°C, unless otherwise specified.

Symbol	Parameter	MIN	MAX	Units	Test Conditions
IVcc	Internal Power Supply Voltage	4.75	5.25	V	5.0V Operation
BVcc	I/O Bus Interface Power Supply Voltage	4.75 3.0	5.75 3.6	V V	5.0V Bus Interface 3.3V Bus Interface
ICC	Power Supply Current		350	mA	MCLK = 50 MHz VCLK = 80MHZ
VIL	Input Low Voltage	0	0.8	V	
VIH	Input High Voltage	2.0	Vcc + 0.5	V	
VOL	Output Low Voltage		0.5	V	IOL = 16mA
VOH	Output High Voltage	2.4		V	IOH = -10mA
IOH	Output High Current		16	mA	VOH = 2.4V
IOL	Output Low Current		16	mA	VOL = 0.5V
IOZ	Input Leakage	-10	10	µA	0 < VIN < VCC
CIN	Input Capacitance		7	pF	
COUT	Output Capacitance		10	pF	

6.3 DAC Characteristics

(Vcc = 5V ± 5%, T_A = 0° to 70° C)

Parameter	MAX	Units	Test	Note
Resolution (each DAC)	8	Bits		
Output Current (White Level)	20	mA	VO <1V	1,2
Analog Output Rise/Fall Time	8	ns		4
Analog Output Settling Time	15	ns		5
Analog Output Skew	TBD	ns		
DAC-to-DAC Matching	5	%		
Glitch Impulse Typical	TBD	pV-Sec		
Integral Linearity Error	±1	LSB		
Differential Linearity Error	±1	LSB		

Notes:

1. IREF = 8.39mA.
2. Load is 37.5Ω and 10 pF per analog output.
3. TD is measured from the 50% point of VCLK to 50% point of full-scale transition.
4. Rise time is measured from 10% to 90% full-scale; fall time is measured from 90% to 10% full-scale.
5. Settling time is measured from 50% of full-scale transition to output remaining within 2% of final value.

7. Package Dimensions

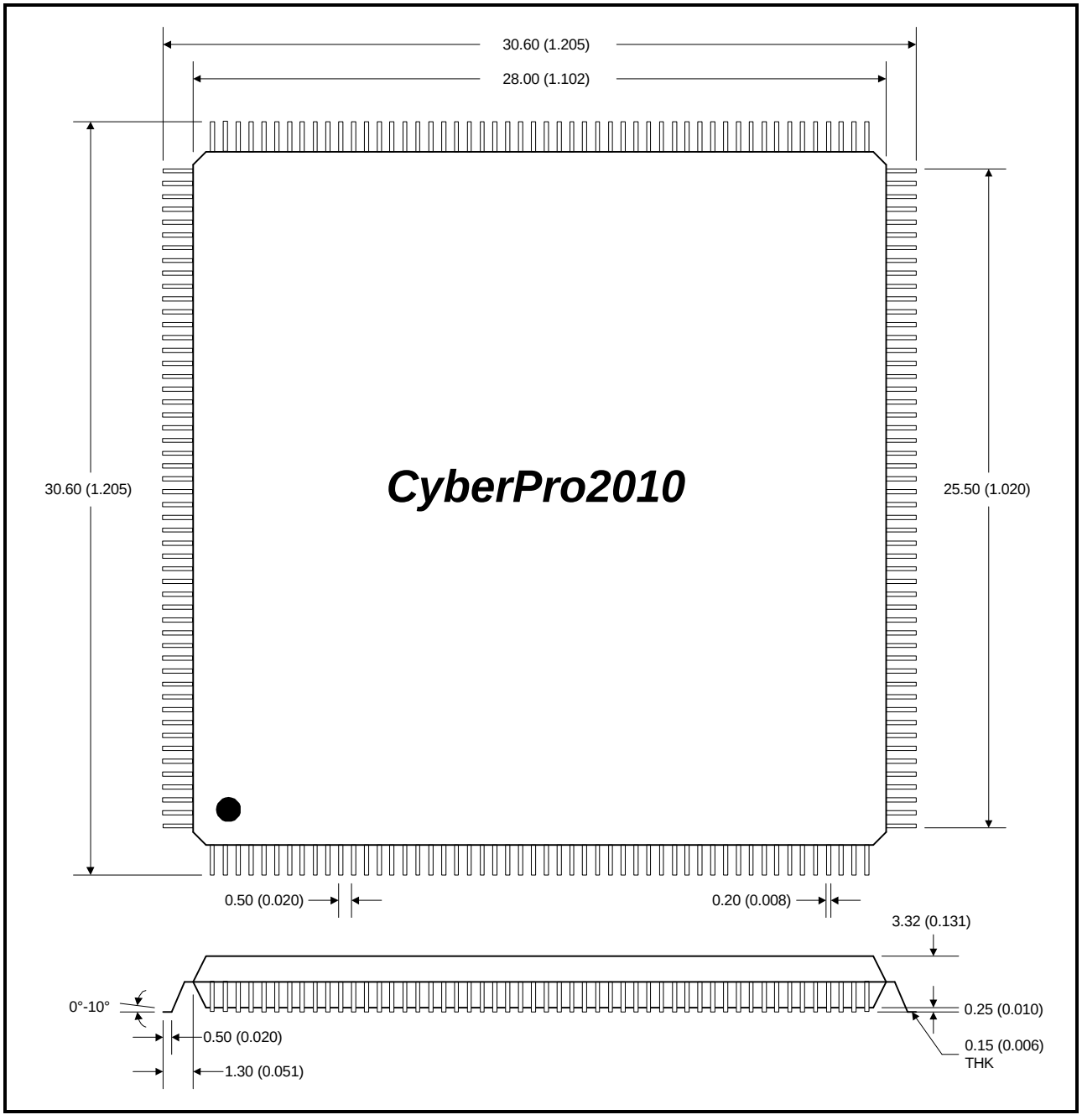

Figure 7-1. CyberPro2010 Physical Dimensions