

Date: 09/13/00

Re: Aspen CDP Board Rev. 1.3 - Board Issues/Errata

□ #1.3.1 Jumpers for routing the GP DMA signals to ISA DMA signals are mislabeled

Schematic Page 15

Problem The silkscreen for JP6, JP7, JP8, and JP9 is incorrect.

The signals DRQ0, DRQ1, DRQ2, and DRQ3 on JP6 and JP8 are incorrectly labeled as DRQ1, DRQ2, DRQ3, and DRQ4 respectively.

The signals DACK0#, DACK1#, DACK2#, and DACK3# on JP7 and JP9 are incorrectly labeled as DACK1#, DACK2#, DACK3#, and DACK4# respectively.

The labels ISA1 and ISA0 that identify the JP6/JP7 and JP8/JP9 jumper blocks are incorrect. They should be removed entirely.

JP6 should be labeled GPDRQ0, JP7 should be labeled GPDACK0, JP8 should be labeled GPDRQ1, and JP9 should be labeled GPDACK1.

Board Rework Solution

Relabel the jumper headers. Refer to figure 1.

Next CAD Solution

Change the silkscreen to correct the labeling error. It should appear exactly as the schematic indicates with the top-down view on page 15 (with the exception of the ISA0 and ISA1 labels being removed and the GPDACK0, GPDACK1, GPDRQ0, and GPDRQ1 labels being added). Refer to figure 1.

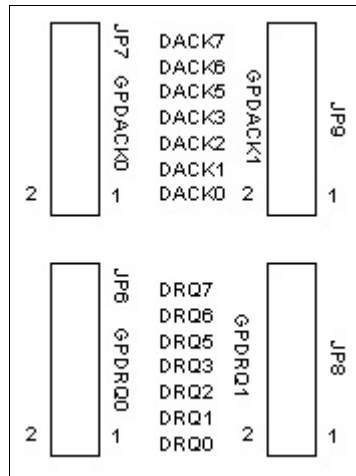


Figure 1

□ **#1.3.2a IDE DMA Does Not Function**

Schematic Pages 6 and 14

Problem DMA from the IDE interface does not work. The data transceiver, U23, is not enabled by the PAL, U4, during an IDE DMA transfer. In addition, the IDE Data Bit 7 is not activated properly during a DMA cycle.

To fix this problem, the PAL needs a signal indicating that an IDE DMA cycle is in progress. The equations for the data transceiver enable outputs on the PAL must be changed to activate the enable signals during an IDE DMA cycle. In addition, the IDE Data Bit 7 must be properly activated for read or write during an IDE DMA cycle.

Board Rework Solution

Remove U4 PAL.

Remove U4 PAL socket.

Cut trace from the VIA to U4-pin 9.

Replace U4 PAL socket.

Wire from the via indicated in Figure 2 to U4-pin 9. This puts the signal IDE DACK# onto pin 9 of the PAL for use in the equations.

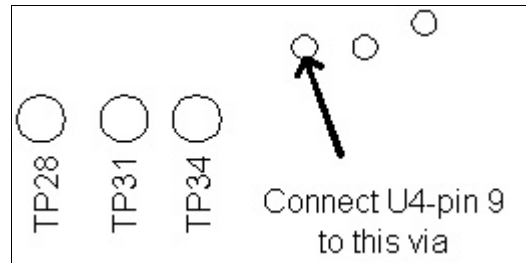


Figure 2

(This step is an alternative to the previous step, either connect from the via or from the backside of the board, but not both.) Wire from P4-pin 20 to U4-pin 9. Run the wire through the hole in the board for TP32, which is located right next to U4.

Reprogram the PAL with the Revision 1.3 Equations (*see rework 1.3.4*), which adds terms for asserting the missing IDE signals whenever IDEDACK# is asserted.

Next CAD Solution

Delete the signal GPAEN from the U4 PAL and instead put the signal IDEDACK# onto pin 9.

□ #1.3.3 Buffer for SDRAM Header Is Not Connected to VCC5

Schematic Page 20

Problem 16 of the 32 memory data signals are not visible on the SDRAM Header. The buffer (U44) that is connected between the SDRAM header (P7) and these signals is not connected to VCC5.

Pins 7, 18, 31, and 42 on U44 are connected to C221 and C222 through a trace that spans across the entire board. U44 should be utilizing C233 and C234 as its source of filtered power, as they are located near U44. The VCC5 side of these capacitors should be connected directly to pins 7, 18, 31, and 42 of U44 through a via. The VCC5 side of C221 and C222 should be connected to pins 7, 18, 31, and 42 of U43 (a buffer for the PCI Header) through a via, as they are local to that chip and should be used to filter its power.

Board Rework Solution

See figure 3.

Wire from U44 pin 42 via to VCC5 side of C233 and C234.

Wire from U43 pin 18 via to VCC5 side of C221.

Wire from U43 pin 42 via to VCC5 side of C222.

Next CAD Solution

Connect VCC5 to C221, C222, and U44 pins 7, 18, 31, and 42.

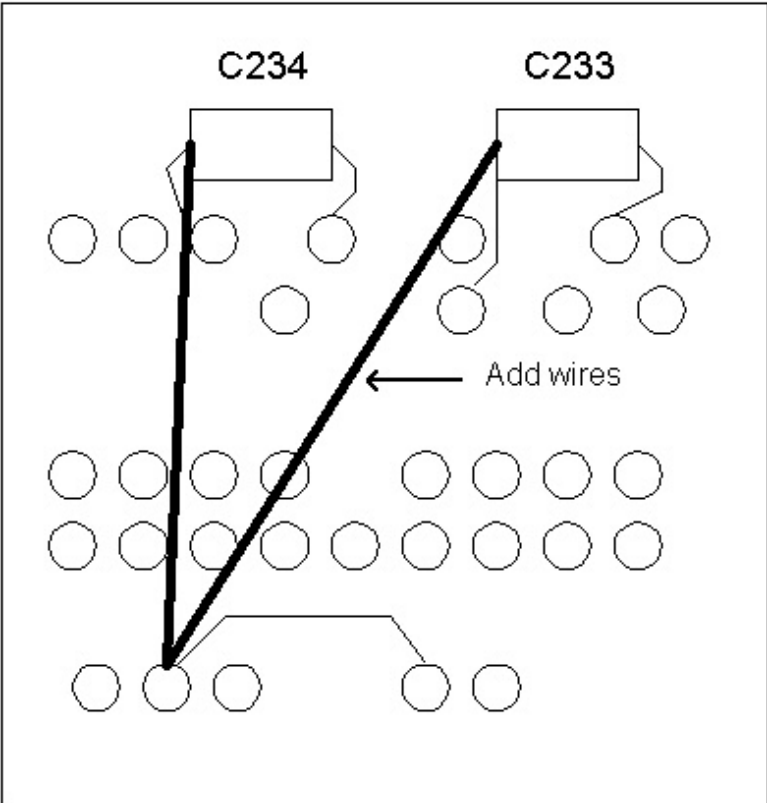
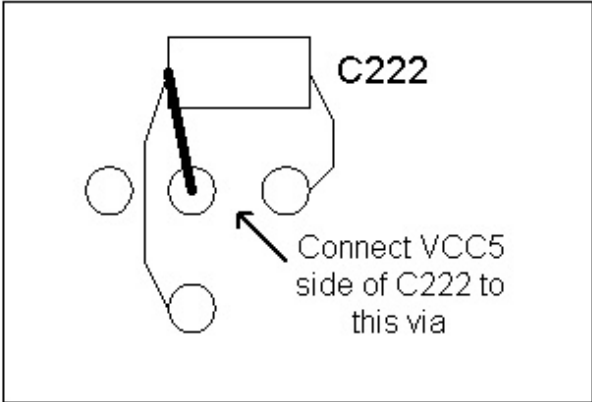
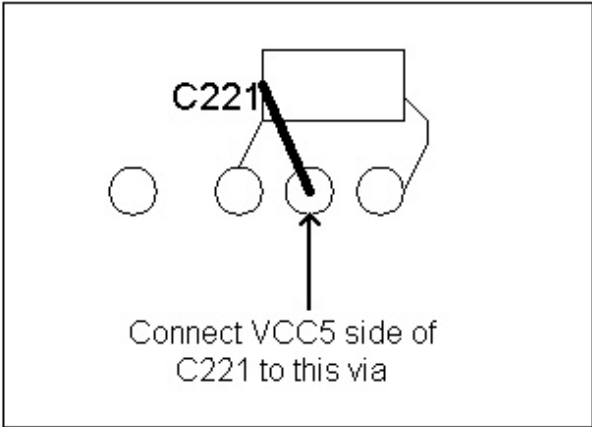


Figure 3

□ **#1.3.4 IDE DMA fails because of incorrect PAL equations**

Schematic Page 6

Problem DMA from the IDE interface does not work. The IDE Data Bit 7 is not activated properly during a DMA cycle.

To fix this problem, the U4 PAL needs to be programmed with the 1.4 IDE PAL equations so that the IDE Data Bit 7 is properly activated for read or write during an IDE DMA cycle.

Board Rework Solution

Reprogram the U4 PAL with the Revision 1.4 Equations, which correctly set the IDE Data Bit 7.

Next CAD Solution

Use Revision 1.4 Equations for the U4 PAL.