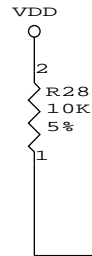
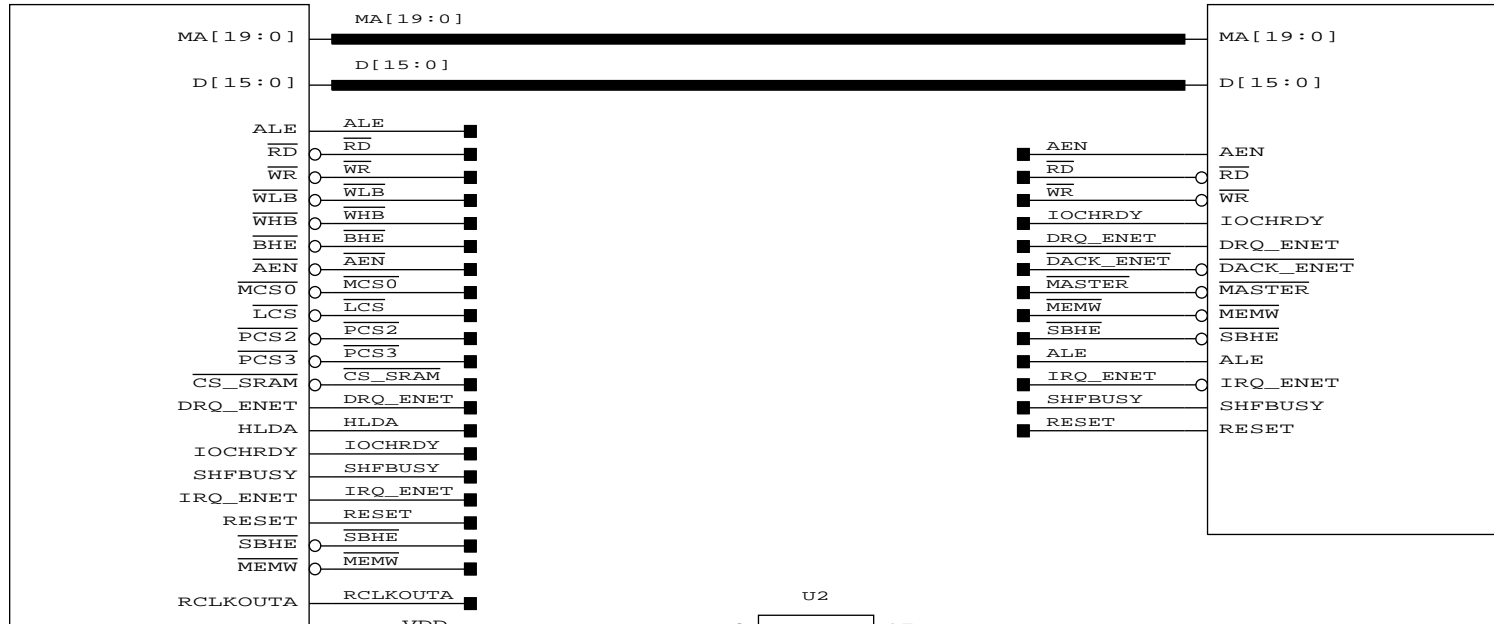


CPU/Memory Subsection

Ethernet Subsection



U2

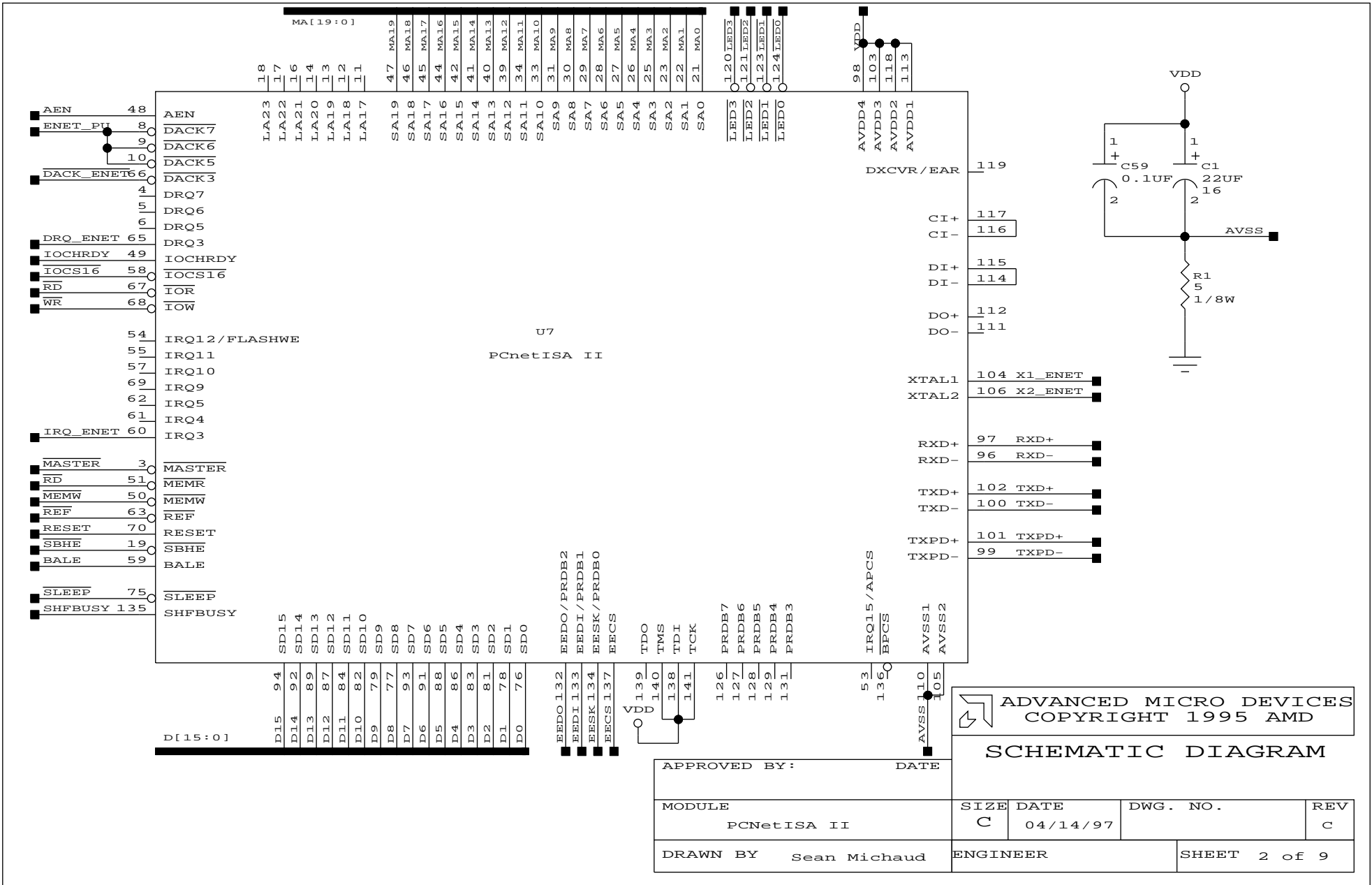
RCLKOUTA	2	I0	I00	17
MASTER	3	I1	I01	18
LCS	4	I2	I02	19
HLDA	5	I3	I03	20 AEN
BHE	6	I4	I04	21
WLB	7	I5	I05	23
WHB	9	I6	I06	24 SBHE
MCS0	10	I7	I07	25 DACK_ENET
PCS2	11	I8	I08	26 MEMW
PCS3	12	I9	I09	27 CS_SRAM
PU_PAL	13	I10	I11	16

PAL22V10

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SCHMATIC DIAGRAM

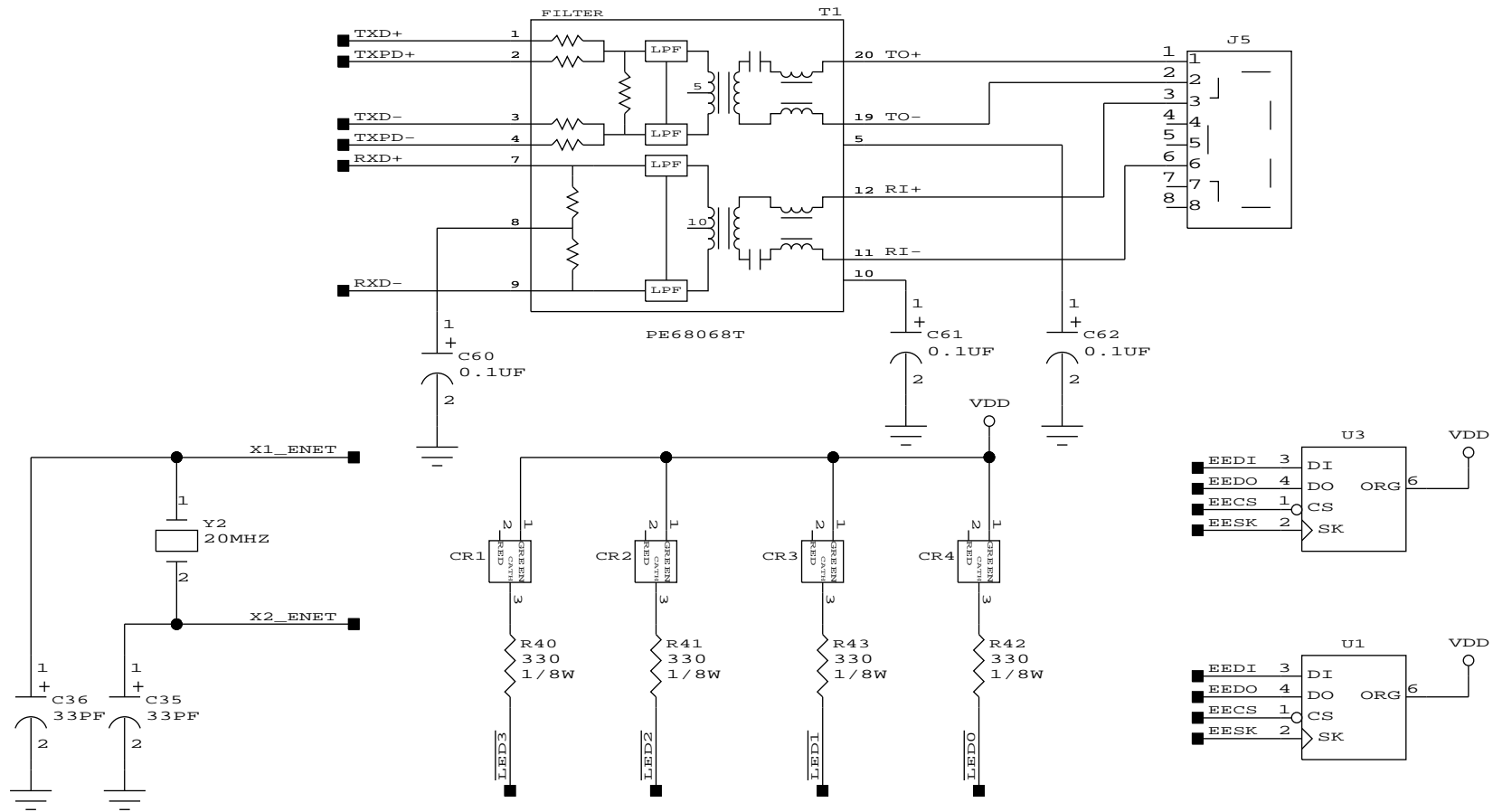
APPROVED BY:	DATE			
MODULE	SIZE	DATE	DWG. NO.	REV
Net186 Top Level	C	04/14/97		C
DRAWN BY Sean Michaud	ENGINEER	Mark Bowers Rick Purvis	SHEET 1 OF 9	



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**SCHEMATIC DIAGRAM**

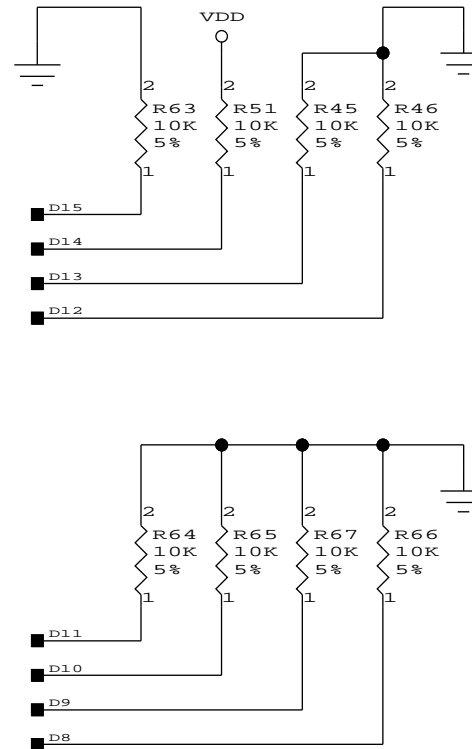
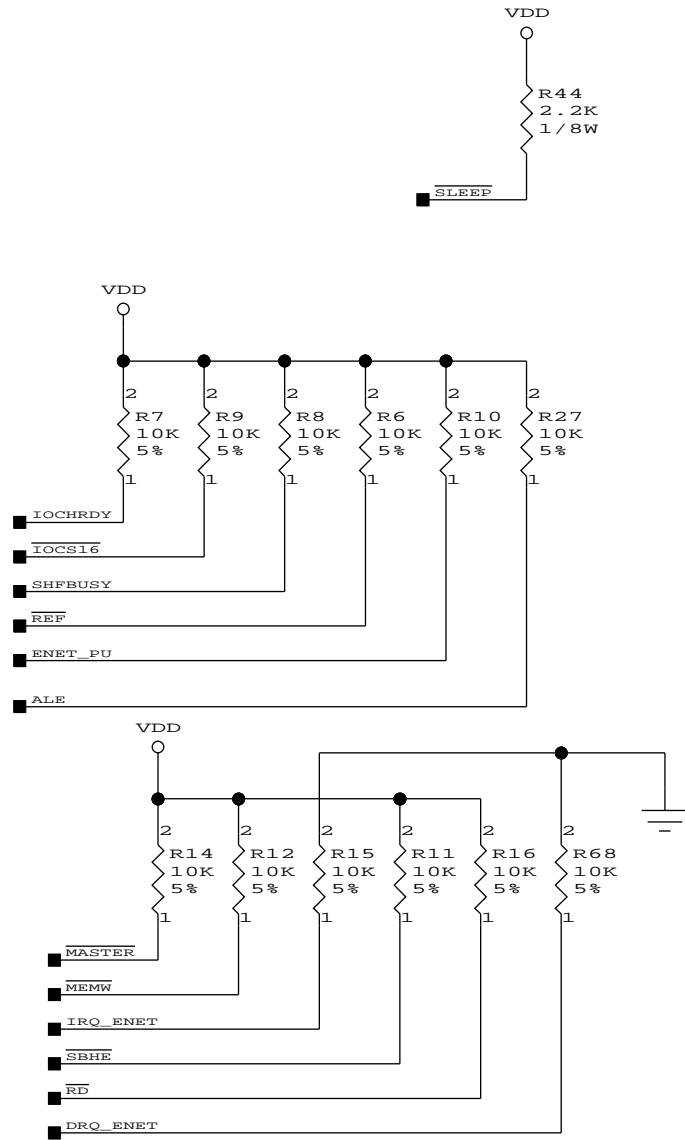
APPROVED BY:		DATE		
MODULE	SIZE	DATE	DWG. NO.	REV
PCNetISA II	C	04/14/97		C
DRAWN BY	ENGINEER		SHEET 2 of 9	
Sean Michaud				



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**SCHEMATIC DIAGRAM**

APPROVED BY:	DATE		
MODULE Ethernet Support	SIZE C	DATE 04/14/97	DWG. NO.
DRAWN BY Sean Michaud	ENGINEER	SHEET 3 OF 9	
			REV C

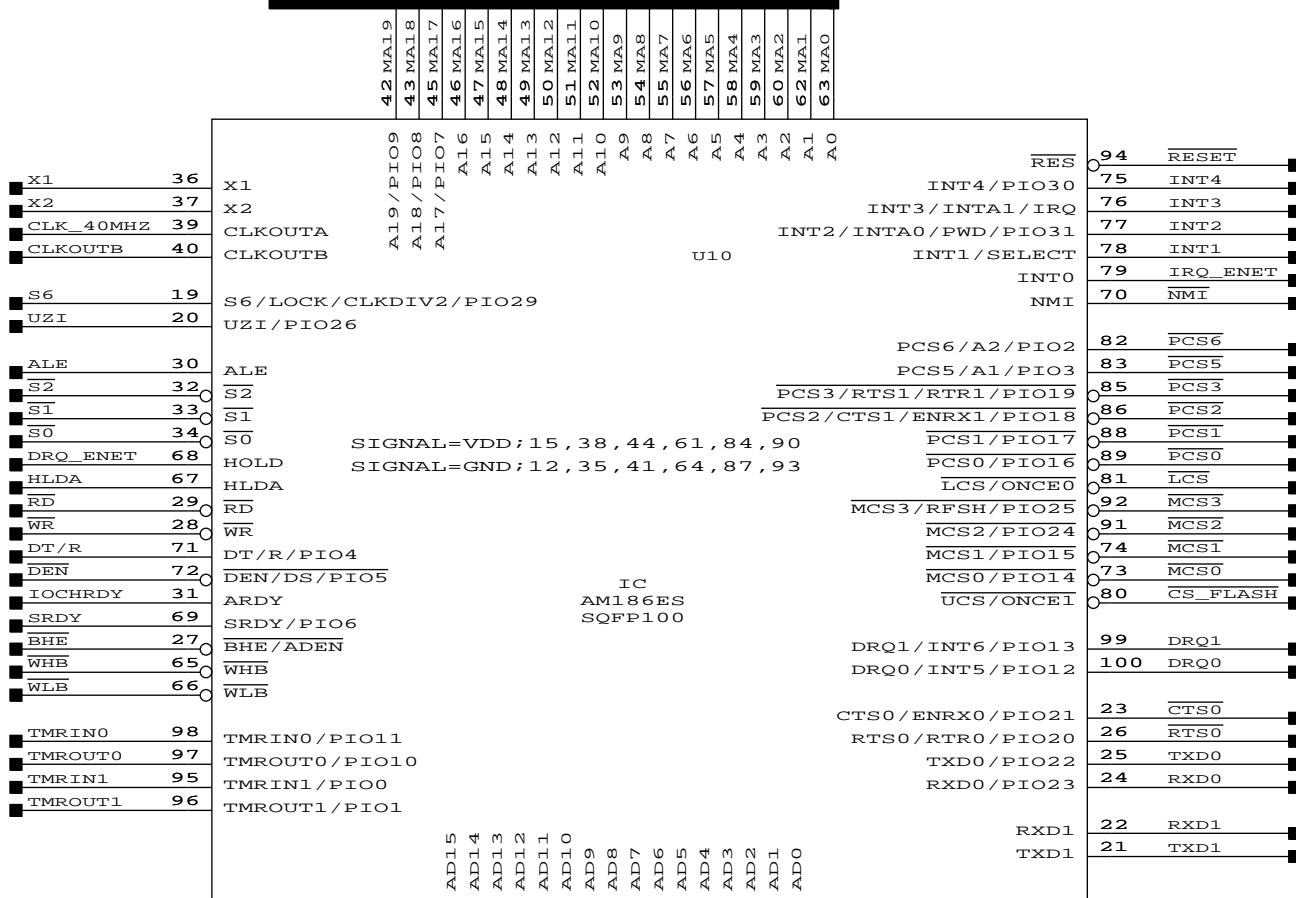


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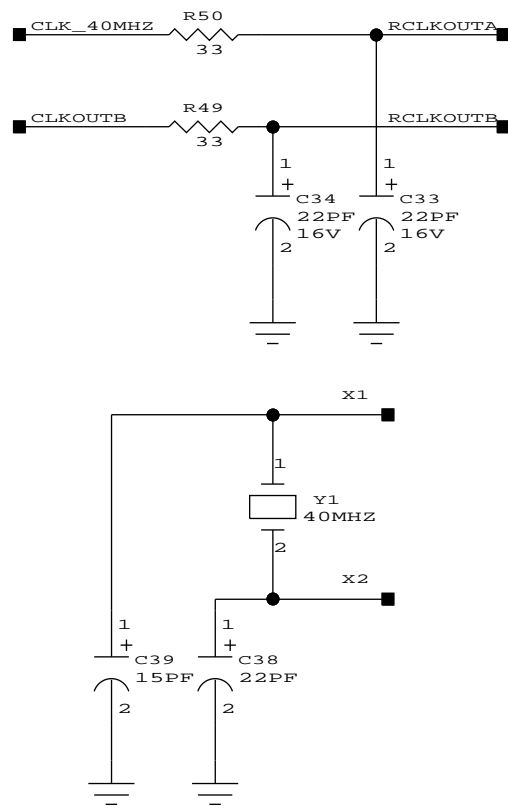
**SCHEMATIC DIAGRAM**

APPROVED BY:		DATE			
MODULE Ethernet Pullup Resistors		SIZE C	DATE 04/14/97	DWG. NO.	REV C
DRAWN BY Sean Michaud		ENGINEER		SHEET 4 OF 9	

MA[19:0]



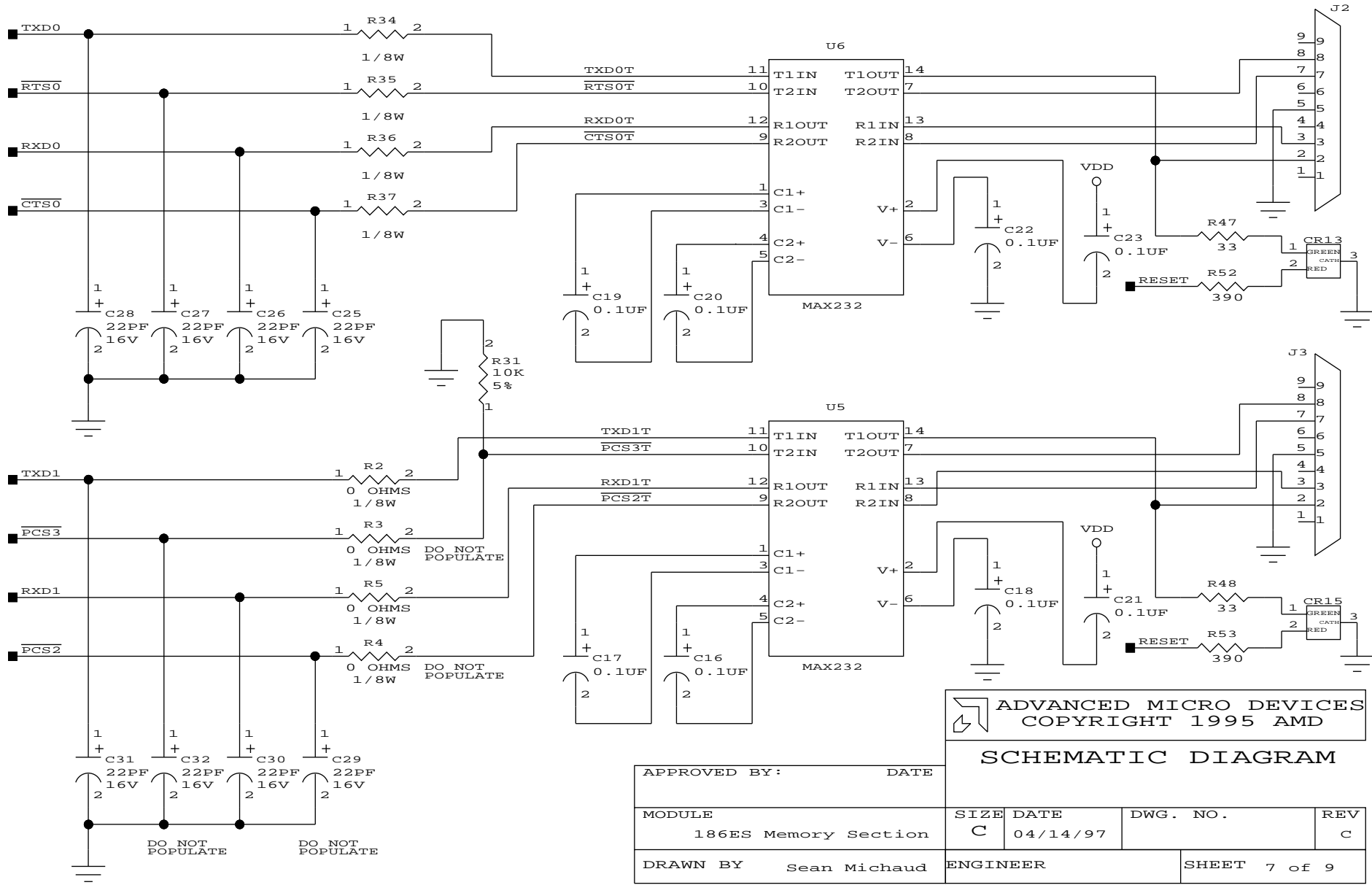
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**SCHEMATIC DIAGRAM**

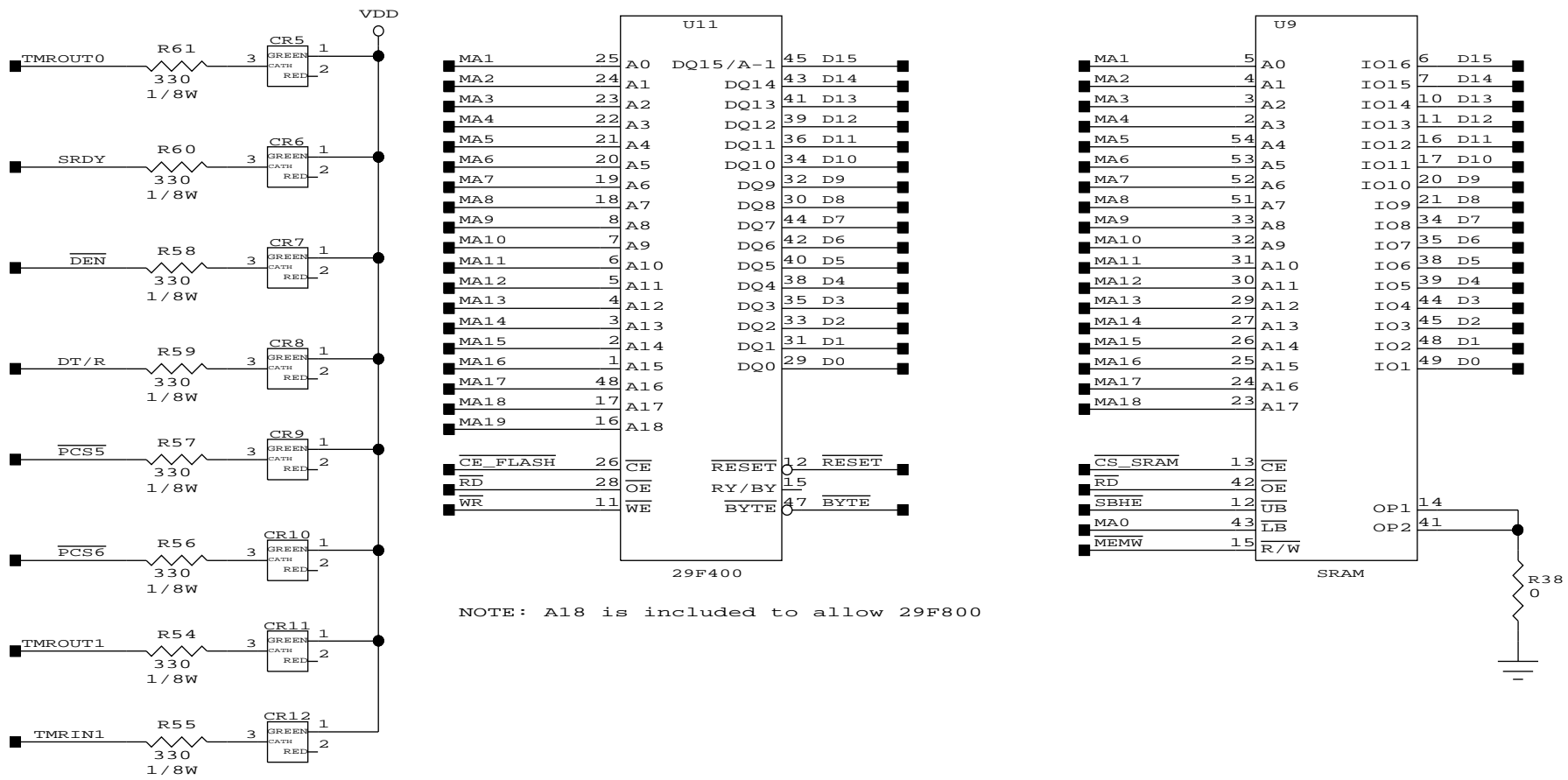
APPROVED BY:		DATE		
MODULE	SIZE	DATE	DWG. NO.	REV
186ES CPU Subsystem	C	04/14/97		C
DRAWN BY Sean Michaud			ENGINEER	SHEET 5 of 9



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**SCHEMATIC DIAGRAM**

APPROVED BY:	DATE			
MODULE	SIZE	DATE	DWG. NO.	REV
186ES Memory Section	C	04/14/97		C
DRAWN BY	ENGINEER		SHEET 7 of 9	
Sean Michaud				

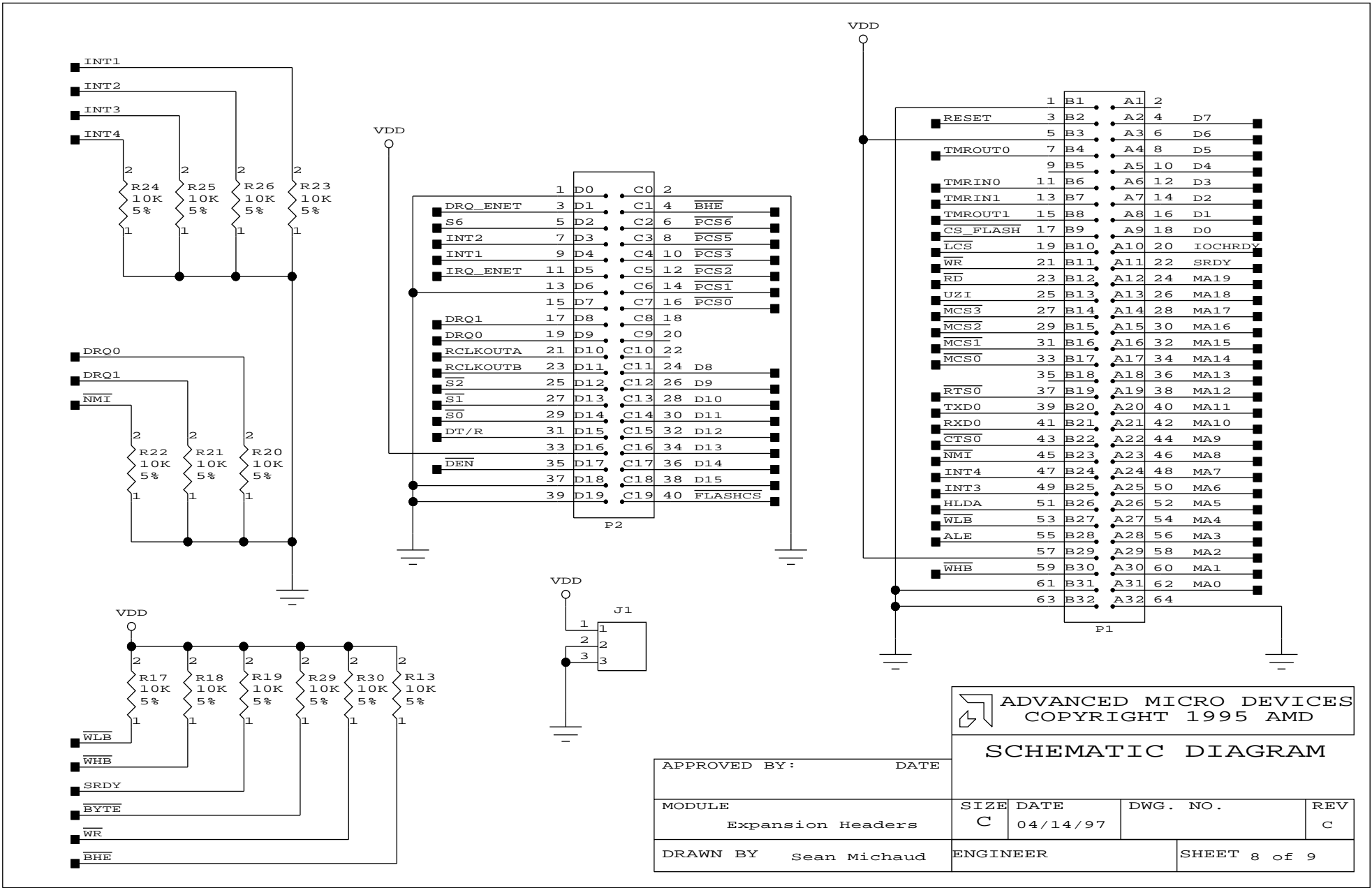


NOTE: A18 is included to allow 29F800

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SCHMATIC DIAGRAM

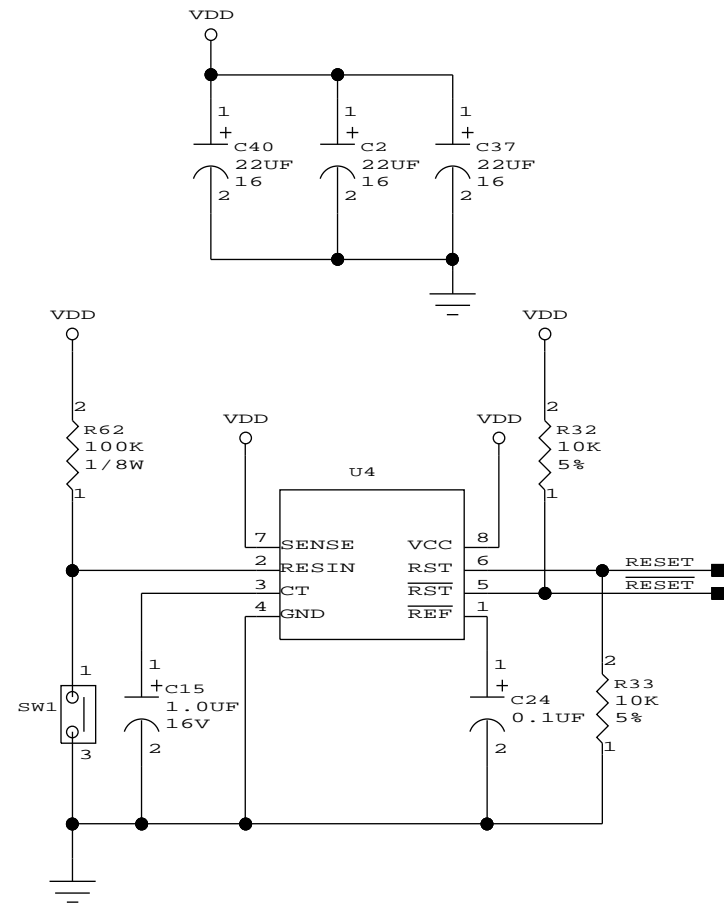
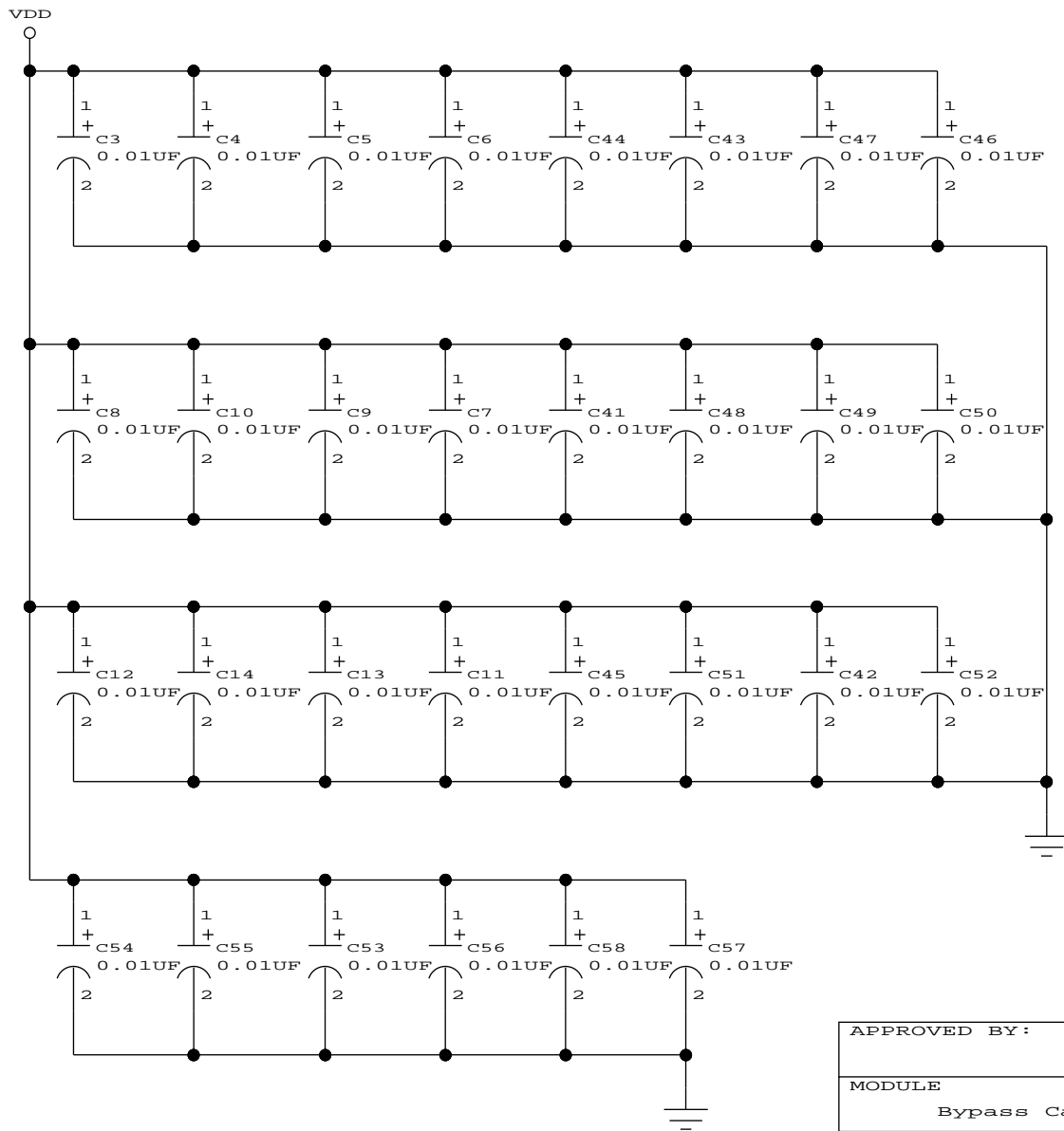
APPROVED BY:		DATE		
MODULE	SIZE	DATE	DWG. NO.	REV
186ES Memory Section	C	04/14/97		C
DRAWN BY Sean Michaud			ENGINEER	SHEET 6 of 9



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APPROVED BY:		DATE		
MODULE	SIZE	DATE	DWG. NO.	REV
Expansion Headers	C	04/14/97		C
DRAWN BY Sean Michaud			ENGINEER	SHEET 8 of 9



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APPROVED BY:	DATE			
MODULE Bypass Capacitors	SIZE C	DATE 04/14/97	DWG. NO.	REV C
DRAWN BY Sean Michaud	ENGINEER		SHEET 9 of 9	