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
Page 1: Cover Sheet (COVER.SCH)  
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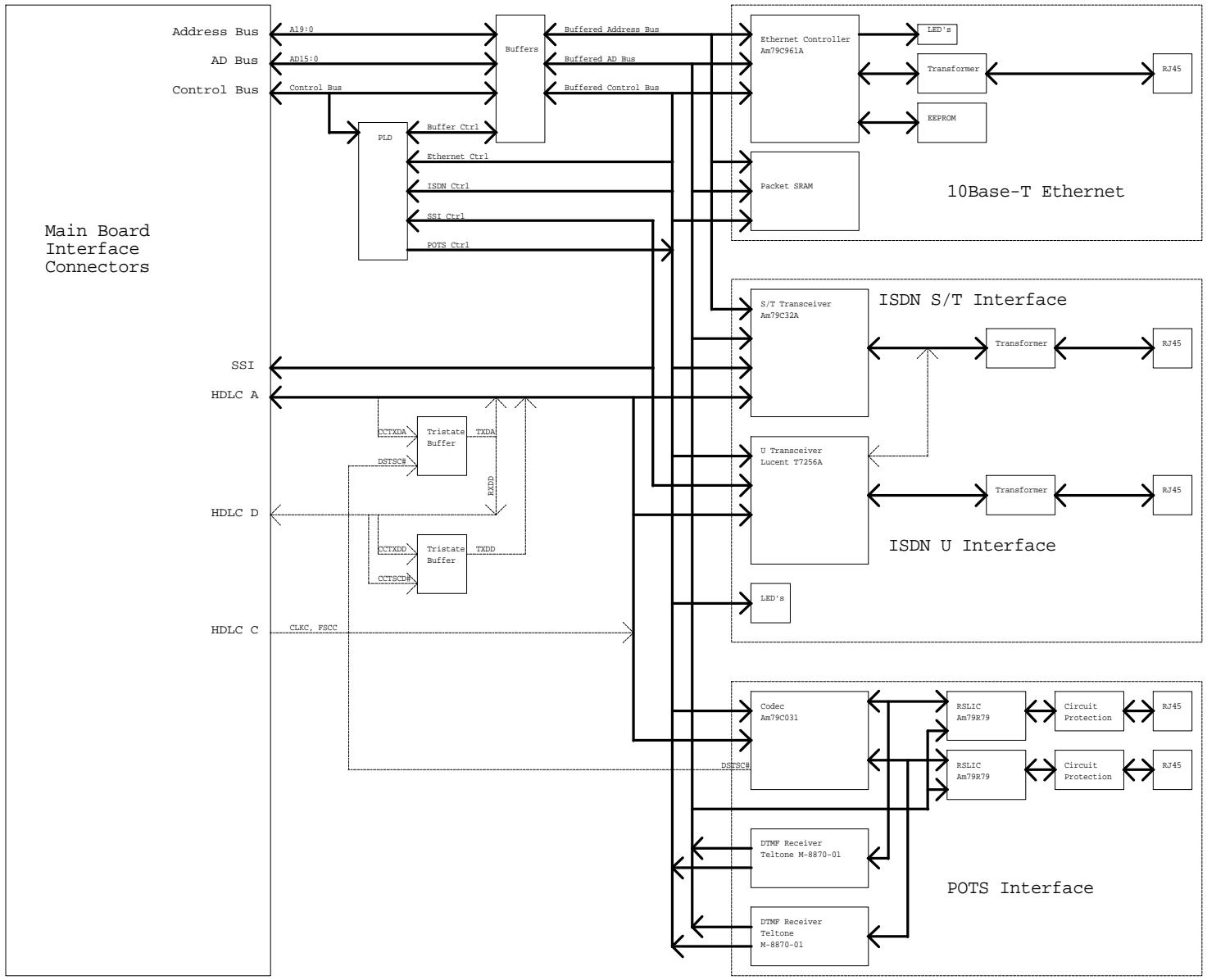
# *Am186CC Validation Platform Schematics*


## *Router/ISDN Development Module*

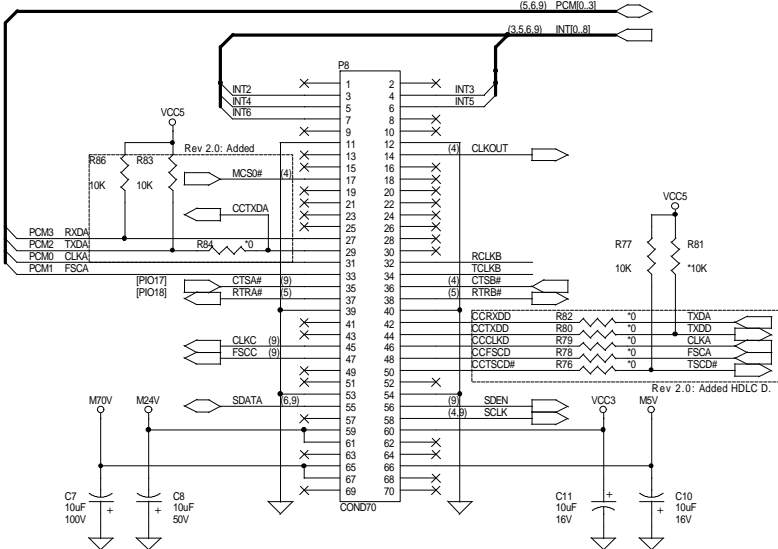
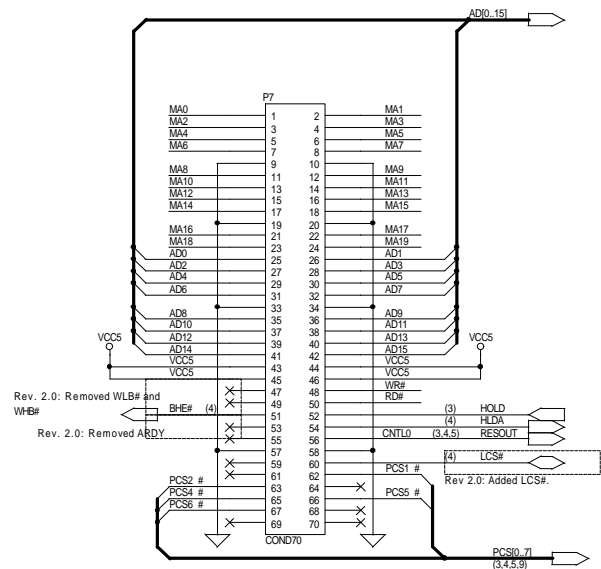
**Rev. 2.1**

- Rev 1.0:** Original design
- Rev 2.0:** Sheet 2: Change buffer control  
Sheet 4: Change Packet SRAM to 64Kx16  
Change PAL routing for Ethernet and Buffer control  
Add Ethernet LED0 and delete LED2  
Sheet 5: Correct S/T interface RJ45 pinout  
Add S/T protection circuitry  
Change S/T transceiver to 16-bit addressing  
Remove ISDN diagnostic LED  
Sheet 6: Add S/T interface names to U transceiver  
Sheet 9: Add Time Slot Control buffering
- Rev 2.1:** Sheet 2: Change data buffer control  
Added RING\_IN PIO's thru buffer  
Sheet 4: Change PAL for DTMF and Data Buffer control  
Changed Packet SRAM select circuitry  
Sheet 10: Added DSLAC clocking jumper select  
Swapped DTMF data bit order

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Design Name Router/ISDN Development Module - Cover Page		
Size Hex12.5	Schematic Sheet Name COVER.SCH	Rev 2.1
Date: Thursday, February 11, 1999		Sheet 1 of 11

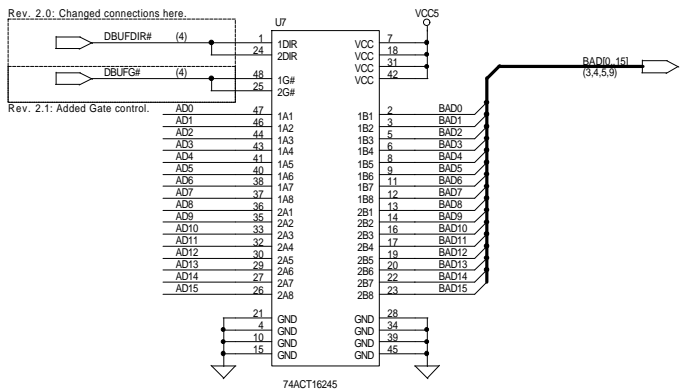
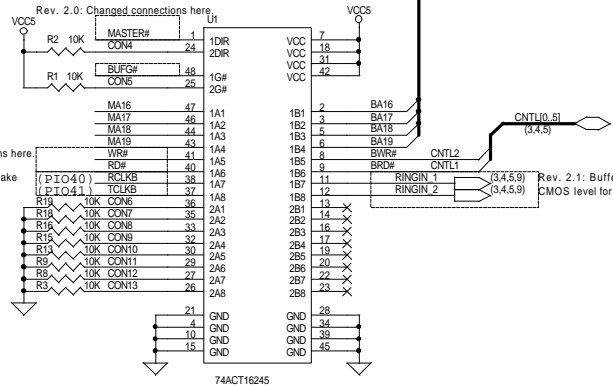
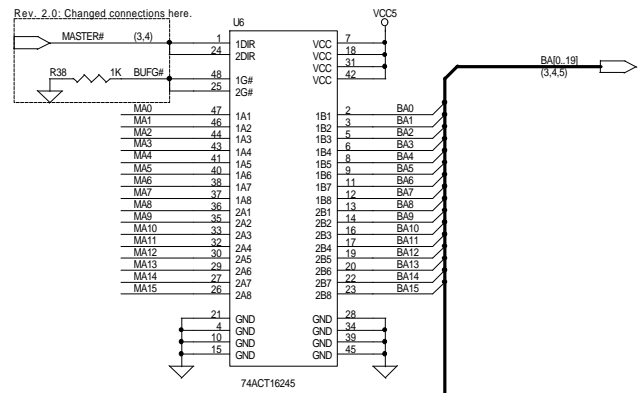
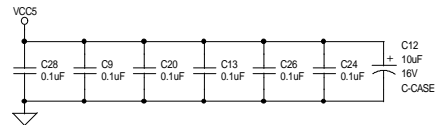


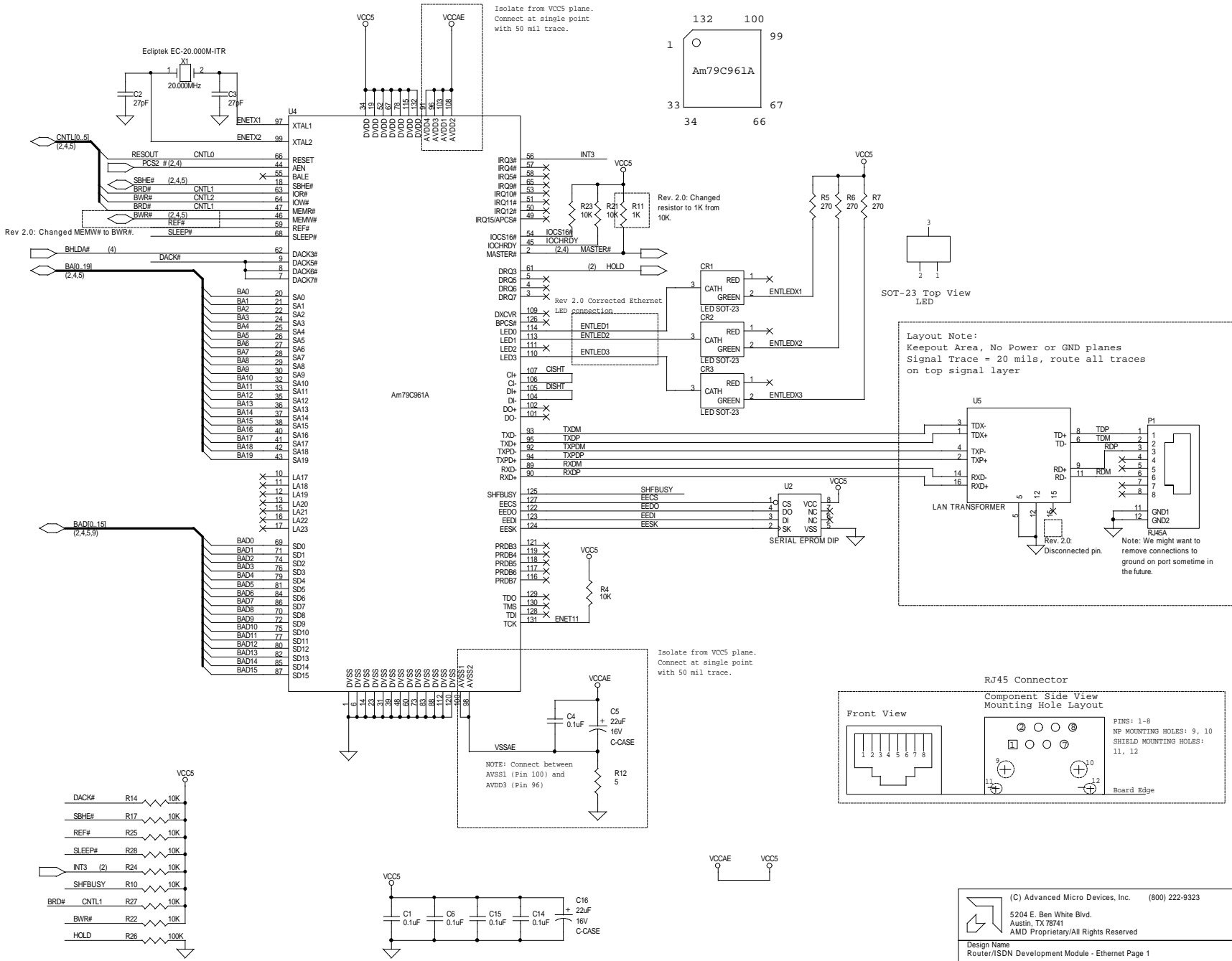
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Design Name Router/ISDN Development Module - Block Diagram		
Size 16x12.5	Schematic Sheet Name BLOCK DIAGRAM	Rev 2.1
Date: Thursday, February 11, 1999      Sheet 2 of 11		



HDLC Channel D is used if the Aml86CC is required to communicate directly across the PCM bus with the DSLAC. The HDLC Channel A TXD is connected to the Channel D RXD and vice-versa, the Clock and Frame Sync is derived from Channel A source

WARNING: If HDLC channel D is used, the Low speed UART is unavailable



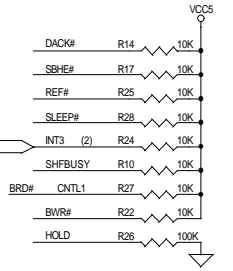
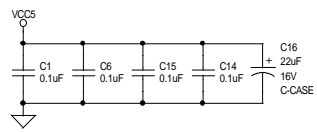
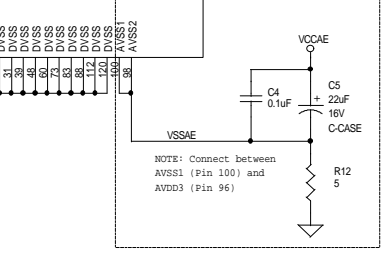
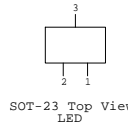
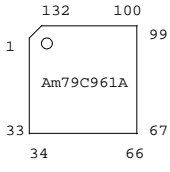
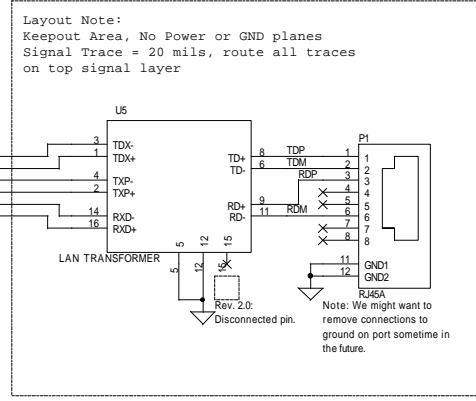
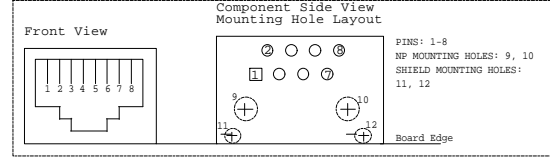


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Design Name: Router/ISDN Development Module - Ethernet Page 1

Size: Hx12.5	Schematic Sheet Name: ETHERNET1.SCH	Rev: 2.1
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Date: Wednesday, February 17, 1999 Sheet 4 of 11

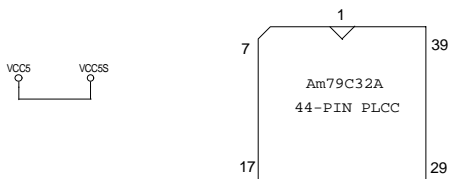
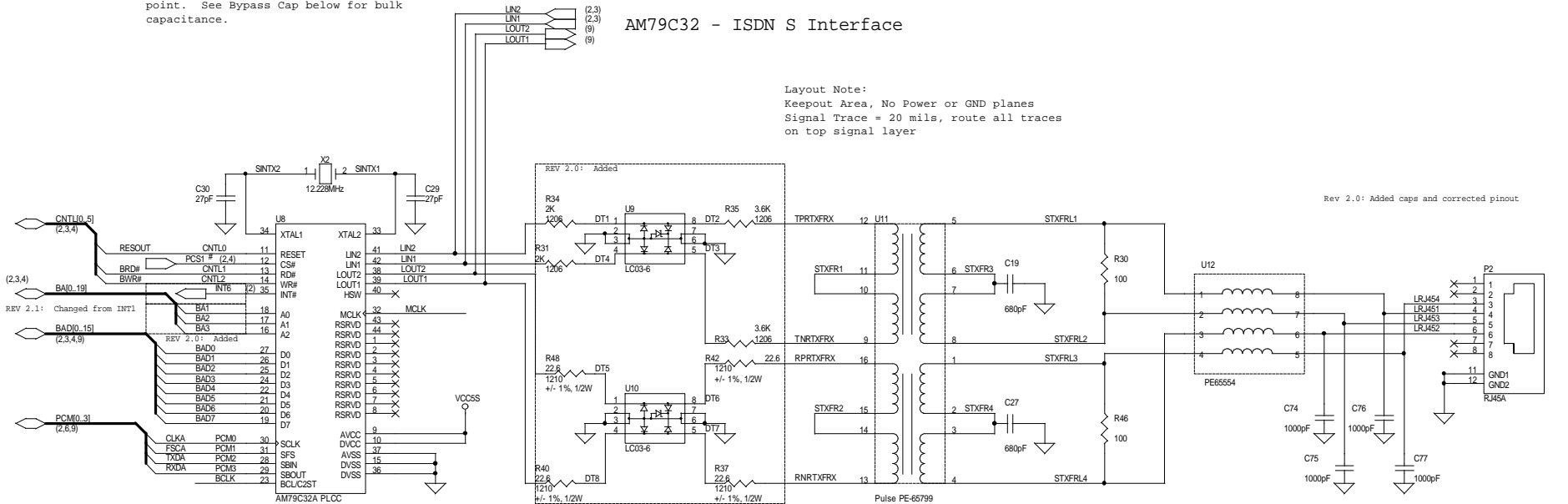




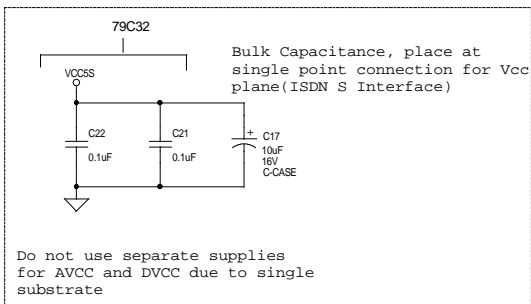
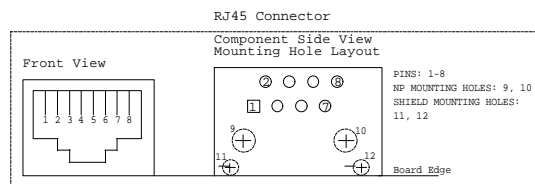
Layout Note:  
79C32 is a single substrate device.  
Separate Vcc plane for this area,  
connected to System Vcc through single  
point. See Bypass Cap below for bulk  
capacitance.

### AM79C32 - ISDN S Interface

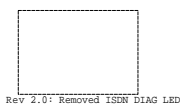
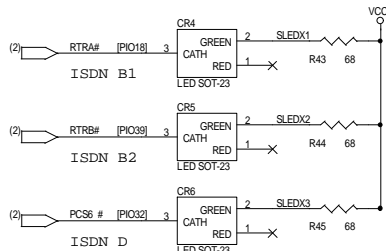
Layout Note:  
Keepout Area, No Power or GND planes  
Signal Trace = 20 mils, route all traces  
on top signal layer



MCLK\_C32 drives MCLK\_DSLAC when ISDN S Interface is functional. Alternate source for MCLK\_DSLAC is T7237/U Interface.  
Note - MCLK\_C32 is controlled by the PAL22V10



### LEDs Connected to PIOs

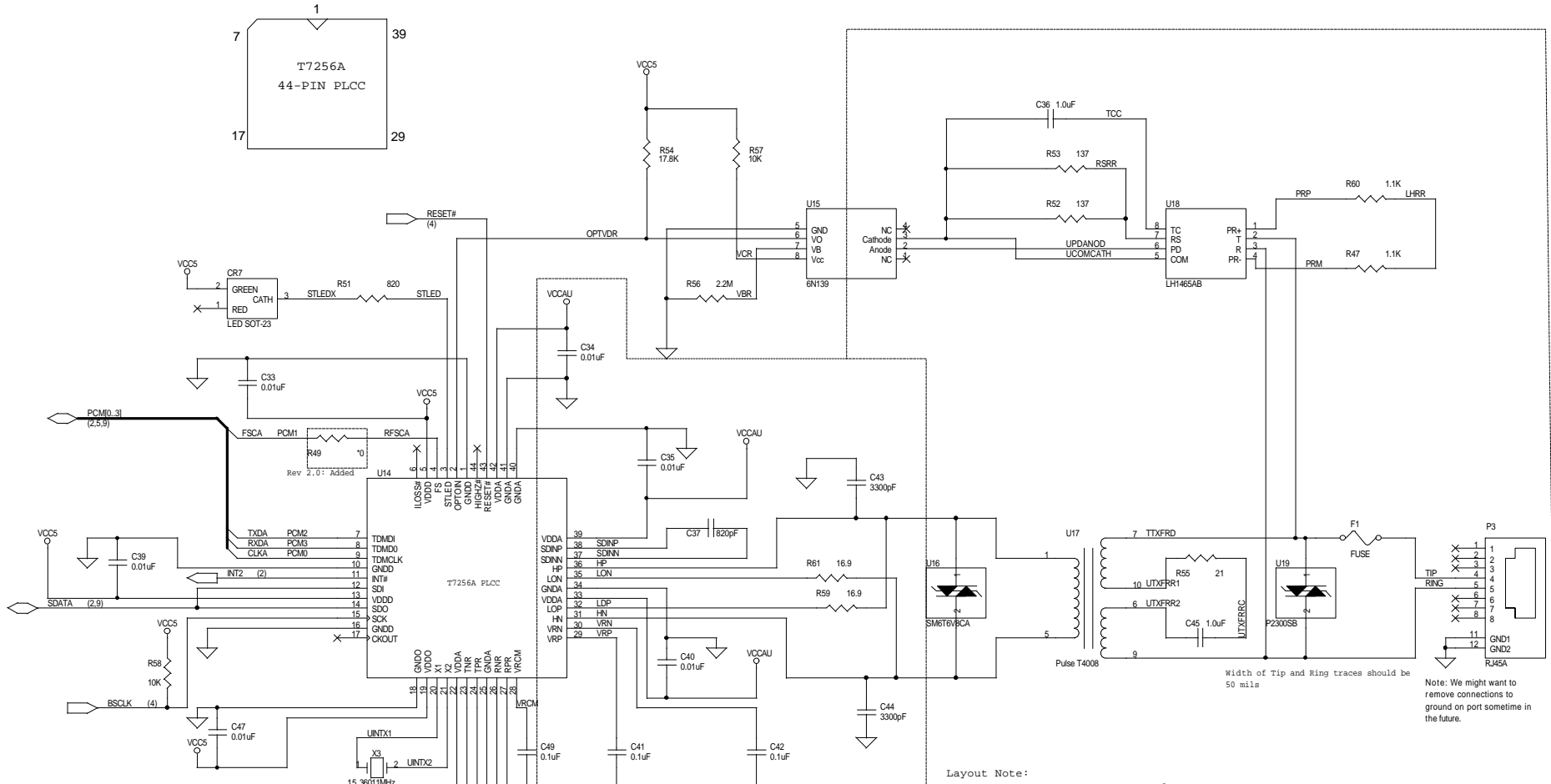


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Design Name: Router/ISDN Development Module - ISDN S Interface

Size: Rev12.5	Schematic Sheet Name: ISDN_S.SCH	Rev: 2.1
Date: Friday, April 09, 1999	Sheet: 6 of 11	

# U Interface

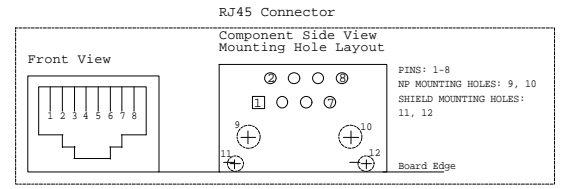
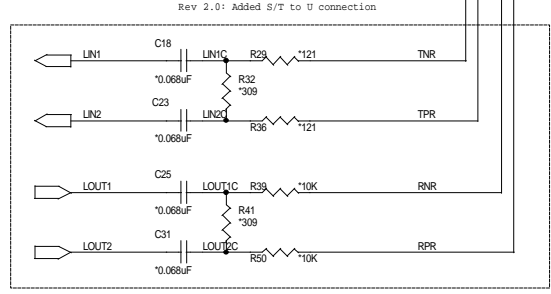


BSCCLK - From PAL22v10. PIO38 is used to tri-state (with pull-up) SCLK when T7237 is not accessed by 186CC.

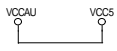
CLK\_U drives MCLK\_DSLAC when ISDN U Interface is functional. Alternate source for MCLK\_DSLAC is the 79C32/U Interface. Note - MCLK\_C32 is controlled by the PAL22v10.

Layout Note:  
Keupout Area, No Power or GND planes  
Signal Trace = 20 mils, route all traces on top signal layer

Note: We might want to remove connections to ground on port sometime in the future.



NOTE: VCCAUI is isolated from VCC5 plane. Connect at single point.

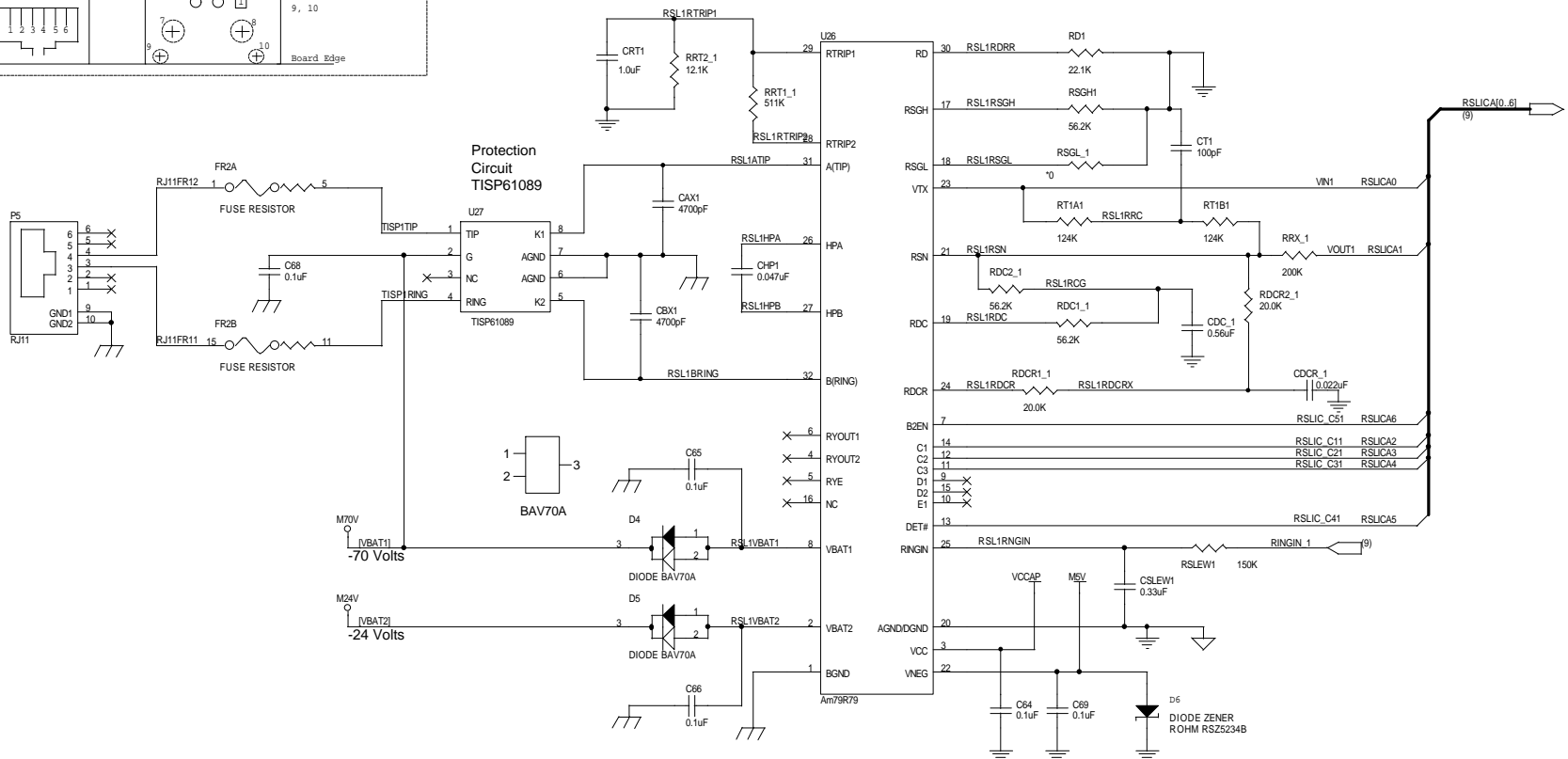
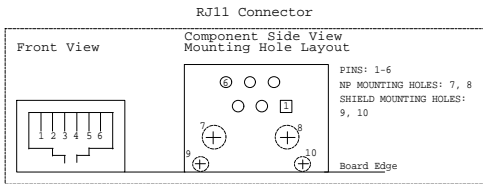


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Design Name  
 Am186CC ISDN Terminal Adapter (Reference Design) - ISDN U Interface

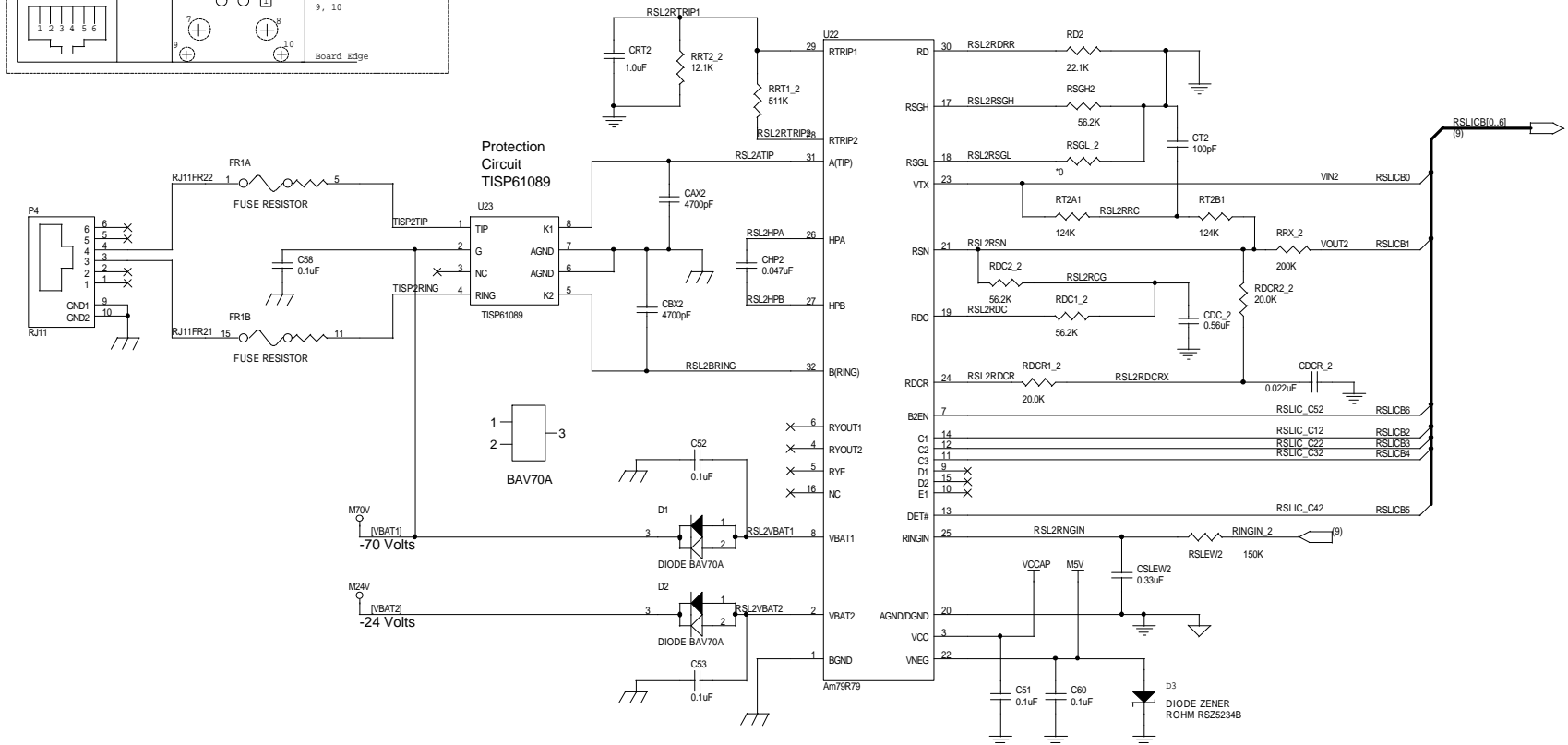
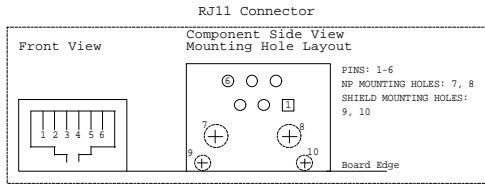
Size Rev12.5	Schematic Sheet Name ISDN_U.SCH	Rev 2.1
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Date: Wednesday, February 17, 1999 Sheet 7 of 11



NOTE: VSSCP and VSSAP 50 mil traces connected to GND plane at single point.  
No VCC or GND plane in this area.  
M70V is a 50 mil trace.  
M24V is a 50 mil trace.  
M5V is a 50 mil trace.  
VCCAP is a 50 mil trace connected to VCC5 at a single point.

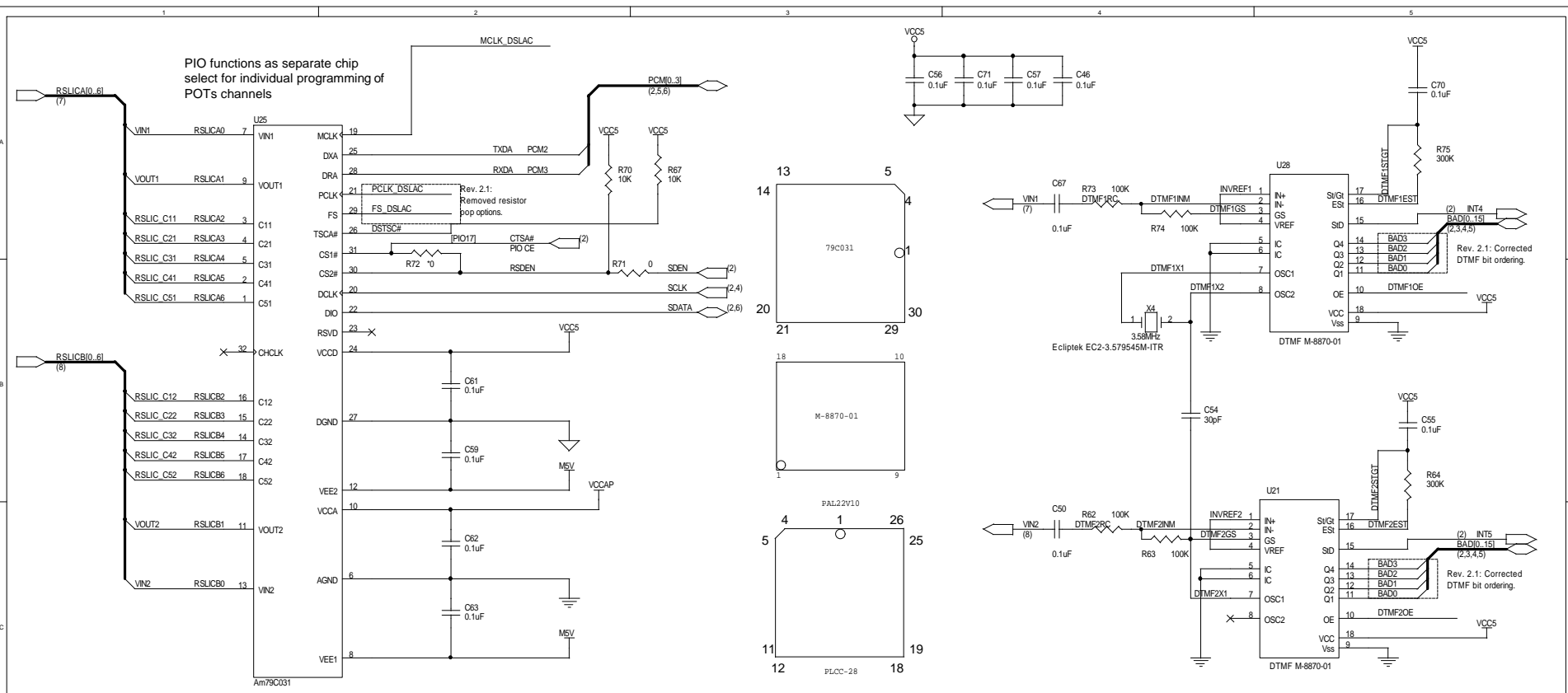
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Design Name Am186CC ISDN Terminal Adapter (Reference Design) - RSLIC Page 1		
Size Hex12.5	Schematic Sheet Name POTS_RSLIC1.SCH	Rev 2.1
Date: Thursday, February 11, 1999	Sheet	8 of 11



NOTE: VSSCP and VSSAP 50 mil traces connected to GND plane at single point.  
 No VCC or GND plane in this area.  
 M70V is a 50 mil trace.  
 M24V is a 50 mil trace.  
 M5V is a 50 mil trace.  
 VCCAP is a 50 mil trace connected to VCC5 at a single point.

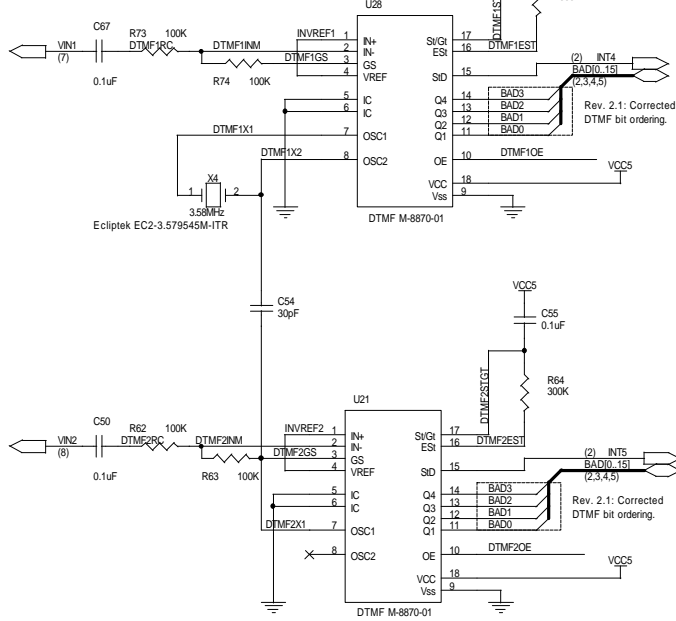
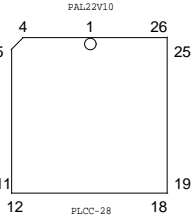
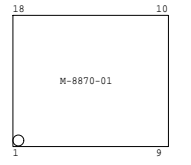
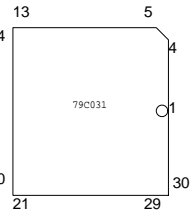


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Design Name Am186CC ISDN Terminal Adapter (Reference Design) - RSLIC Page 2		
Size Hex12.5	Schematic Sheet Name POTS_RSLIC2.SCH	Rev 2.1
Date: Thursday, February 11, 1999	Sheet	9 of 11



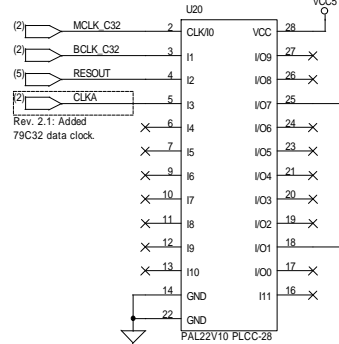
PIO functions as separate chip select for individual programming of POTs channels

Am79C031

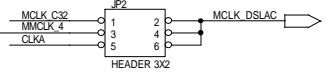
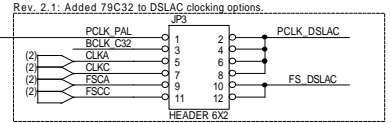


**U24 PAL DESCRIPTION**

DTMF2OE = PCS5; DTMF2OE is an inverted PCS5#/PIO2 used for DTMF OE.  
 DTMF1OE = PCS4; DTMF1OE is an inverted PCS4#/PIO2 used for DTMF OE.  
 TXDA = OCTXDA; TXDA is the Am186CC TXDA output when the DSLAC is NOT transmitting on the PCM bus. This is needed in case the HDLC TSA's are configured in muxed mode and a POTS line is needed. The Am186CC TXDA output will be tristated when the POTS interface is transmitting.  
 RXDA = TXDD; RXDA is the Am186CC TXDD output when PCM channel D is transmitting. This is used if the Am186CC is required to transmit data to the DSLAC.



DSLAC Clocking Options Mode	PCLK_DS	FS_DS	MCLK_DS
S/T SBP	5-6	9-10	1-2
S/T SBP with CLK Sync	1-2	9-10	3-4
S/T IOM-2 with GCI/PCM Conv	7-8	11-12	3-4
S/T IOM-2	3-4	9-10	1-2
S/T IOM-2 with CLK Sync	1-2	9-10	3-4
U PCM	5-6	9-10	5-6

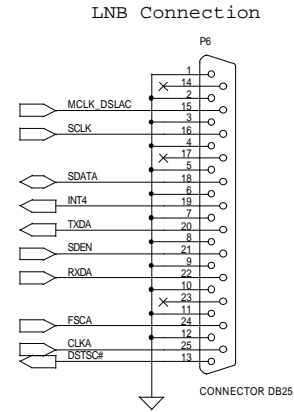
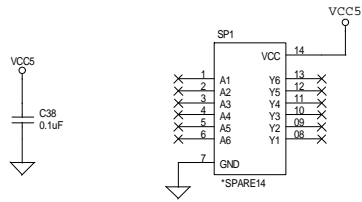


U20 is used to define the clocking used for the DSLAC device. The DSLAC is a PCM device only and may require clocking modifications for PCLK, FS, and MCLK, if PCLK is asynchronous to MCLK. Clocking options provided allow synchronous and asynchronous clocking based on clock masters running in PCM and GCI mode.  
 Options include :  
 1) GCI master - Use BCLK, FS, and MCLK outputs from master device.  
 2) GCI master - Use PAL to derive correct timing from GCI master for MCLK and PCLK. FS is a direct connection from GCI master.  
 3) GCI/PCM conversion - PCLK and FS are generated from the CLKC and FSCC outputs from the Am186CC device.  
 4) PCM master - PCLK and FS are a direct connection from the PCM master device.

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Design Name  
 Am186CC ISDN Terminal Adapter (Reference Design) - DSLAC

Size: 16x12.5 Schematic Sheet Name: POTS\_DSLAC.SCH Rev: 2.1  
 Date: Friday, February 26, 1999 Sheet: 10 of 11



If using the external LNB board to interface to a SLAC device, all connections on JP2 and JP3 must be removed.

### PIO RESOURCE ASSIGNMENTS

PIO	SIGNAL	FUNCTIONALITY
PIO18	RTRA	LED ISDN B1
PIO39	RTR_B#	LED ISDN B2
PIO32	PCS6#	LED ISDN D
PIO17	CTSA#	CE FOR DSLAC
PIO38	CTS_B	T7256 SCLK CNTL
PIO40	RCLK_B	POTS LINE 1 RINGING SIGNAL
PIO41	TCLK_B	POTS LINE 2 RINGING SIGNAL

### CHIP SELECT ASSIGNMENTS

CHIP SELECTS	DEVICE	INTERFACE
MCS0#	SRAM	16 BIT
PCS1#	79C32	16 BIT
PCS2#	PCNetISA II	8 BIT
PCS4#	DTMF1 OE	8 BIT
PCS5#	DTMF2 OE	8 BIT

### INTERRUPT ASSIGNMENTS

INTERRUPT	DEVICE	POLARITY
INT1	79C32	ACTIVE LOW EDGE
INT2	T7256	ACTIVE LOW EDGE
INT3	PCNetISA II	ACTIVE HIGH EDGE

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Design Name  
 Router/ISDN Development Module - Miscellaneous

Size: Hex12.5 Schematic Sheet Name: Rev: 2.1

Date: Wednesday, February 17, 1999 Sheet 11 of 11