



Systems in Silicon

ÉlanSC400 Microcontroller Evaluation Board Overview



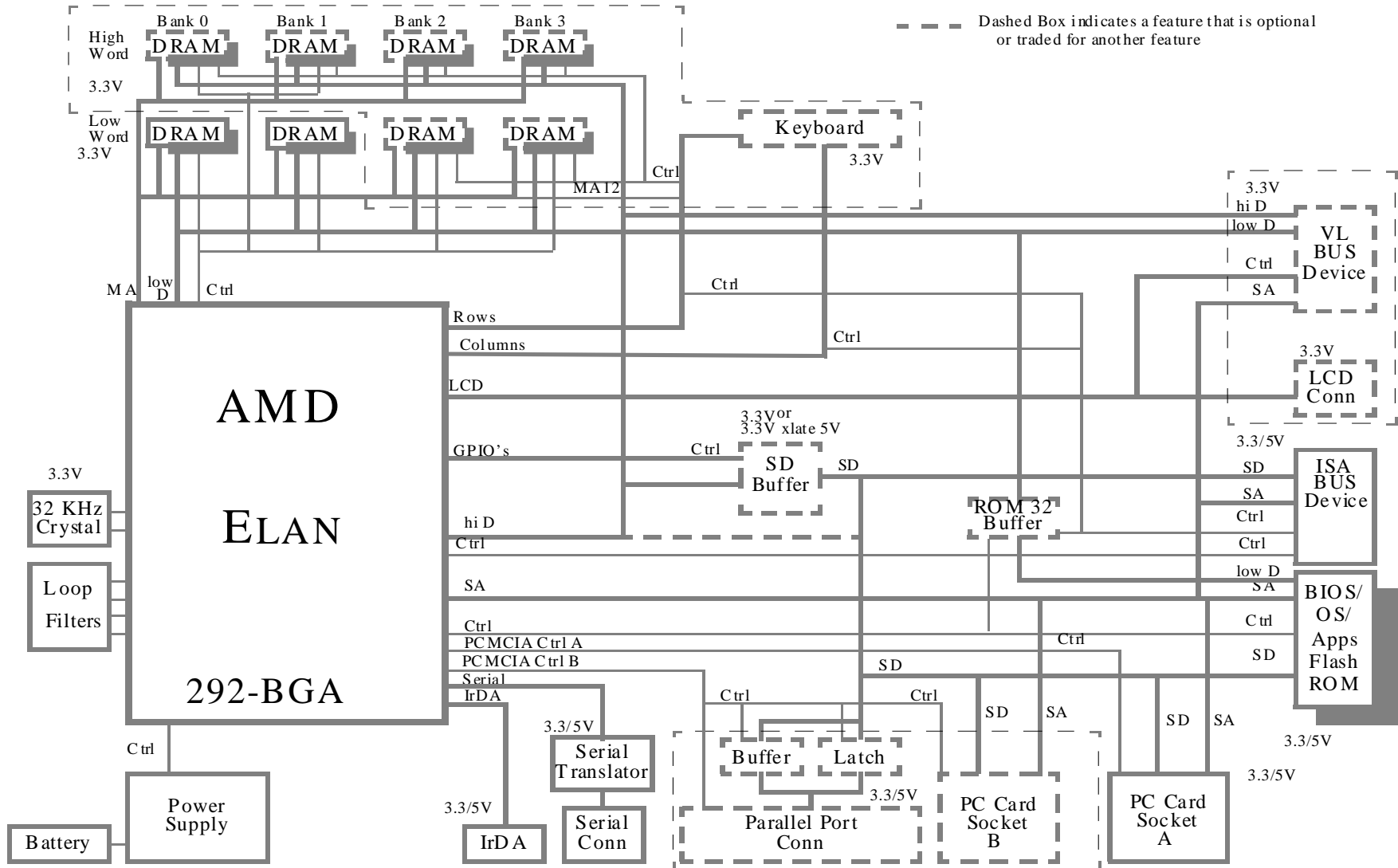


Systems in Silicon

System Block Diagram

ALL INTERFACES SHOWN

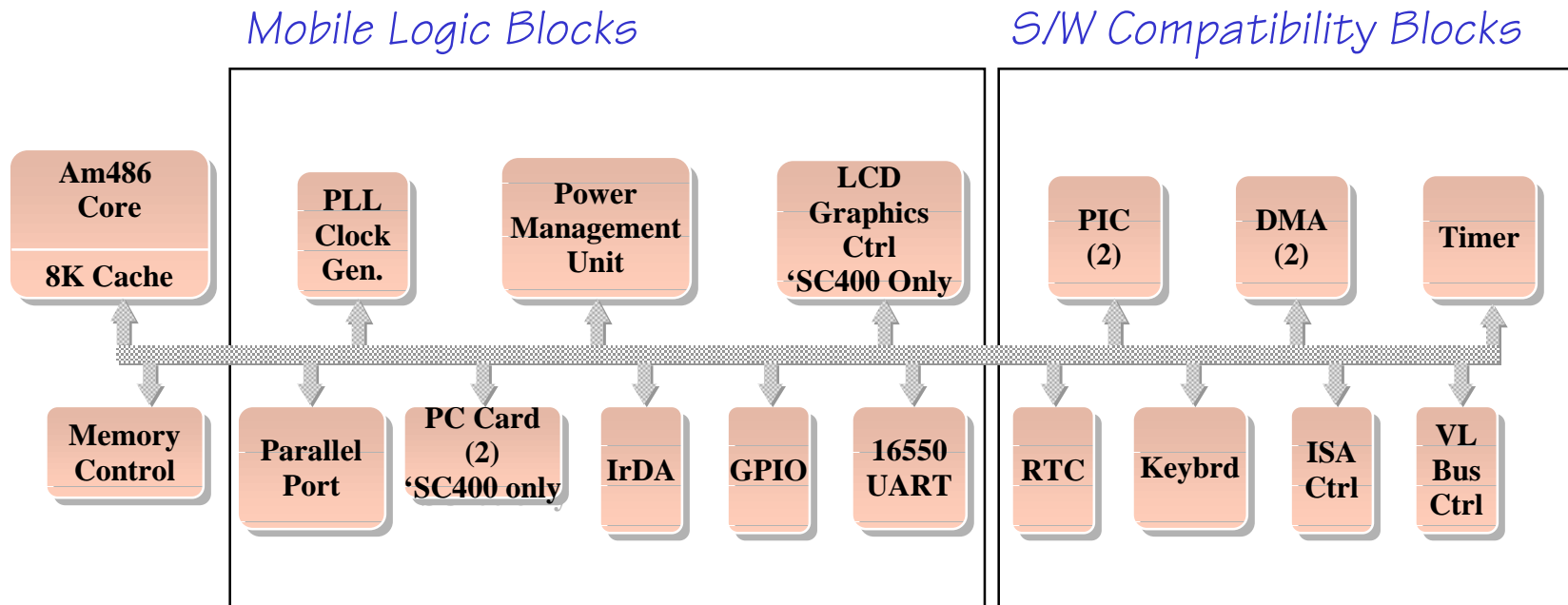
- - - Dashed Box indicates a feature that is optional or traded for another feature





Systems in Silicon

Internal Block Diagram



ÉlanSC400/SC410 Microcontroller





Systems in Silicon

Am486SLE CPU Core

- 8KByte Cache integrated
 - Tag and data RAM
 - 4 way set associative
 - Writeback Cache
- Speeds 33MHz, 66MHz and 100MHz
- Ultra Low Power
 - Fully static design
 - 2.7v and 3.3v
 - System Management Mode
- High Speed Mode
 - Up to 33MHz
 - Stop Clock on any edge
- Hyper Speed Mode
 - Clock doubled
 - 66 MHz or 100MHz
 - Automatic control for entering and leaving Hyper Speed mode (Stpclk,StpGrnt)

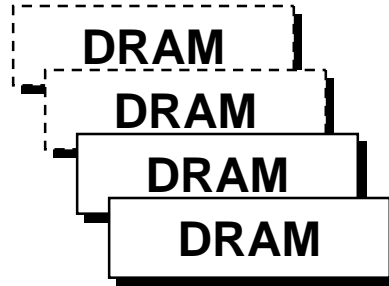




Systems in Silicon

DRAM Memory Controller

1-4 bank



**x16 & x32
Data Bits**



- Comprehensive integrated DRAM Controller
 - Just Add Memory, all timing internal to '400
 - Higher performance from x32 data bus, but system will have more memory
 - 256K, 1M, 4M, 16M, 64Mbit DRAM
 - Fast Page Mode or EDO
- 3.3v DRAM only
 - D[15:0] are not 5V safe





Systems in Silicon

DRAM Memory Controller cont.

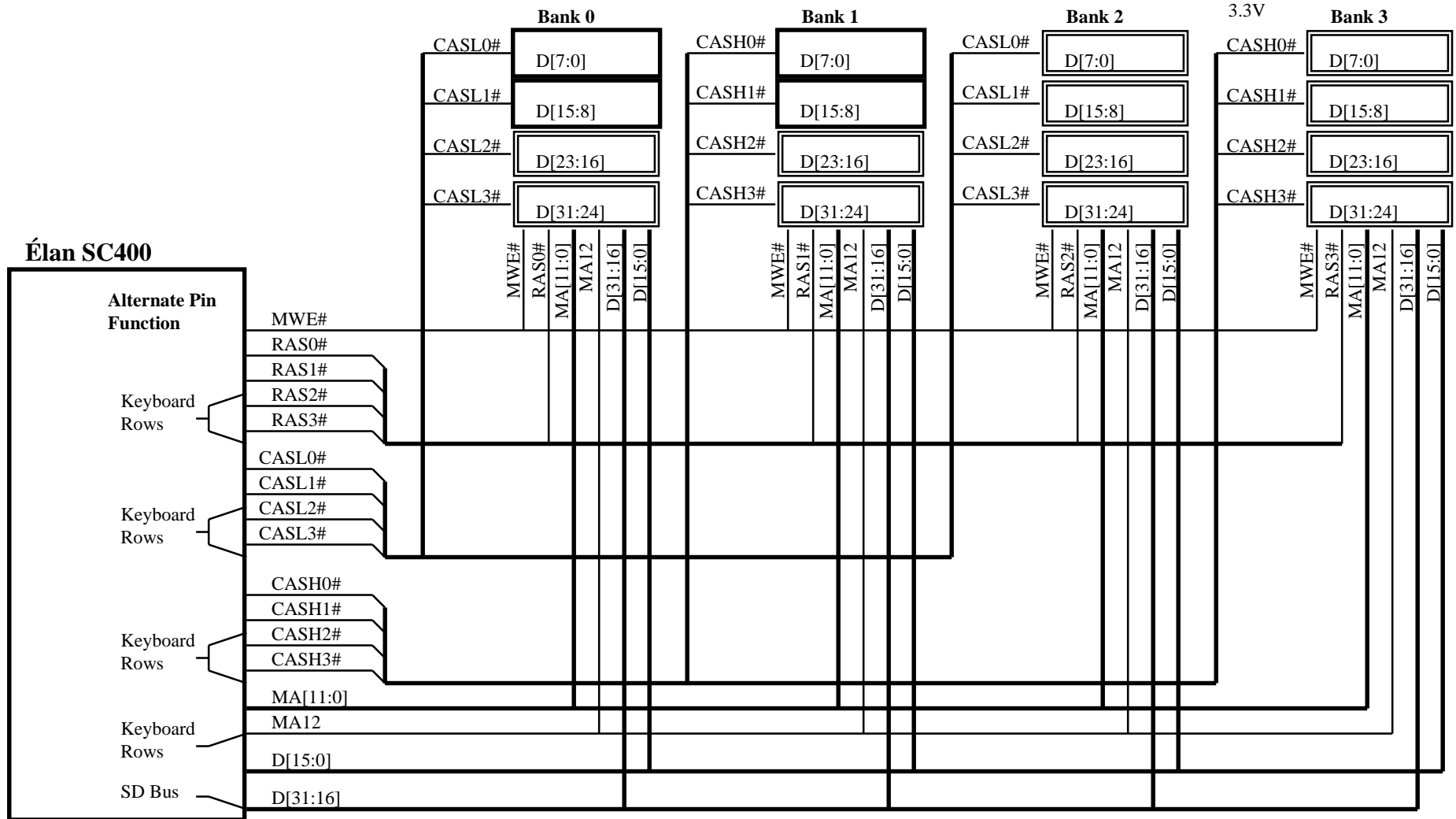
- Self Refresh DRAM support
- 1 RAS per Bank; 1 CAS per Byte configuration
- Bank 2 & 3 RAS signals are shared with Matrix Keyboard Row signals
- High word CAS signals are shared with Matrix Keyboard Row signals
- DRAM Shared between the CPU and Graphics Controller
 - Video image is stored in main memory





Systems in Silicon

DRAM Interface





Systems in Silicon

ROM Memory Controller

**BIOS ROM
Chip Select**

**O/S & App
ROM Chip
Select**

**Burst Mode
ROM
Support**

- ❖ 3 Programmable ROM Chip Selects
 - ROMCS0, ROMCS1, ROMCS2
 - ROMCS2 is programmable to appear on any GPIO_CS
- ❖ Programmable timing - ISA or CPU Speeds
 - Flash, OTP, EPROM, Mask ROM
 - Burst/Page mode support
- ❖ Programmable sizes

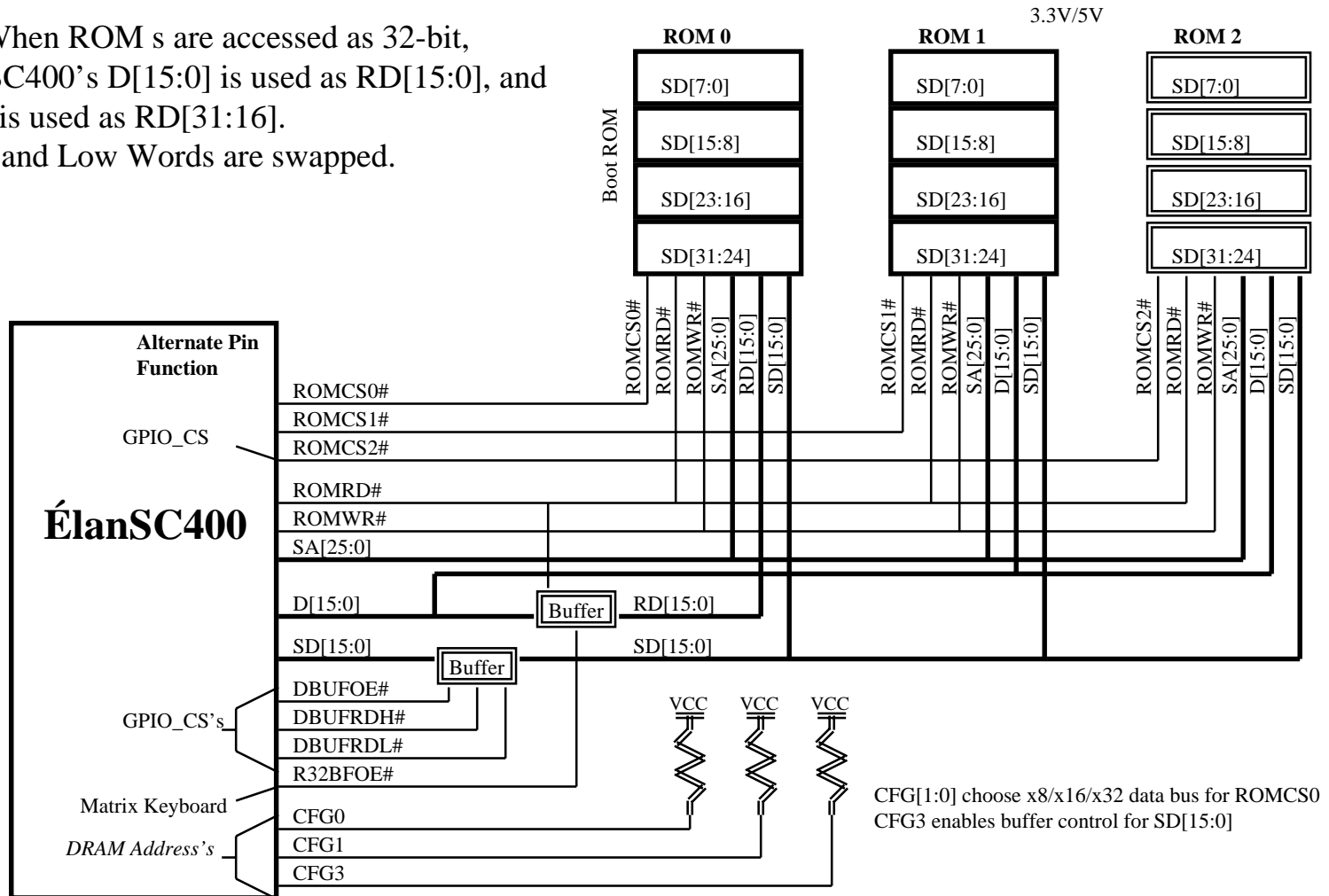




Systems in Silicon

ROM Interface

NOTE: When ROM s are accessed as 32-bit, the Élan SC400's D[15:0] is used as RD[15:0], and SD[15:0] is used as RD[31:16]. The High and Low Words are swapped.





Systems in Silicon

Memory Management System

- Dedicated Memory Mapping Registers
 - Similar to Expanded Memory System (EMS)
 - Allows Real Mode access to More than 1MByte of ROM
- Special BIOS boot loading
- Required for ROM DOS, Geoworks support
 - ROM Memory Mapped below 1MByte





Systems in Silicon

Power Management Unit (PMU)

- Single chip - fewer buses to operate
- 7 Power Management Modes
 - Allows great flexibility in configuring power/performance issues
- Events to automatically climb/fall through PMU Modes
 - Timers
 - Activities
 - Wake Ups – SMI/NMI's
- Interrupts & Force Mode feature make PMU software controllable also





Systems in Silicon

Power Management Unit cont.

- General Purpose I/O signals to control power to other components on board
 - Gives external control based on the PMU state
- Internal PLL's to generate all system clocks
 - PMU manages clock speeds
- Battery monitoring to affect the PMU based on battery power level
- 0.35 micron technology
 - 2.7V CPU VCC / 3.3V rest of the chip





Systems in Silicon

PMU - Modes

- Hyper-Speed Mode
 - Uses the CPU's PLL to double or triple the 33MHz clock
 - Slower to enter and exit
- High-Speed Mode
 - CPU clock of 8MHz to 33MHz
 - CPU is used in Static Clock mode
 - Can enter and exit quickly
- Low-Speed Mode
 - CPU clock of 1MHz to 8MHz
 - Slow down the system during non critical tasks to save power





Systems in Silicon

PMU - Modes cont.

- Standby Mode
 - CPU clock stopped, waiting for Event (i.e. key press, serial access, etc.)
 - System quickly responds to Events
- Temporary Low-Speed Mode
 - Mode to service Secondary Activities and SMI/NMI's
 - Allows non-critical tasks to be done out of the normal PMU flow





Systems in Silicon

PMU - Modes cont.

- Suspend Mode
 - System stopped, Power still on to maintain state
 - Slow to start system back up again, but still much faster than re-booting
- Critical Suspend Mode
 - System response to a very low battery
 - Same as Suspend, but system must be “unlocked” to wake up
- Real Time Clock Only Mode
 - The RTC has its own VCC so can be powered independently of the other power planes





PMU - Modes

Systems in Silicon
Reset

High Speed

33/16/8 MHz

Hyper Speed

100/66 MHz

Hyper Speed has to be Enabled before use

Low Speed

8/4/2/1 MHz

Normal PMU Progression to Suspend Mode

Temp Low Speed is outside the normal flow

Temporary Low Speed

Standby

0 MHz

Suspend

0 MHz

Critical Suspend is the same as Suspend, but will be locked in.

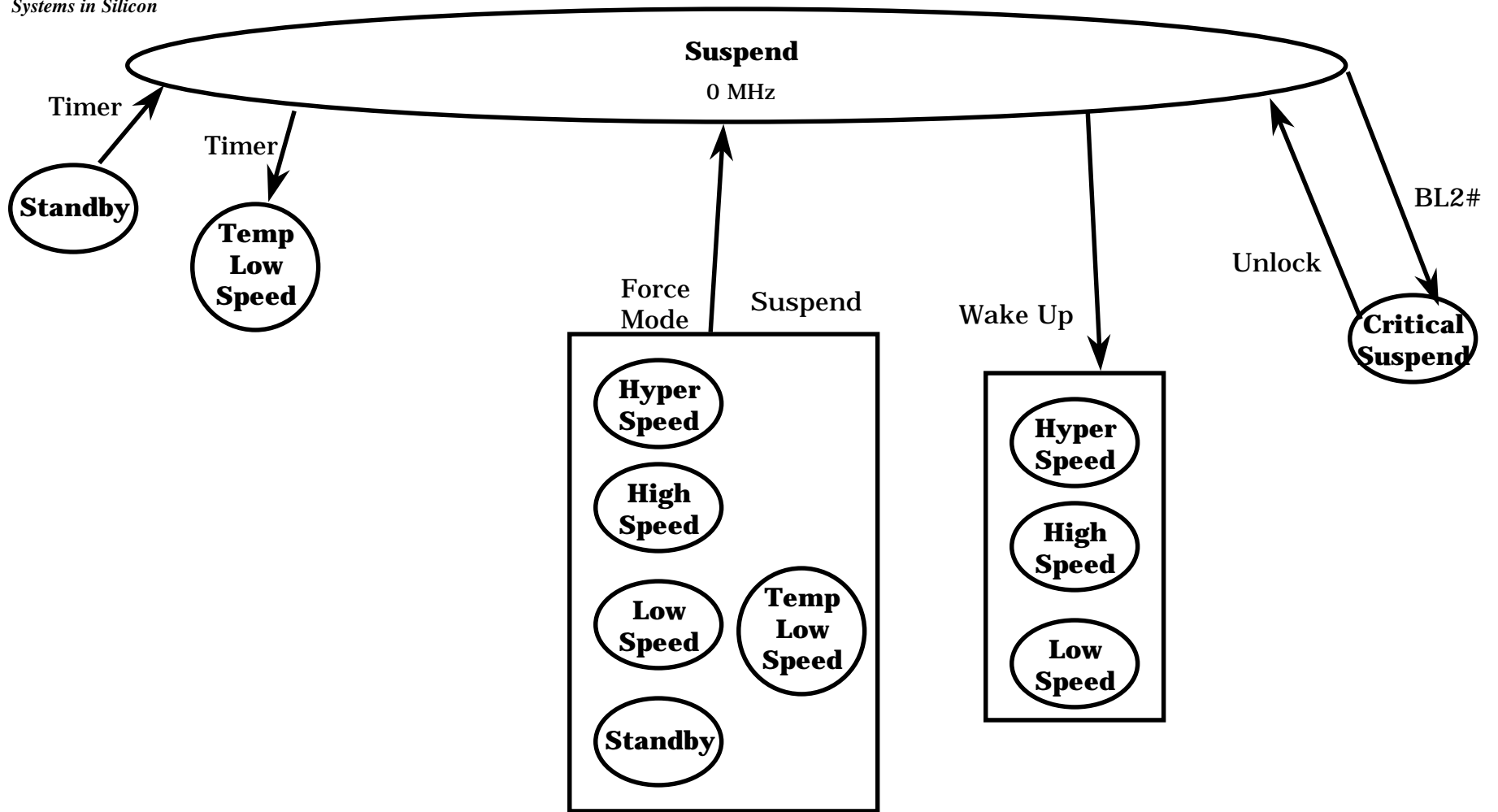
Critical Suspend





Systems in Silicon

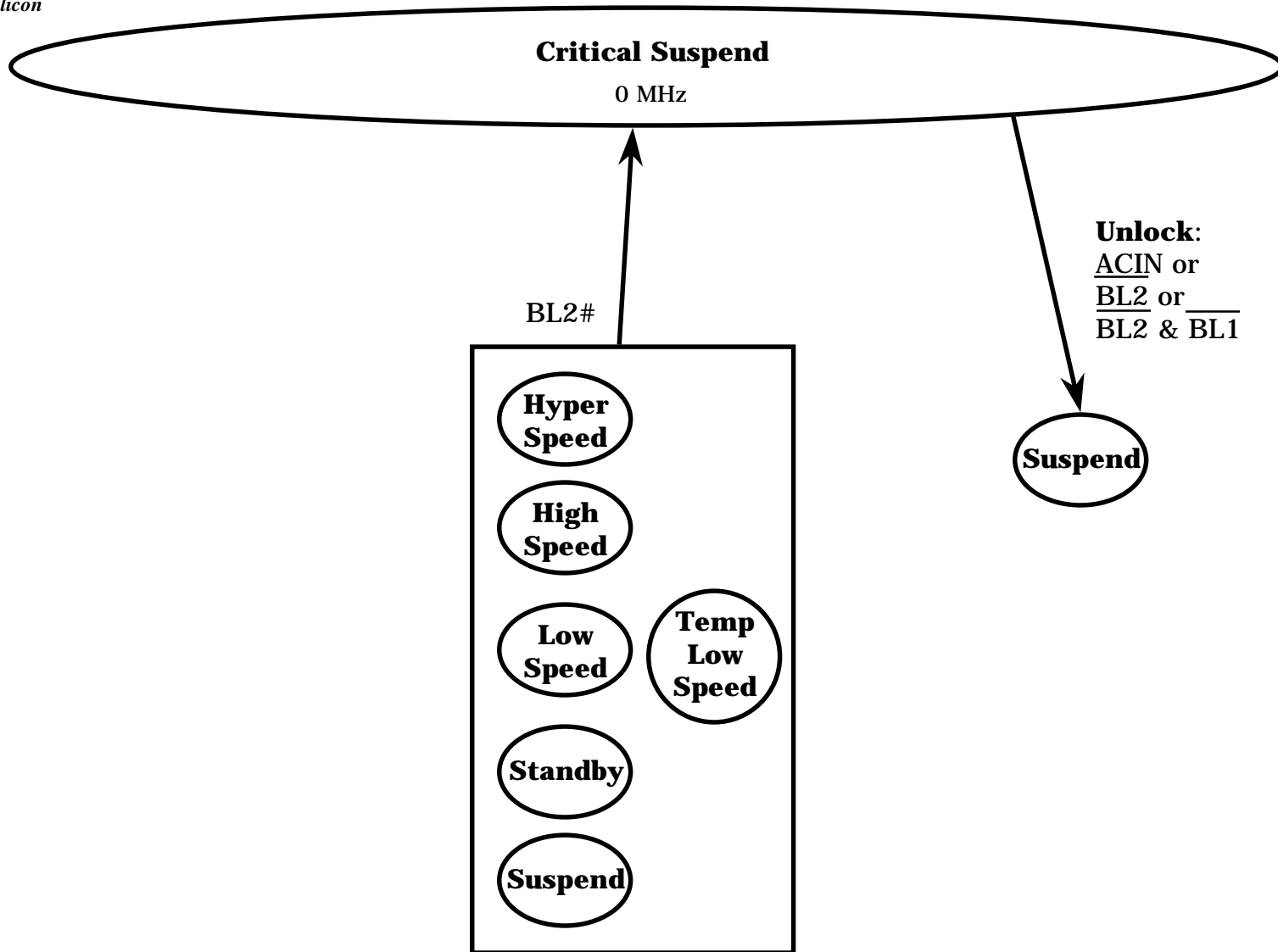
PMU Modes - Suspend





Systems in Silicon

PMU Modes - Critical Suspend





Systems in Silicon

PMU - Events

- Timers
 - Each PMU mode has its own timer
 - Cause automatic stepping down PMU modes to Suspend
 - Lowers system power when there is no activity
 - Allows hardware control of PMU state reduction
- Wake Ups
 - Start the system back up from Suspend
 - Separated out from Activities since wake up is different than changing modes during operation





Systems in Silicon

PMU - Events cont.

- Activities
 - Stop the PMU progression to Suspend and activate the system to respond to something that needs to be done
 - Two levels of activity Primary & Secondary
 - Needed even in a software controlled power management scheme





Systems in Silicon

PMU - Events cont.

- SMI/NMI Interrupts
 - Allow system events to cause an interrupt for special handling
 - SMI's have the advantage of being completely hidden from the application software that is running. The disadvantage is they take longer to enter and exit because the entire state is saved off.
 - NMI's have the advantage of being faster to service than SMI's since less of the CPU's state is saved. Their disadvantage is in they are AT compatible and application software can reprogram them.





Systems in Silicon

PMU - Wake Ups

- SUS_RES pin
- RTC Alarm
- UART Ring Indicate
- UART Receive signal
- Keyboard Key Press
- GPIO's
- DMA Request's
- Interrupt Requests
- Battery signals
- Suspend Timer
- PC Card
 - Card Detects
 - Ring Indicates
 - Interrupt Requests
 - Status Changes





Systems in Silicon

PMU - Activities

- UART Ring Indicate
- UART Receive signal
- Keyboard
 - Key Press
 - Timer Time-out
- GPIO's
 - Pins
 - Address Mapped
- DMA Request's
- Interrupt Requests
- ACIN signal
- PC Card
 - Ring Indicates
 - Interrupt Requests
- CPU Accesses
 - UART
 - Internal Video Controller
 - I/O
 - Memory
 - ROM
 - External Video Controller
 - I/O
 - Memory
 - Floppy
 - Hard Drive
 - Parallel Port
 - PC Card
 - I/O
 - Memory
 - DRAM
 - Internal Registers





Systems in Silicon

PMU - SMI/NMI

- UART Ring Indicate
- UART Receive signal
- Keyboard
 - Key Press
 - Timer Time-out
- GPIO Pin
- Suspend/Resume Signal
- PMU Timer time-out
- ACIN signal
- Wake Ups
- PC Card
 - Ring Indicates
 - Interrupt Requests
 - Card Detects
- Peripheral I/O Trapping
 - GPIO Address Mapping
 - UART Access
 - Parallel Port Access
 - Internal Video I/O
 - External Video I/O
 - Floppy Access
 - Hard Drive Access
 - Keyboard I/O Access
 - PC Card I/O Access





Systems in Silicon

General Purpose I/O Signals (GPIO's)

- 32 Total GPIO's, most shared with another function (ISA, DRAM, etc.)
- 2 Classes - GPIO_CS & GPIO
 - 15 GPIO_CS's are full featured
 - 17 GPIO's are Input/Output only
- GPIO_CS's can be Inputs to be read at a register location
- GPIO_CS's can be Outputs that can be written at a register location





Systems in Silicon

GPIO's cont.

- One GPIO_CS can be programmed to cause an SMI or NMI
- One GPIO_CS can be programmed to be the third ROM Chip Select
- One GPIO_CS can be programmed to toggle for an external keyboard (address 60H/64H)





Systems in Silicon

PMU - GPIO's cont.

- Four GPIO_CS's can be programmable Chip Selects
 - 2 I/O's with a decode of SA9:0 and a mask of SA3:0
 - Address decode qualified with IOR#, IOW#, both, or neither
 - 2 Memories with a decode of SA25:14 and a mask of SA17:14
 - Address decode qualified with MEMR#, MEMW#, both, or neither
 - Programmable for x8 or x16 bit data bus
- Four GPIO_CS's can be outputs that change state based on the PMU mode





Systems in Silicon

PLL - Clocks

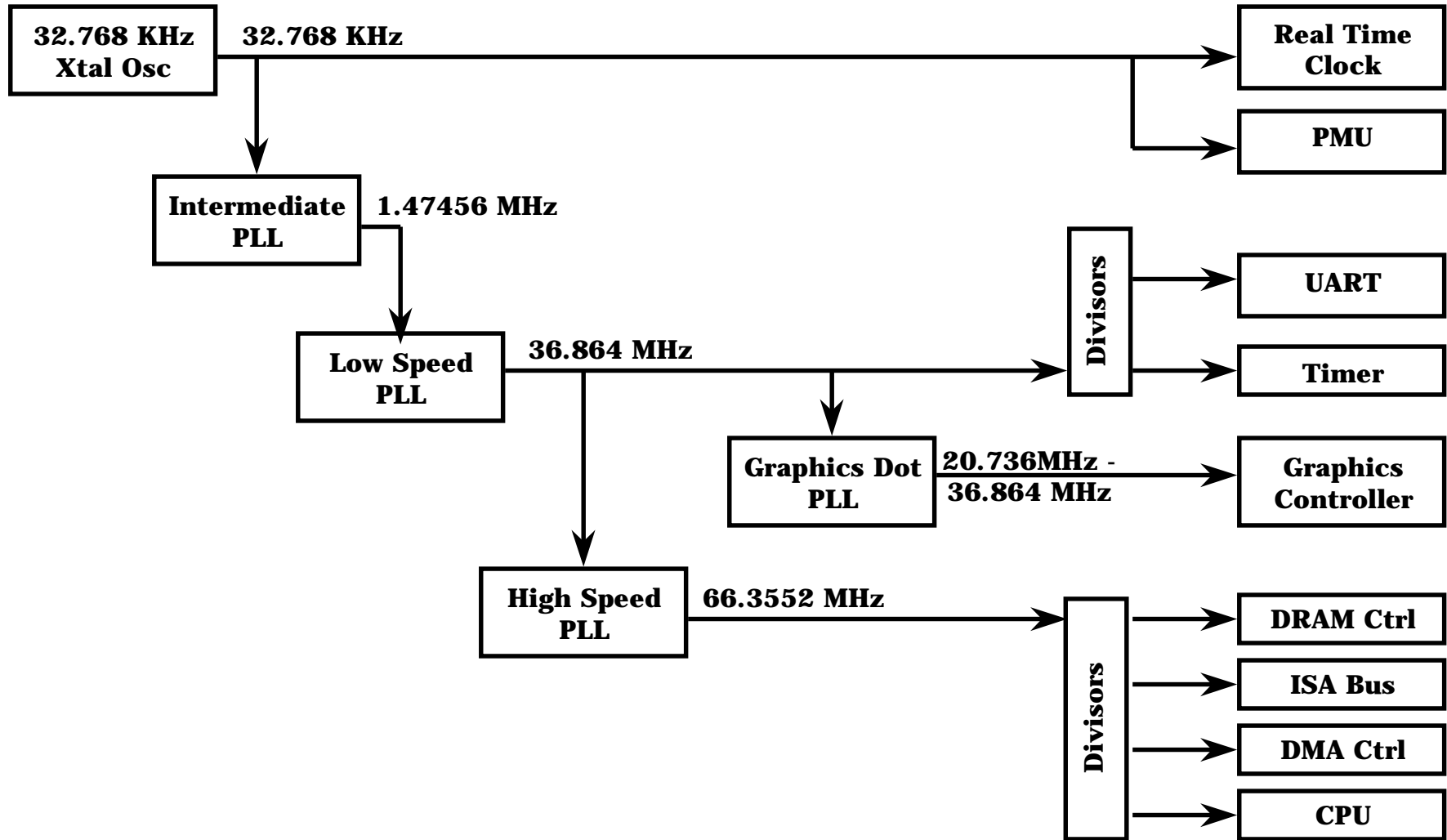
- Phase Lock Loops (PLL) to Reduce Power
 - Four PLLs eliminate external clock oscillators
 - Gives greater control over clocks
 - Generates all '400 clocks and system clocks
 - Only 32KHz Crystal or Oscillator required
- Hyper Speed mode (2x or 3x CPU clock) uses the CPU's internal PLL
 - Multiplies the 33MHz CPU clock to 66MHz or 100MHz
 - 100MHz will need to be soldered to 4 layer board





Systems in Silicon

PLL - Clocks cont.





Systems in Silicon

PMU - Battery Monitoring

- AC In signal to disable most PMU functions
 - Automatically change system to maximum performance when “unlimited” power is available
- Three programmable Battery Low signals available





Systems in Silicon

PMU - Battery Monitoring cont.

- BLO# & BL1#
 - Disable Hyper-Speed mode
 - High Speed Mode becomes the highest mode available
 - Disable High-Speed mode
 - Low Speed Mode becomes the highest mode available
 - Limit High-Speed mode to 8MHz
- BL2#
 - Force the PMU into Suspend mode (Critical Suspend)
 - Saves system state when the battery is too low to power the system





Systems in Silicon

Voltage Partitioning

- No 5 Volt VCC's on the chip
 - Many signals are 5V safe
 - ISA Bus
 - ROM
 - 32 bit low word needs data buffers
 - D[15:0] not 5V safe
 - PC Card
 - Parallel Port
 - XT Keyboard
 - LCD
 - Not all signals 5V safe to reduce die size, 5V safe pads are larger than normal pads
 - 5V safe signals are limited to two sides of the die





Systems in Silicon

Voltage Partitioning cont.

- Power planes are segmented to allow additional power savings
 - CPU voltage can go down to 2.7 volts
 - The CPU accounts for 75% (@33MHz) to 90% (@100MHz) of the chip power
 - Real Time Clock voltage can be run separate from rest of chip, can go down to 2.4 volts
 - The Core voltage is 3.3V
 - The rest of the power planes are 3.3V and are for the pads
 - Separated by interface to allow easier debug of problem currents





Systems in Silicon

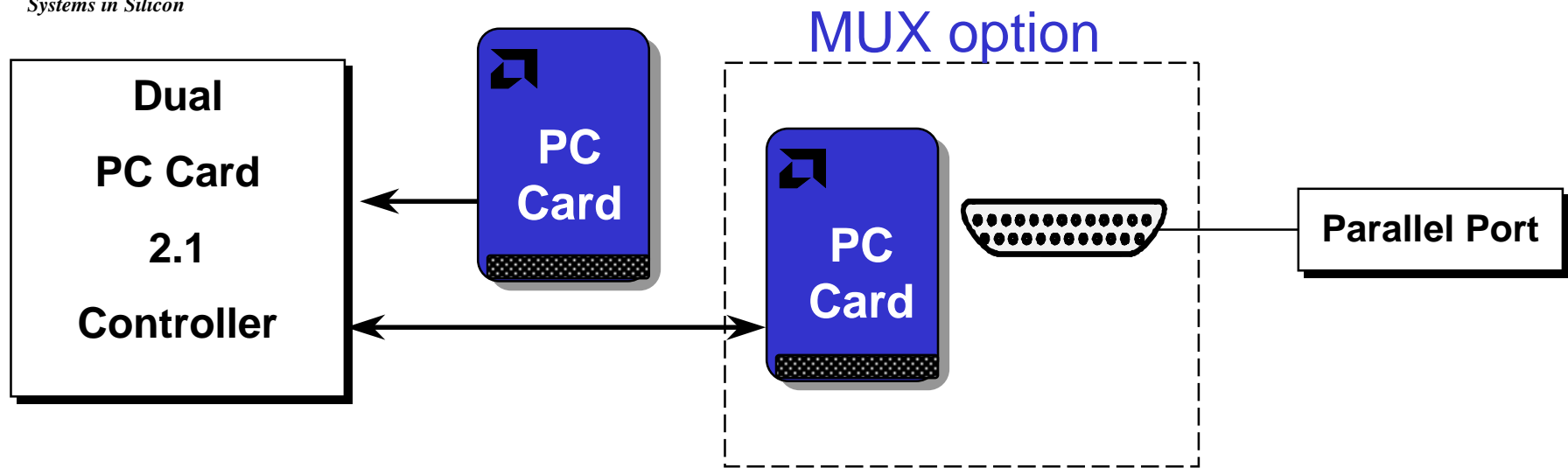
Segmented Power Planes

- Core Power Planes:
 - 486 CPU..... 2.7V - 3.3V
 - Core Logic other than the CPU..... 3.3V
 - Analog..... 3.3V
 - Real Time Clock..... 2.4V - 3.3V
- I/O Power Planes:
 - DRAM Interface 3.3V
 - Data Bus Interface 3.3V (5v tolerant)
 - System Interface..... 3.3V (5v tolerant)
 - LCD / VL Bus Interface..... 3.3V(5v tolerant)
 - PC Card Interface..... 3.3V(5v tolerant)
 - Serial Port Interface..... 3.3V





PC Card Controller



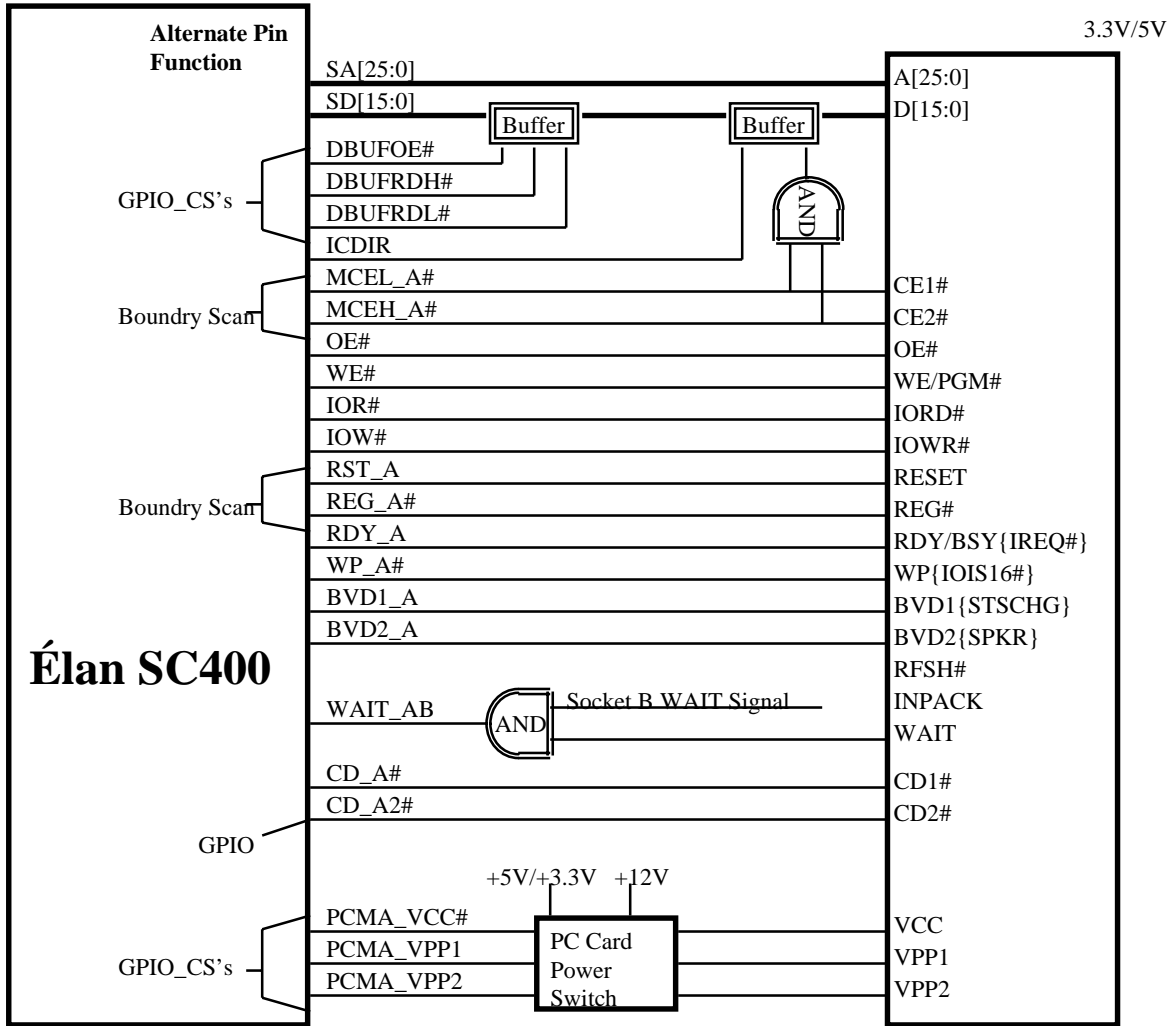
- Support for one or two slots
 - Slot A is dedicated
 - Slot B is mux option with Parallel Port
- ExCA register set compatible
 - Benefit: Standard Card and Socket Services
- PC Card 2.1 compliant
- 5 volt tolerant, 3.3v drive

**Note: ÉlanSC410
Microcontroller
Only has Parallel Port
No PC Card!**



Systems in Silicon

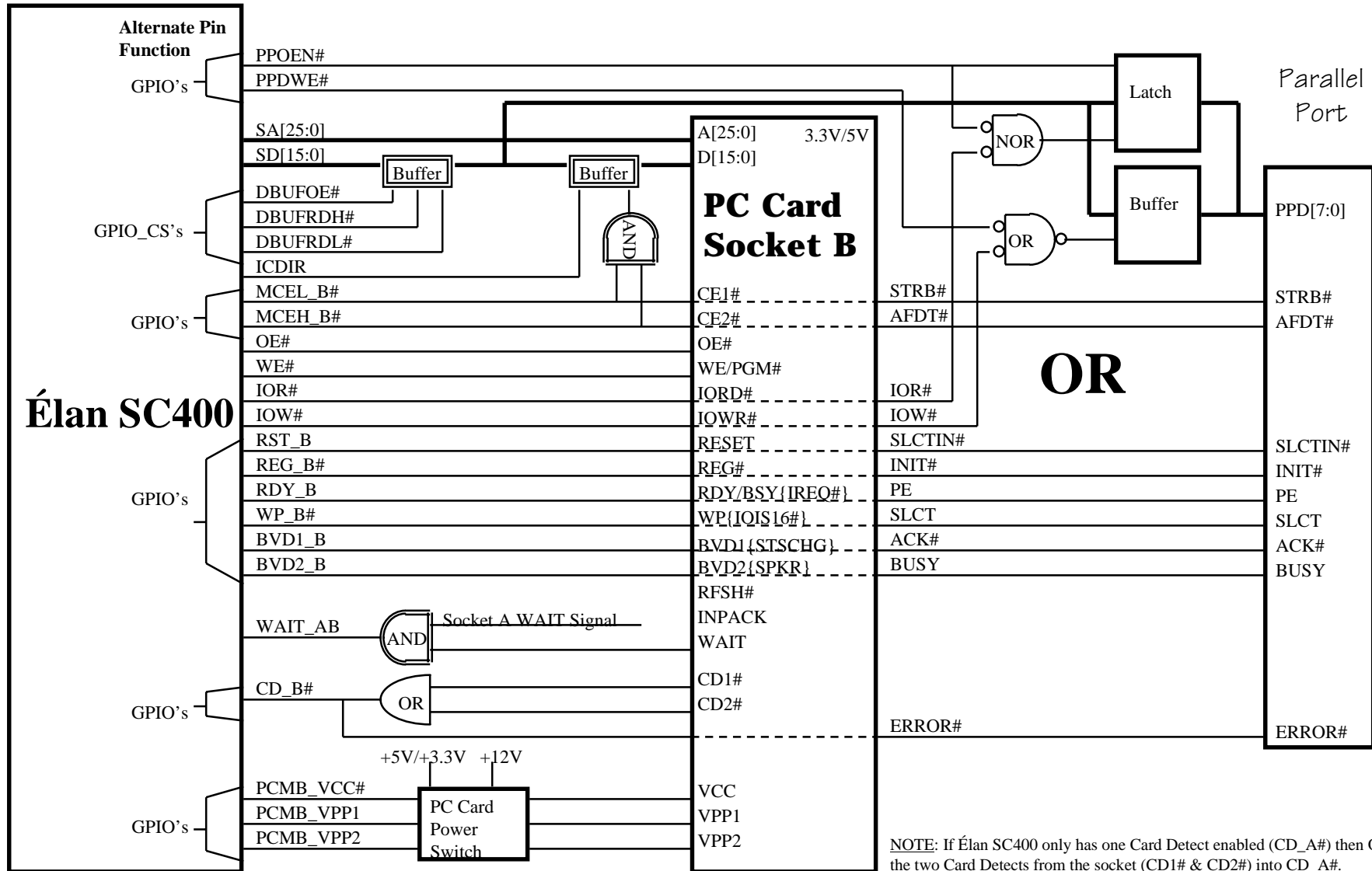
PC Card Socket A Interface



NOTE: If Élan SC400 only has one Card Detect enabled (CD_A#) then OR the two Card Detects from the socket (CD1# & CD2#) into CD_A#.



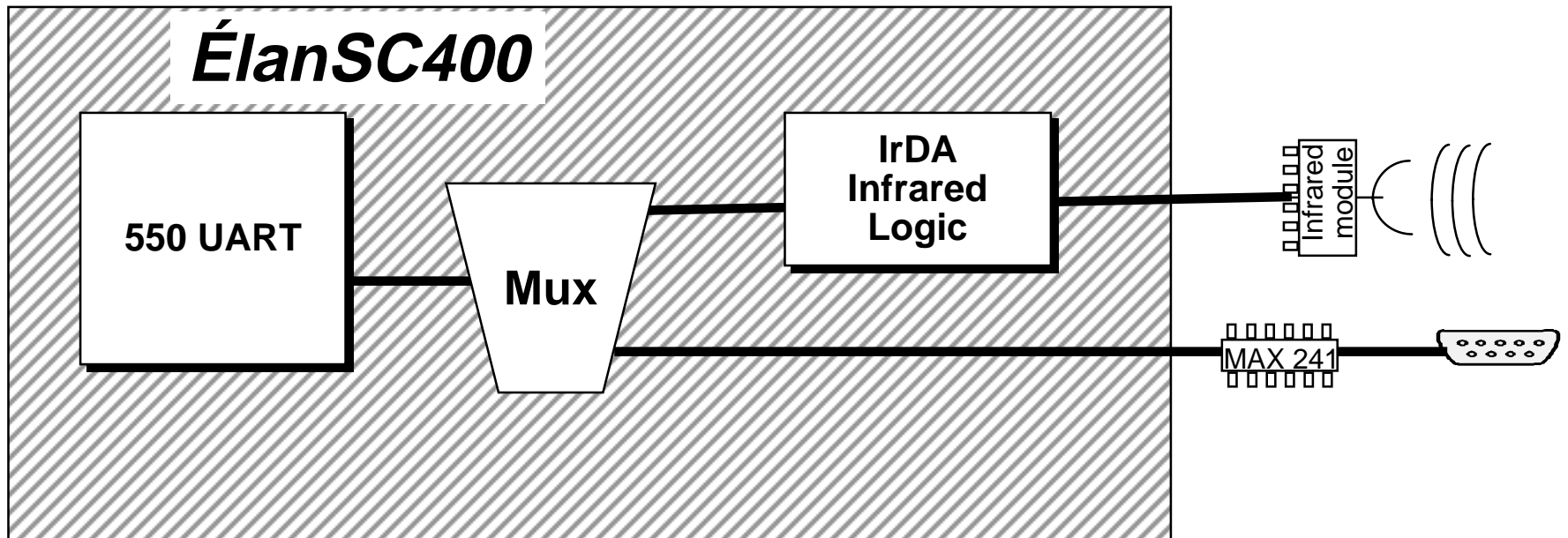
PC Card Socket B / Parallel Port Interfaces





Systems in Silicon

UART and Infrared

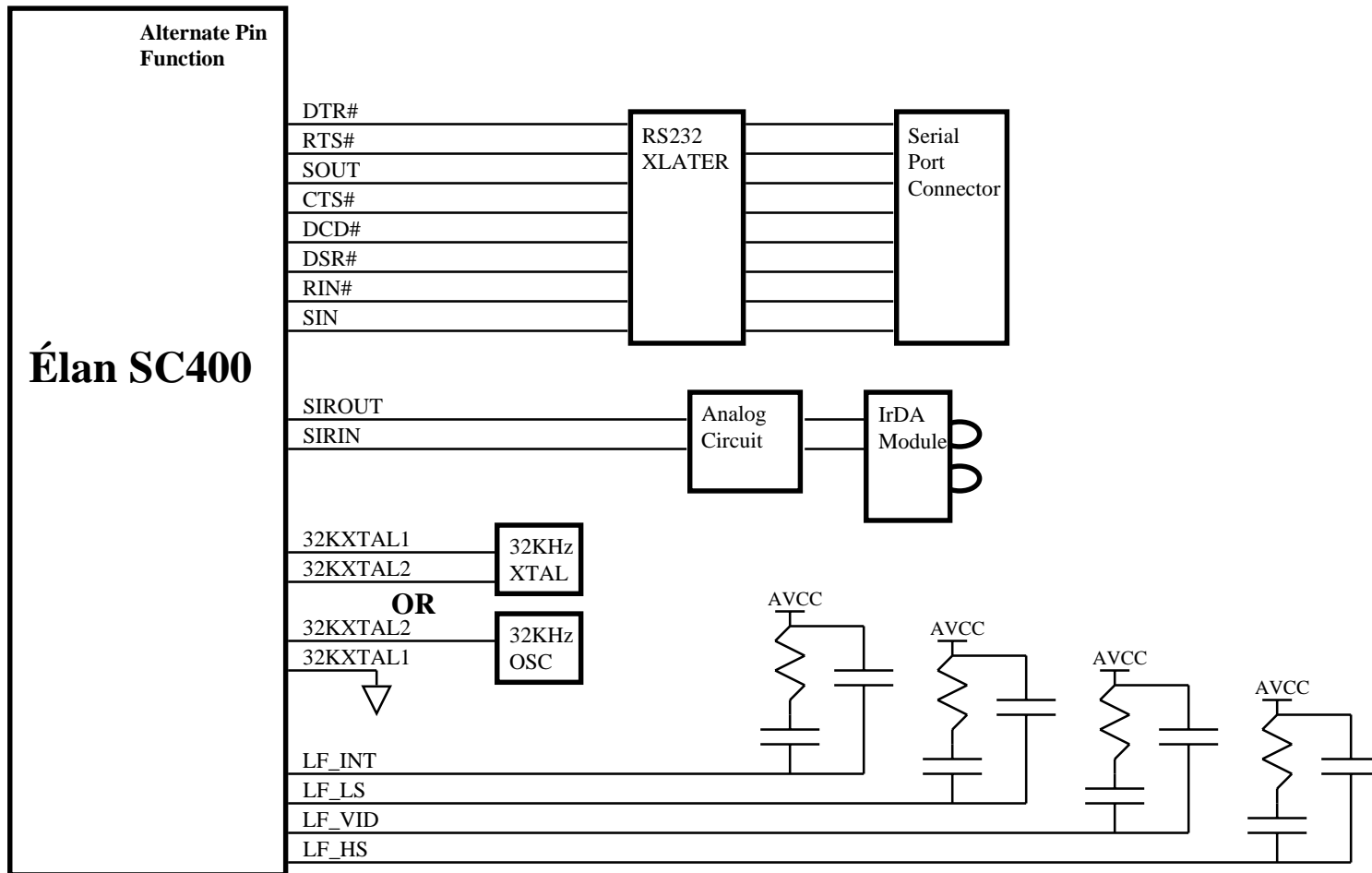


- 550 UART
 - Either RS232 out or Infrared (register programmable)
 - Can support both in a system, but not simultaneous
- Infrared (IrDA 2.0 compliant)
 - 115 kbps and 1.15 Mbps



Systems in Silicon

UART / IrDA / Misc Interfaces





Systems in Silicon

Keyboard Interface

- 3 Keyboard Types Supported
 - XT Keyboard
 - Matrix Scan Keyboard
 - External SCP supported with a chip select
- Matrix Scan
 - 15 Row & 8 Column Signals
 - Typical Implementation: 88 keys (11 Rows x 8 Columns)
 - 3 Rows dedicated to multi-press keys (Shift, Ctrl, Alt)
 - 1 Row for Suspend/Resume switch or Lid Switch
 - Supports PC/AT compatible emulation registers 60/64H
 - Signals MUX'ed over extra ISA & 32bit DRAM control signals





Systems in Silicon

Keyboard Interface cont.

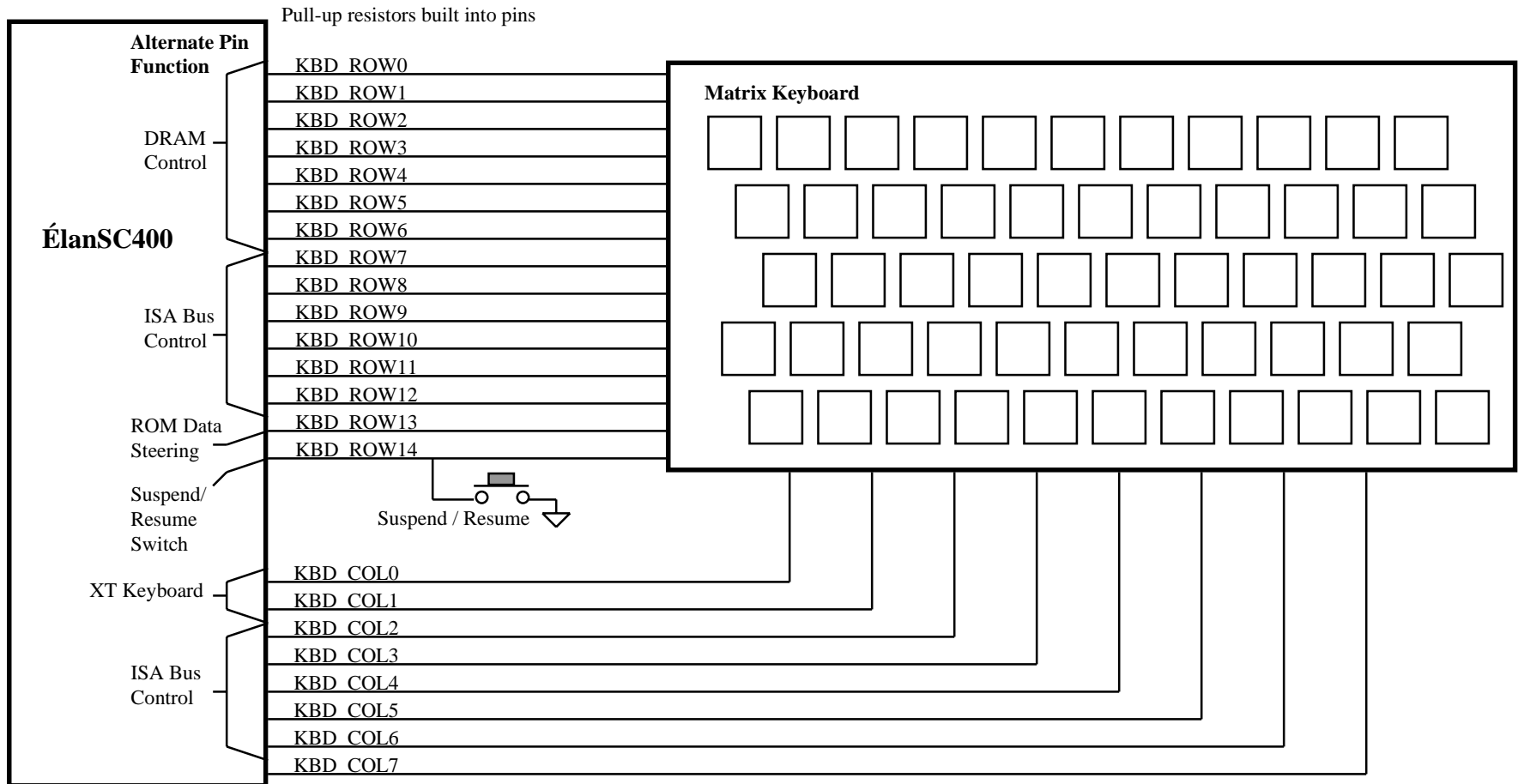
- Keyboard Row 14 is shared with the Suspend / Resume switch function
 - Independent Suspend & Resume enables
 - Rising / Falling Edge programmable
- Can be programmed for use as:
 - Push button switch
 - Lid switch
 - Ordinary keyboard row





Systems in Silicon

Matrix Keyboard Interface





Systems in Silicon

Graphics Controller

- LCD Graphics controller built in
 - On the Local Bus for highest performance
 - Does not support a CRT
 - Supports Text and Graphics modes
 - Font support for 8, 10, & 16 pixels wide
- Support for Monochrome & Color STN LCD's
 - Single Scan Color STN LCD
 - Single & Dual Scan Mono STN LCD
 - Up to 640x480 resolution
 - Up to 4 bits per pixel





Systems in Silicon

Graphics Controller cont.

- Capable of Supporting many O/S's
 - RTOS
 - DOS
 - Windows 3.1 & 95
 - Geos
- LCD voltage controls
 - Programmable sequence timing when panel enabled & disabled





Systems in Silicon

Graphics Controller cont.

- Dot clock selection and division to match LCD timing needs
 - Dot Clock PLL programmable from 20.7MHz - 36.9MHz in ~2MHz increments
 - PLL Dot Clock output further division x 1, 2, or 4
 - Final Dot Clock frequencies from 5.2MHz - 36.9MHz
- Gray Scale remapping to adjust contrast to clarify images on the LCD





Systems in Silicon

Graphics Controller cont.

- CGA register set with additional registers for flexibility
 - Not VGA support
 - Too much die area (>30K gates)
 - UMA is much less effective at full VGA resolutions
 - Panel size and memory size are individually programmable
 - On a smaller than normal LCD allows easy panning around full screen
 - With custom applications image can fit to screen
- AC Modulation
 - Programability to help eliminate ghosting on LCD

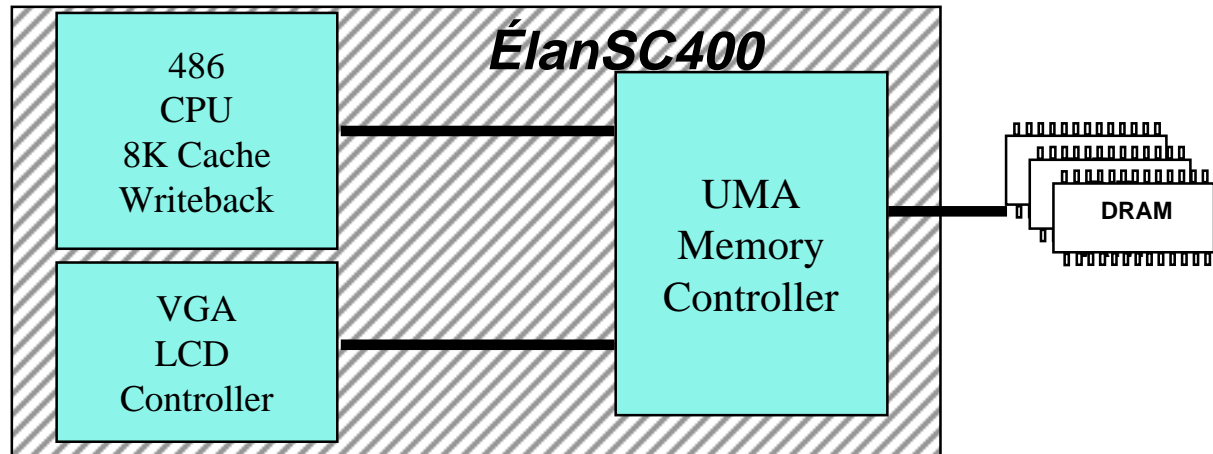




Systems in Silicon

ÉlanSC400 Microcontroller Unified Memory Architecture

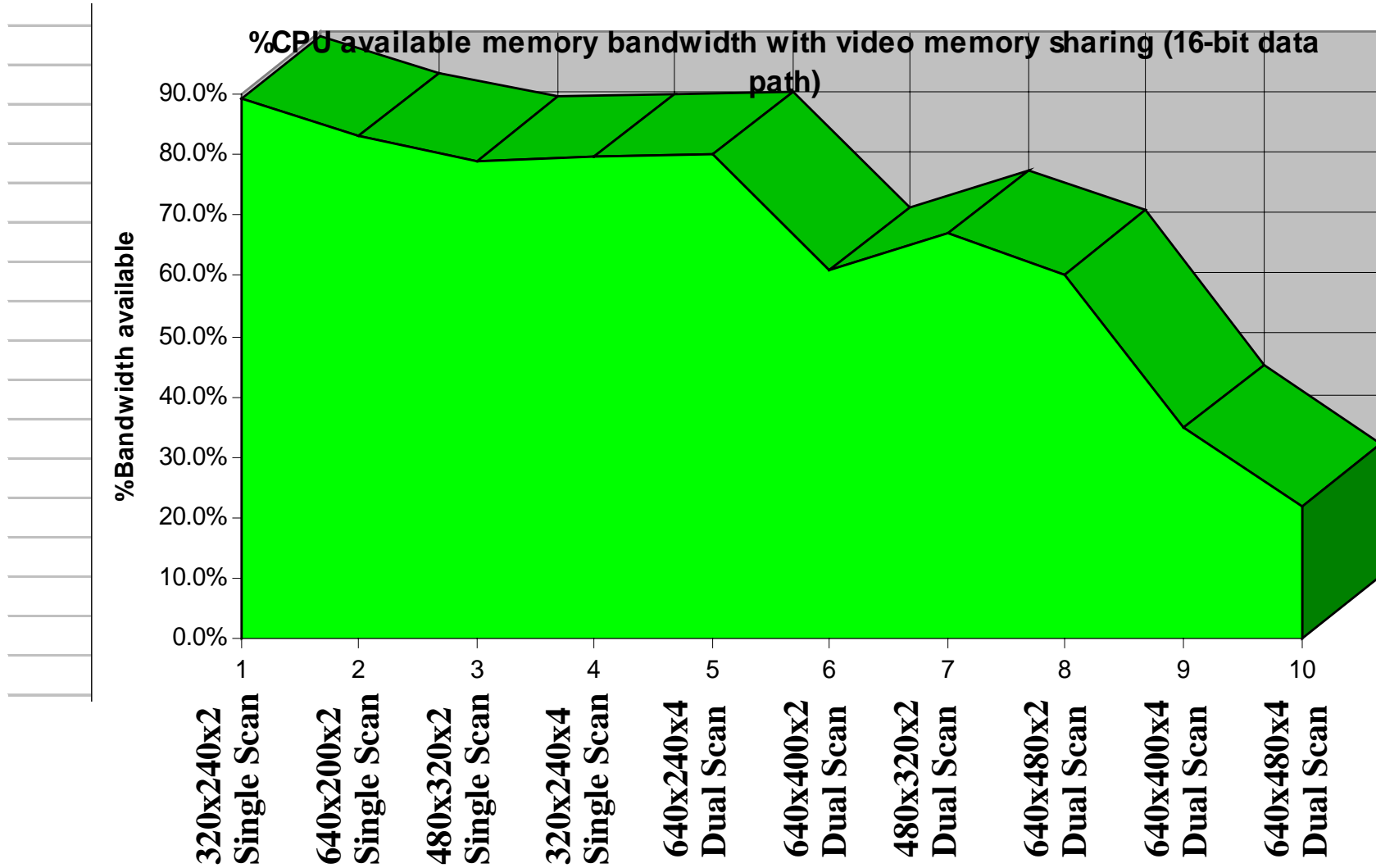
- Feature - Single memory interface for both Video and CPU
 - Eliminates need for a video memory on the board
 - 320x240 4bpp => 37.5K Bytes - No acceptable SRAM solution
 - Smallest available DRAM leaves a lot of unused memory
- Architecture designed for performance
 - 486 cache provides isolation from video refresh
 - Writeback further decreases CPU memory needs





Systems in Silicon

CPU Bandwidth -vs- Graphics Mode



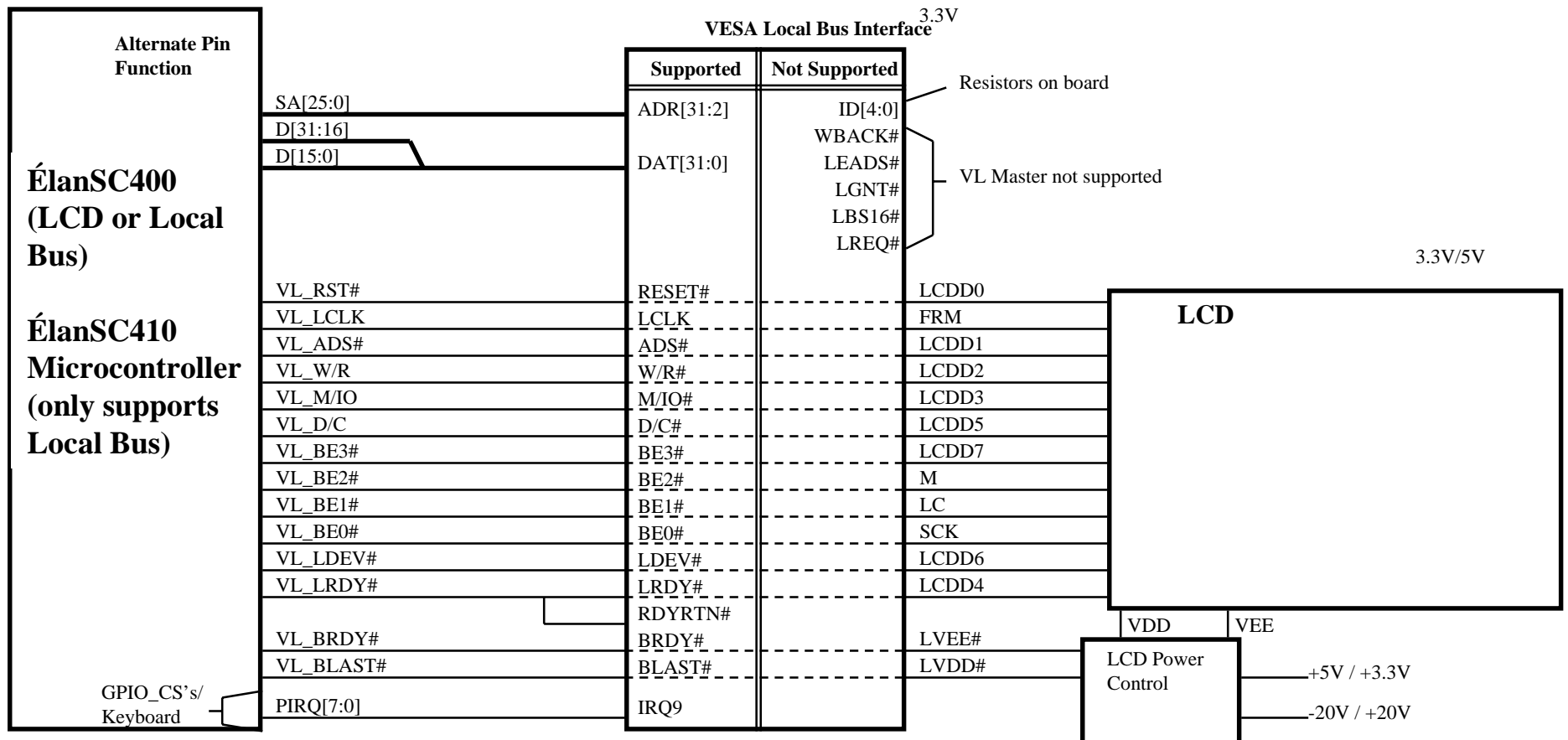


Systems in Silicon

Local Bus / LCD Interfaces

The Internal Graphics Controller is only available when there are NO 32-bit devices in the system (VL bus, x32 DRAM banks, x32 ROM).

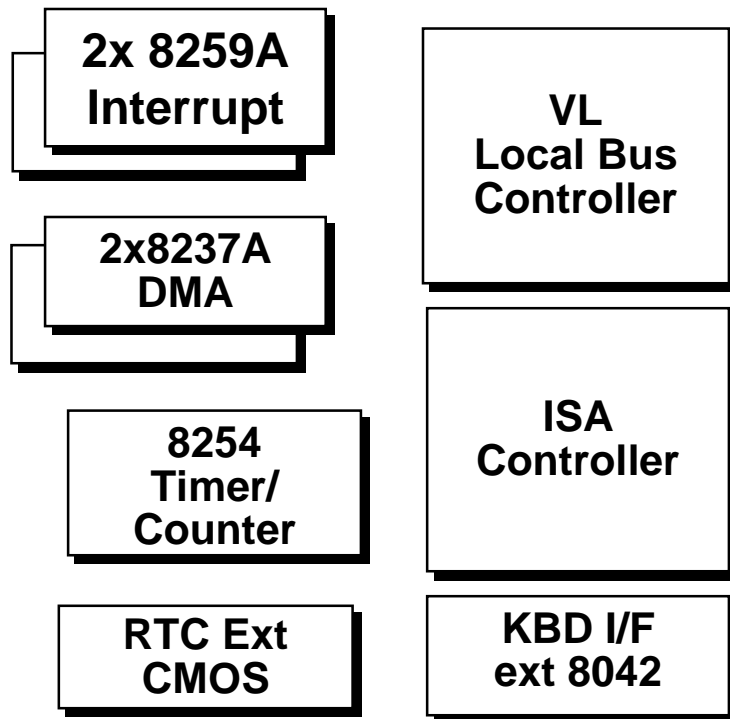
VL Bus OR LCD





Systems in Silicon

PC/AT Logic Compatibility



- DMA allows
 - High Speed IR (1Mbit/sec)
 - Floppy, Audio
- ISA bus
 - Extensibility to standard peripherals
 - Standard ISA signals are supported, but no masters
- VL Local Bus
 - High speed standard bus allows for higher performance straight from 486 CPU bus



Systems in Silicon

PCI/AT Architecture Advantages

- 100% compatible with existing systems
 - Hardware, software and data
- Excellent price / performance metrics
- Time To Market and low development investment
 - Easily prototyped products
 - Legacy software and hardware
 - Desktop industry provides economical standards
- Ease of development & debug
 - Powerful tools from desktop industry
 - BIOS and RTOS support





Systems in Silicon

ISA Bus

- Not a full ISA Bus - Several signals eliminated to reduce complexity & save pins
 - Master Mode (MASTER#)
 - Zero Wait State (OWS#)
 - Not necessary for ISA operation
 - Refresh (REF#)
 - DRAM refresh cycles are not echoed to the ISA Bus
 - Low Meg Memory Read & Write (SMEMR#, SMEMW#)
 - If needed can be generated with address decode and MEMR# & MEMW#





Systems in Silicon

ISA Bus cont.

- I/O Channel Check (IOCHCHK#)
 - Used to generate an NMI in the system
 - GPIO_CSx can generate an NMI
- ISA Bus clocks (SYSCLK, 14.3MHz)
 - If needed, can be generated with oscillators on the board

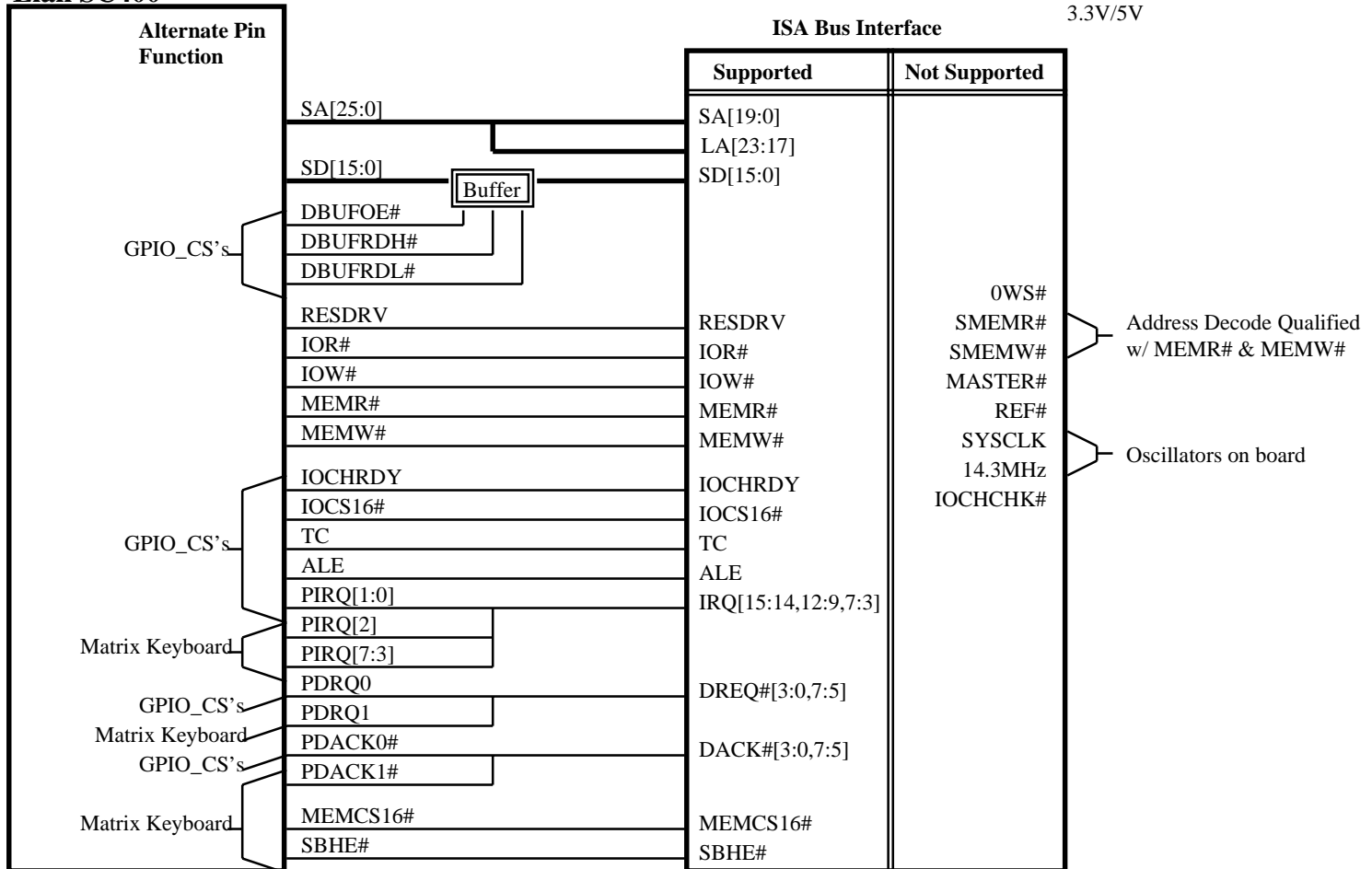




Systems in Silicon

ISA Bus Interface

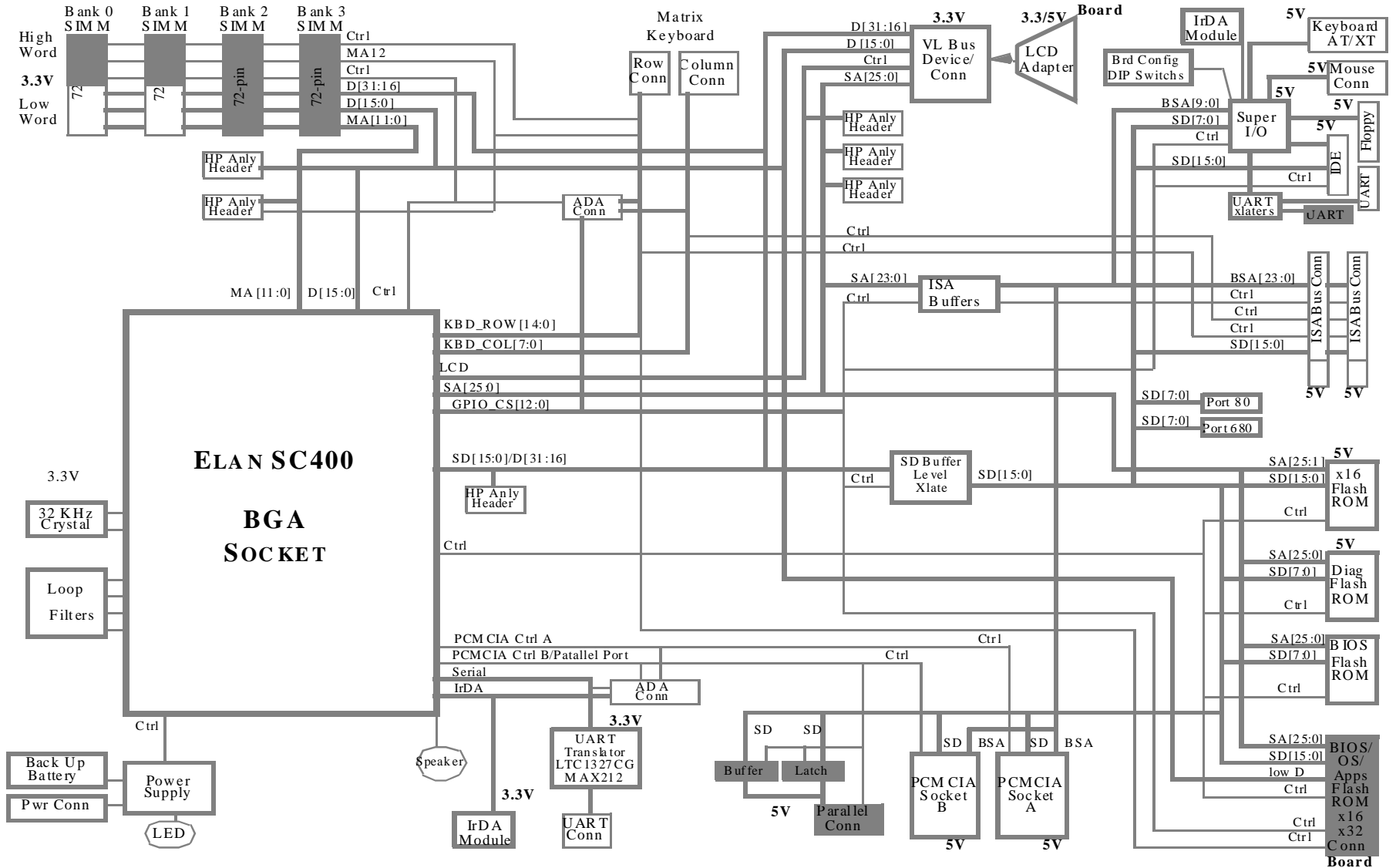
Élan SC400





Systems in Silicon

Evaluation Board Block Diagram

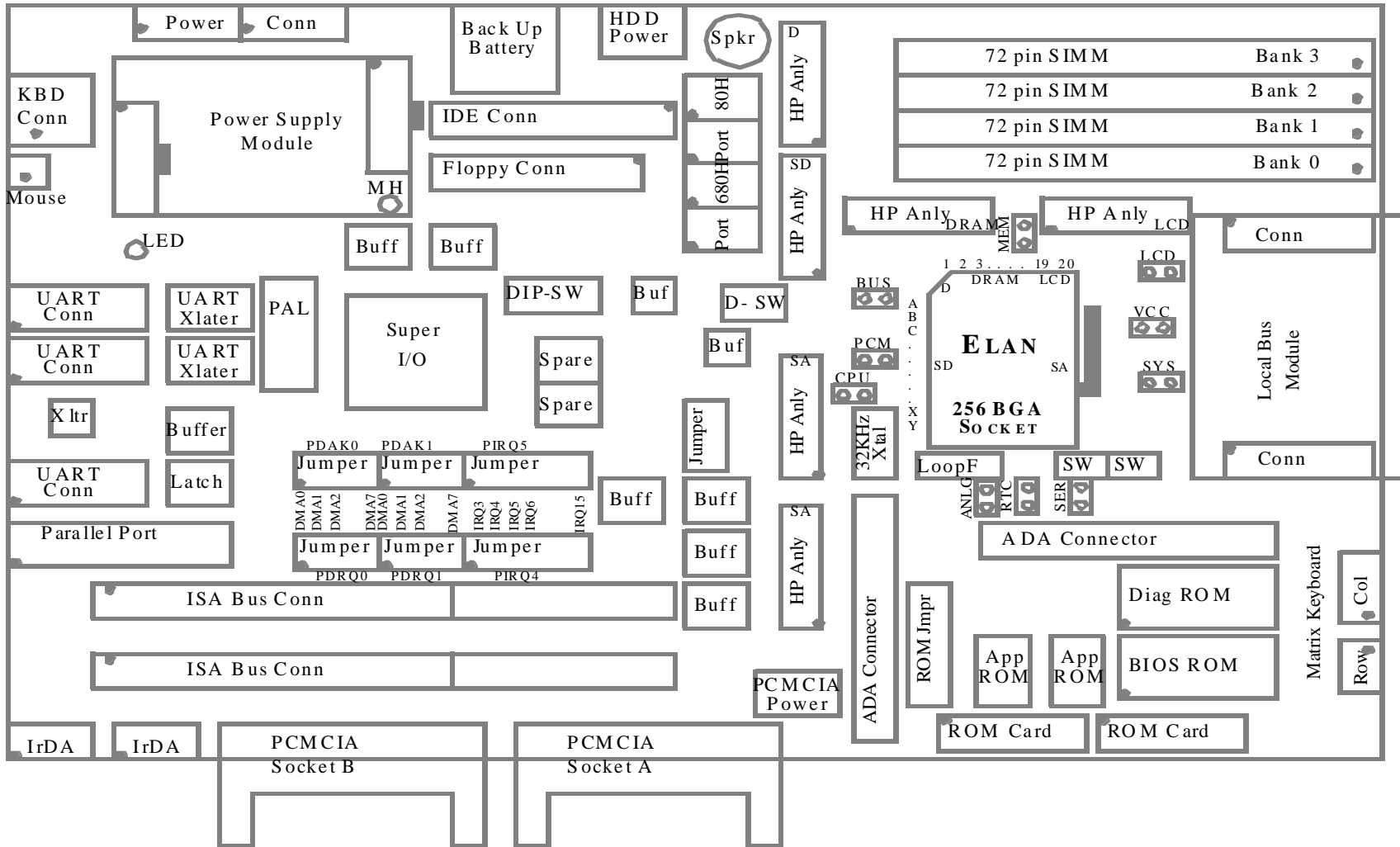




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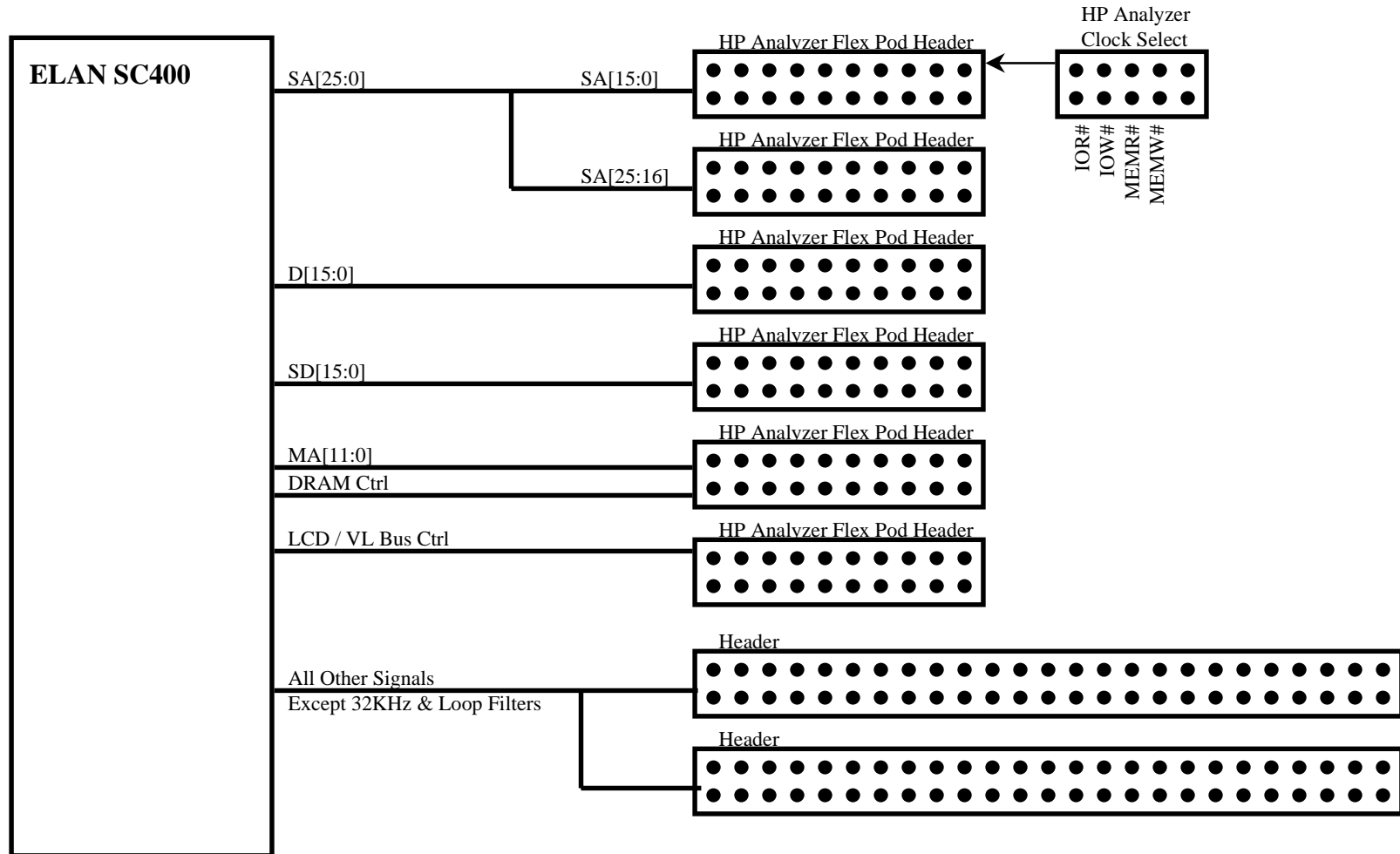
Evaluation Board Layout

Board is Baby AT Size: 8.5" x 13"
 6 layer - VCC, GND, 4 Signal - All components on TOP





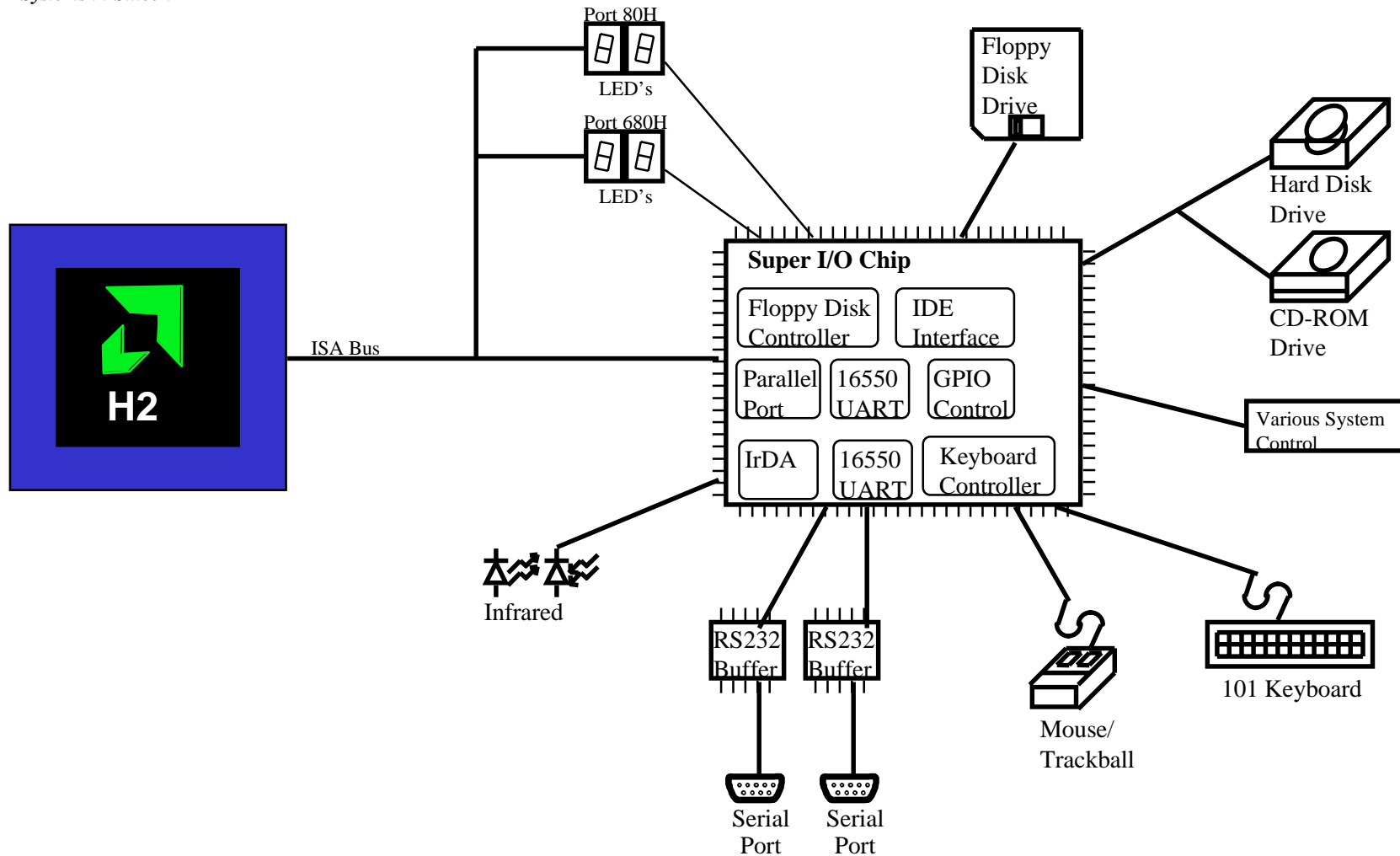
Development Features





Systems in Silicon

Development Features cont.





Systems in Silicon

Switches & Jumpers

- Jumpers to measure all Power Planes on the board and on the ELAN SC400 chip.
- Board sections:
 - DRAM (3.3V)
 - ISA Bus Devices (5V)
 - Serial Port (3.3V)
 - ROM's (5V)
 - PC Card (5V)





Systems in Silicon

Switches & Jumpers cont.

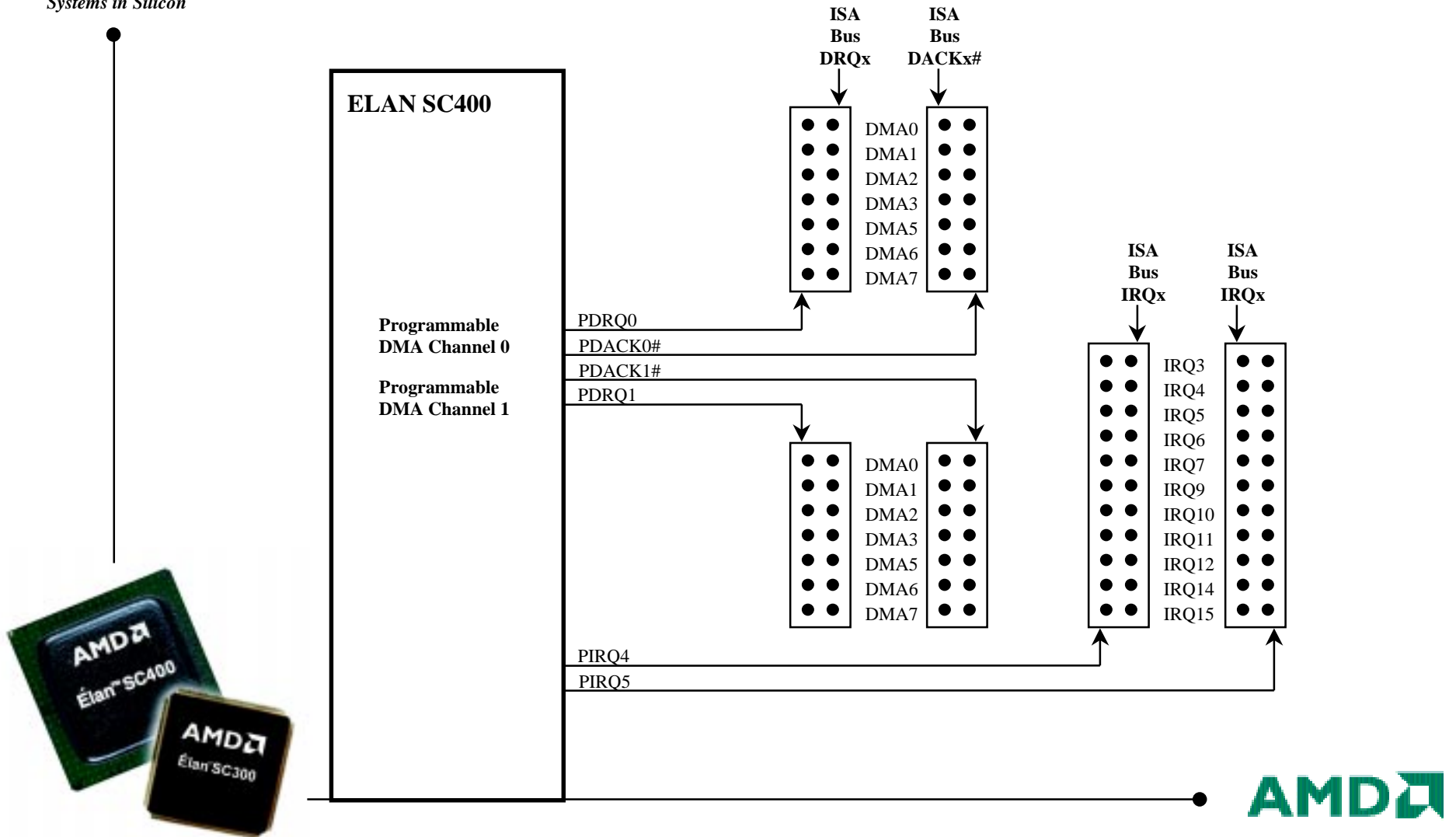
- ELAN SC400 Power Planes:
 - 486 CPU (2.7V - 3.3V)
 - Analog (3.3V)
 - Core Logic other than the CPU (3.3V)
 - Real Time Clock (2.4V - 3.3V)
 - DRAM Interface (3.3V)
 - Data Bus Interface (3.3V)
 - System Interface (3.3V)
 - LCD / VL Bus Interface (3.3V)
 - PC Card Interface (3.3V)
 - Serial Port Interface (3.3V)





Systems in Silicon

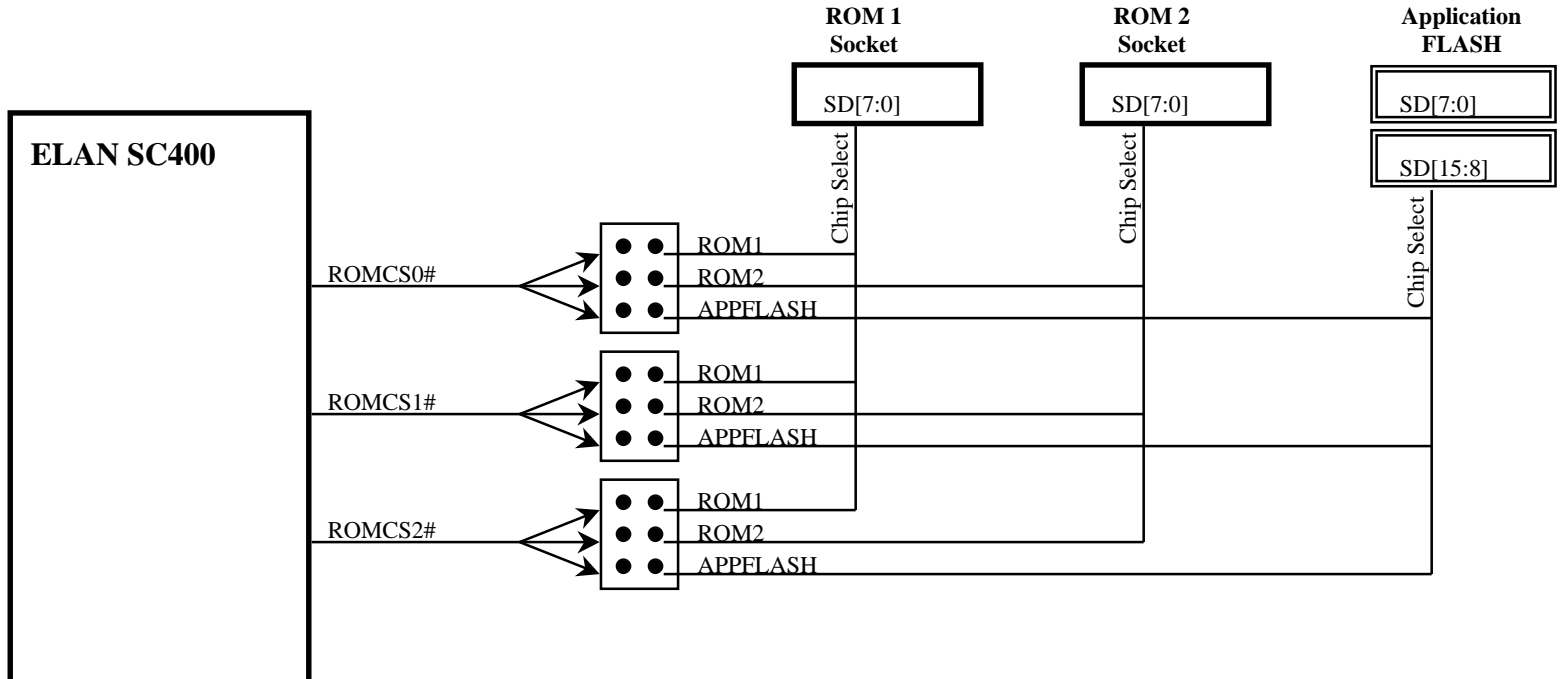
ISA Bus DMA & IRQ Routing





Systems in Silicon

ROM Selection



The Application FLASH is two 2Mx8 TSOP FLASH parts soldered on the board.
 The ROM1 & ROM2 Sockets are DIP Sockets on the board; they can be jumpered to be ROM, FLASH, or SRAM.

