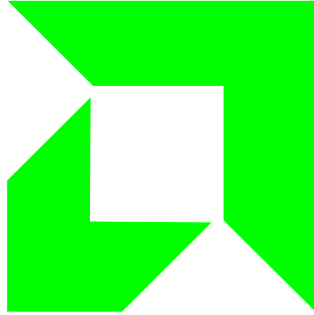


Gigabit Ethernet PHY Solutions



AMD

Users Manual

GigaPHY-SD

Gphysd_1a

Gigabit Evaluation Board

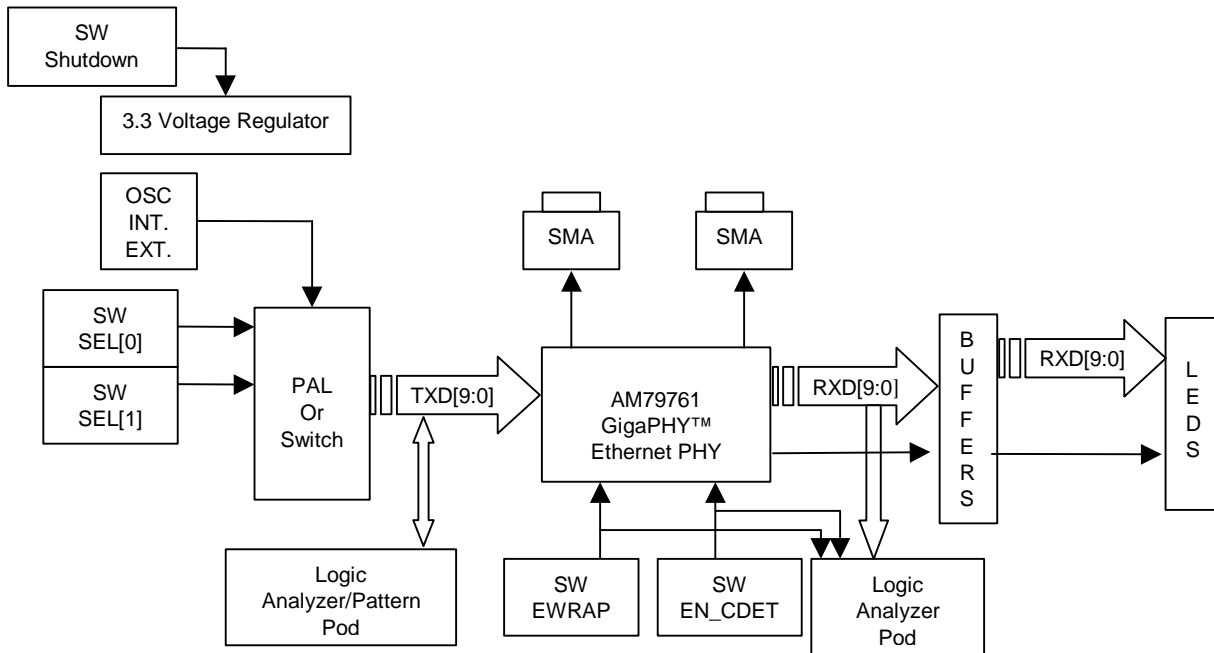
GigaPHY™-SD Device

Physical Layer 10-Bit Transceiver for Gigabit Ethernet

Features

- Evaluation System for use in studying the GigaPHY™ Am79761.
- Switches for Driving Control Lines.
- LED's for Monitoring Control Lines.
- On Board Generation of 3.3V from External 5V through 12V supply.
- Internal or External Clock Source.
- 10-bit Transmit Data Provided From Switches or onboard PAL or from a Pattern Generator.
- 10-bit Receive Data Monitored on LED's or Through a Logic Analyzer Pod.

Block Diagram



GigaPHY™ -SD Device

GDPHYSD_1A
Eval Board

General Description

The GigaPHY™ GPHYSD_1A Board, provides a low cost, easy-to-use tool to evaluate the Gigabit Transceiver, AM79761, with regard to signal quality and performance. It is intended that the GigaPHY™ board be a self-contained Evaluation Unit. In its simplest form, the switches on the GPHYSD_1A can be used to set the transmit data and control lines while monitoring received data and status lines with LED's. A pre-programmed PAL in addition to the switch settings can generate simple word patterns.

More in-depth evaluations can be implemented by connecting a Pattern Generator (10-bits at 125MHz) to pods on the board in order to generate transmit data and control signals. A logic analyzer can also be connected to pods on the board in order to monitor receive data and status signals. With this setup 8B/10B data can be sent to the transmitter on the Evaluation Unit to generate Gigabit data and monitored on the Logic Analyzer.

Other useful features of the board include the presence of an on-board, removable oscillator with Tri-state (normally at 125MHz) in a DIP, half DIP or Surface Mount form. An on-board voltage regulator is used to provide 3.3V to the board with a shutdown switch used to turn off power to all components.

Scope of this Document

It is intended that the AM79761 datasheet be used for reference in understanding the device function. Additionally, the following items are enclosed in this document:

1. Schematics for the board
2. Artwork for the board (copies of each layer)
3. Fabrication drawing for the board
4. Bill of materials for the board.

Operation and Switch Settings

HP1	TXD	Logic Analyzer/Pattern input	P4	EWRAP
HP2	RXD	Logic Analyzer	P5	EN_CDET
LED0	RXD[0]	Status	PWR1	Ext. Lab bench +5V DC supply
LED1	RXD[1]	Status	PWR2	Ext. Wallmount +5V DC supply
LED2	RXD[2]	Status	SMA1	External 125Mhz Clock Install [0]ohm resistor R2 and W1[to Tristate Clock Crystal].
LED3	RXD[3]	Status	SMA2	TX[+] Output
LED4	RXD[4]	Status	SMA3	TX[-] Output
LED5	RXD[5]	Status	SMA4	RX[+] Output
LED6	RXD[6]	Status	SMA5	RX[-] Output
LED7	RXD[7]	Status	SMA6	RCLKN Output
LED8	RXD[8]	Status	SMA7	RCLK Output
LED9	RXD[9]	Status	SW1	Manual Setting to TXD[0:9]
LED10	COMDET	Comma Character Status	U1	AM79761
LED11	+5POS	External Power Supply Input indicator	U2	PAL for TXD[0:9] inputs
LED12	+3.3	Power Supply Input indicator	U3	Buffer to LED's
LED13	/SHDN	Status for Voltage Regulator if [ON] Shutdown [OFF] Enabled	U4	Buffer to LED's
LED14	SEL[0]		VR1	+5POS to +3.3POS Voltage Regulator with Shutdown.
LED15	SEL[1]		W1	TRI-STATE Jumper to Tri-State Clock Crystal output.
LED16	EWRAP		X1	125 MHz Clock Crystal.
LED17	EN_CDET		ZTP1	VDDIN [+5 volt power supply].
P1	/SHDN	[H] Voltage Regulator is [ON] Power to DUT [L] Shuts down the Voltage Regulator[OFF] No power to DUT.	ZTP2	+5POS going to Voltage regulator.
P2	SEL[0]		ZTP3,5,6,7	DVSS
P3	SEL[1]		ZTP4	DVSS

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Layout Considerations

The board has been designed in a simple, straightforward manner in which highest priority was given to properly routing of high-speed signals. This four layer, controlled impedance PCB contains signal layers on the top and bottom of the board with internal Power (Vdd=3.3V) and GND planes. Components are mounted on both sides of the board so that passives may be placed as close as possible to their ideal location regardless of which side of the board the part is placed. The PCB accommodates a special socket for the AM79761 so placement of passives on the topside near the pins was not possible.

The 1Gb/s transmit and receive signals between the chipset and the connector were the first priority. Since they form a differential PECL pair these traces were of minimal and equal length and, in this example, have characteristic impedance of 50 ohm. The passive components should be packed as closely as possible to minimize stub lengths and maximize signal quality. On the receiver inputs, minimization of trace length between the AC Coupling Caps (C28/C29), the input pins (RX[+],RX[-]) and the 182 ohm termination resistors are very important since the terminator resistors act as the virtual end of the line. Stubs on these lines will cause degradation of signal quality into the receivers due to reflections.

Diagonal corners were used so as to avoid the impedance mismatches found in right angle traces. The same considerations as other high-speed signals apply here.

Transmit data jitter is generated through two main factors: Power Supply Noise and TBC jitter. Proper layout of the REFCLK traces is essential to minimize REFCLK jitter into the part. Curved traces are used to minimize reflections. Generous bypassing of the power supplies and separate isolation and decoupling for each sensitive supply type is one easy method to eliminate much of this noise.

In general, common layout/placement techniques developed for lower speed PCBs apply here and should lead to first-pass success.

GigaPHY™ -SD Device

GDPHYSD_1A
Eval Board

Table 1: Bill of Materials

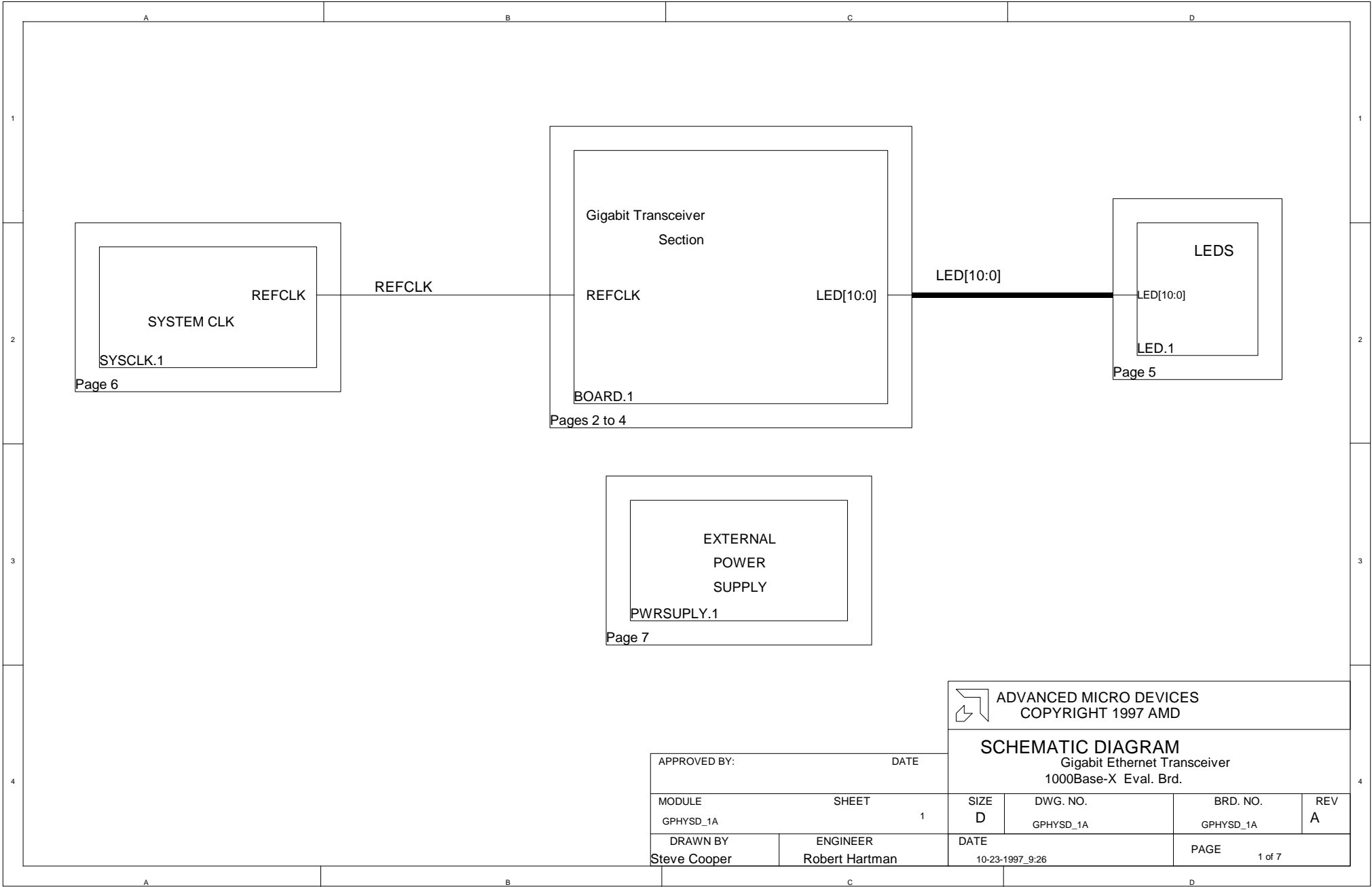
Item	Qty.	Device Description	Part Number	Manufacture	Reference Number
1)	2	Straight .1"x.1" 20 pin Low Profile Header	2520-6002UG	3M	HP1-2
2)	1	Gigabit Ethernet Transceiver	AM79761	AMD	U1
3)	1	64 pin QFP socket	SKT-QFP-14M-17.2-1.0M-VIT	OZ TEK	U1
4)	4	Head Cap Screw #4 ,40UNRC ,3/32-Key ,3/8"length	63086	ASMCO Accurate Screw Machine Company	U1
5)	4	#4 Hex Nut	#4 Hex Nut	ASMCO	U1
6)	4	#4 Washer	#4 Washer	ASMCO	U1
7)	1	2 pin jumper	103240-1	AMP	W1
8)	1	Shunt	15-38-1024	MOLEX	W1
9)	1	Euro Terminal Block 2 PIN	5LEV-02	Augot	PWR1
10)	1	10 Position Surface Mount Extended Actuator Dip Switch	ADE10S	Augot/Alcoswitch	SW1
11)	5	Surface Mount Toggle Switch SPDT	GT11MSCKE	C&K	P1-5
12)	7	P.C. Pin	10-8025-2-03	Concord	ZTP1-7
13)	1	Power Supply Jack	PJ-002	Cui/Stack Inc.	PWR2
14)	1	49.9 ohm Resistor	CRCW080549R9F	DALE	R1
15)	1	0 ohm Resistor	CRCW1206000J	DALE	R3
16)	5	0 ohm Resistor	CRCW0805000J	DALE	R4,R6,R31-33
17)	4	182 ohm Resistor	CRCW12061820F	DALE	R5,R7,R34-35
18)	5	10K ohm Resistor	CRCW08051002F	DALE	R8,R11,R14,R26,R29
19)	16	301 ohm Resistor	CRCW08053010F	DALE	R9,R13,R25,R27,R30,R36-46
20)	1	1K ohm Resistor	CRCW08051001F	DALE	R10
21)	1	619 ohm Resistor	CRCW08056190F	DALE	R12
22)	10	4.75K ohm Resistor	CRCW08054751F	DALE	R15-24
23)	1	750 ohm Resistor	CRCW08057500F	DALE	R28
24)	3	Straight PC mount Jack Receptacle	142-0701-201	E-F-Johnson	SMA1,SMA6-7
25)	4	End Launch PC mount Jack Receptacle	142-0701-801	E-F-Johnson	SMA2-5
26)	1	Wound Bead	29-43-666681	Fair-Rite	FB1
27)	6	0.01MF COG Ceramic Capacitor	C1812C103J5GAC	Kemet	C6-9,C30-31
28)	1	0.1MF X7R Ceramic Capacitor	C1206C104K5RAC	Kemet	C10
29)	1	1000pf X7R Ceramic Capacitor	C0805C102J5RAC	Kemet	C32
30)	1	High Performance EECMOS PLD 3.3volt	GAL22LV10D-4LJ	Lattice	U2
31)	1	28 pin PLCC SMT socket	822066-4	AMP	U2
32)	10	"ULTRA Yellow" Surface Mount LED	SML10Y4B-TR	LEDTRONICS	LED0-9
33)	7	"HI-EFF Green" Surface Mount LED	SML10G4B-TR	LEDTRONICS	LED10-12,LED14-17
34)	1	"ULTRA Red" Surface Mount LED	SML10R6C-TR	LEDTRONICS	LED13
35)	1	+.3.3V Low Dropout Micropower Voltage Regulator 3A	LT1529CT-3.3	Linear Technology	VR1
36)	1	TO-220 Mounting Kit	Thermalloy	4880	VR1
37)	1	Heat Sink for To-220	Thermalloy	6078B	VR1
38)	1	SMF Omni-Blok Fuse Block with 750MA Fuse	154750	LittleFuse	F1
39)					

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GigaPHY™ -SD Device

GDPHYSD_1A Eval Board

Item	Qty.	Device Description	Part Number	Manufacture	Reference Number
40)	1	125 MHz Half-size Clock Crystal 3.3Volt with TRI_STATE	H3390-125	MF Electronics	X1
41)	6	Mini Spring Socket	50935-1	AMP	X1
42)	1	Empty do not stuff	N/A	N/A	R2
43)	2	Low Voltage Octal Buffer/Line Driver	74LCX540WM	National Semiconductor	U3-4
44)	20	0.01MF X7R Ceramic Capacitor	ECU-V1H103KBG	Panasonic	C4-5,C11-21,C23-29
45)	3	33MF Tantalum Chip Capacitor 16WV	293D336X9016D2T	Sprague	C1,C3,C22
46)	1	100MF Electrolytic Capacitor	518D107M016AX7S	Sprague	C2
47)	1	Ferrite Bead inductor	TDKBC50-1206	TDK	FB2
48)	6	NYLON Slotted Round Head Machine Screw Thread 6-32 Length 3/8"	112508	ASMCO	ZM1-6
49)	6	Nylon Threaded Spacer, Thread 6-32 Length 1/2"	1530 H - N - .500 - 1	ASMCO	ZM1-6
Lab Bench Power Supply Cable					
50)	1	12" Hookup wire for power supply Red	M16878/5-BGE-2	Anixter	
51)	1	12" Hookup wire for power supply Black	M16878/5BGE-0	Anixter	
52)	2	Plastic tiedowns 3-3/4"	4200	ASMCO	
Wall Power Supply					
53)	1	Switching Power Supply	DSA-0301-05	DVE	

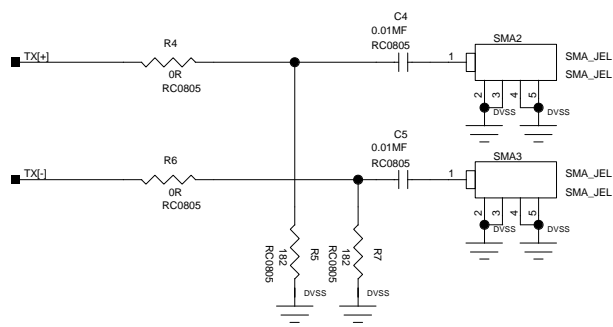
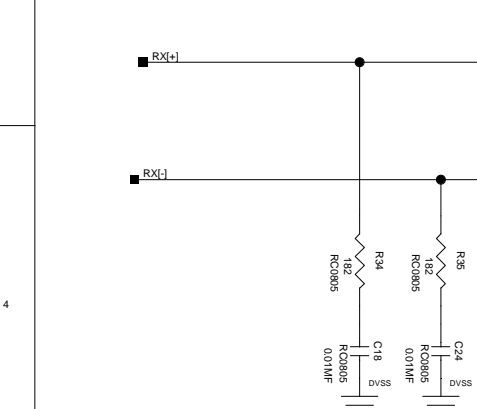
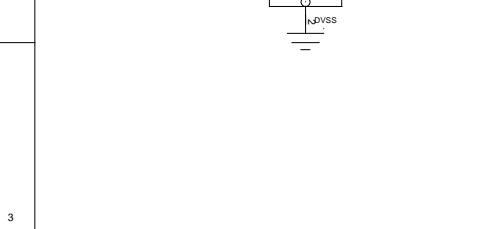
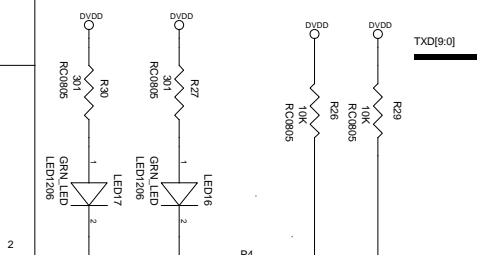
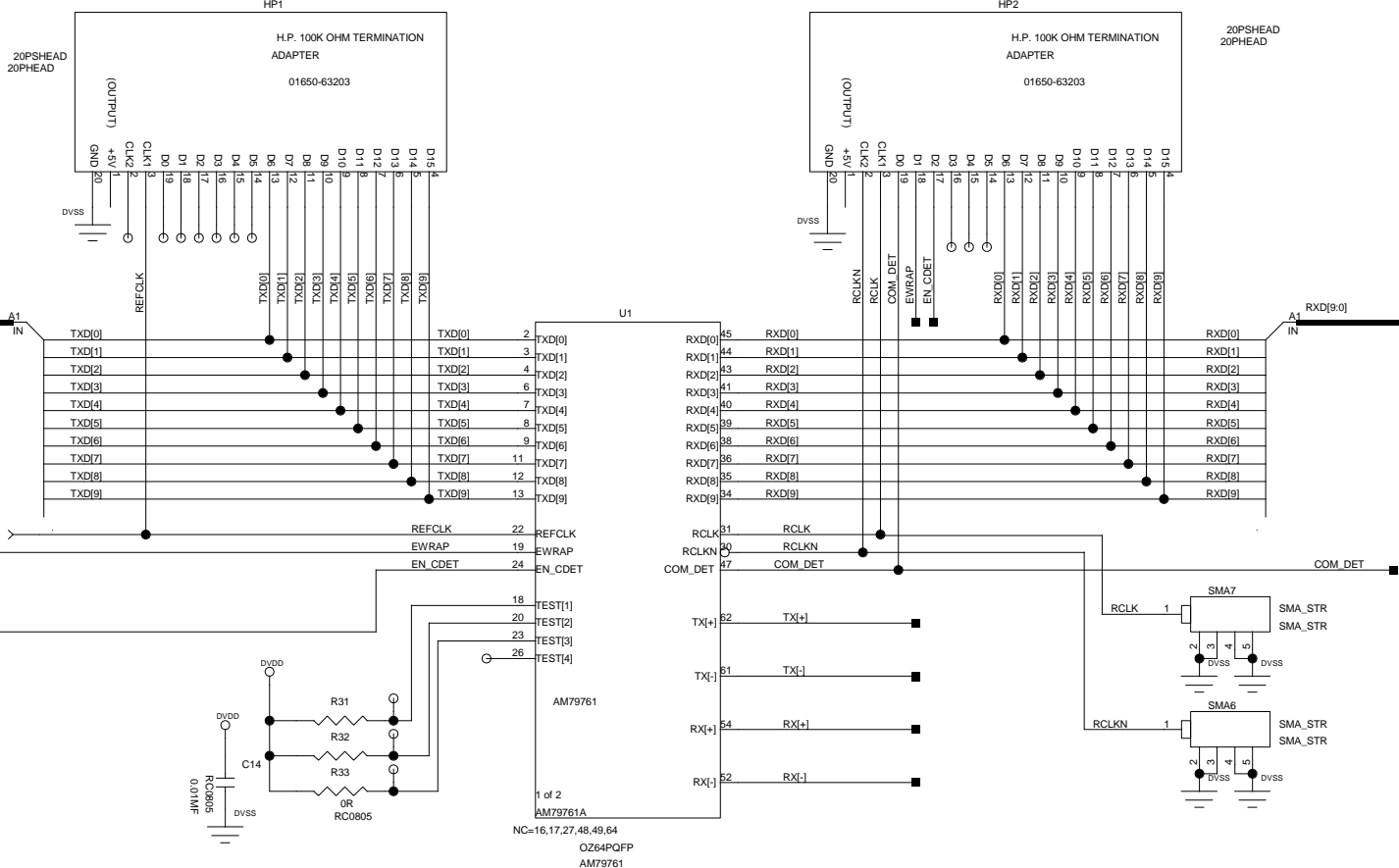



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SCHEMATIC DIAGRAM
 Gigabit Ethernet Transceiver
 1000Base-X Eval. Brd.

APPROVED BY:		DATE					
MODULE		SHEET		SIZE	DWG. NO.	BRD. NO.	REV
GPHYS1_1A		1		D	GPHYS1_1A	GPHYS1_1A	A
DRAWN BY		ENGINEER		DATE		PAGE	
Steve Cooper		Robert Hartman		10-23-1997_9:26		1 of 7	

EWRAP
 LOW Normal operation.
 High Internal loopback
 EN_CDET
 LOW Current word alignment.
 LOW disables COM_DET
 HIGH Enables COM_DET
 HIGH Enables word resynchronization.



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SCHEMATIC DIAGRAM			
Gigabit Ethernet Transceiver 100Base-X Eval. Brd.			
MODULE BOARD	SHEET 1	SIZE D	DWG. NO. GPHYS1A
BRD. NO. GPHYS1A	REV A	DATE 10-22-1997 16:19	PAGE 2 of 7

APPROVED BY: _____ DATE _____
 DRAWN BY: Steve Cooper ENGINEER: Robert Hartman

From 10-bit receive outputs.

RXD[9:0]

A1 IN

A2 RXD[0]

A3 RXD[1]

A4 RXD[2]

A5 RXD[3]

A6 RXD[4]

A7 RXD[5]

A8 RXD[6]

A9 RXD[7]

RXD[0]

RXD[1]

RXD[2]

RXD[3]

RXD[4]

RXD[5]

RXD[6]

RXD[7]

U3

74LCX540

20PSOLIC

DVDD:20

DVSS:10

2

A1

Y1

18

LED[0]

3

A2

Y2

17

LED[1]

4

A3

Y3

16

LED[2]

5

A4

Y4

15

LED[3]

6

A5

Y5

14

LED[4]

7

A6

Y6

13

LED[5]

8

A7

Y7

12

LED[6]

9

A8

Y8

11

LED[7]

10

19

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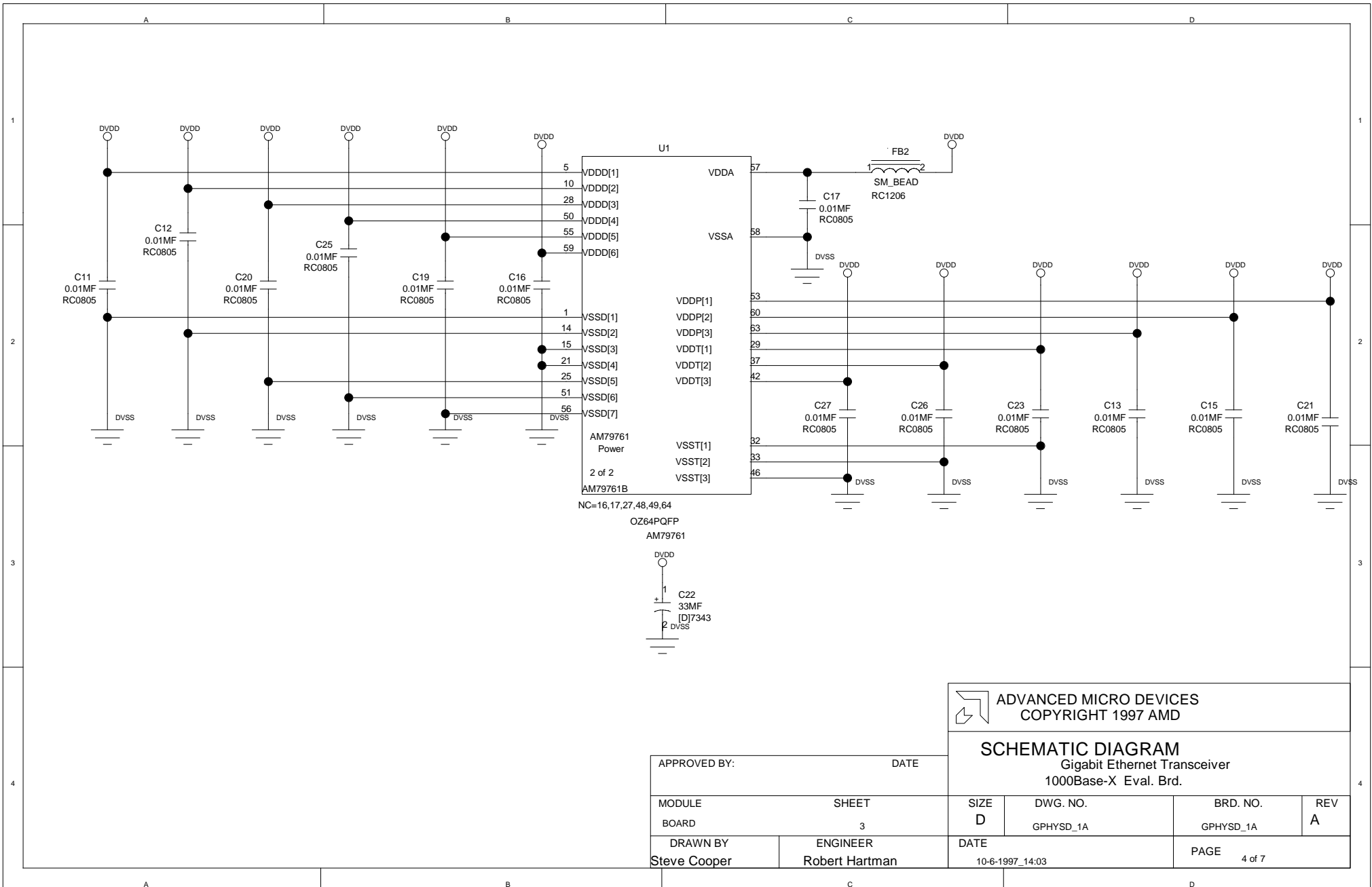
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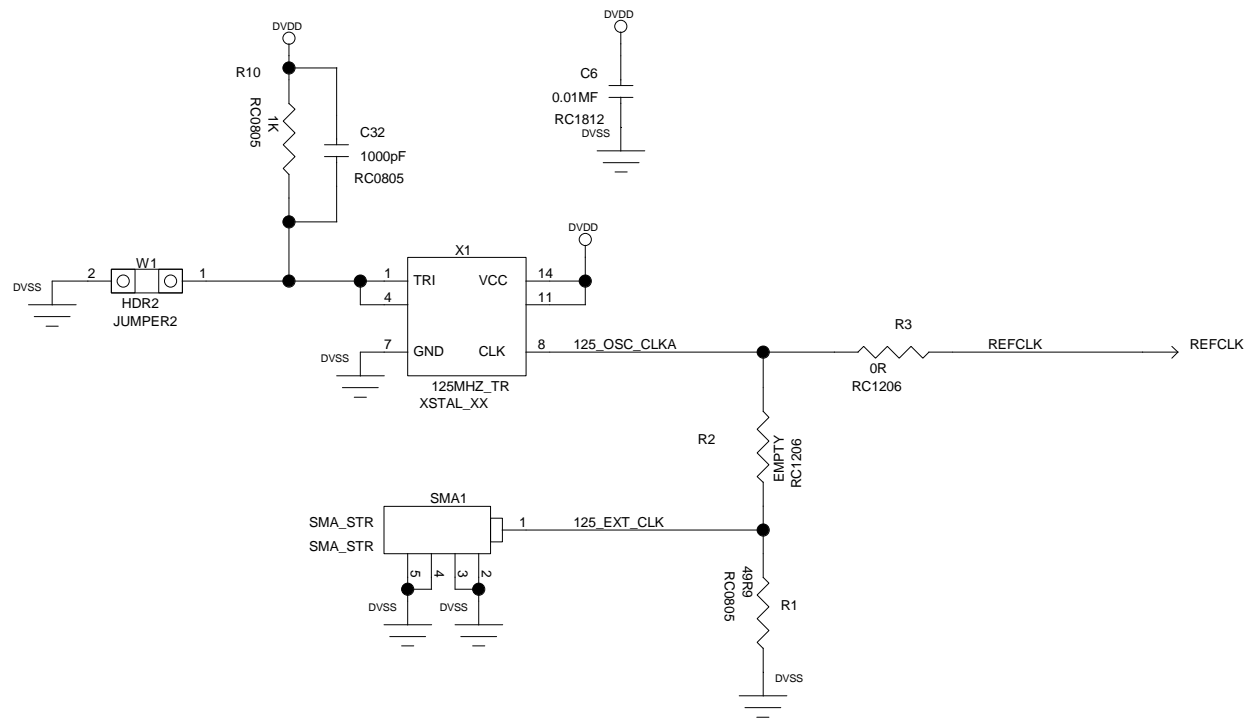



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SCHEMATIC DIAGRAM
 Gigabit Ethernet Transceiver
 1000Base-X Eval. Brd.

APPROVED BY:		DATE					
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BOARD		3		D	GPHYSD_1A	GPHYSD_1A	A
DRAWN BY		ENGINEER		DATE		PAGE	
Steve Cooper		Robert Hartman		10-6-1997 14:03		4 of 7	

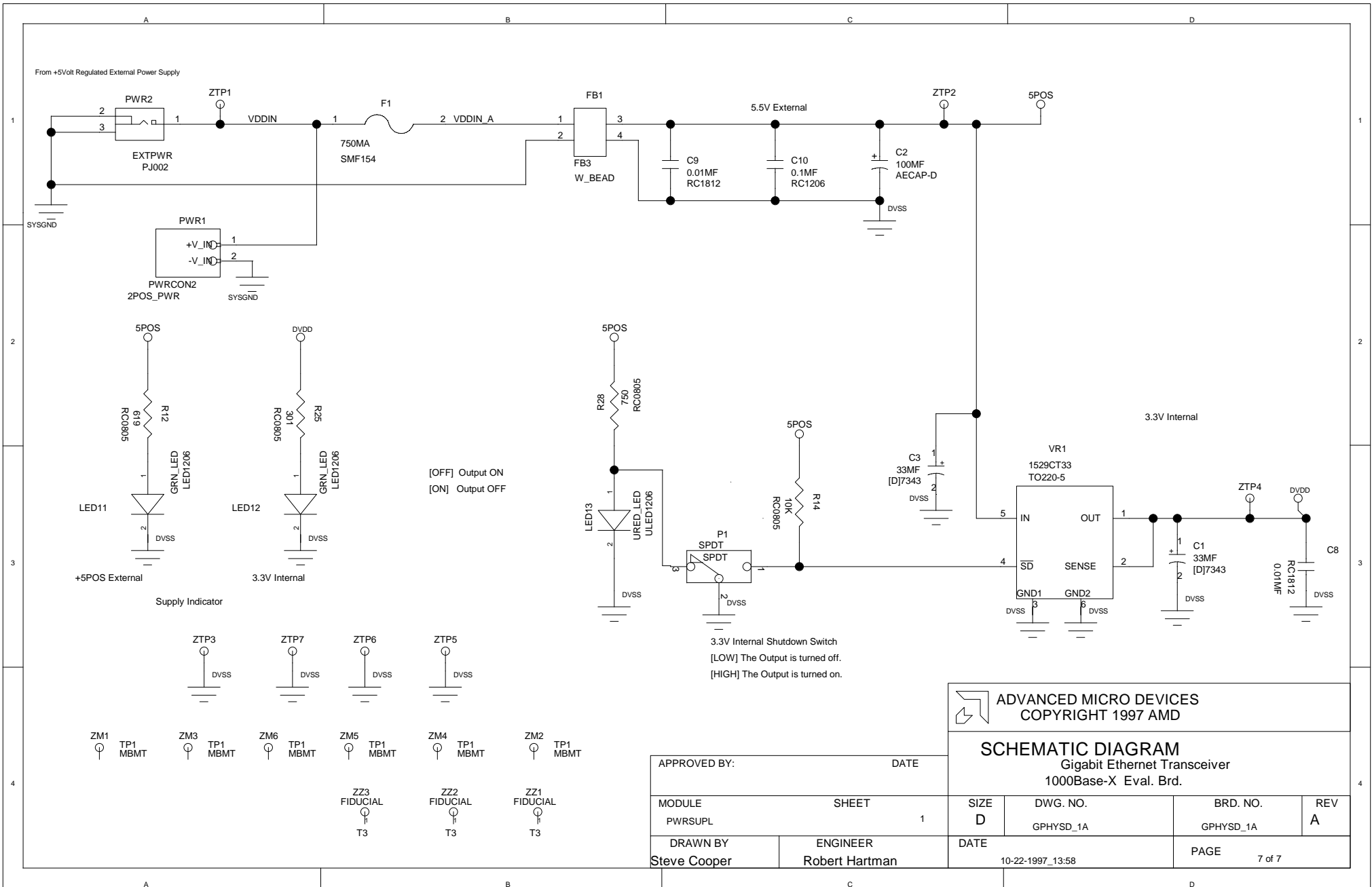
P8 +3.3V ENABLES CLK OUTPUT
P8 DVSS DISABLES CLK OUTPUT



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SCHEMATIC DIAGRAM
Gigabit Ethernet Transceiver
1000Base-X Eval. Brd.

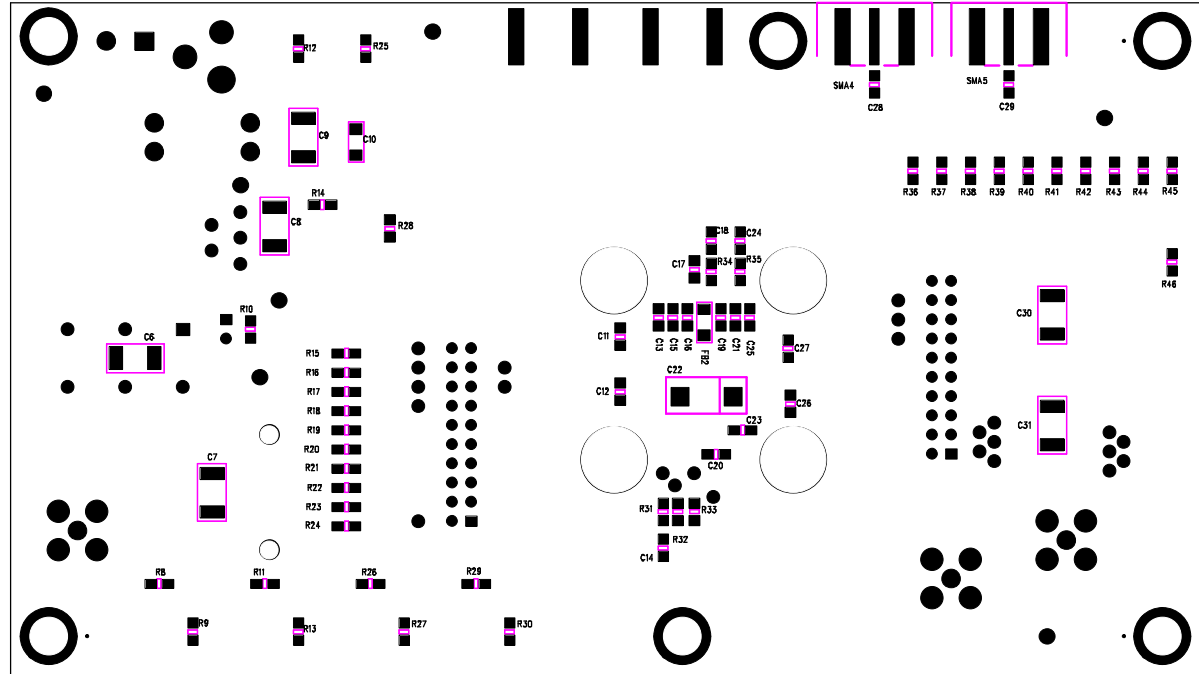
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DRAWN BY		ENGINEER		DATE	BRD. NO.
Steve Cooper		Robert Hartman		10-23-1997_8:46	GPHYSD_1A
PAGE				REV	
6 of 7				A	



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SCHEMATIC DIAGRAM
Gigabit Ethernet Transceiver
1000Base-X Eval. Brd.

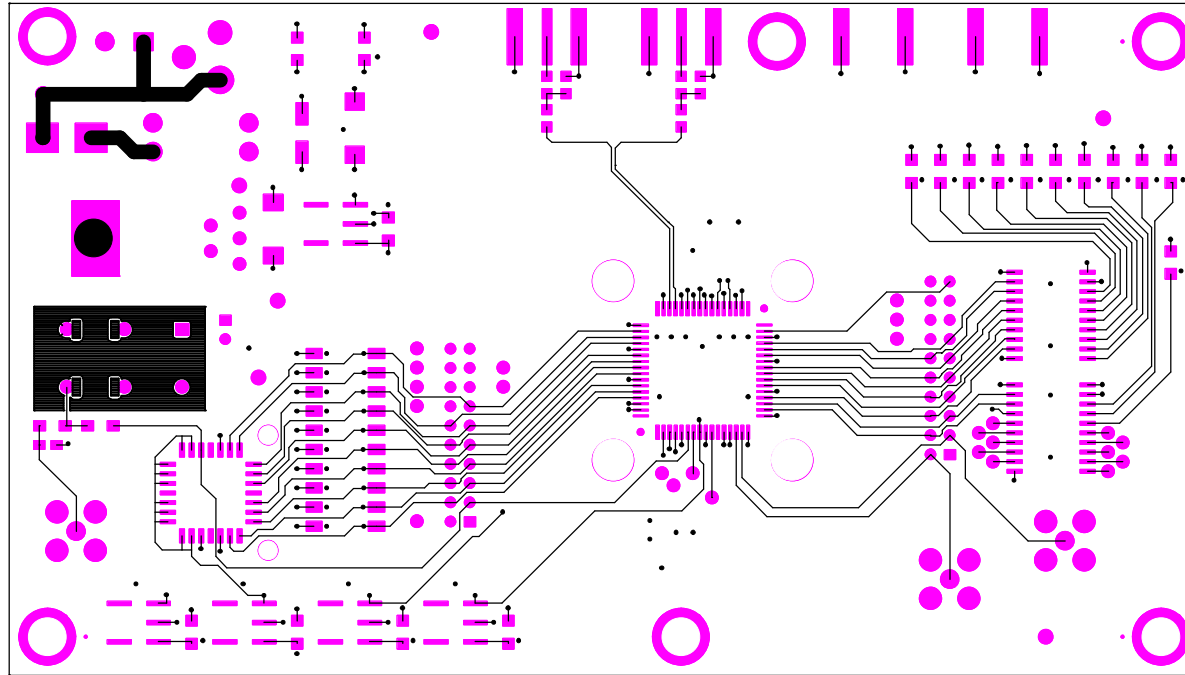
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BRD. NO. GPHYSD_1A	REV A	DATE 10-22-1997_13:58	
DRAWN BY Steve Cooper		ENGINEER Robert Hartman	
PAGE 7 of 7			



SILKSCREEN BOTTOM

LAYER 4 BOTTOM ROUTING
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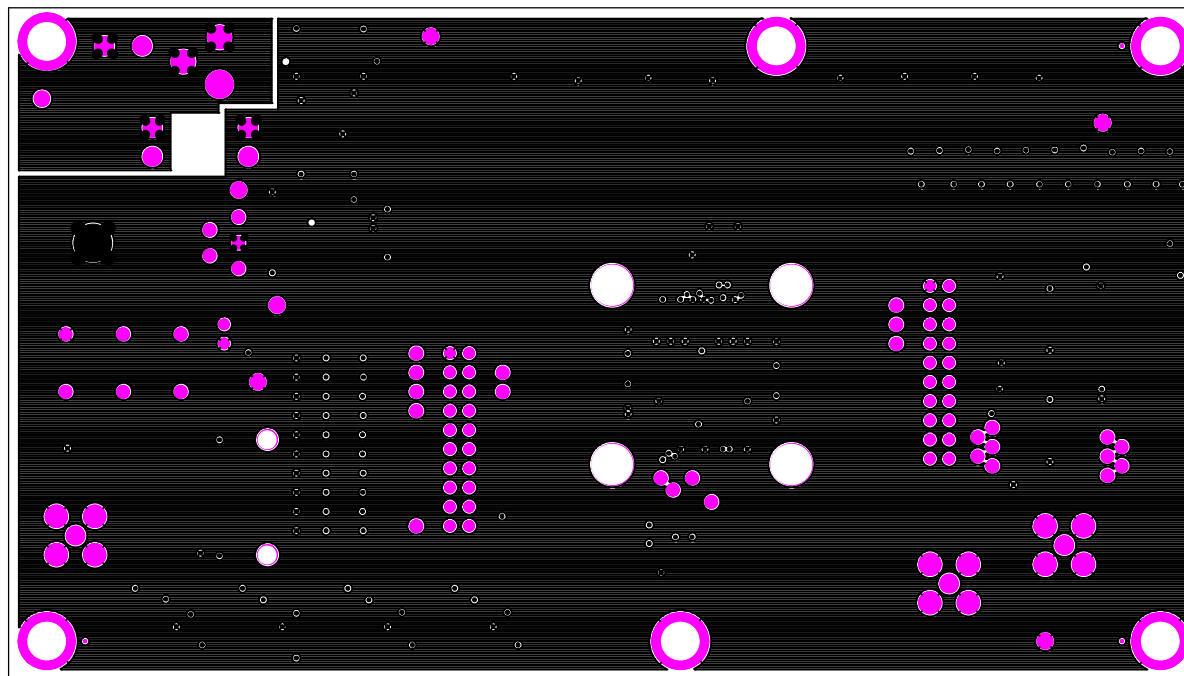
GPHYS_D_1A REV A 09/12/97
 GigaBIT Ethernet Transceiver



LAYER 1 TOP ROUTING

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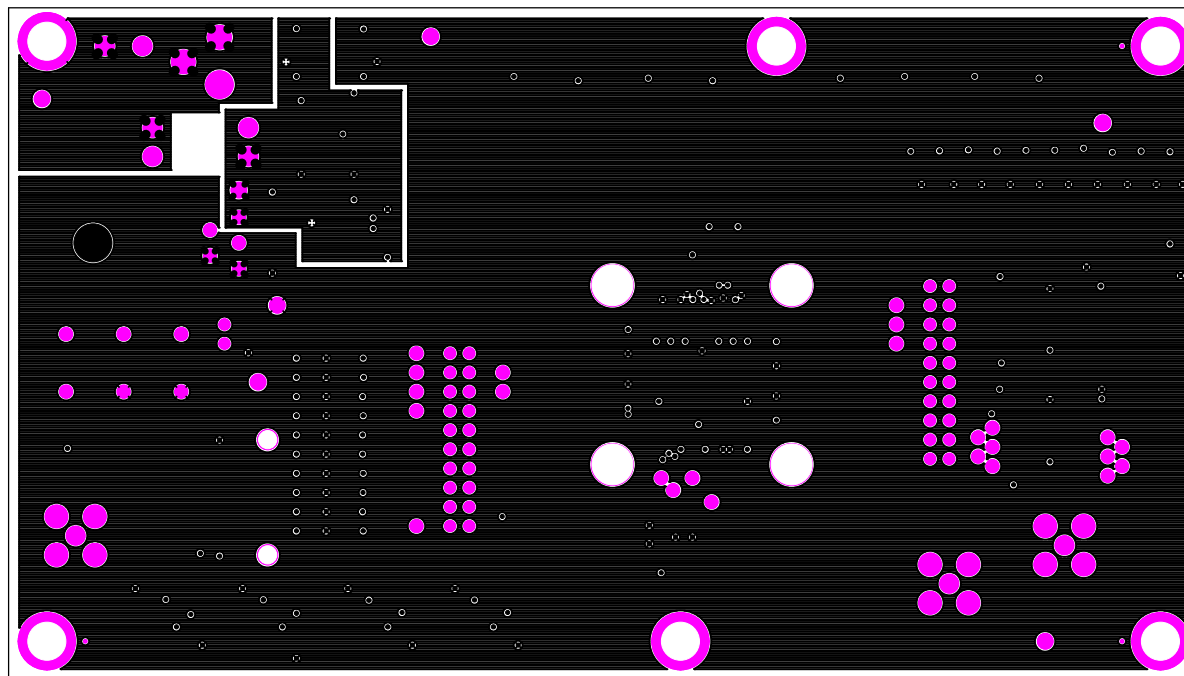
GPHYSD_1A REV A 09/12/97
GigaBIT Ethernet Transceiver



LAYER 2 INNER ROUTING DVSS

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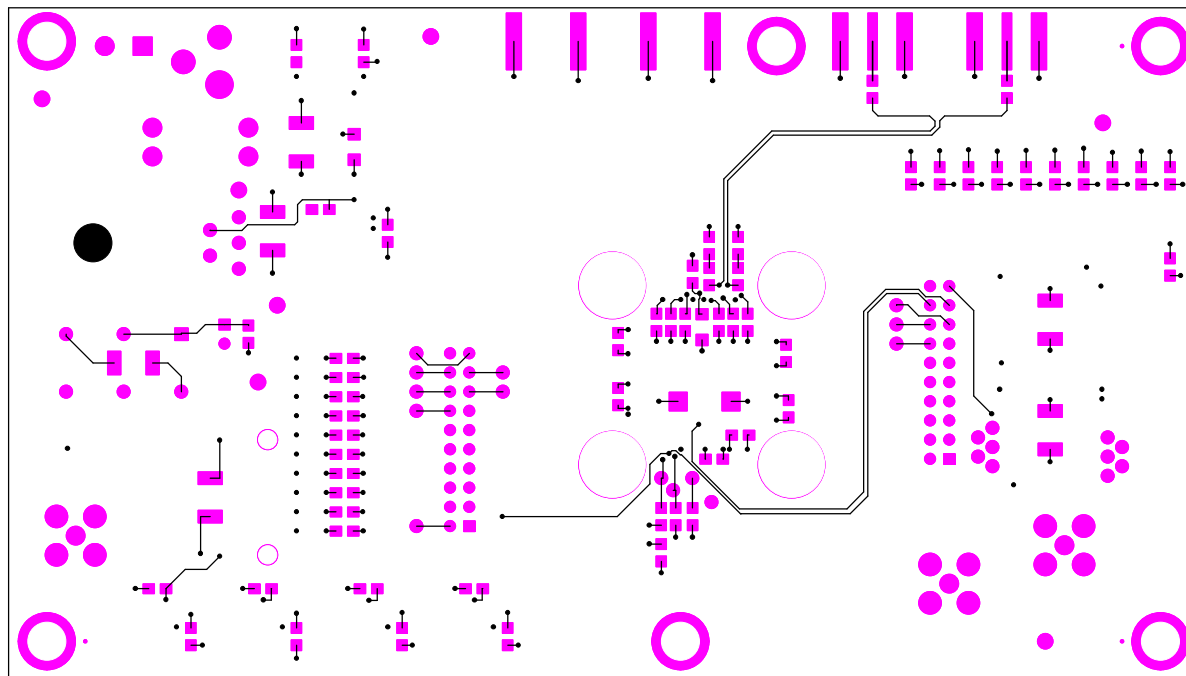
GPHYSD_1A REV A 09/12/97
GigaBIT Ethernet Transceiver



LAYER 3 INNER ROUTING DVDD

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GigaBIT Ethernet Transceiver



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GigaBIT Ethernet Transceiver