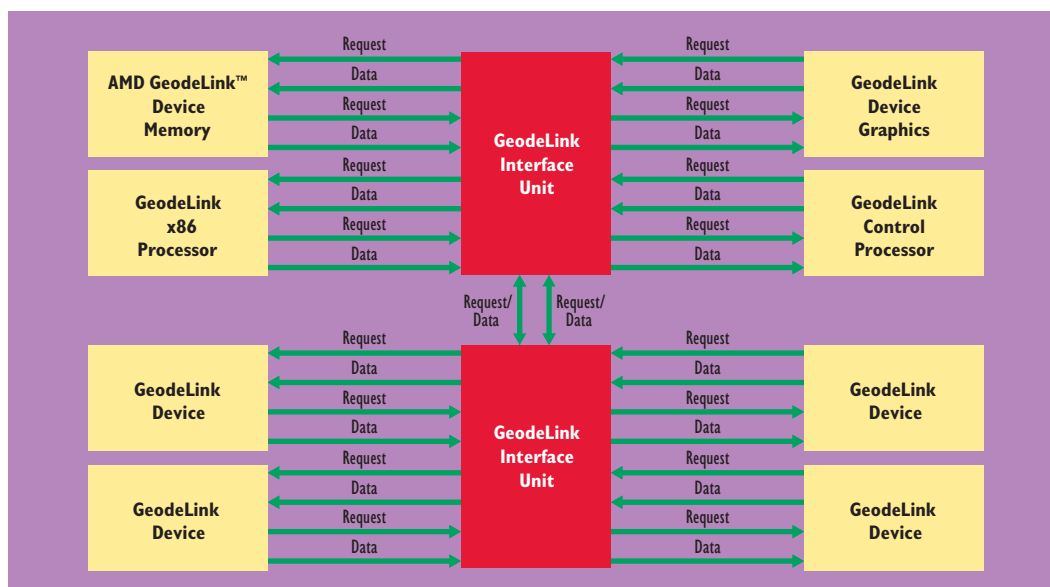


Processor Architecture Facilitates
Integration, Efficiency, Performance



AMD GeodeLink™ Architecture

GeodeLink System Architecture

AMD announces its top-to-bottom system architecture for system-on-a-chip. The AMD GeodeLink™ architecture offers a single on-chip interconnect that facilitates the integration of modules and allows the use of Unified Memory Architecture (UMA).

Unified Memory Architecture (UMA)

At the heart of the GeodeLink architecture is the built-in arbiter. The arbiter enables dynamic allocation of memory bandwidth, with “on-the-fly” prioritization. Use of out-of-order data streams coupled with a high-performance peer-to-peer communication enables direct communication between modules, resulting in more efficient use of shared memory.

On-Chip Switched Fabric

At the core of the GeodeLink architecture lies a very high-bandwidth interface unit that can handle up to 6 GB/s of data transfer. With up to 31 pipelined transactions, the architecture increases the level of performance by allowing devices to have multiple simultaneous outstanding requests. This single bus architecture improves performance and facilitates IP reusability, thus improving our customers’ time-to-market.

Advanced Hardware Power Management (AHPM)

The GeodeLink architecture has embedded power management features. This allows our OEM and ODM customers to take advantage of advanced power management without writing a single line of code. It is also OS independent, since the power management calls are handled at the BIOS level.

Development Software

The GeodeLink architecture has an embedded Enhanced JTAG interface that provides a consistent debug environment. With full bus master access and branch trace messaging capabilities, software development can be significantly accelerated.

Technical Specifications

Architecture Characteristics

- Standard bus interface for modular reusable IP
- Support for prioritization of accesses from real-time and isochronous devices

AMD GeodeLink™ Architecture

Architecture Characteristics *(continued)*

- Pipelining of multiple read and/or write requests from various devices (up to 31 pipelined transactions)
- Extensible to a variety of bus widths (from 16 to 256 bits) and clock rates (33–300 MHz)
- Standard bridges to legacy buses (XBus, PCI)
- Peer-to-peer communication
- Advanced Hardware Power Management
- Suspend clocks and power controls
- Standard test and scan interface
- Standard diagnostic signals
- On-chip logic analyzer functions
- Full scan for debug
- Error reporting for debug
- GeodeLink virtual PCI headers

Operating Systems

AMD supports the following operating systems for all of its devices using the GeodeLink architecture

- Windows® CE 3.0 and 4.0
- Linux (Kernel 2.4)
- Windows XP and XPe

Other Operating Systems

Any x86-compatible operating system can be used with the GeodeLink architecture by developing the appropriate device drivers.

AMD GeodeLink™ System Architecture

Software Model	Design Verification	Layout Methodology
System Topology		
Packet Protocol		
Transaction Protocol		
Signal Description		

About AMD

Founded in 1969 and based in Sunnyvale, California, AMD (NYSE: AMD) is a global supplier of integrated circuits for the personal and networked computer and communications markets with manufacturing facilities in the United States, Europe, Japan

and Asia. AMD, a Standard & Poor's 500 company, produces microprocessors, Flash memory devices and silicon-based solutions for communications and networking applications.



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