

Addendum for NetPHY-4LP 12 PORT DEMONSTRATION KIT (NetPHY-4LP-KT/12PT)

Date: 7/6/99

Fixed Errata

1. The design schematics had reversed the RX+- pairs on the schematics, which will affect the layout. The new schematics have the corrected TX/RX connections. The following schematics pages were changed: pages 2, 4, 6, dated 3/23/99.

Effect

None. The NetPHY-4LP design remains functional. The reversal of the data pairs is corrected by the enabled auto-polarity detection and correction function which compensates for the reversal, such that the data received remains intact. The schematics change is minor and the layout does not change due to this. It is critical to ensure that the pairs are as straight and matched as possible to avoid skewing and differences in impedance.

2. One pin on the top row of pins of the leftmost IC (with the RJ45 connectors at the bottom) was missing a ground connection. The following layout pages were changed: layer 1 artwork, dated 3/1/99.
3. The CMTx pins of T1, T2, T3 appear crossed on the schematics. This is due to incorrect resistor labeling. **The changes have been made to the schematics and posted to the AMD website.** Sheets 2, 4, 6 are affected with incorrect resistors: the changes are as follows:
 - Sheet 2 CMT1: R65 is changed to R66
 - Sheet 2 CMT2: R66 is changed to R65
 - Sheet 2 CMT3: R67 is changed to R70
 - Sheet 2 CMT4: R70 is changed to R67
 - Sheet 4 CMT1: R85 is changed to R86
 - Sheet 4 CMT2: R86 is changed to R85
 - Sheet 4 CMT3: R87 is changed to R90
 - Sheet 4 CMT4: R90 is changed to R87
 - Sheet 6 CMT1: R105 is changed to R106
 - Sheet 6 CMT2: R106 is changed to R105
 - Sheet 6 CMT3: R110 is changed to R107
 - Sheet 6 CMT4: R107 is changed to R110

PORTS1-4

TXD1_A
TXD0_A
TXEN_A
RXD1_A
RXD0_A
CRSDV_A
RXER_A
TXD1_B
TXD0_B
TXEN_B
RXD1_B
RXD0_B
CRSDV_B
RXER_B
TXD1_C
TXD0_C
TXEN_C
RXD1_C
RXD0_C
CRSDV_C
RXER_C
TXD0_D
CRSDV_D
RXER_D
RXD1_D
TXD1_D
RXD0_D
TXEN_D
MDIO
MDC
RST_N
REFCLK

RXN_D
RXP_D
RXN_C
RXP_C
RXN_B
RXP_B
RXP_A
RXN_A
TXN_C
TXP_C
TXN_A
TXP_A
TXN_B
TXP_B
TXP_D
TXN_D
SPD_A
LINK_A
SPD_B
LINK_B
DPX_B
DPX_D
LINK_D
SPD_D
DPX_C
LINK_C
SPD_C
DPX_A

4PORTS

PORTS5-8

TXD1_A
TXD0_A
TXEN_A
RXD1_A
RXD0_A
CRSDV_A
RXER_A
TXD1_B
TXD0_B
TXEN_B
RXD1_B
RXD0_B
CRSDV_B
RXER_B
TXD1_C
TXD0_C
TXEN_C
RXD1_C
RXD0_C
CRSDV_C
RXER_C
TXD0_D
CRSDV_D
RXER_D
RXD1_D
TXD1_D
RXD0_D
TXEN_D
MDIO
MDC
RST_N
REFCLK

RXN_D
RXP_D
RXN_C
RXP_C
RXN_B
RXP_B
RXP_A
RXN_A
TXN_C
TXP_C
TXN_A
TXP_A
TXN_B
TXP_B
TXP_D
TXN_D
SPD_A
LINK_A
SPD_B
LINK_B
DPX_B
DPX_D
LINK_D
SPD_D
DPX_C
LINK_C
SPD_C
DPX_A

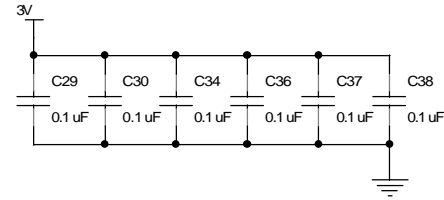
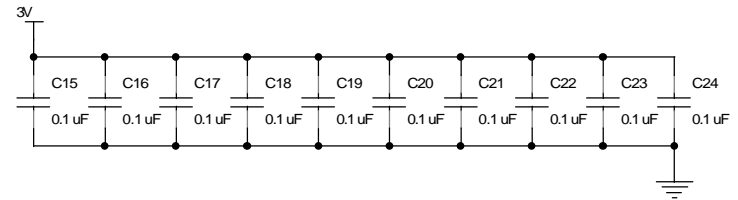
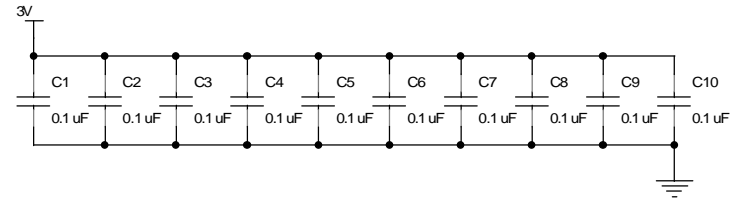
4PORTS

PORTS9-12

TXD1_A
TXD0_A
TXEN_A
RXD1_A
RXD0_A
CRSDV_A
RXER_A
TXD1_B
TXD0_B
TXEN_B
RXD1_B
RXD0_B
CRSDV_B
RXER_B
TXD1_C
TXD0_C
TXEN_C
RXD1_C
RXD0_C
CRSDV_C
RXER_C
TXD0_D
CRSDV_D
RXER_D
RXD1_D
TXD1_D
RXD0_D
TXEN_D
MDIO
MDC
RST_N
REFCLK

RXN_D
RXP_D
RXN_C
RXP_C
RXN_B
RXP_B
RXP_A
RXN_A
TXN_C
TXP_C
TXN_A
TXP_A
TXN_B
TXP_B
TXP_D
TXN_D
TXN_C
SPD_A
LINK_A
SPD_B
LINK_B
DPX_B
DPX_D
LINK_D
SPD_D
DPX_C
LINK_C
SPD_C
DPX_A

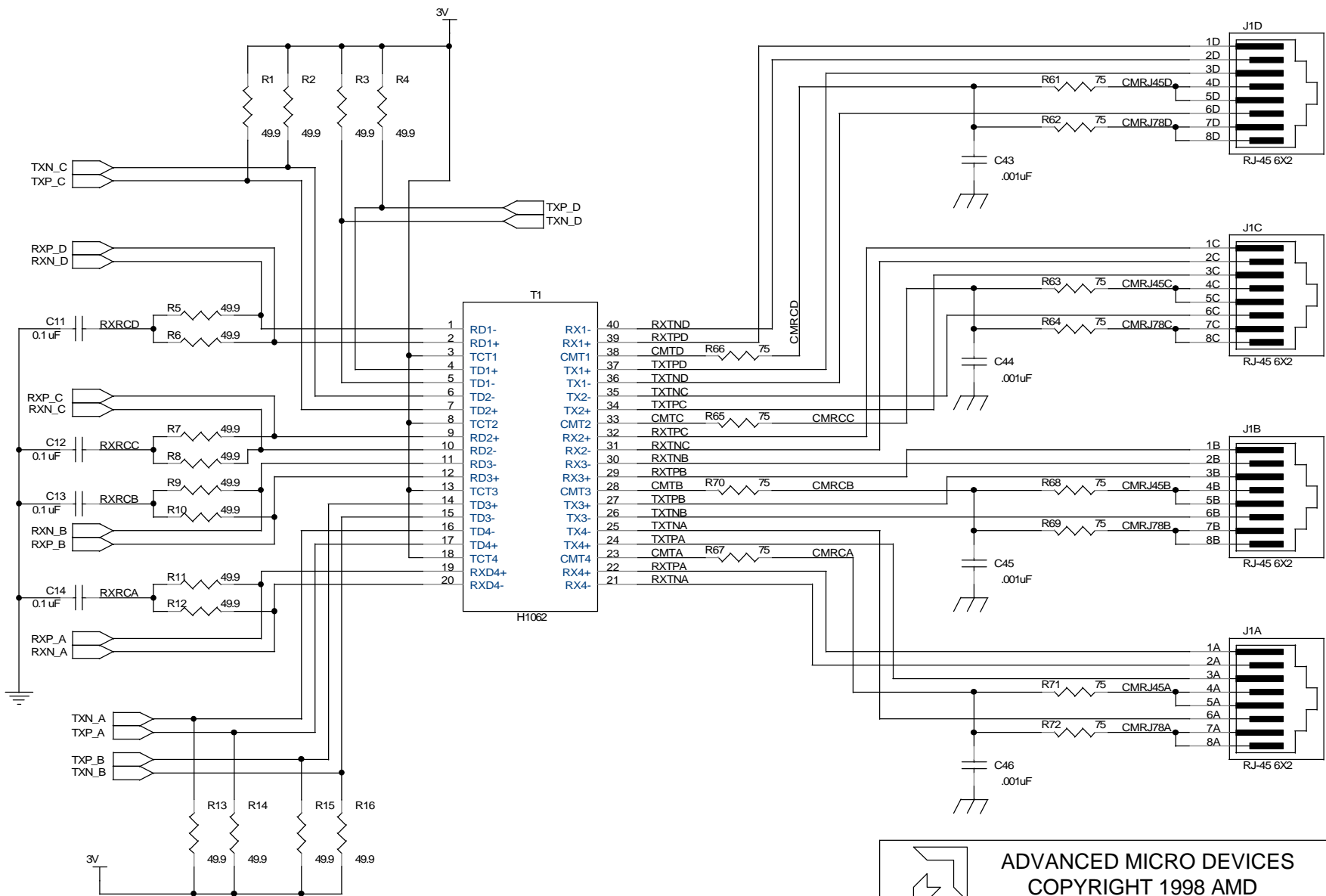
4PORTS



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SCHEMATIC DIAGRAM
12-Port Fast Ethernet Front End NETPHY-4LP

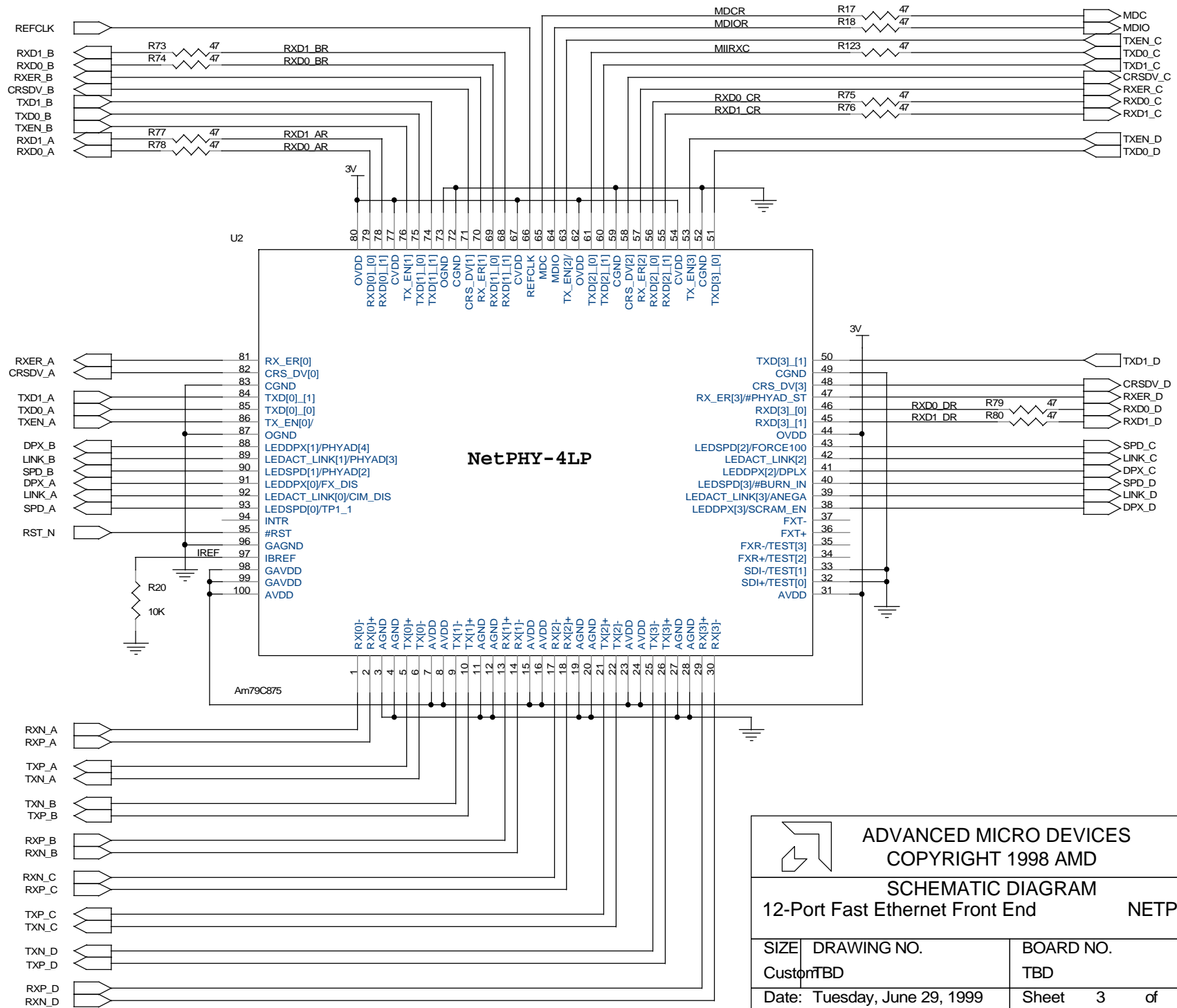
SIZE	DRAWING NO.	BOARD NO.	REV
Custom	TBD	TBD	C
Date: Tuesday, March 23, 1999		Sheet 1 of 7	



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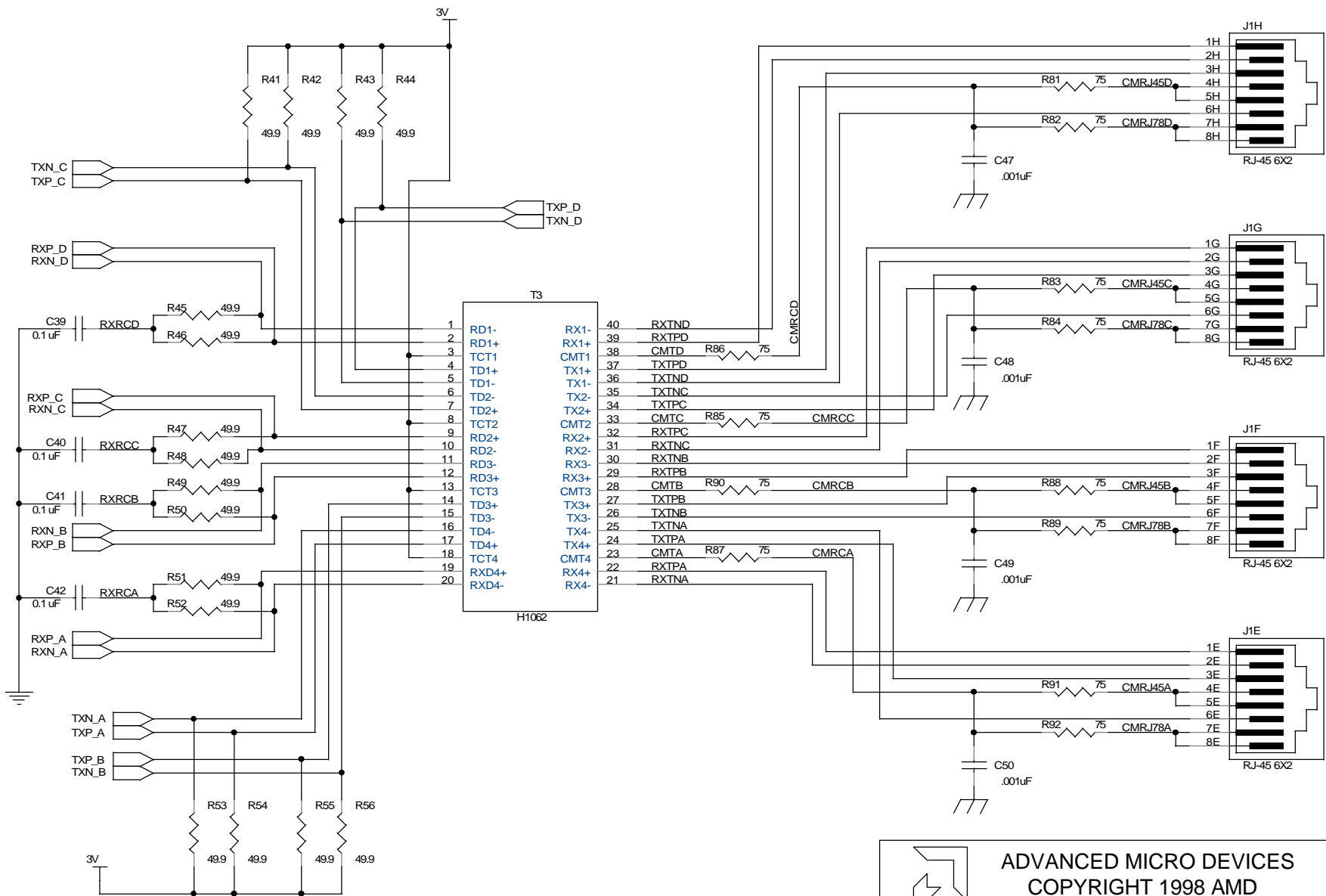
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


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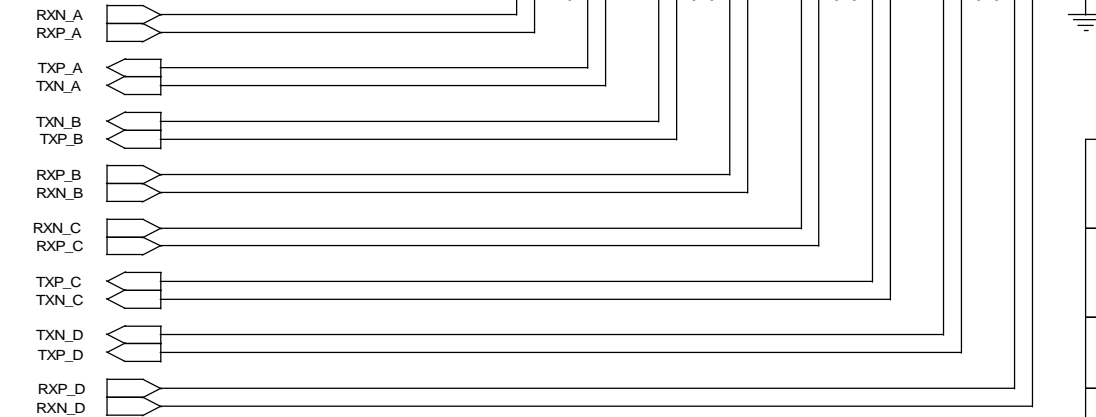
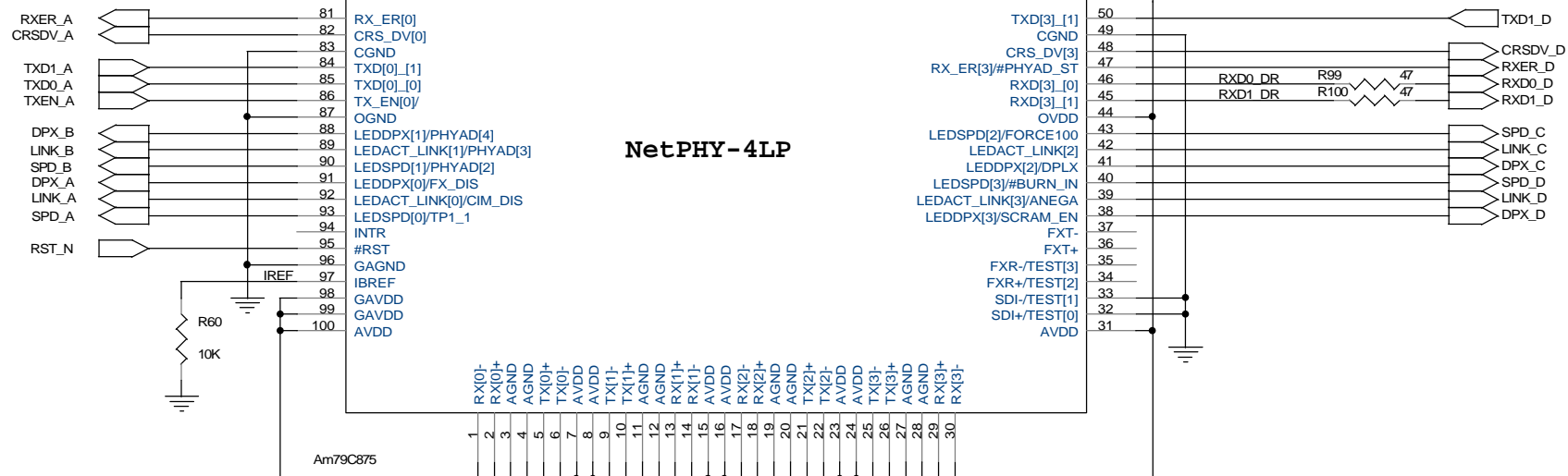
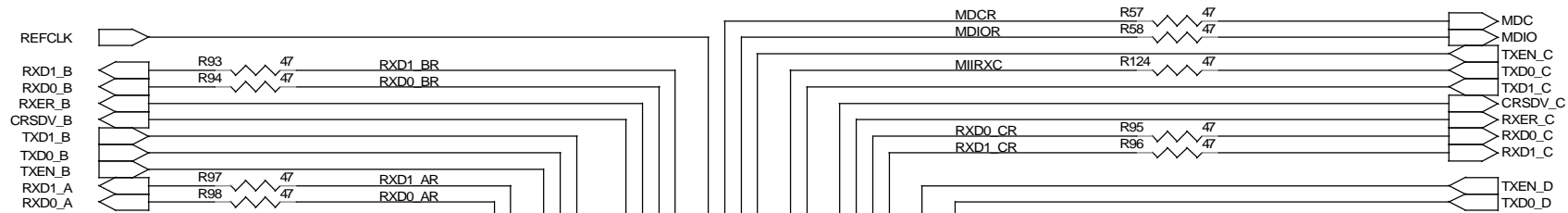
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



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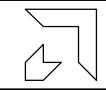
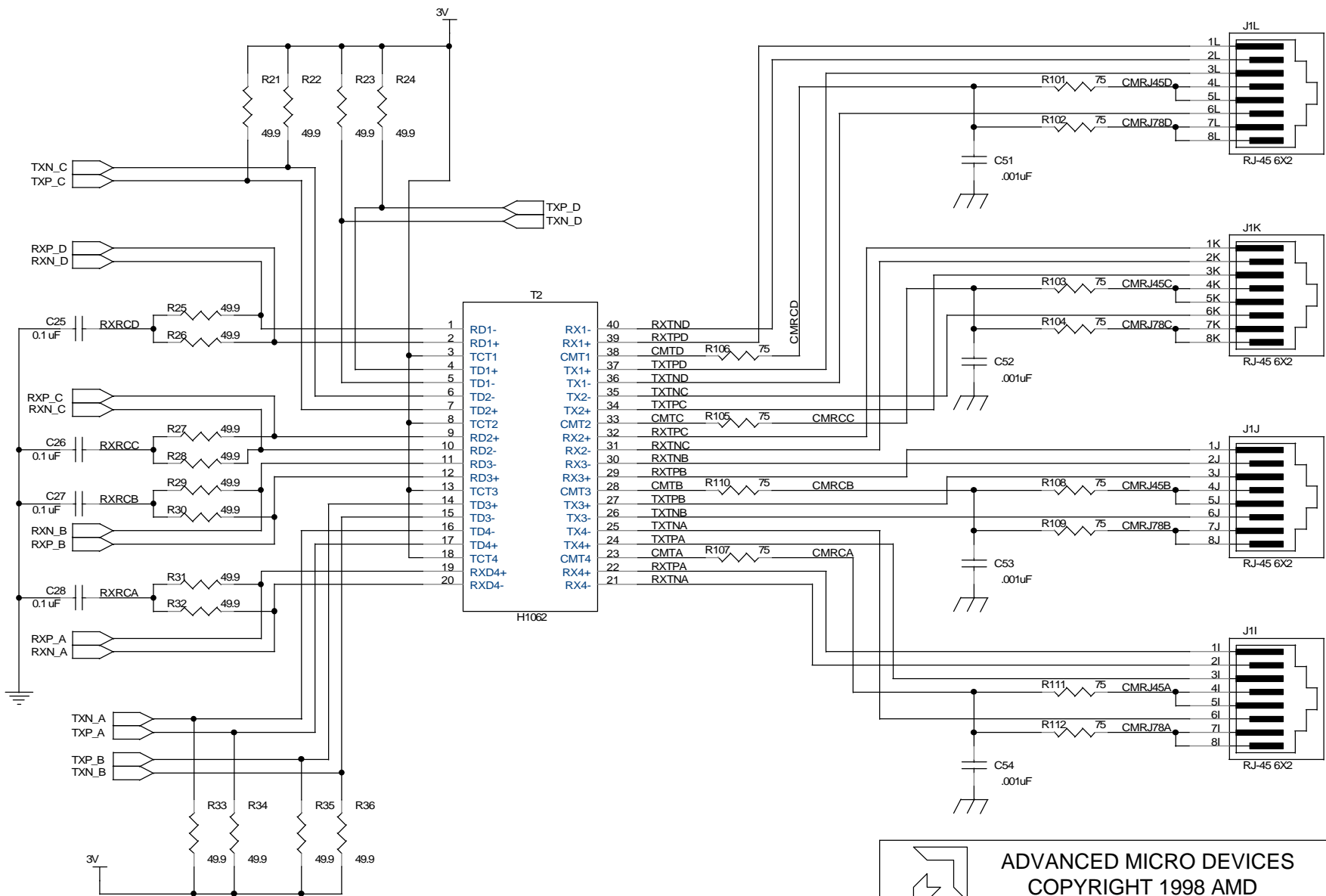
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Custom	TBD	TBD	C
Date: Monday, July 05, 1999		Sheet 4 of 7	




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12-Port Fast Ethernet Front End **NETPHY-4LP**

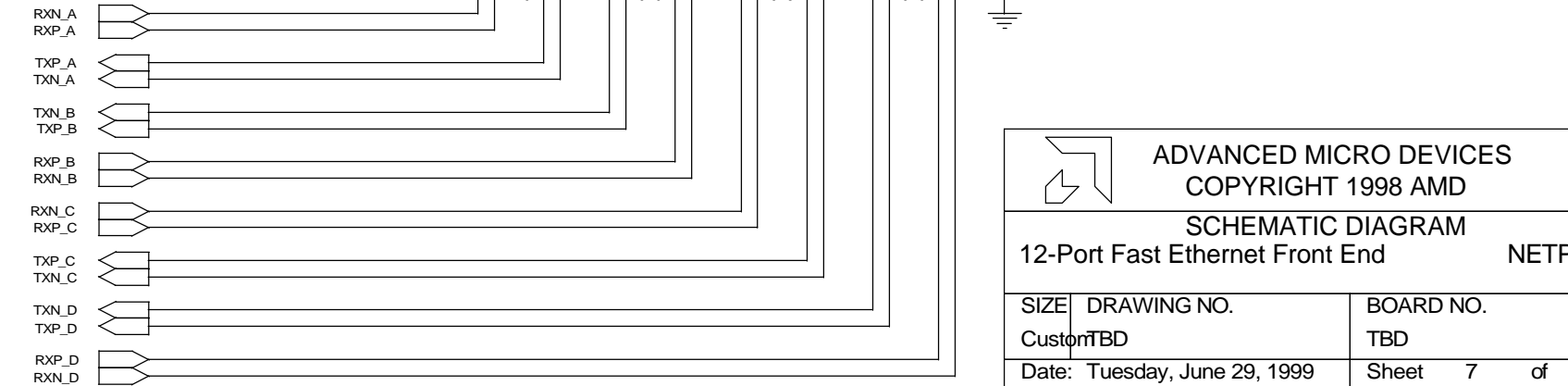
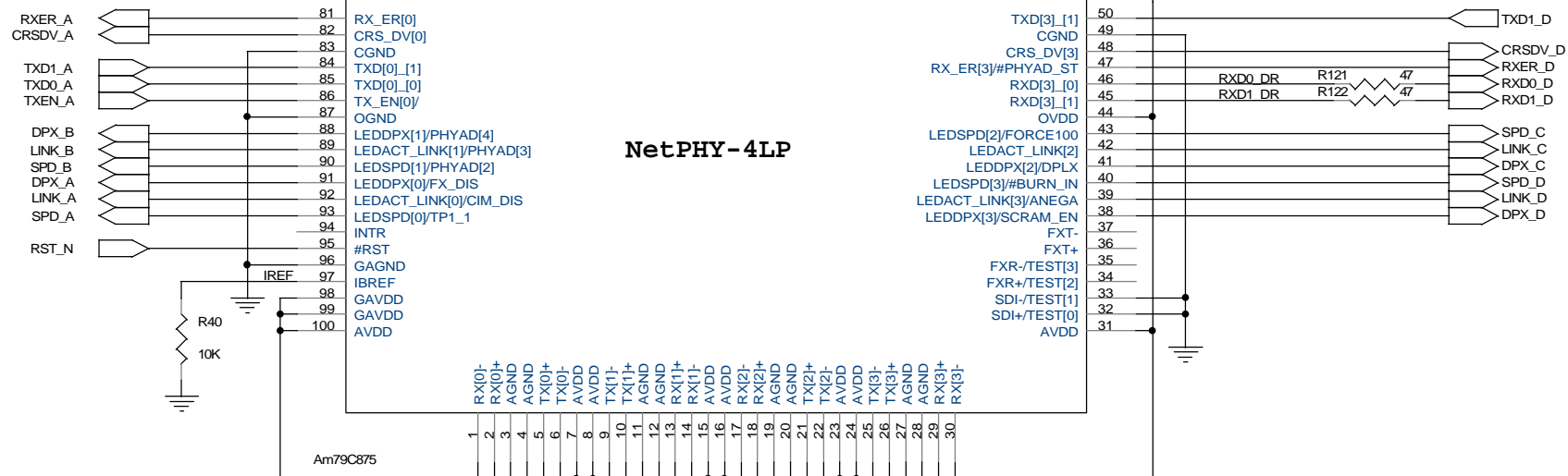
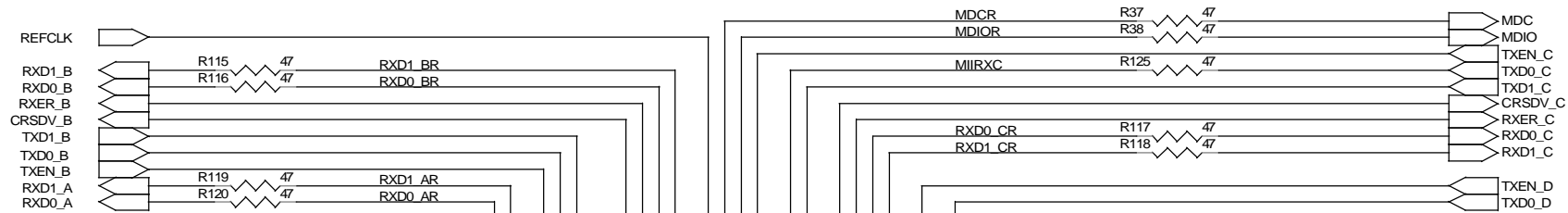
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


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12-Port Fast Ethernet Front End NETPHY-4LP

SIZE	DRAWING NO.	BOARD NO.	REV
Custom	TBD	TBD	C
Date: Monday, July 05, 1999	Sheet	6	of 7




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SCHEMATIC DIAGRAM
12-Port Fast Ethernet Front End **NETPHY-4LP**

SIZE	DRAWING NO.	BOARD NO.	REV
Custom	TBD	TBD	C
Date: Tuesday, June 29, 1999		Sheet 7 of 7	

NetPHY-4LP 12-Port Fast Ethernet Front End Revised: Thursday, February 11, 1999									
Bill Of Materials February 14,1999 18:01:38									
Item	Qty	Reference	Value	Tolerance	Rating	Type	PCB Footprint	Mfg	PN
1	38	C1,C2,C3,C4,C5,C6,C7,C8, C9,C10,C11,C12,C13,C14, C15,C16,C17,C18,C19,C20, C21,C22,C23,C24,C25,C26, C27,C28,C29,C30,C34,C36, C37,C38,C39,C40,C41,C42	0.1 uF	5%	50V	Ceramic	0805	Digikey	
2	12	C43,C44,C45,C46,C47,C48, C49,C50,C51,C52,C53,C54	.001uF	5%	2KV	Ceramic	1808	Digikey	
3	1	J1	RJ-45 6X2					Amp	569263-1
4	48	R1,R2,R3,R4,R5,R6,R7,R8, R9,R10,R11,R12,R13,R14, R15,R16,R21,R22,R23,R24, R25,R26,R27,R28,R29,R30, R31,R32,R33,R34,R35,R36, R41,R42,R43,R44,R45,R46, R47,R48,R49,R50,R51,R52, R53,R54,R55,R56	49.9	1%	1/8W	SMT	0805	Digikey	
5	33	R17,R18,R37,R38,R57,R58, R73,R74,R75,R76,R77,R78, R79,R80,R93,R94,R95,R96, R97,R98,R99,R100,R115, R116,R117,R118,R119,R120, R121,R122,R123,R124,R125	47	1%	1/8W	SMT	0805	Digikey	
6	3	R20,R40,R60	10K	1%	1/8W	SMT	0805	Digikey	
7	36	R61,R62,R63,R64,R65,R66, R67,R68,R69,R70,R71,R72, R81,R82,R83,R84,R85,R86, R87,R88,R89,R90,R91,R92, R101,R102,R103,R104,R105, R106,R107,R108,R109,R110, R111,R112	75	1%	1/8W	SMT	0805	Digikey	
8	3	T1,T2,T3	H1062	1%	2 KV	SMT		Pulse Eng.	H1062
9	3	U2,U4,U6	79C875	3.3V	5%	SMT	QFP100-1	AMD	NetPHY-4LP