

Board Level reliability of Lead-free packages

(Interim Report)

By

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Executive Summary:

The purpose of this study is to understand the board level solder joint reliability of the packages (SOIC,PBGA,FBGA) built with lead-free alternatives.The units assembled to daisy chained boards will be subjected to thermal cycling test to understand the solder joint reliability.

The status of the project is as follows:

- Assembly of all SOIC ,PBGA & FBGA units has been completed.
- Assembly of units for thermal cycling test was taken up after validating the process. This interim report describes the tests performed to validate the process and hence does not represent the reliability of packages.
- Assembled units will be subjected to thermal cycling test . This will start on or before WW50.
- The solder joint fatigue of lead-free joints will studied and reported after completion of thermal cycling test.

1.0 Project objective:

To study solder joint reliability of SOIC, PBGA & FBGA packages with lead-free replacements.

1.2 Packages studied and purpose:

SO44: This leaded packages are plated with four types of lead-free plating chemistries. Board assembly and testing of this lead free plated parts will draw a comparison on solder joint reliability between plating finishes.

PBGA: This ball grid array package is attached with three types lead-free solder spheres. Board assembly and testing of this lead-free parts will draw a comparison on solder joint reliability between lead-free solder alloy.

FBGA: This ball grid array package is attached with Sn/Ag/Cu alloy system from three different vendors. Board assembly and testing of this lead-free parts will draw a comparison on solder joint reliability of lead-free solder between vendors and alloys as well.

***The plating chemistries / solder ball alloys, that is taken up for assembly and test is listed in the next slide.*

Assembly matrix

Lead-free plating SOIC (SO44)

Plating alloy	PCB finish	Solder paste
1)Sn MSA 2)Sn Sulphate 3)Sn/Bi 4)Sn/0.7Cu	1)Ni/Au 2)OSP	1) Sn/Ag/Cu

*Control Lot: Sn/Pb plating assembled to Ni/Au PCB with Sn/Pb paste

Lead-free solder ball PBGA256

Solderball composition	PCB finish	Solder paste
1)Sn3.8Ag0.7Cu 2)Sn0.7Cu 3)Sn3.5Ag	1)Ni/Au 2)OSP	1) Sn/Ag/Cu

*Control Lot: Sn/Pb ball assembled to Ni/Au PCB with Sn/Pb paste

Lead-free solder ball FBGA63

Solderball composition	PCB finish	Solder paste
1)Sn3.8Ag0.7Cu (Indium) 2)Sn3.8Ag0.7Cu (Qualitek) 3)Sn3.8Ag0.7Cu (Senju) 4)Sn3.5Ag	1)OSP	1) Sn/Ag/Cu

*Control Lot: Sn/Pb ball assembled to OSP PCB with Sn/Pb paste

The table here shows the type of lead/ball alloys, PCB finish & solder paste that is used in the board assembly for reliability study.

- The lead-free solder paste used for assembly is Qualitek LF217 with an alloy combination of Sn95.5Ag4.0Cu0.5.

- There is a control lot assembled for SOIC, PBGA and FBGA units. This control lot is a combination Sn/Pb finish(Leads/balls) assembled to PCB using Sn/Pb paste from Qualitek.

- Kester lead-free paste is used only during process evaluation to draw a comparison with Qualitek.

- The temperature cycling of SOIC and PBGA parts will be conducted at Gintic. The test condition for SOIC and PBGA will be

- -55/+125 o C to 1000 cycles
- 10min ramp & 10 min dwell

- The temp cycle for FBGA will be conducted in AMD Singapore. The test condition for FBGA is

- -40/+125 o C to 1000 cycles
- 3min ramp 17min dwell

AMD SINGAPORE PROJECT TIMELINE # QED7.4.3-049

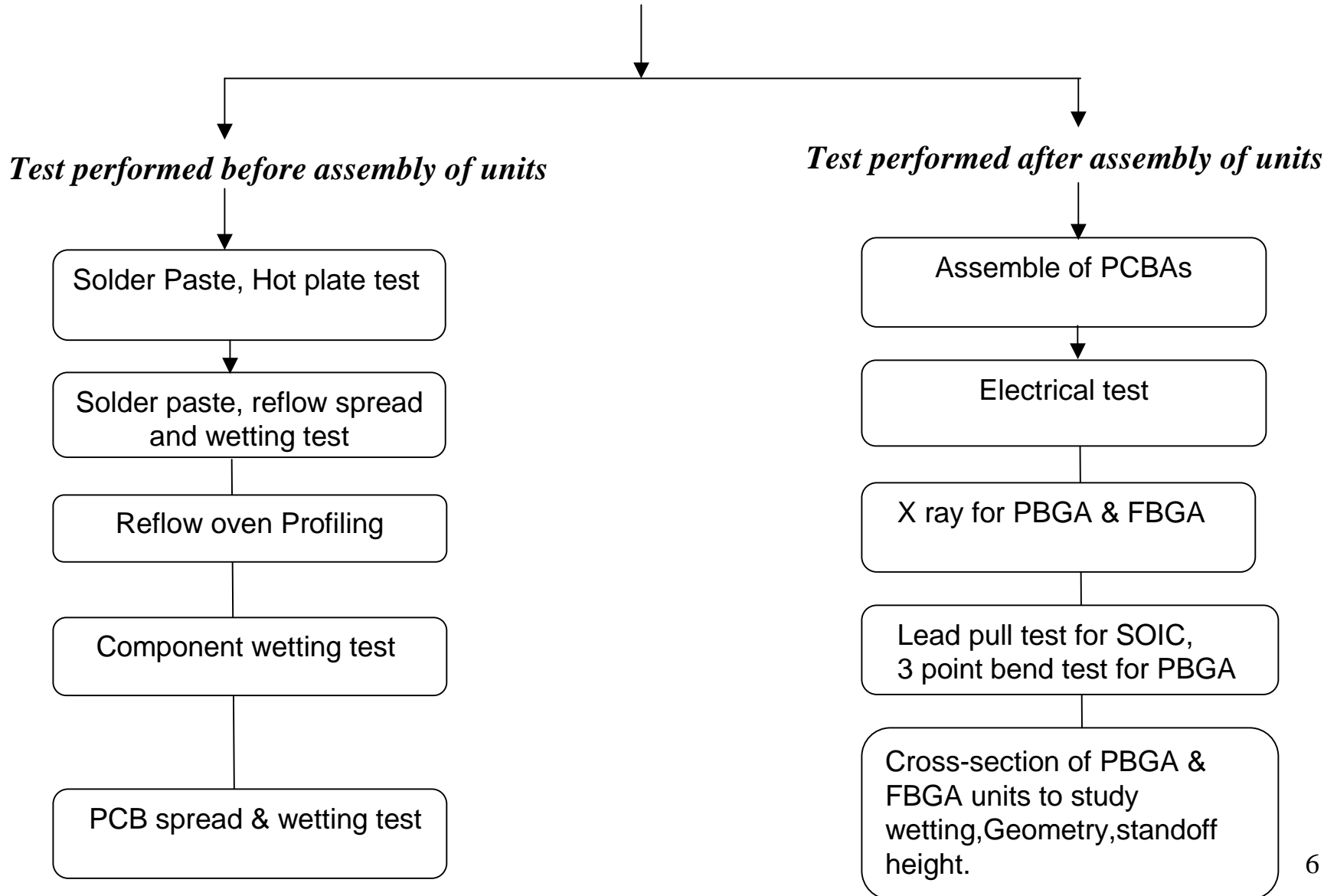
PROJECT TITLE :Board assembly and solder fatigue test

PROJECT TASK	RESP	WORKWEEK 2001											2002			
		40	41	42	43	44	45	46	47	48	49	50	02	06	12	
Finalize Gerber files modification for PCB	Ashok	▲	▲													
Pack &ship PCB, Compt to gintic	Ashok		▲	▲												
Finalization of stencil design & receipt	Ashok		▲	▲												
Solder paste finalization and receipt	Ashok	▲			▲											
programming of pick and place	Gintic		▲	▲												
Solder paste & flux evaluation	Gintic				▲	▲										
Build boards for profiling	Gintic					▲	▲									
Profile the oven for PCBA	Gintic						▲	▲								
Solder paste wetting and spread test	Gintic							▲	▲							
Components wetting test	Gintic							▲	▲							
PCB wetting test	Gintic							▲	▲							
Build process validation boards	Gintic								▲	▲						
Electrical test/lead pull test/bend test/cross-section	Gintic									▲	▲					
Build board for test	Gintic										▲	▲				
Tempertaure cycle test**	Gintic/ LSlim												▲	▲		▲

**Note: As Gintic has one oven only for temp cycle .Temperature cycling of Boards will be done in three batches and will be executed in sequence.

Process validation flow

Test performed to validate the board mount process



Tests performed in Pre- Assembly

Hot Plate test

Alloy:Sn/Ag/Cu, Vendor:Kester



Alloy:Sn/Ag/Cu, Vendor:Qualitek



Alloy:Sn/Pb, Vendor:Kester



Alloy:Sn/Pb, Vendor:Qualitek



The above pictures display the spread of solder paste on PCB test coupons when reflowed using hot plate.

This test is similar to the test method of IPC-TM-650. The objective of this validation test is to have a qualitative data on the ability of the solder paste to wet the surface at specific process conditions. The result of this evaluation should provide the data on dewetting, non wetting and spattering characteristics of the flux..

The solder paste, Sn/Ag/Cu alloy system from Kester and Qualitek was printed on FR4 1.6mm PCB coupon using an 8 mils stencil over 3 round holes of 6.5 mm. Using hot plate the solder paste is melted at 245°C above the eutectic point of the lead-free solder paste.

The inference from the experiment show that lead-free paste from Qualitek wets the surface a little better than Kester. More flux residue is seen with Qualitek lead-free paste than Kester. No spattering of flux is observed in either paste.

Solder paste spread test using linear profile

Paste: Kester; Profile Linear



Paste: Qualitek; Profile Linear



Paste: Kester; Profile Linear



Paste: Qualitek; Profile Linear



The above pictures display the spread of solder paste on PCB test coupons when reflowed using a linear profile.

The objective of this validation test is to have a qualitative data on the ability of the solder paste to wet the surface under conditions closer to product manufacturing conditions under forced air convection reflow. The result of this evaluation provide the data on the dewetting, non-wetting and spattering characteristics of the flux that would be expected on a real life situation.

Test specimens with FR4 1.6mm PCB coupons size of 60 x 15 mm. The solder paste is printed using an 8 mils stencil over 3 round holes of 6.5 mm, with at least of 10 mm apart.

The test is conducted using the forced air convection oven by getting solder paste to reflow at two different peak temperatures of soak and linear profile at profile conditions as shown below.

Solder paste spread test using Soak profile

Paste: Kester; Profile: Soak



Paste: Qualitek; Profile Soak



Paste: Kester; Profile: Soak



Paste: Qualitek; Profile Soak



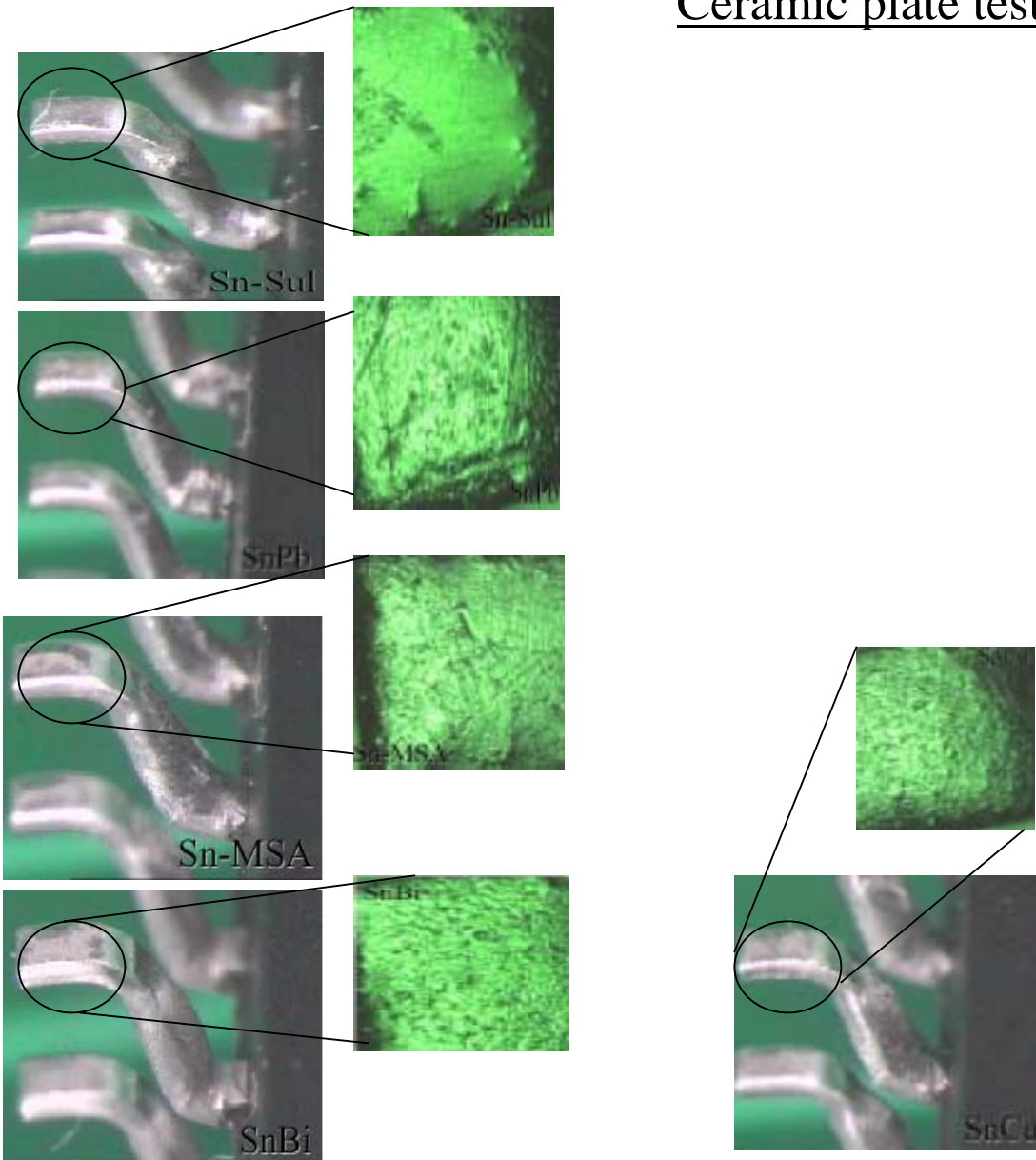
The above pictures display the spread of solder paste on PCB test coupons when reflowed using a soak profile.

Reflow parameters	Linear profile	Soak profile
Peak Temp 1	235°C	235°C
Peak Temp 2	245°C	245°C
Soak time (s) (150-170 °C)	25	70 ± 10
Dwell time (s)	90 ± 3	60 ± 3
Ramp rate (°c/s)	< 2	< 3
Reflow atmosphere	air	air

The following was the inference from the above test

- Both lead-free paste from Kester & Qualitek shows good wetting and spread on test coupon.
- Qualitek shows larger paste-spread area.
- More flux residue is observed with Qualitek than Kester.
- Flux residue of Kester is light to colorless while Qualitek's is brownish.
- No spattering of flux is observed in either of the paste
- Linear profile exhibits better solder spread for Qualitek and Kester solder pastes.

Ceramic plate test



The picture here shows the wicking of solder onto the leads of SOIC packages with different plating finish.

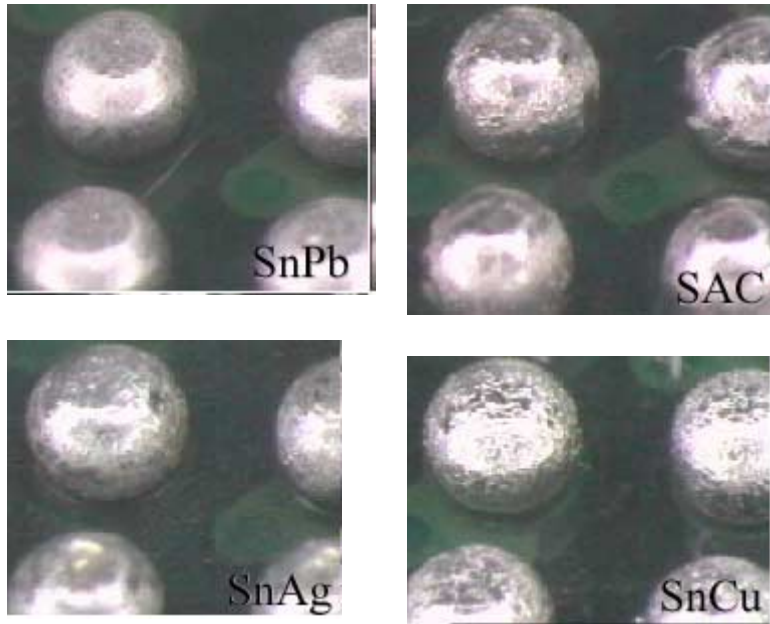
The objective of this test is to test the lead-free component termination's interaction and wetting with the proposed solder paste alloy. This test is done by printing the solder paste on to a ceramic substrate, placing the component onto the substrate and reflowing the ceramic substrate using a typical lead-free reflow profile. Qualitative observation would be done to assess the compatibility by inspecting the amount of solder left over on the ceramic substrate and the flow of the wicked solder on the surface of the lead / Balls.

The inference of this experiment shows that all the leaded packages performed well with no left over of paste on the ceramic plate. All the solder wicks onto the leads. No signs of dewetting or non wetting is observed on the leads.

The above picture shows the wicking of solder after ceramic plate test.
The respective plating finishes are marked on the picture.

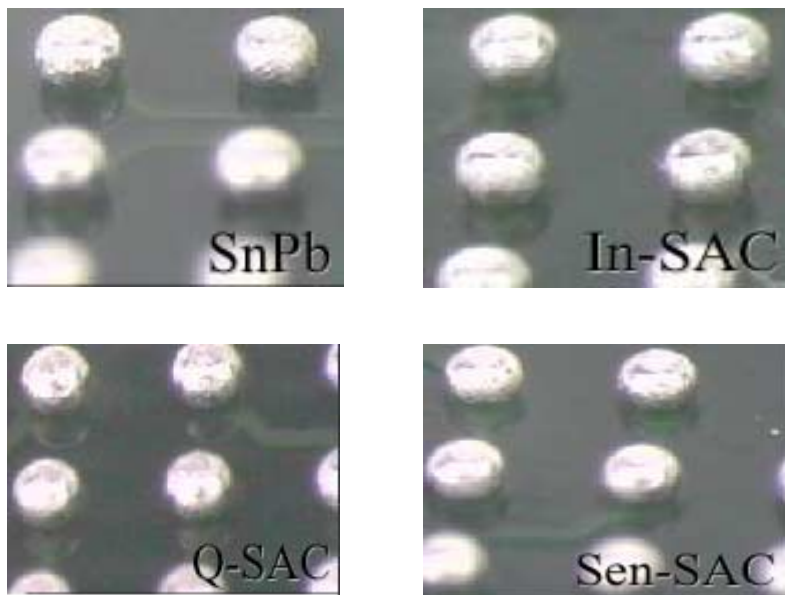
Ceramic plate test

PBGA

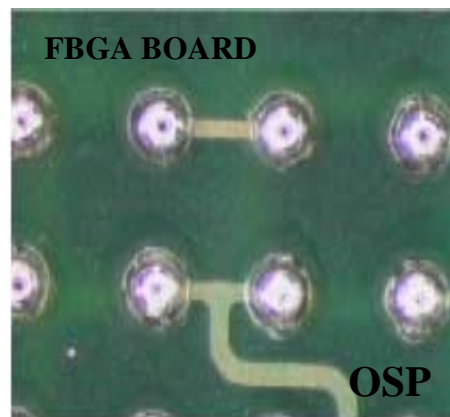
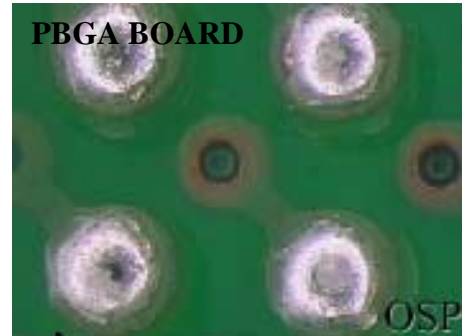
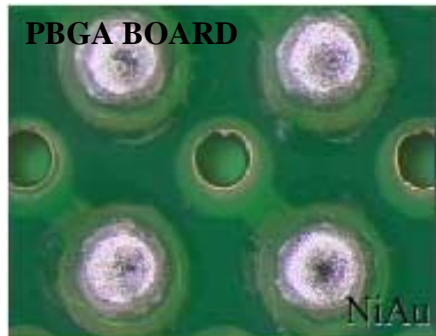


The picture here shows the FBGA and PBGA solder ball after ceramic plate test. The solder coalesces well with solder ball with no remains on the ceramic substrate.

FBGA



PCB Wetting test



The objective of this test is to test the compatibility of wetting and spread characteristics of the solder paste to the actual PCB. The wetting & Spread test on the PCB is done by printing the solder paste on the PCB (In total 5 different PCBs) and reflowing the board using a typical lead-free reflow profile.

Qualitative observation is done by inspecting the wetted, non wetted, de-wetted surface & solder balls..

The inference from this test show that Ni/Au finish PCB boards used for SOIC & PBGA mounting showed very good wetting. But OSP boards used for PBGA mounting showed exposed copper along the corners of pads.

Test performed after assembly of units
Package: SOIC

Electrical test

After assembly: SOIC PKG

SOIC								
Termination	Solder Paste	PCB	Readings in Ohms					AVG
			1	2	3	4	5	
SnPb	SnPb	OSP	2.6	2.7	2.7	2.7	2.7	2.7
SnPb	SnPb	NiAu	2.7	2.7	2.7	2.8	2.8	2.7
SnPb	SnAgCu	OSP	2.7	2.6	2.6	2.6	2.7	2.6
Tin Sul	SnAgCu	OSP	2.7	2.7	2.7	2.7	2.7	2.7
SnCu	SnAgCu	OSP	2.8	2.8	2.8	2.8	2.8	2.8
SnBi	SnAgCu	OSP						#DIV/0!
Tin MSA	SnAgCu	OSP	2.6	2.7	2.6	2.7	2.7	2.7
SnPb	SnAgCu	NiAu	2.8	2.8	2.8	2.8	2.8	2.8
Tin Sul	SnAgCu	NiAu	2.8	2.8	2.8	2.8	2.8	2.8
SnCu	SnAgCu	NiAu	2.8	2.8	2.8	2.8	2.8	2.8
SnBi	SnAgCu	NiAu	2.6	2.6	2.6	2.6	2.7	2.6
Tin MSA	SnAgCu	NiAu	2.8	2.8	2.8	2.7	2.8	2.8

After assembly of SOIC units onto the daisy chain board, the units were checked for electrical continuity.

This table here shows the resistance measured for SOIC components assembled to Ni/Au finish and OSP finished boards. There was no open failures. The average resistance measured across the boards was 2.8ohms.

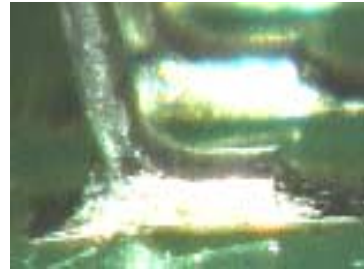
Inspection of Heel & Toe Joint

After assembly: SOIC PKG

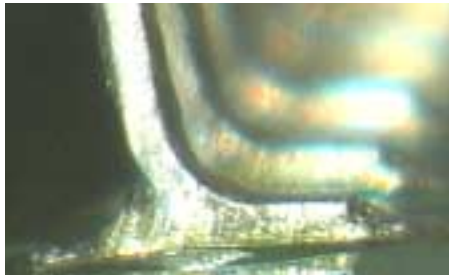
Ni/Au Finish PCB



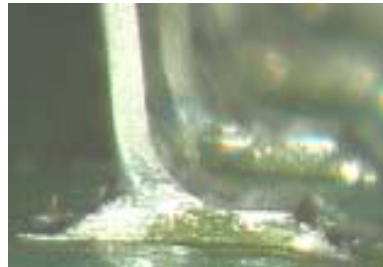
SnPb lead finish/SnPb paste



SnPb lead finish/SnAgCu Paste



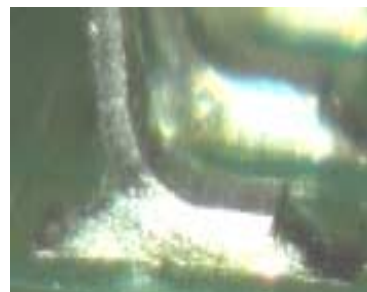
Tin sulphate lead finish/SnAgCu Paste



Sn/Bi lead finish/SnAgCu Paste



Tin MSA lead finish/SnAgCu Paste

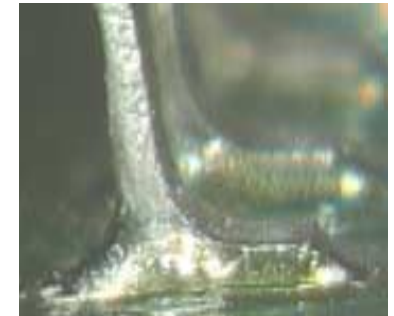


Sn/Cu lead finish/SnAgCu Paste

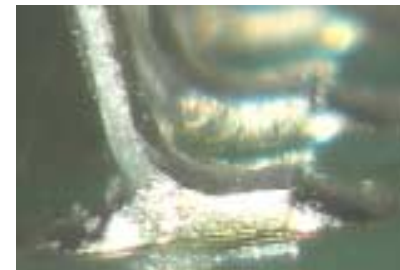
OSP Finish PCB



SnPb lead finish/SnPb paste



SnPb lead finish/SnAgCu Pas



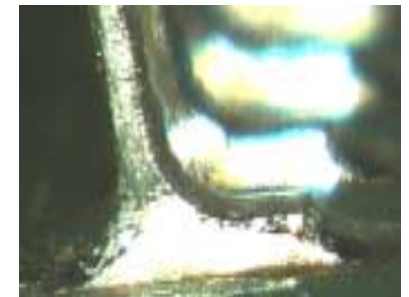
Tin sulphate lead finish/SnAgCu Paste



Sn/Bi lead finish/SnAgCu Paste



Sn/Cu lead finish/SnAgCu Paste



Tin MSA lead finish/SnAgCu Paste

Comment: Good heel and Toe joint was observed on all the units assembled onto Ni/Au and OSP finish

Lead Pull test

After assembly: SOIC PKG

SAC	NiAu						OSP					
	SnCu	SnPb	SnBi	Sn_MSA	Sn	Control	SnCu	SnPb	SnBi	Sn_MSA	Sn	Control
ANOVA-Desig	NSC	NSP	NSB	NSM	NSN	NCO	OSC	OSP	OSB	OSM	OSN	OCO
	1.70	1.80	1.73	1.75	1.55	1.55	1.53	1.60	1.65	1.35	1.58	1.40
	1.63	1.70	1.93	1.58	1.68	1.60	1.73	1.90	1.75	1.68	1.60	1.45
	1.70	1.95	2.15	1.95	1.88	0.80	2.05	1.83	2.03	1.13	1.70	1.58
	1.75	1.35	1.93	1.93	1.95	1.20	1.98	1.98	2.05	1.65	1.60	1.53
	1.68	1.80	1.83	1.80	1.70	1.48	1.83	1.88	1.98	1.20	1.73	1.60
	1.58	1.65	1.83	1.73	0.78	1.40	1.33	1.13	1.85	1.53	1.60	1.50
	1.75	1.60	1.93	1.80	1.63	1.38	1.38	1.50	1.90	1.35	1.55	1.50
	1.58	1.95	1.73	1.73	1.55	1.38	1.75	1.70	2.05	1.45	1.25	1.70
	1.88	1.75	2.33	1.95	1.63	1.28	1.73	1.25	2.05	1.30	0.90	1.30
	2.03	1.98	1.75	1.88	1.70	1.53	1.23	1.33	1.93	1.10	0.90	1.43
Average	1.73	1.75	1.91	1.81	1.61	1.36	1.65	1.61	1.92	1.37	1.44	1.50
S.D.	0.14	0.19	0.19	0.12	0.32	0.23	0.28	0.30	0.14	0.20	0.31	0.11

AMD spec: 06-917

>500 grams

- The assembled units were subjected to lead pull test . This was done to check the solder joint strength & observe the location of fracture.
- Pull test was performed using Dage pull tester and readings were registered.
- The table here shows the pull strength of lead-free plated units assembled to a Ni/Au & OSP finished PCB.
- The inference of reading shows that all plating finishes performed equivalent to control lot.
- There was no significant difference in pull force between plating finish. All the plating finishes registered pull force well above spec of 500gms. Inspection of fracture location show that all the fracture occurred in solder.

Test performed after assembly of units
Package: PBGA

Electrical test & X ray

After assembly: PBGAPKG

PBGA								
			Readings in Ohms					
Termination	Solder Paste	PCB	1	2	3	4	5	AVG
SnPb	SnPb	OSP						#DIV/0!
SnPb	SnPb	NiAu	2.2	2.3	2.3	2.3		2.3
SnPb	SnAgCu	OSP	1.8	1.7	1.8	1.7	1.4	1.7
SnAgCu	SnAgCu	OSP	2.1	2.4	1.8	1.5	2.1	2.0
SnAg	SnAgCu	OSP	1.4	1.8	2.1	1.9	1.7	1.8
SnCu	SnAgCu	OSP	1.9	1.6	1.8	1.9	1.7	1.8
SnPb	SnAgCu	NiAu	1.7	1.8	2.1	1.7	2.1	1.9
SnAgCu	SnAgCu	NiAu	1.6	2.1	2.1	2.1	2.2	2.0
SnAg	SnAgCu	NiAu	2.1	2.2	1.9	2.2	2.3	2.1
SnCu	SnAgCu	NiAu	1.7	1.8	1.6	1.9	2	1.8

Assembled PBGA units were checked for electrical continuity. This table here shows the resistance measured for SOIC components assembled to Ni/Au finish and OSP finished boards. There was no open failures. The average resistance measured across the boards was 2.0ohms.

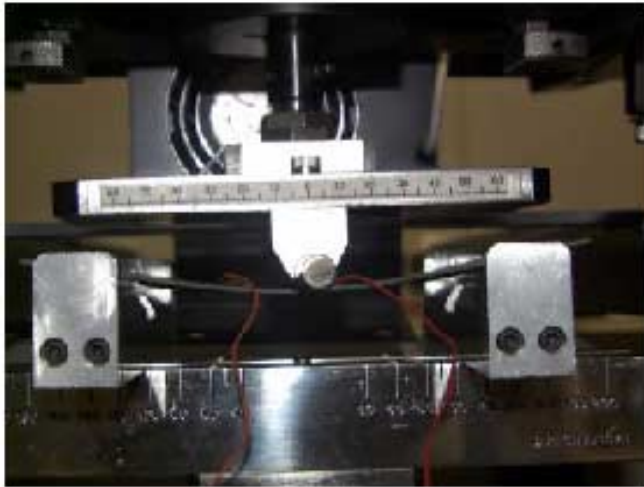


X ray image of PBGA unit, shows alignment Ball to pad.

X-ray test was done to check for misalignment, and solder short.

3-Point Bend Test

After assembly: PBGA PKG



#	Component	PCB	Daisy Chain Failure		Max Load N	Max Disp MM	Remarks/Failure Mode
			DistM M	Load N			
1	SnCu	NiAu	13.7		162	18.5	SJ Interface to PCB
2	SnCu	NiAu	10.1	82	137	15.3	SJ Interface to PCB
1	SnCu	OSP	No SJ Failure		118	18.3	Mould peel off
2	SnCu	OSP	No SJ Failure		143	18.3	Mould Crack
1	SnAgCu	NiAu	6.9	64	130	16.0	SJ Interface to PCB
2	SnAgCu	NiAu	10.4	54	90	10.5	SJ Interface to PCB
1	SnAgCu	OSP	10.2	82	97	13.7	SJ Interface to PCB
2	SnAgCu	OSP	6.2	56	58	6.2	SJ Interface to PCB
1	SnAg	NiAu	No SJ Failure		160	17.5	Mould Crack start at 9 mm
2	SnAg	NiAu	No SJ Failure		150	17.0	Mould peel off start at 9mm
1	SnAg	OSP	No SJ Failure		130	17.5	Mould Crack start at 8.3mm
2	SnAg	OSP	No SJ Failure		105	16.5	Mould peel off start st 9 mm
1	SnPb	OSP	No SJ Failure		115	18.5	Mould Crack start at 10 mm
2	SnPb	OSP	No SJ Failure		105	18.0	Mould Crack start at 11 mm
1	SnPb	NiAu	5.4	58	58	6.2	SJ Interface to PCB
2	SnPb_SnPb	NiAu	6.4	66	68	7.1	SJ Interface to PCB

The 3 point bend test is conducted on the Instron universal testing machine by deflecting the board at a constant load to induce package break-off from the PCB. The time for the first failure of the DC circuit & the maximum load at which the package breaks off the PCBA were measured. The test results were compared in relation to each other, apart from observing the failure mode. The inference of this test shows that

-The lead-free solder joint performance were as good as or better than the Sn/Pb solder joint.

-At location, where a crack in the mould or peel off of the mould occurred, solder joint was inspected and found to be good.

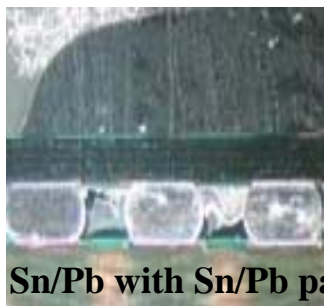
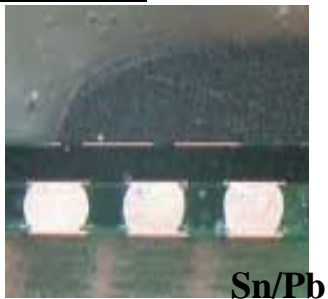
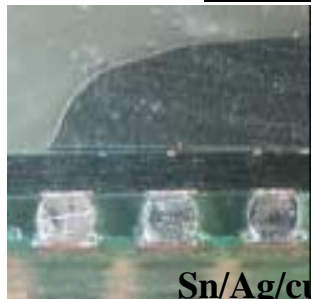
-Most of the solder joint failure mode was between the solder ball and the PCB pad. (More than 95% of the balls were attached to the package)

-No major issues that could lead to any poor reliability performance was detected.

Cross-section of PBGA units

After assembly: PBGA PKG

Ni/Au Finish PCB



OSP Finish PCB



Comment: Assembled PBGA units were cross-sectioned for inspection. The wetting of joints was found to be good. The joint geometry was good, which measured an average stand-off height of 20mils.

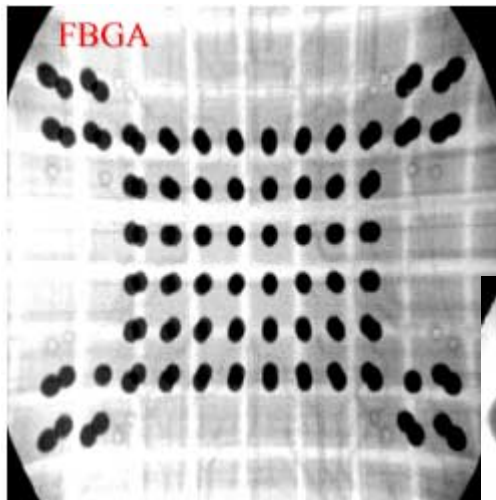
Test performed after assembly of units
Package: FBGA

Electrical test & X ray

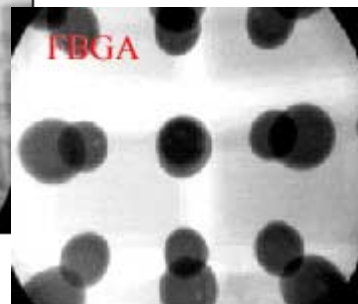
After assembly: FBGA PKG

FBGA								
			Readings in Ohms (Top/Bottom N1-N2)					
Termination	Solder Paste	PCB	1	2	3	4	5	AVG
SnPb	SnPb	OSP						#DIV/0!
SnPb	SnAgCu	OSP	0.9	0.9	0.9	0.9	0.9	0.9
Senju SnAgCu	SnAgCu	OSP	0.8	0.8	0.9	0.8	0.8	0.8
Indium SnAgCu	SnAgCu	OSP	0.7	0.8	0.7	0.8	0.8	0.8
Qua.SnAgCu	SnAgCu	OSP	0.7	0.8	0.8	0.7	0.8	0.8
SenjuSnAg	SnAgCu	OSP	0.8	0.9	0.8	0.8	0.8	0.8

Assembled FBGA units was checked for electrical continuity. This table here shows the resistance measured for SOIC components assembled to Ni/Au finish and OSP finished boards. There was no open failures. The average resistance measured across the boards was 2.0ohms.

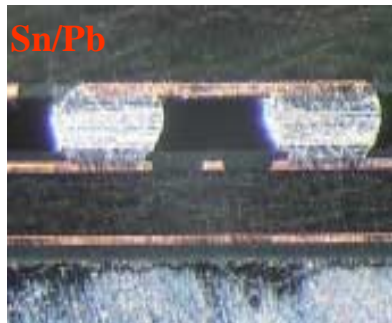
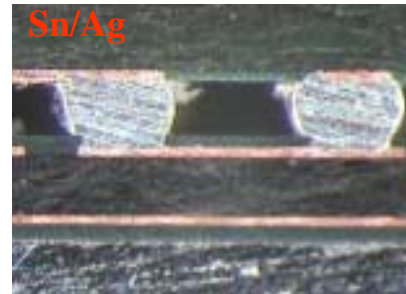
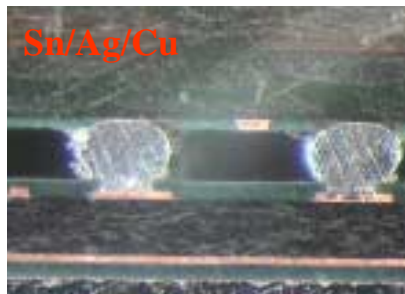


X ray image of PBGA unit, shows alignment of Ball to pad.



X-ray test was done to check for misalignment, and solder short. X-ray image here gives an appearance of misalignment, but this is not true. The appearance was due to the assembly of units on a two-sided board.

Cross-section of FBGA units assembled onto OSP PCB



Comment: Assembled FBGA units were cross-sectioned for inspection. The wetting of joints was found to be good. The joint geometry was good which measured an average stand-off height of 10.5mils.

Status Summary:

- All the combinations of SOIC ,PBGA & FBGA units has been assembled after validating the process.
- These units have to be subjected to thermal cycling test . This will start on or before WW50 ahead of plan.
- The solder joint fatigue of lead-free joints will studied and reported after completion of test.