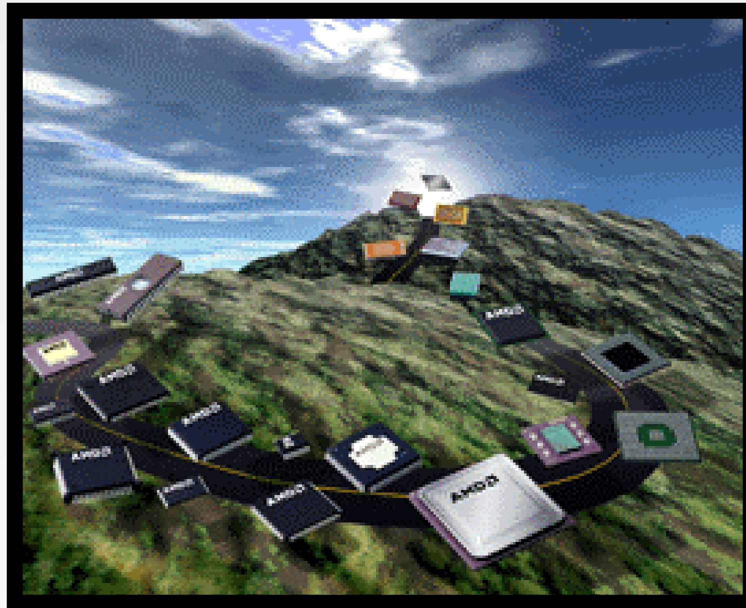
Lead-Free Project
Phase 1: Package Evaluation Plan



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Pb-FREE PROGRAM

OBJECTIVE

Define alternatives for production of Pb-free packaging based on an understanding of technical requirements

Phase 1: Evaluate current packaging materials & assembly processes (Program described in this report)

Phase 2: Evaluate and develop available solutions to material & process incompatibility (Program to be defined)

Phase 3: Production implementation (will only happen when required by business forecast)

Pb-FREE PROJECT TEAM

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EVALUATION PROJECTS

- **Evaluate the sensitivity of current packages to higher temperature reflow profiles and determine the impact of the higher temperatures on device reliability.**
  - Select representative IC packages
  - Assess the moisture & reliability impact using standard qualification tests with "Pb-free" preconditioning at 260 °C.
  - Determine the effect on device performance of exposure to higher processing temperatures
- **Evaluate lead finish options for leadframe packages**
  - Evaluate metallurgical, process, and cost parameters
- **Evaluate solder ball options for BGA/FBGA packages**
  - Evaluate metallurgical, process, and cost parameters

DEVICE/PACKAGE ASSESSMENT

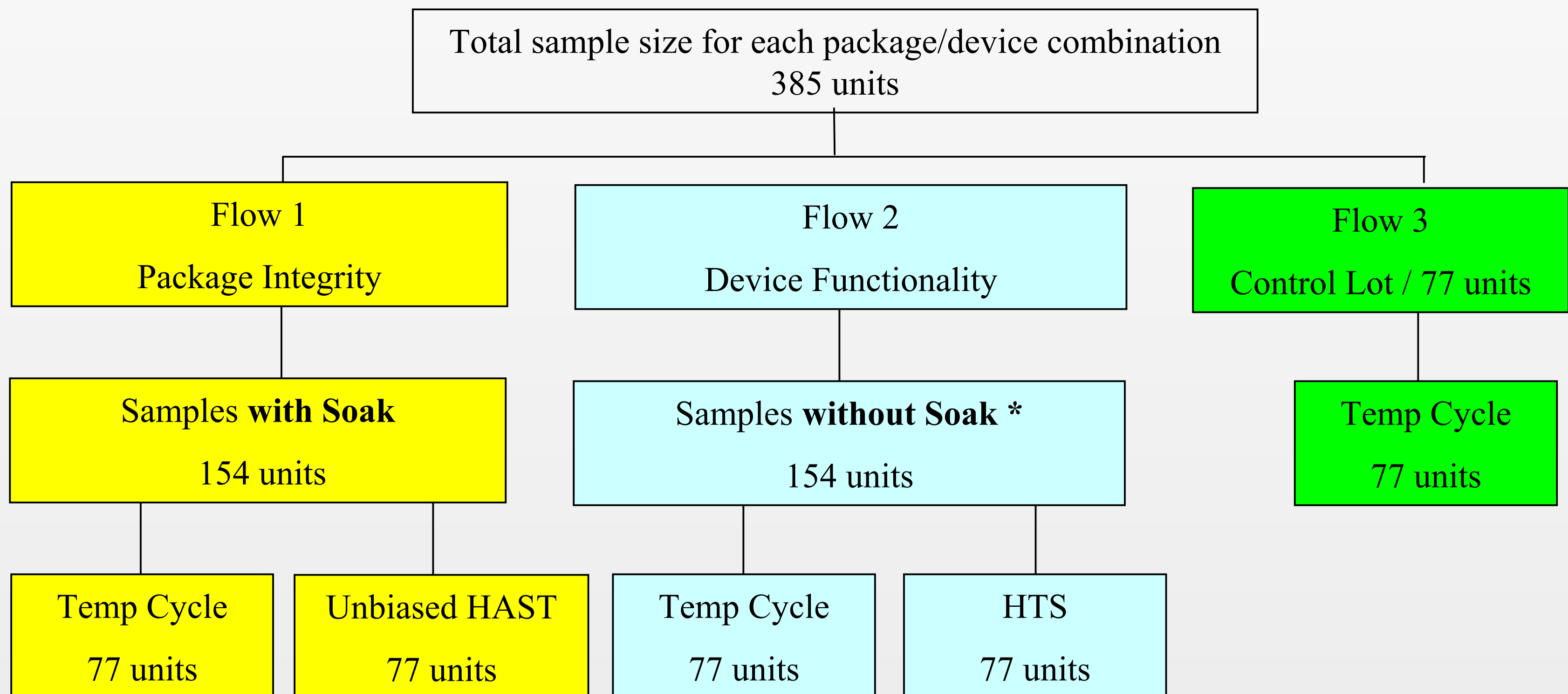
Background

- All likely replacement solder alloys have liquidus between 210 to 220 ^{o}C.
- Peak reflow temperatures expected to be 20 to 40 ^{o}C above melting point. Will vary from customer to customer, so have to be concerned with worst case.
- Pop-corn, cracking of chip components, and device functionality are potential issues.
- Higher reflow temperatures and faster ramps may result in higher incidence of delamination in packages. Additional package warpage could result in coplanarity problems especially with large IC packages.
- An assessment of existing components to a Tmax >240 °C is necessary.
- Addition of 260 °C preconditioning to JESD22-A113 is being proposed in JEDEC.

DEVICE/PACKAGE ASSESSMENT

Test Plan

- Select IC package and device types (based on package size, forecast volumes, device type, availability, fabrication technology, die size, *etc.*)
- Electrical test at each read point in addition to C-SAM and failure analysis procedures



* Note : Conduct without soak to differentiate temperature-induced failures from package-related failures

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DEVICE/PACKAGE ASSESSMENT

Device/Package Matrix

	Evaluation Lots					*Contol Lots*
#	Pkg Type	Rel Lab Location	Jedec PC Level	T/C Conditions	HAST Conditions	Jedec PC Reflow Temp
1	FLB 73 (MCP)	PNG	3	-40/150	**110/85**	**235**
2	FDE 48	PNG	3	-40/150	**110/85**	**235**
3	TS 44 (Type 2)	PNG	3	-40/150	130/85	**235**
4	FBD 48 (6x12)	PNG	3	-40/150	**110/85**	**235**
5	FBD 63 (8x14)	PNG	3	-40/150	**110/85**	**235**
6	TS 40	PNG	3	-40/150	130/85	**235**
7	FBB 48	BKK	3	-40/150	**110/85**	**235**
8	TS 48	BKK	3	-40/150	130/85	**235**
9	SO 44	BKK	3	-40/150	130/85	**235**
10	PL 32	BKK	2	-40/150	130/85	220
11	PDE 208	SGP	3	-40/150	130/85	220
12	PQR 208	PNG	3	-40/150	130/85	220
13	PQR 160	SGP	3	**-40/125**	130/85	220
14	PQL 176	SGP	3	-40/150	130/85	220
15	PL 84	SGP	3	-40/150	130/85	220
16	PL28	SGP	1	-40/150	130/85	220

Notes:

1. Reflow temperature for all Evaluation Lots = 255 +5/-0 C.

2. PC Level, T/C, HTS and HAST conditions are SAME for both evaluation and control lots.

3. High temp storage condition is 150 C.

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DEVICE/PACKAGE ASSESSMENT

Pre-conditioning Profile

- There is no accepted standard profile, but a 260 °C peak (based on the 217 °C melting point of SnAgCu alloy) is gaining ground.
- IBM presented some initial data that 255 +5/-0 °C is a recommendable peak temperature for components <350 mm^3. For components >350 mm^3 they recommend 240 +5/-0 °C.
- ANAM reviewing 255 +5/-0 °C for all packages including BGAs.
- NEMI proposed a preconditioning profile that is being used by several organizations.

Condition	Existing J-Std 020A	Proposed Precon reflow profile (per NEMI)
Average ramp up rate to melting point	2.5 °C /sec (max	2.5 °C - 3 °C /sec (max)
Preheat temperature and dwell time	60 - 120 sec (max) at 125 °C (+/- 25 °C)	60 - 120 sec (max) at 125 °C (+/- 25 °C)
Time above melting point 217 °C	60 - 150 secs	80 secs
Time within 5 °C of actual peak temperature	10 - 20 secs	10 - 20 secs
Peak temperature range	220 +/- 5 °C	255 (+5 ° / -0 ° C)
Ramp down rate	6 °C/sec (max)	6 °C/sec (max)
Time from 25 °C to peak temperature	4 - 6 mins (max)	6 min (max)

DEVICE/PACKAGE ASSESSMENT

BangkokTest Plan (4 Packages)

Samples in Test

		FBE48	TS48	SO44	PL32
Flow1					
T/C (-40/150)	500 cycles	77	77	77	77
	1000 cycles	77	77	77	77
HAST (110C/85%RH)	96 hours	77	NA	NA	NA
	264 hours	77	NA	NA	NA
HAST (130C/85%RH)	48 hours	NA	77	77	77
	96 hours	NA	77	77	77
Flow2					
HTS(150C)	168 hours	77	77	77	77
	500 hours	77	77	77	77
T/C (-40/150)	500 cycles	77	77	77	77
	1000 cycles	77	77	77	77
Flow3					
T/C (-40/150)	500 cycles	77	77	77	77
	1000 cycles	77	77	77	77

DEVICE/PACKAGE ASSESSMENT

Penang Test Plan (7 packages)

Samples in Test

		TS40	TS44	FLB73	FDE48	FBD48	FBD63	PQR208
Flow1								
T/C (-40/150)	500 cycles	77	77	77	77	77	77	77
	1000 cycles	77	77	77	77	77	77	77
HAST(110C/85%RH)	96 hours	NA	NA	77	77	77	77	77
	264 hours	NA	NA	77	77	77	77	77
HAST(130C/85%RH)	48 hours	77	77	NA	NA	NA	NA	NA
	96 hours	77	77	NA	NA	NA	NA	NA
Flow2								
HTS(150C)	168 hours	77	77	77	77	77	77	77
	500 hours	77	77	77	77	77	77	77
T/C (-40/150)	500 cycles	77	77	77	77	77	77	77
	1000 cycles	77	77	77	77	77	77	77
Flow3								
T/C (-40/150)	500 cycles	77	77	77	77	77	77	77
	1000 cycles	77	77	77	77	77	77	77

DEVICE/PACKAGE ASSESSMENT

SingaporeTest Plan (6 Packages)

Samples in Test

		PL84	**PQL176**	**PL28**	**PDE208**	**PQR160**	**BGA569**
Flow1							
T/C (-40/150)	500 cycles	77	77	77	77	77	77
	1000 cycles	77	77	77	77	77	77
HAST(110C/85%RH)	96 hours	NA	NA	NA	NA	NA	77
	264 hours	NA	NA	NA	NA	N.A	77
HAST(130C/85%RH)	48 hours	77	77	ww10	77	77	NA
	96 hours	77	77	77	77	77	NA
Flow2							
HTS(150C)	168 hours	77	77	77	77	77	77
	500 hours	77	77	77	77	77	77
T/C (-40/150)	500 cycles	77	77	77	77	77	77
	1000 cycles	77	77	77	77	77	77
Flow3							
T/C (-40/150)	500 cycles	77	77	77	77	77	77
	1000 cycles	77	77	77	77	77	77

Pb-FREE LEADFRAME PLATING ASSESSMENT

Objective:

To determine feasible replacements for Pb/Sn plating on leadframe packages

Scope:

- Include Sn, Sn0.7Cu, and SnBi in lab scale and production scale evaluation
- Conduct characterization and tests comprised of:

Plating thickness & composition	Morphology
VM after plating & DTFS	Solderability
Steam aging	Adhesion
Metallurgical change after bake	Whisker growth
SMT lead quality	SMT lead pull strength

- Test vehicles to include different bend angles and copper type leadframes. Included PL20, PL32, PL84 & TS48.

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Pb-FREE SOLDER SPHERE ASSESSMENT

Objective:

To determine feasible replacements for Pb/Sn solder balls on BGA packages

Scope:

- Determine existing Pb/Sn solderball compatibility to various Pb-free pastes (this is in case where supplier decides to use lead-free before AMD is ready with Pb-free BGA offerings)

- Determine Pb-free solderball compatibility to Au/Ni/Cu substrate padsand fluxes **(Package Level)**

Solderball shear test	Solder ball structure
HTS for metallurigical changes	3x reflow and metallurgical changes
Wettability	

- Determine selected Pb-free solder ball compatibility to various PCB finishes and Pb-free pastes **(Board Level)**

Package shear test	Solder fatigue test

- Cost analysis of material alternatives

- FEA simulation at board level to predict solder-joint reliability for both FBGAs

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