

AMD Server Workstation Roadmap Update Fact Sheet

May 7, 2008 — Today, Randy Allen, corporate vice president and general manager, Server and Workstation, AMD provided updates to AMD's server workstation processor roadmap.

"Based on input from our OEM partners, AMD is updating its server roadmap to strengthen its alignment with end-customer priorities," said Allen. "Today's roadmap updates support AMD's long-standing goal of meeting our OEM partners' demands for platform longevity while driving increased performance-per-watt and more advanced virtualization features and functionality."

- **"Shanghai" on track to begin production in 2H08.** Development of AMD's first 45nm server processor, codenamed "Shanghai," is on schedule to begin production in the second half of 2008 and will now feature coherent HyperTransport 3.0 for processor-to-processor communication. In addition to increasing the shared Level-3 cache from 2 MB to 6 MB, "Shanghai" will include core and instruction-per-clock (IPC) enhancements.
- **"Istanbul" to bring 6-core processing within current socket in 2H09.** New to the AMD server roadmap, "Istanbul" is will be a 6-core server processor that will fit within the current Socket F1 (1207), which will enable OEMs to preserve platform investments and increase system performance-per-watt. "Istanbul" is planned to be available for 2P and above configurations, and leverage AMD's industry-leading Direct Connect Architecture, which alleviates the system communication bottlenecks in other processors.
- **The third-generation AMD Opteron processor Socket G34 platform is planned for 1H10.** In 2010, AMD expects to introduce its third-generation AMD Opteron processor Socket G34 platform. The Socket G34 platform is planned to offer features such as DDR3 memory capabilities and the AMD RD890 chipset for non-coherent HyperTransport 3.0, along with an additional HT link.

- **New six- and twelve-core AMD Opteron processors for Socket G34 planned for 1H10.** A six-core processor, codenamed "Sao Paolo," is planned to incorporate DDR3 memory and an additional HyperTransport 3.0 link as well as a 6-core design. "Magny Cours," a 12-core processor will also leverage these features.