High Performance 25nm FDSOI Devices with Extremely Thin Silicon Channel

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* Applied Materials

Outline

- **Introduction**
- Device Fabrication
- Device Performance
- Control of Device Parameters
- NiSi Gate Reliability
- Conclusions

FDSOI Requirements

- We successfully implement three crucial processing steps that enable short channel FDSOI devices.
- Electrostatic control is achieved by very thin Silicon channel and mid-gap metal gate work function.
- Performance is enhanced by successful selective epitaxial growth in the source/drain region.
- We achieve high mobility and low vertical field due to undoped channel.

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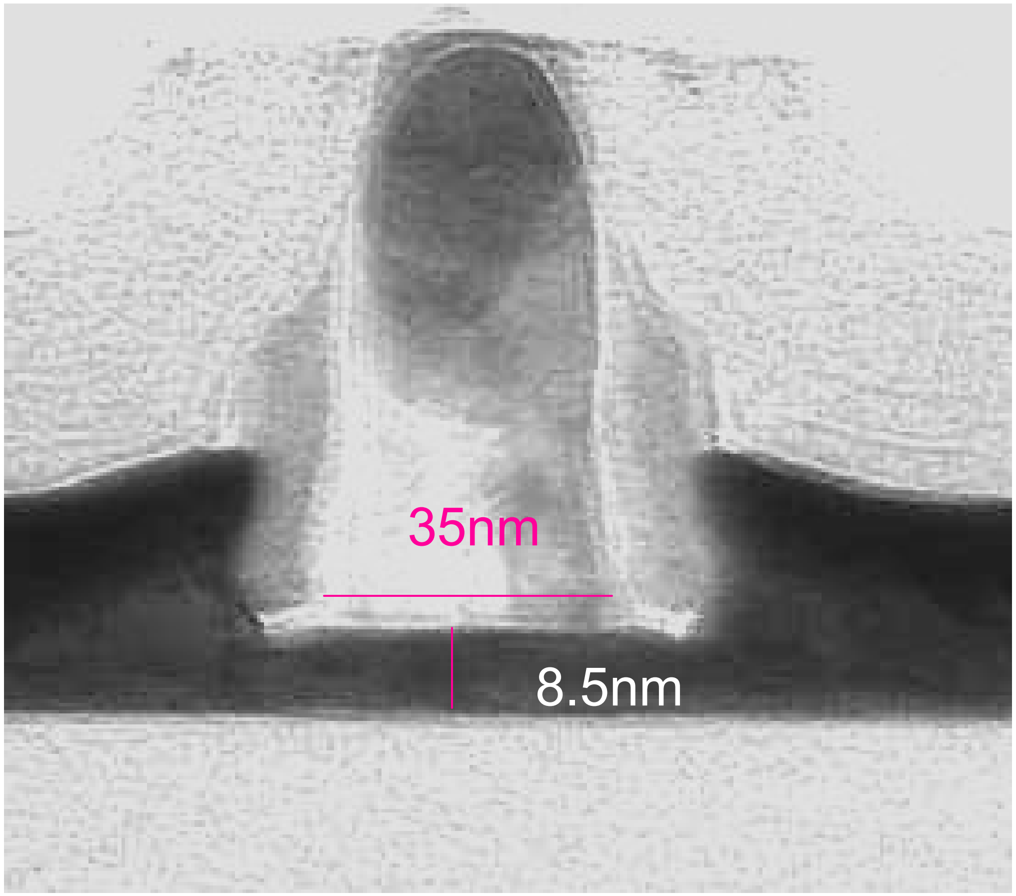
Device Fabrication

- SOI wafer with 200nm buried oxide with Silicon thinned down to sub-10nm thickness.
- Mesa isolation is used for simplicity.
- Nitrided oxide with EOT = 1.3nm is used.
- Polysilicon is patterned with nominal gate length of 35nm.
- After very thin nitride spacer (<15nm) we grow 30nm of selective epitaxial Silicon on very thin (3-7 nm) undoped silicon.
- Extension is doped by using tilted implants.
- After source/drain formation and planarization the Polysilicon gates are fully silicided.

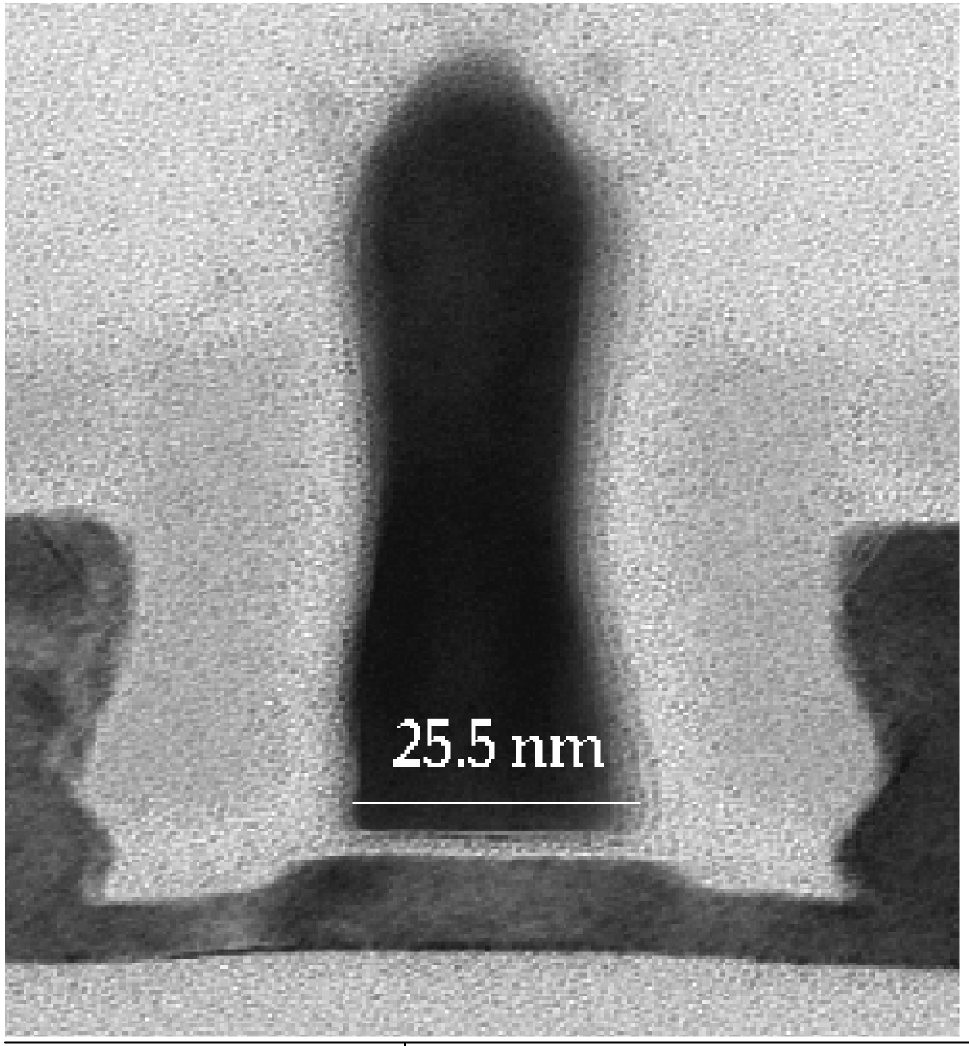
35nm FDSOI with SEG



Nominal devices have:

- 35nm gate with 8.5nm thick silicon channel
- 12-15 nm nitride spacer with 5nm oxide liner
- 30nm SEG on undoped silicon

25 nm FDSOI



Sub-nominal devices feature:

- fully silicided NiSi gate
- 8nm thick channel
- 5nm thick extension region
- Successful epitaxial growth without faceting on undoped very thin silicon

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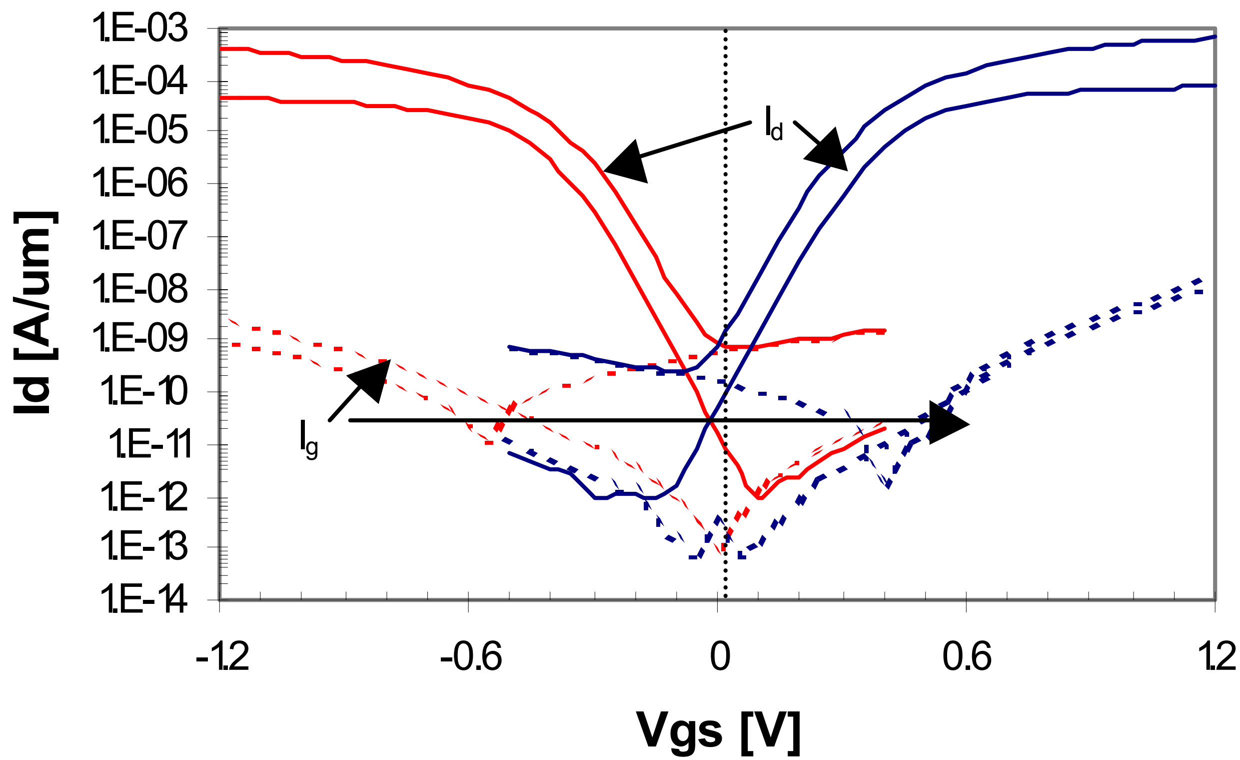
35nm FDSOI Devices



S_n=68mV/dec

S_p=70mV/dec

D_n=80mV/V

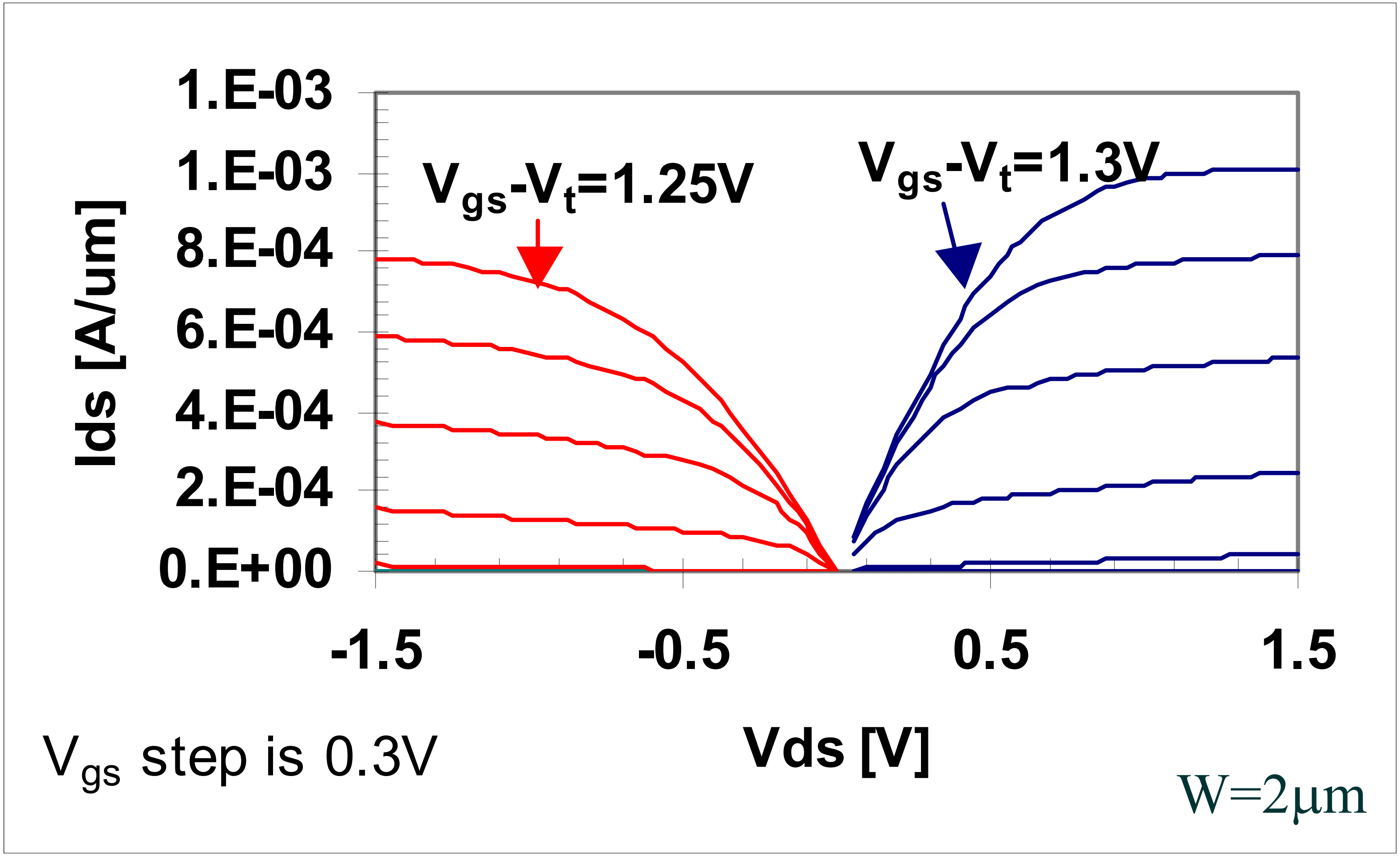
D_p=61mV/V

j_{gn}=25A/cm^2 *

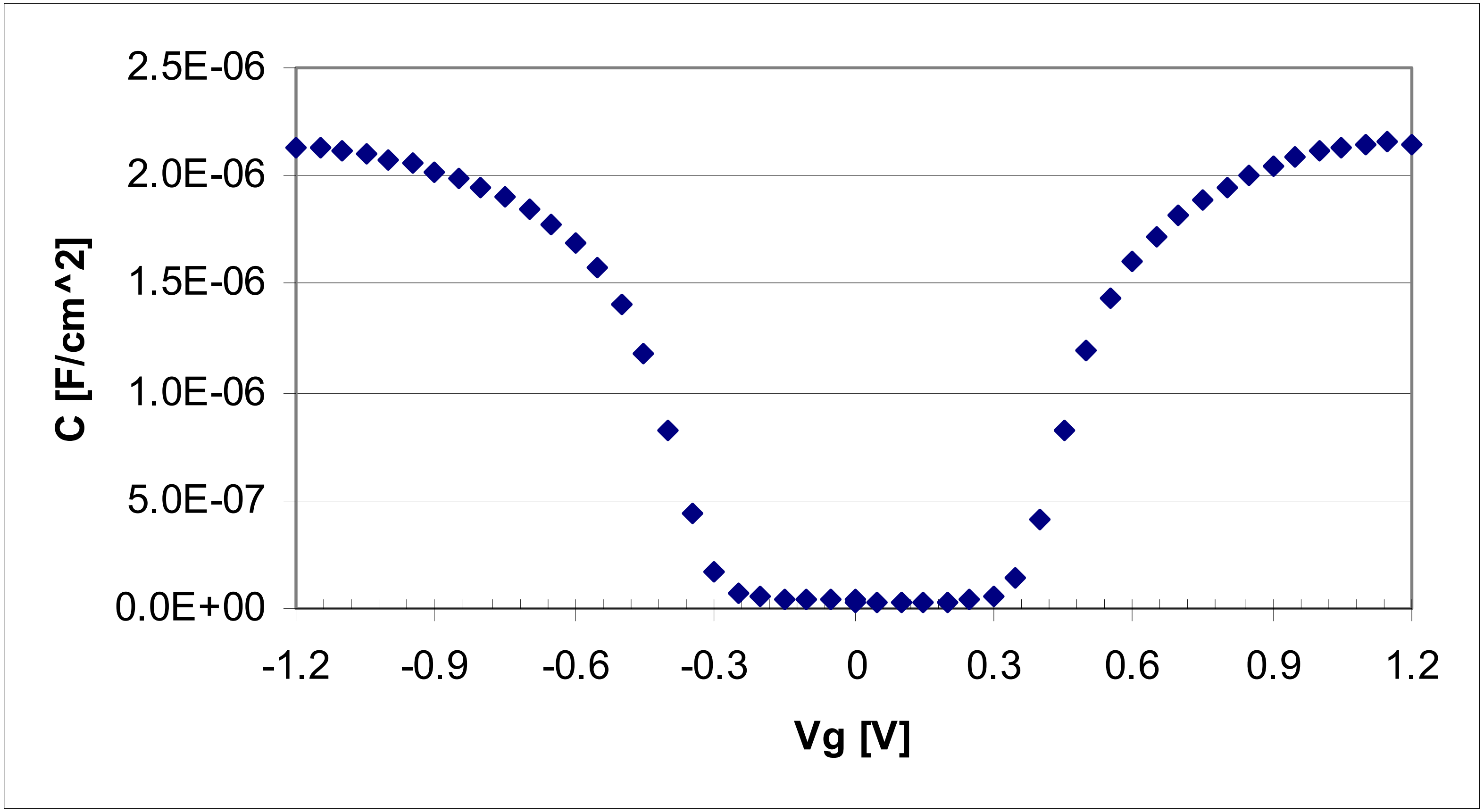
j_{gp}=6A/cm^2 *

*Gate leakage is measured on large area transistors.

25nm FDSOI Devices

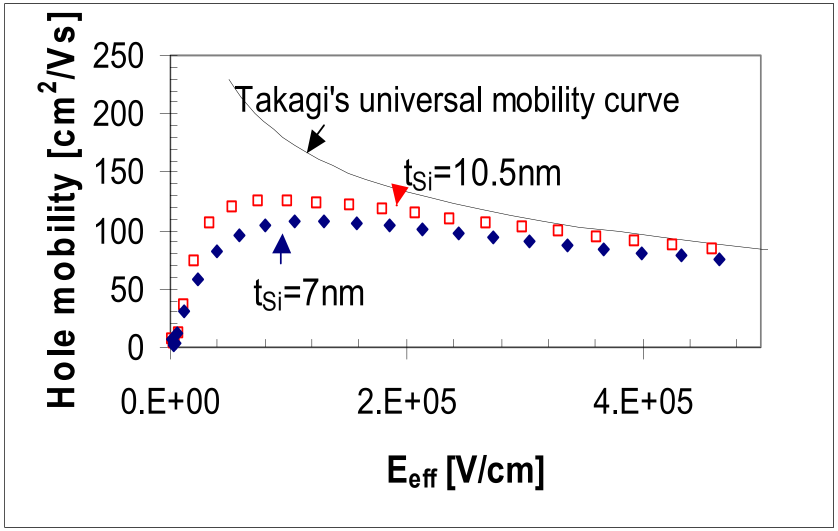


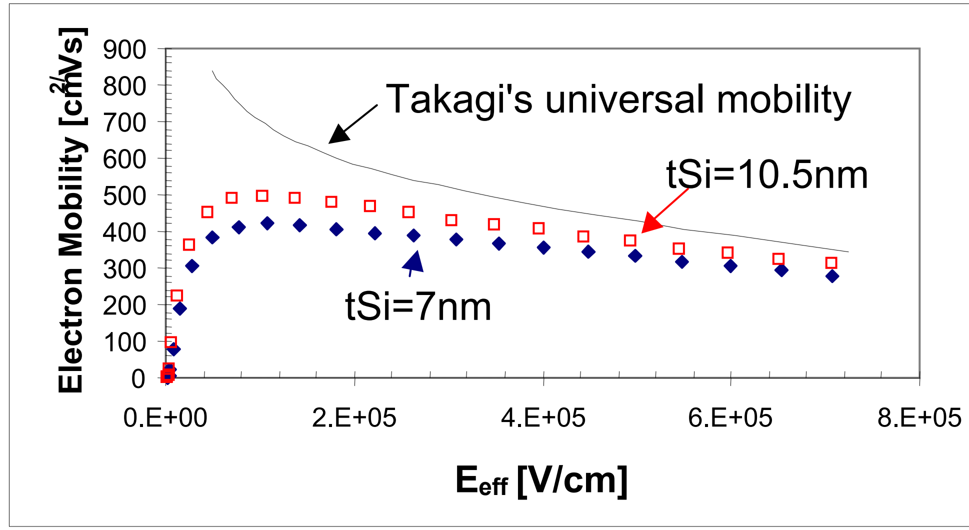
C-V Curve for 1.3nm Gox



- Symmetric threshold voltage
- CET = 1.6nm

Mobility for Sub-10nm Si





- Very high mobility at operating voltages.
- 7nm channel has 19% electron and 14% hole mobility degradation.
- Mobility is extracted by using split C-V technique on a 5-finger transistor with L=3.2μm and W=6.25μm.

Performance Comparison for FDSOI

* estimate

Parameter	FDSOI	FDSOI	FDSOI	FDSOI	[1]	[1]	[2]	[2]	[3]	[3]
	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
Lgate[nm]	25	25	35	35	65	50	60	60	35	14
tSi[nm]	8.5	10	8.5	10	15*	15*	40	40	7	4.6
GOX [nm]	1.3	1.3	1.3	1.3	1.5	1.5	N/A	N/A	2.2	1.2
Vdd [V]	1.5	1.5	1.5	1.5	1.3	1.3	1.3	1.3	1.5	1.2
Vgs-Vt [V]	1.3	1.25	1.2	1.2	1.2*	1.2*	1.2*	1.2*	1.5*	1.4*
S [mV/dec]	95	82	68	70	75	70	69	71	90	71
DIBL [mV/V]	146	108	80	61	45	40	41	52	100*	24
Ion [uA/um]	1006	**789**	888	**645**	1180	**650**	930*	**460***	700	**440**
Ioff [nA/um]	140	**27**	0.8	**1.5**	60	**9**	100*	**20***	N/A	**270**

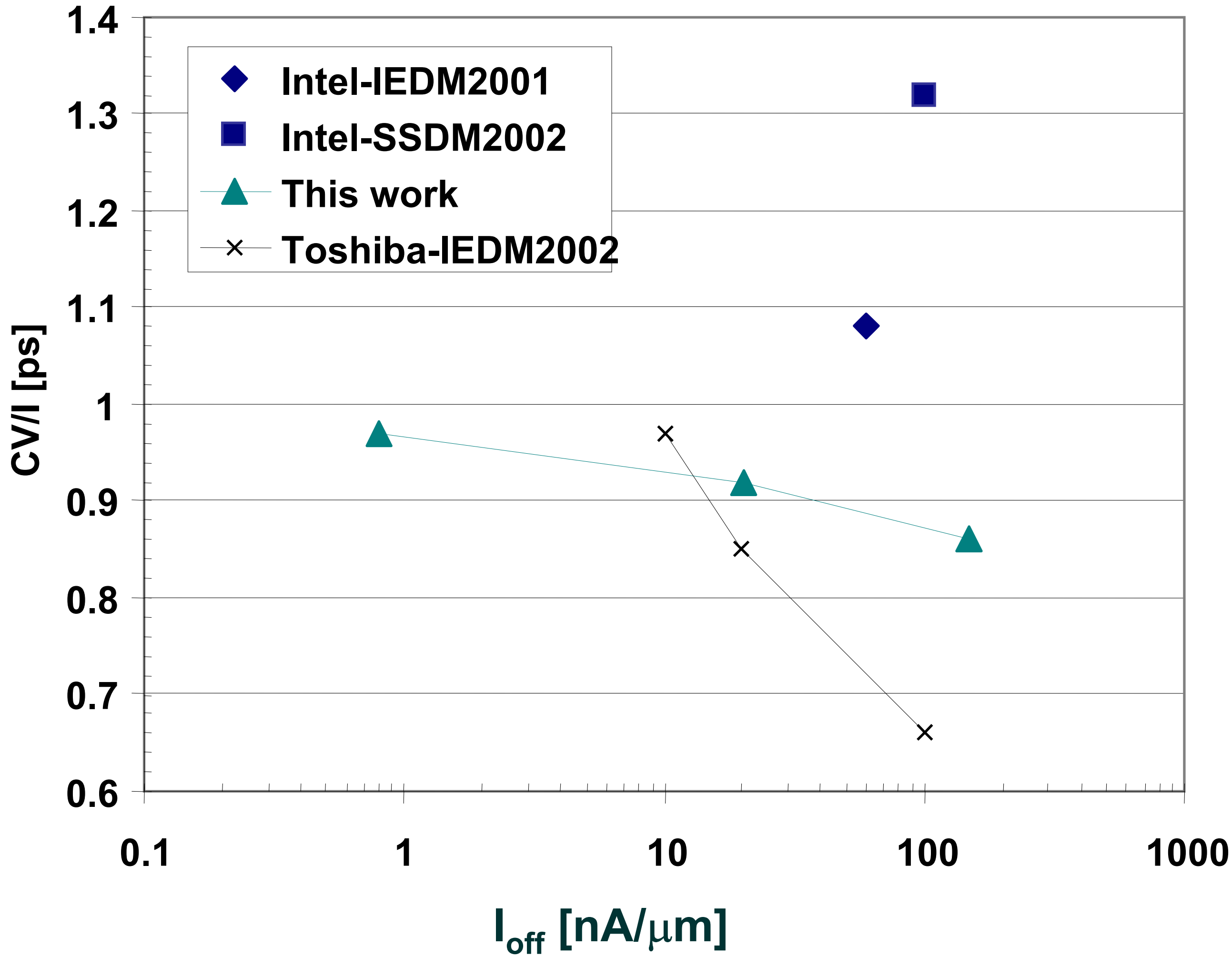
This Work

IBM, IEDM 2002

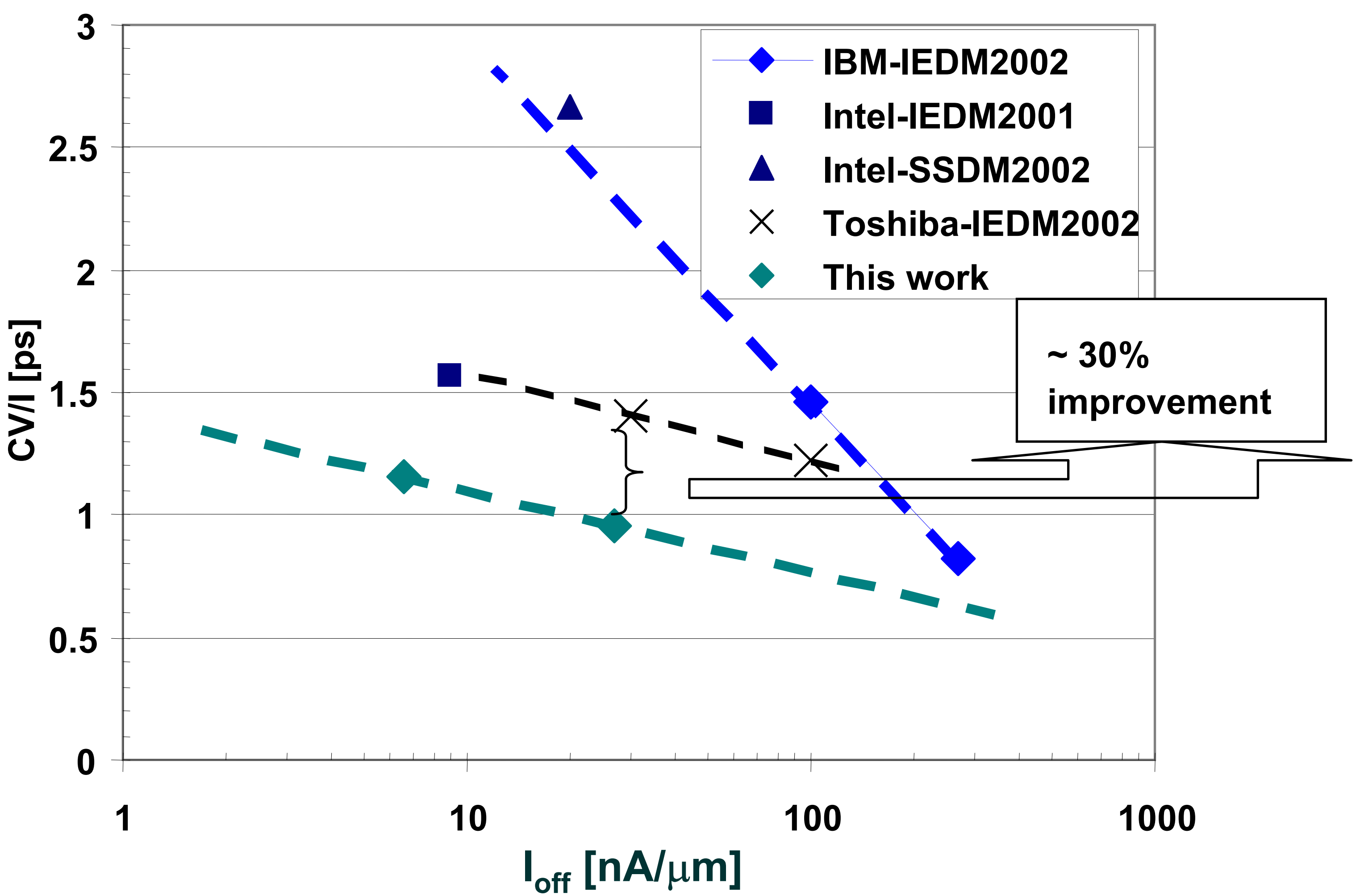
Tri-Gate – Intel

DST- Intel

NMOS CV/I Comparison



PMOS CV/I Comparison



How to Improve Performance?

- Threshold voltage can be lowered by engineering gate work function.
- Stress study of various silicides is needed to maximize strain in the channel.
- Extension and source/drain implants need to be optimized.

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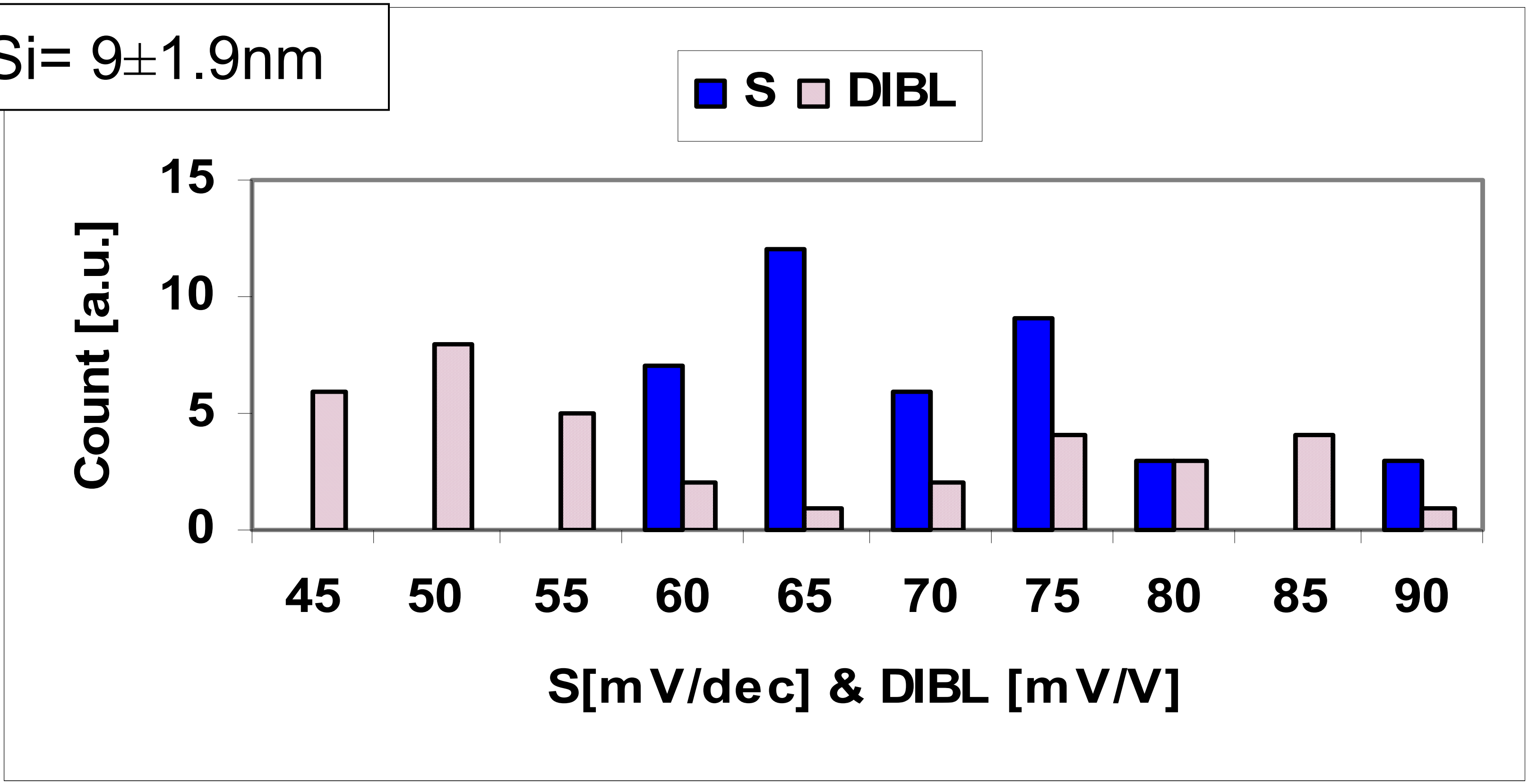
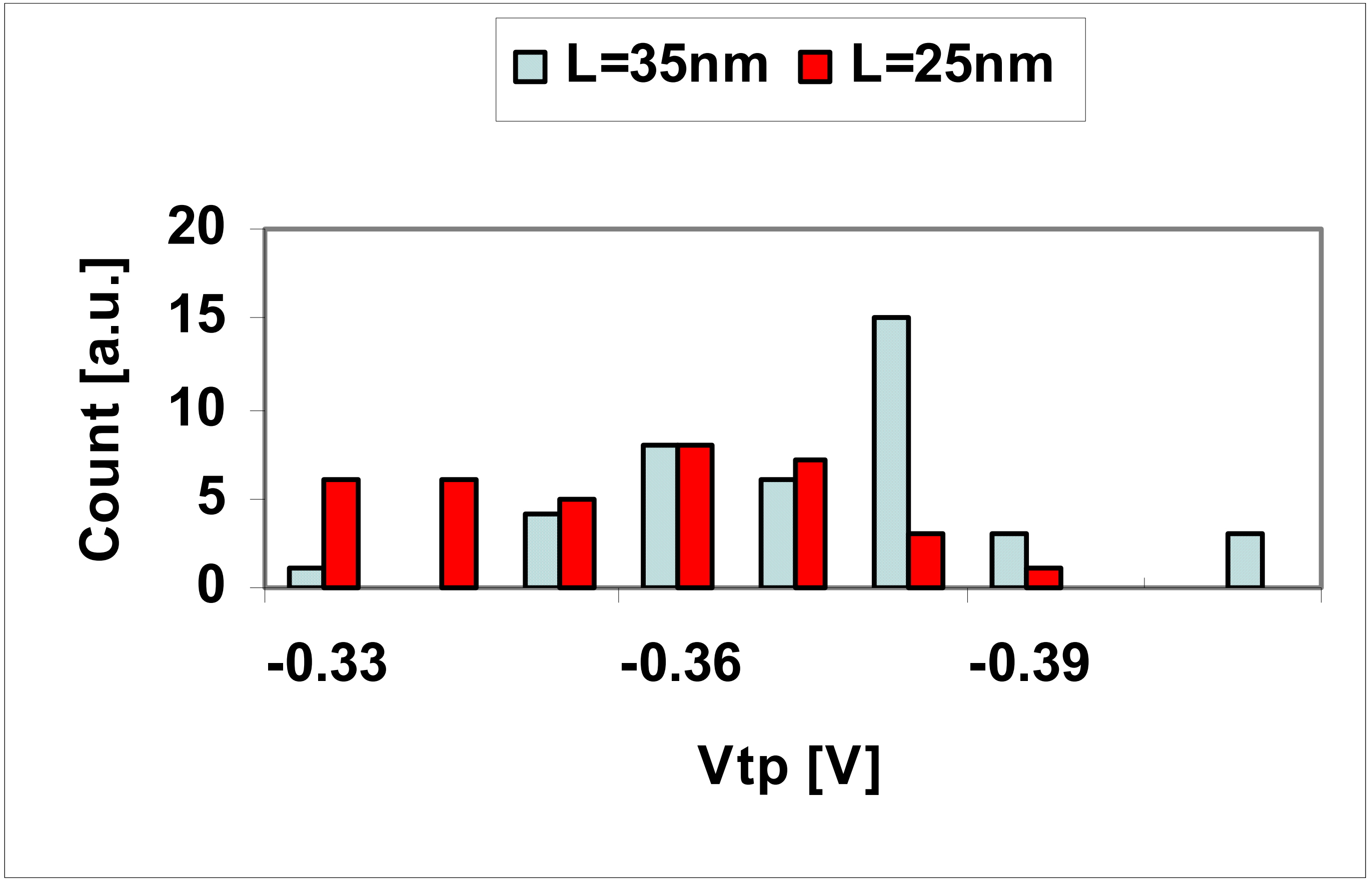
Silicon Thickness Control and Device Parameters

Si= 9±1.9nm



- Silicon channel variations cause bi-modal distributions of the subthreshold slope and DIBL.

PMOS Vt Distribution



- Distribution comparable to Vt distributions due to LER.

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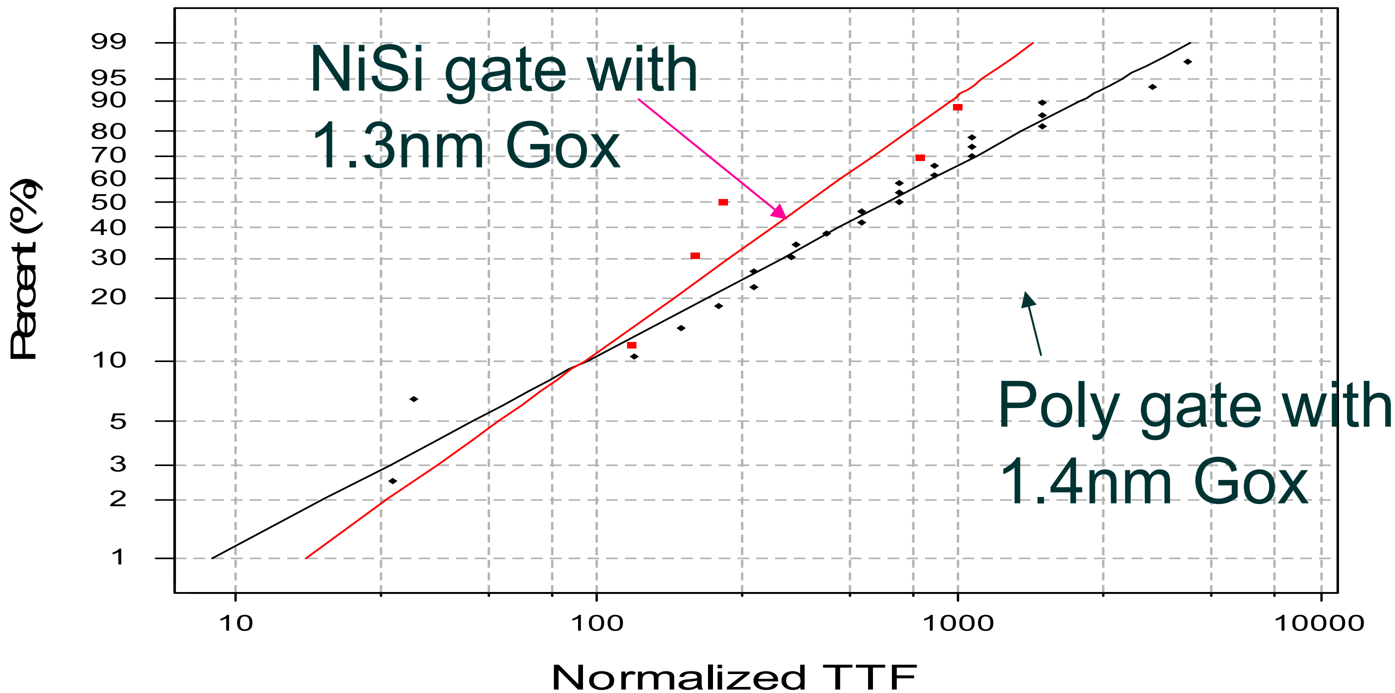
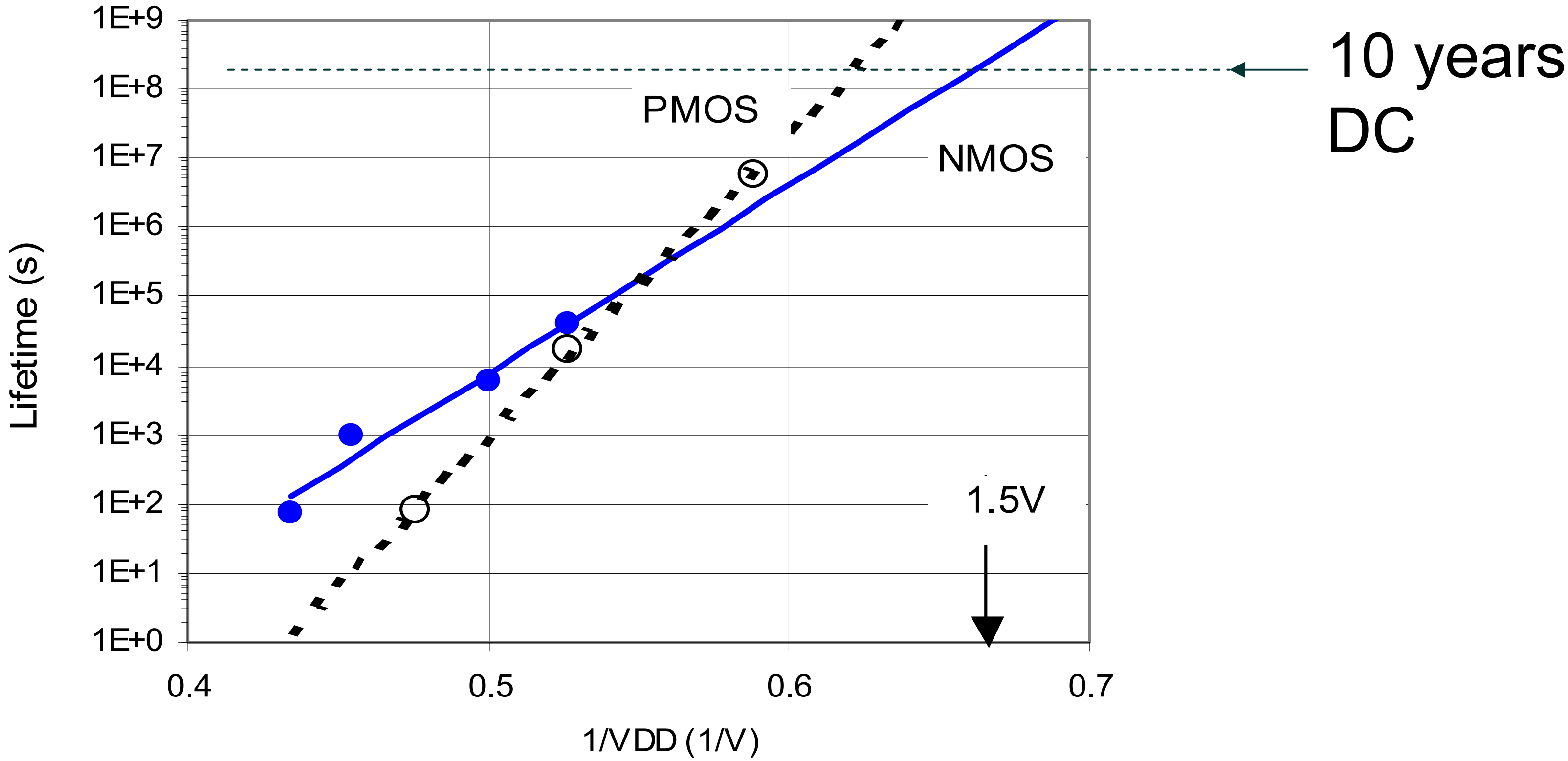
Gate Dielectric Reliability: TDDB



- TDDB for NiSi gate is comparable to the one for Polysilicon gate.

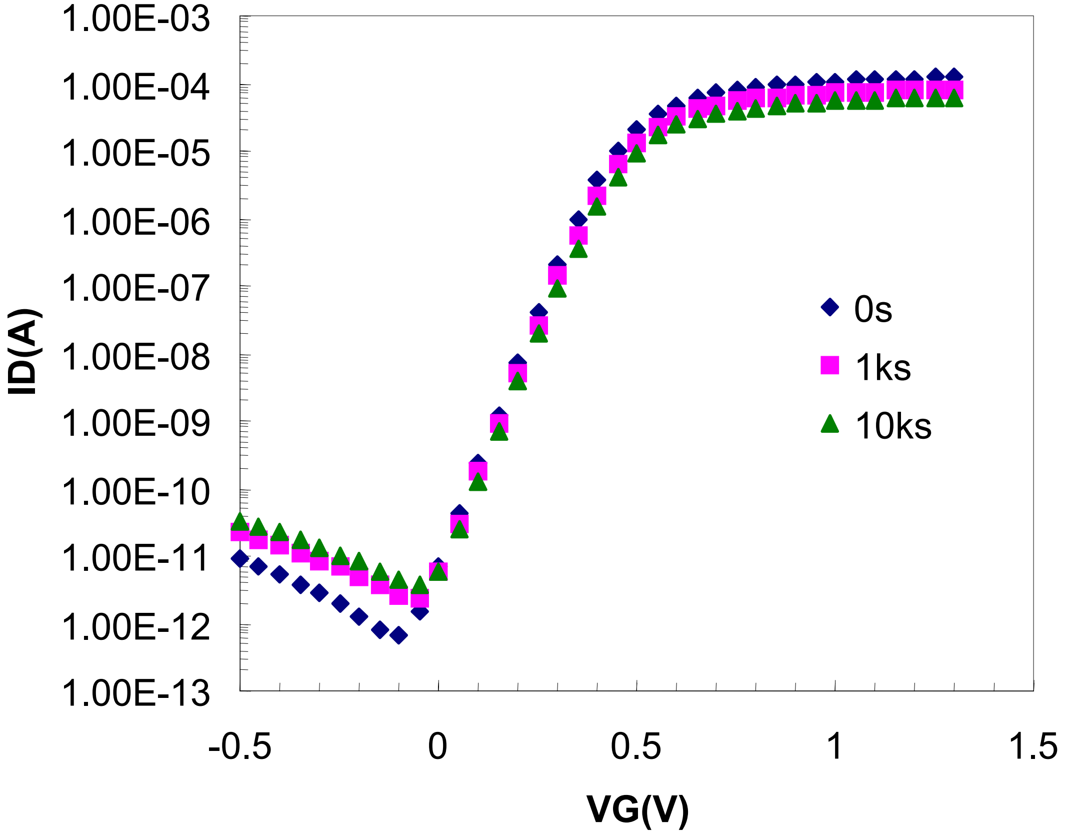
Hot Carrier Reliability for NiSi Gate FDSOI



- 25nm FDSOI devices achieve DC hot carrier lifetime for Vdd<1.5V.

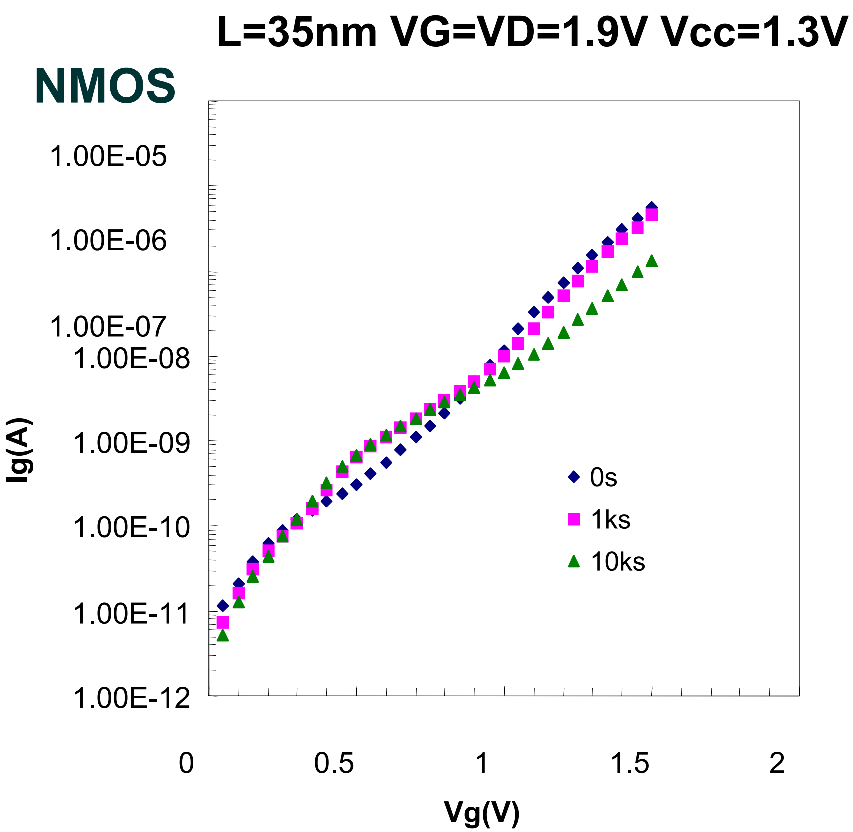
Hot Carrier Stress Degrades NMOS Subthreshold Slope

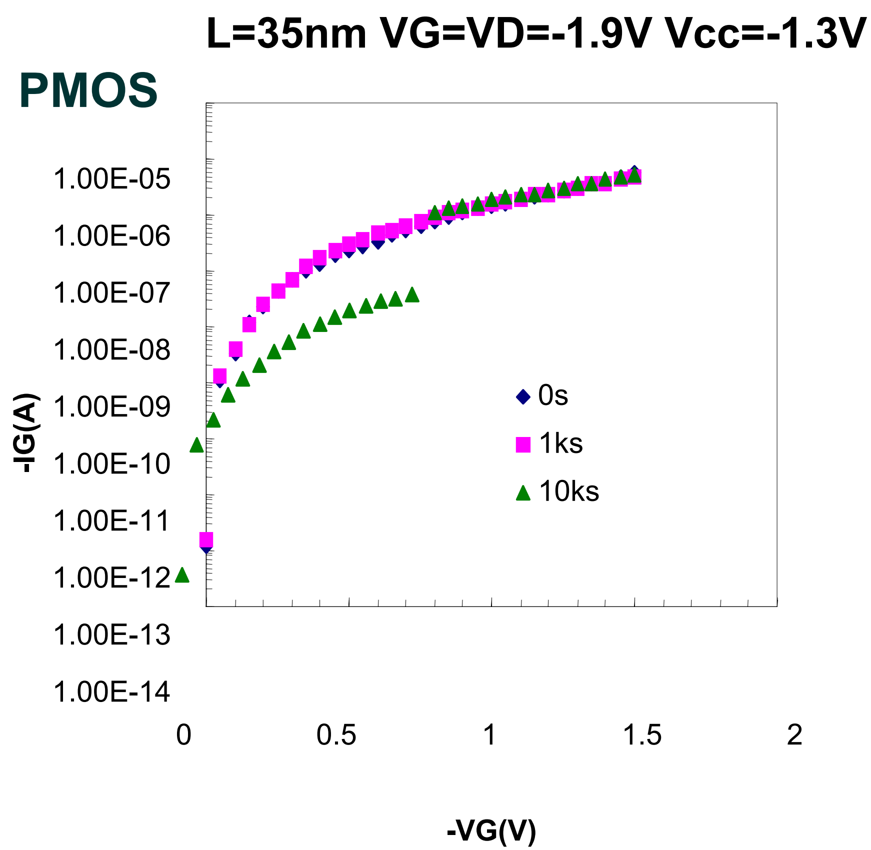
25nm NMOS $V_g=V_d=1.9V$



- Sinitial= 70mV/dec
- Sstress= 80mV/dec.

Hot Carrier Stress and Gate Leakage



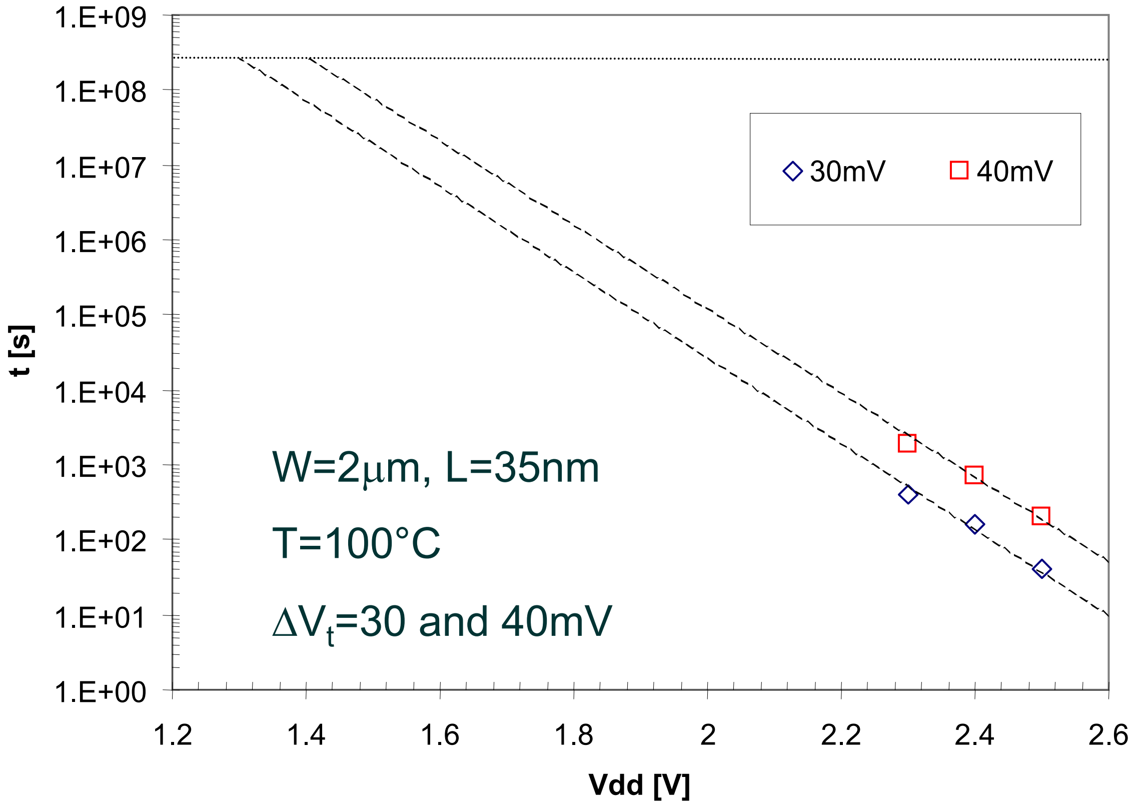


- PMOS Ig doesn't change with hot carrier stress. NMOS Ig changes depending on the position of trapped states in nitride layer.

NBTI

ΔV_t=30mV has 10 year lifetime at V_{dd}=1.3V

ΔV_t=40mV has 10 year lifetime at V_{dd}=1.44V



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Conclusions

- We demonstrate NiSi gate FDSOI devices with CET 1.6nm for 1.3nm physical nitrided oxide thickness.
- We demonstrate very high mobility even for very thin Silicon channel.
- We see feasible manufacturability.
- Gate dielectric has good reliability and excellent hot carrier and NBTI immunity.
- We report the highest PMOS performance, while NMOS is degraded due to strained channel.

Acknowledgments

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