PCnet Family Board Design and Layout Recommendations

Application Note

INTRODUCTION

The devices in the PCnet family implement the functions of an Ethernet node controller, a serial interface adapter, a 10BASE-T transceiver, and an industry standard bus interface (ISA in the PCnet-ISA, PCnet-ISA$^+$, and PCnet-ISA II; VESA VL and 486 local buses in the PCnet-32; and PCI in the PCnet-PCI and PCnet-PCI II), leaving the designer relatively few tasks to complete an Ethernet design. However, the mixed analog/digital circuitry present in each of the devices, including a high speed Phase-Lock Loop (PLL), make it important for the board designer to follow common low noise board design practices. The design hints presented in this chapter address these board design practices.

The PCnet-based Ethernet board designer must be concerned with two issues: 1) reducing noise coupling into the PCnet signals, power and ground to allow a fully functional design, and 2) reducing radiated noise to comply with FCC, VDE, and/or other regulatory specifications. Both of these issues can be addressed by the same low-noise design techniques. Any noise that is coupled to the PCnet-ISA circuitry has the potential to 1) disrupt the device's operation and 2) be transmitted onto the network with the network media acting as an antenna, radiating high-frequency noise that may violate regulatory specifications. Therefore, the purpose of most layout precautions is to isolate the Ethernet circuitry from noise.

Unless noted otherwise, all of the recommendations presented in this application note apply to both motherboards and adapter cards.

SIGNAL ROUTING AND DEVICE PLACEMENT

Signal traces should be kept as short as possible in all PCnet designs. By keeping signal traces as short as possible, the signals have less chance to pick up high frequency noise from other signals, including power and ground planes. In addition, short signal traces reduce the capacitive loading caused by the signal trace. Pin locations on all PCnet devices have been chosen to allow for minimum length signal routing. By carefully choosing the device orientation and placement in a design, the routing job can be made much easier. For example, the PCnet-ISA adapter card design shown in Figure 1 clearly shows the benefit of orienting the device as shown.

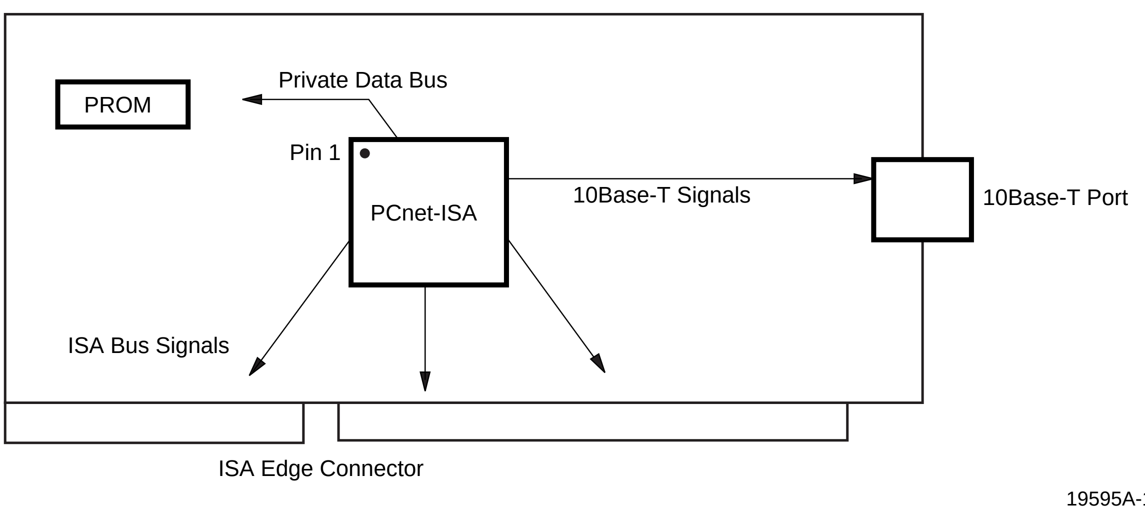

Figure 1. Layout of Components on the PCnet-ISA Adapter Card

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As mentioned earlier, all of the PCnet family devices contain a PLL. PLL circuits are inherently sensitive to noise. For this reason, it is strongly recommended that signals not be routed beneath the PCnet device in the section of the device where the PLL resides. This section shall be called the “analog corner” and is located in the same area of the die for all devices in the PCnet family. The “analog corner” is located in the upper right hand corner of all PCnet devices when the device is viewed with pin 1 oriented as shown in Figure 1. By avoiding signal routing directly beneath this corner of the device, noise coupling into the PLL is minimized.

Motherboard-Specific Recommendations: In motherboard implementations, the area of Ethernet circuitry on the motherboard should be kept free of interference from unrelated signal traces. Thus, the area surrounding the Ethernet components should be considered off limits when routing other signals. To minimize the burden this places on the rest of the motherboard layout, Ethernet circuitry should be placed together at the perimeter of the board, near the media connector. In addition to signal routes, noisy devices themselves should be kept away from the PCnet device and its crystal when placing devices on the motherboard. Obvious sources of noise such as the CPU, clock, cache controller, VGA controller, and numeric coprocessor should be placed some distance away from the Ethernet components.

POWER AND GROUND CONNECTION GUIDELINES

Providing noise-free power and ground connections to the device is of critical importance in all PCnet family designs. Without clean power and ground connections, a design may suffer from high bit error rates or may not function at all. Hence, it is highly recommended that the guidelines presented here are followed to ensure a reliable design.

Dedicated Power and Ground Planes: Although it is not required, using a board with four or more layers with dedicated power and ground planes can make building a reliable PCnet board an easier task. Dedicated power and ground planes are beneficial to a design in many ways: 1) ground bounce is minimized due to reduced inductance in the power and ground paths, 2) radiated emissions and susceptibility to EMI is reduced by the minimized circuit loops, 3) characteristic impedance of signal traces adjacent to power and ground planes is more controlled than those that are not adjacent to a power or ground plane, and 4) crosstalk between signal traces is reduced by the presence of the power and ground planes.

Decoupling/Bypass Capacitors: Adequate decoupling of the power and ground pins and planes is required by all PCnet designs. This includes both low-frequency bulk capacitors and high frequency capacitors. It is recommended that at least one low-frequency bulk (e.g., 22µF) decoupling capacitor be used in the area of the PCnet device. The bulk capacitor(s) should be connected directly to the power and ground planes. In addition, at least 8 high frequency decoupling capacitors (e.g., 0.1 µF multilayer X7R or NPO ceramic capacitors) should be used around the periphery of the PCnet device to prevent power and ground bounce from affecting device operation. Don’t use Z5U dielectric capacitors for high frequency decoupling. The inductance of Z5U capacitors is too high at high frequencies. To reduce the inductance between the power and ground pins and the capacitors, the pins should be connected directly to the capacitors, rather than through the planes to the capacitors. The suggested connection scheme for the capacitors is shown in Figure 2. Note also that the traces connecting these pins to the capacitors should be as wide as possible to reduce inductance (15 mils is desirable).

The most critical pins in the layout of a PCnet design are the 4 analog power and 2 analog ground pins, AVDD[1-4] and AVSS[1-2], respectively. All of these pins are located in one corner of the device, the “analog corner.” All devices in the PCnet family use the same naming convention for the analog power and ground pins. That is, pins with the same name on each of the different devices provide power or ground to the exact same part of the analog circuitry in each of the devices.

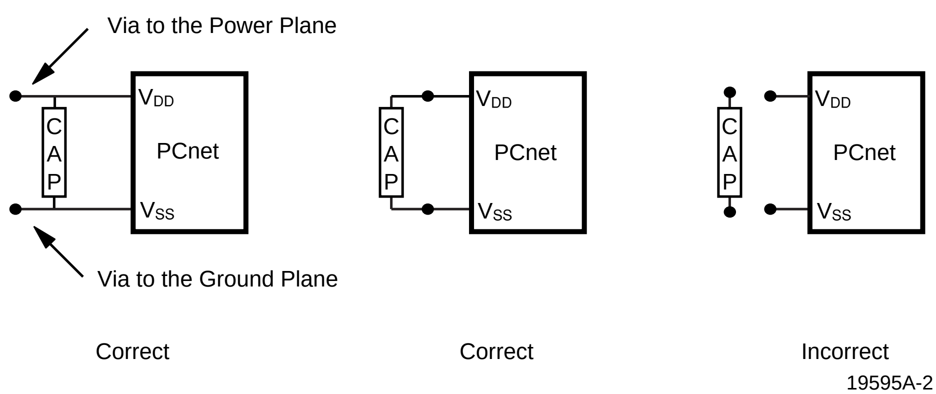

Figure 2. Decoupling Capacitor Connection

Specific functions and layout requirements of the analog power and ground pins are listed below.

AVSS1 and AVDD3: These pins provide the power and ground for the Twisted Pair and AUI drivers. In addition AVSS1 serves as the ground for the logic interfaces in the 20 MHz Crystal Oscillator. Hence, these pins can be very noisy. A dedicated 0.1 µF capacitor between these pins is recommended.

AVSS2 and AVDD2: These pins are the most critical pins on the PCnet devices because they provide the power and ground for the phase-lock loop (PLL) portion of the chip. The voltage-controlled oscillator (VCO) portion of the PLL is sensitive to noise in the 60-200 kHz range. To prevent noise in this frequency range from disrupting the VCO, it is strongly recommended that the low-pass filter shown in Figure 3 be implemented on these pins. Tests using this filter have shown significantly increased noise immunity and reduced Bit Error Rate statistics in designs using PCnet Family devices.

The PLL is sensitive to noise caused by DRAM refresh. Since the refresh current, and therefore, noise, is a function of the amount of memory installed on a board, it is important to evaluate the effectiveness of the low-pass filter with the maximum amount of memory installed.

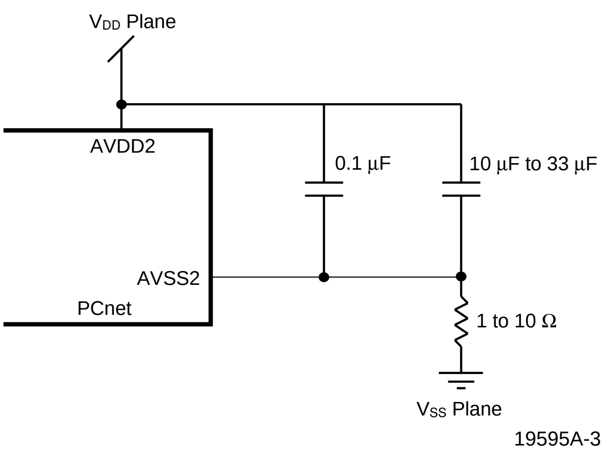

Figure 3. Low-Pass Filter Design

To determine the value for the resistor and capacitor, the formula is:

$$R * C \geq 88$$

Where R is in Ohms and C is in microfarads. Some possible combinations are given in Table 1. To minimize the voltage drop across the resistor, the R value should not be more than 10 Ω.

Table 1. Combinations of R and C for the Low-Pass Filter

R (Ω)	C (µF)
2.7	33
4.3	22
6.8	15
10	10

AVSS2 and AVDD2/AVDD4: These pins provide power and ground for the AUI and twisted pair receive circuitry. In addition, as mentioned earlier, AVSS2 and AVDD2 provide power and ground for the phase-lock loop portion of the chip. Except for the filter circuit already mentioned, no specific decoupling is necessary on these pins.

AVDD1: AVDD1 provides power for the control and interface logic in the PLL. Ground for this logic is provided by digital ground pins. No specific decoupling is necessary on this pin.

Special Note for Adapter Cards: In adapter card designs, it is important to utilize all available power and ground pins available on the bus edge connector. In addition, the connection from the bus edge connector to the power or ground plane should be made through more than one via and with wide traces (15 mils desirable) wherever possible. Following these recommendations results in minimal inductance in the power and ground paths. By minimizing this inductance, ground bounce is minimized.

Crystal Oscillator Guidelines

In order to meet IEEE specifications, the clock source used for the network data rate in an Ethernet design must be tightly controlled. Devices in the PCnet family include on-chip oscillator circuitry allowing the use of a 20 MHz external crystal attached to the XTAL1 and XTAL2 pins. Alternatively, a CMOS level source can be used to drive the XTAL1 pin, in which case the XTAL2 pin should be left unconnected.

When using a crystal, a 20 MHz ± 50 ppm/0.005%, ESR< 35 Ω parallel resonant, AT-cut crystal is required. When using an external oscillator, a 20 MHz ± 100 ppm/0.01% oscillator is required. The tighter tolerance requirement placed on the crystal allows for variance introduced by the external discrete devices required by crystals. This includes component tolerances and board parasitics.

When selecting a crystal for use in a PCnet design, the first and most important criteria is that the crystal meets the 50 ppm requirement at 20 MHz. If the crystal does not meet this requirement, the design will not meet IEEE specifications. Crystals are only guaranteed to meet their accuracy specifications when they are used with the effective load capacitance specified by the crystal manufacturer.

Figure 4 shows the connection of a crystal in the parallel resonant oscillator configuration that is used for PCnet designs. The total load capacitance at each pin of the crystal includes the discrete compensating capacitor (C_C) plus the parasitic capacitance of the board traces and the device pins (C_P). The effective load capacitance seen by the crystal is the series combination of the capacitances on its two pins. Therefore, the load capacitance seen by the crystal (C_L) is given by the formula:

$$C_L = (C_C + C_P) / 2$$

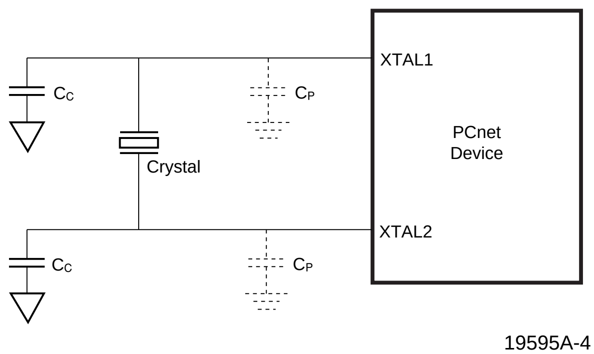

Figure 4. Crystal Connections

For load capacitances less than about 50 pF the effect of parasitic capacitance becomes quite important. When smaller load capacitances are used, it is particularly important to measure the resulting oscillator frequency to insure that parasitics have been compensated for correctly.

When measuring the oscillator frequency, you must make sure that the capacitance of the probe does not affect the measurement. One way to do this is to transmit a very long frame consisting of all ones and measure the frequency at the DO± pins. You can send an arbitrarily long frame by setting up a transmit descriptor ring consisting of a single descriptor that points to a buffer that contains all ones. Set the STP bit of the descriptor to one and the ENP bit to zero. Then put the computer into a tight loop that does nothing but set the OWN bit of the descriptor over and over.

For FCC considerations the case of the crystal should be connected to the ground plane and no signal should be routed under the crystal. Also placing a grounded cross hatched area under the crystal helps to reduce emissions and prevents other signals from being routed through that area.

AUI INTERFACE LAYOUT GUIDELINES

All devices in the PCnet family provide an Attachment Unit Interface (AUI) port for connection to any media type through use of a Medium Attachment Unit (MAU). The AUI interface is provided by the three differential pair pins, DI±, DO±, and CI±. This interface can be used to provide a specific on-board media attachment (e.g., 10BASE2, FOIRL, etc.) or the interface can be brought off-board, providing an AUI port through a standard 15-pin AUI connector (DB15).

To provide an AUI port, all that is needed is termination resistors on the DI± and CI± pairs, AUI isolation transformers, and a 15-pin AUI connector. Figure 5 shows the recommended schematic. To prevent unwanted noise from coupling into the AUI signals, these signals should be routed carefully. Each differential pair should be routed as a pair. AUI signals should be kept away from noisy devices. The 0.01 µF to 0.1 µF capacitors to ground in the middle of the terminators reduce EMI emissions.

The AUI isolation transformer is required to protect the CMOS circuits from high voltages that could be applied to the DB15 AUI connector.

If the AUI port is not used, the AUI pins can be left unconnected.

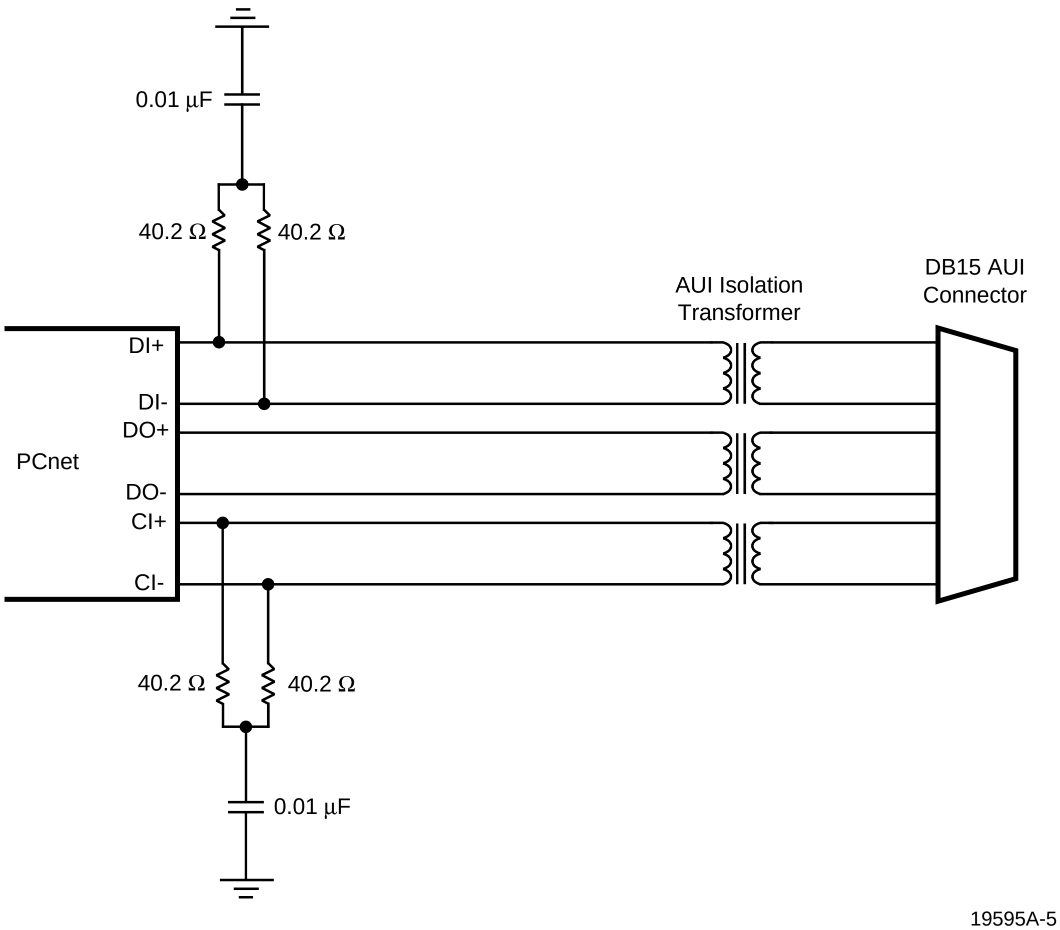

Figure 5. AUI Port Design

10BASE2 INTERFACE LAYOUT GUIDELINES

The AUI port described above can be used to add a 10BASE2 port to any PCnet design by adding 10BASE2 MAU circuitry to the design. Addition of the 10BASE2 port requires the termination resistors shown on the DI± and CI± pairs shown above, the AUI isolation transformers, a 10BASE2 transceiver chip such as an Am7996, a DC-DC converter, a BNC connector, and the miscellaneous discrete components required by the transceiver. Refer to the Am7996 data sheet in the Ethernet/IEEE 802.3 Family data book (AMD PID# 14287C) for a schematic example of a 10BASE2 MAU.

Note that the AUI signal pairs need termination resistors near the line receiver circuits. For the DO± circuit the receiver end of the line is in the transceiver. Therefore, if an onboard transceiver is connected to the AUI interface, termination resistors must be included in the DO± circuit on the transceiver side of the transformer, near the transceiver.

Some transceivers have a pin connection option that disables the Signal Quality Error (SQE) test signal that normally occurs after each transmission. The SQE signal must always be enabled except for transceivers built into repeaters (hubs).

The layout of the 10BASE2 MAU circuitry must be handled carefully to ensure signal and link integrity and to minimize unwanted emissions radiating from the coaxial cable. Receive signal levels from the network can be very low, requiring low noise design techniques at the network interface. To reduce parasitics and also to meet isolation requirements, there should be no power or ground plane present beneath all of the 10BASE2 MAU circuitry. The transceiver should be soldered directly to the circuit board—it should not be in a socket. Refer to layout recommendations in the Am7996 data sheet in the *Ethernet/IEEE 802.3 Family* data book (AMD PID# 14287C).

10BASE-T Interface Layout Guidelines

The only components required to implement a 10BASE-T interface with a PCnet device are the transmit and receive termination resistors, a 10BASE-T filter/transformer module, an RJ45 connector, LEDs, and resistors. The pin layouts of the PCnet devices have been optimized to minimize signal routing cross-over requirements when used with most common filter/transformer pinouts.

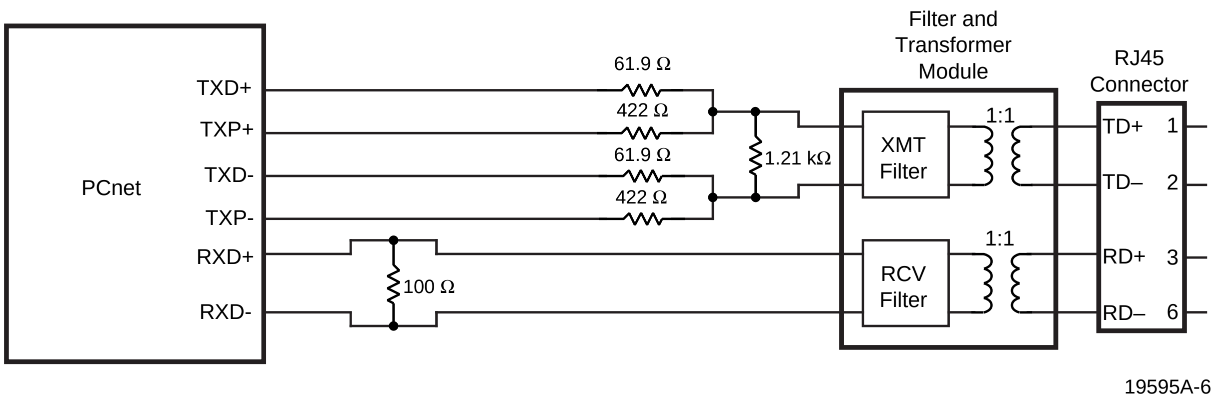

Figure 6. 10BASE-T Layout

The layout of the filter/transformer module and the RJ45 connector must be handled carefully to ensure signal and link integrity and to minimize unwanted emissions radiating from the twisted pair cable. Receive signal levels from the network can be very low, requiring low noise design techniques at the network interface. To prevent power and ground noise from coupling into these components, there should be no power or ground plane present beneath the filter/transformer module and RJ45 connector. Without the power and ground planes beneath the transformer, noise coupling between the primary and secondary sides of the transformer and between the adjacent coils in the transformer is also minimized.

On the other hand, some designers have had good results using frame (chassis) ground under the secondary side of the transformer and the RJ45 connector. AMD has not tested this technique.

The low signal levels on the 10BASE-T RXD± lines make it necessary to pay special attention to the routing of these signal traces. Specifically, to prevent power and ground noise from coupling into these traces, if possible, there should be no power or ground plane present beneath the RXD± signal traces. These signals should all be routed as pairs. In addition, to prevent any coupling into the RXD± signals, the TXD±, TXP± and any other signals on the board should not be routed close to the RXD± traces.

Choosing a filter is an important step toward meeting FCC emission standards. Performance varies between manufacturers. Evaluate your choice carefully.

Common-mode noise is the primary source of radiated energy from the 10BASE-T interface. The use of common-mode chokes, either as discrete components or built into the filter/transformer module, helps to reduce emissions. Make sure that the choke is large enough that it does not saturate.

PCNET-ISA/ISA$^+$/ISA II SPECIFIC LAYOUT GUIDELINES

In addition to the general layout recommendations already mentioned, designs using the PCnet-ISA, PCnet-ISA$^+$, and PCnet-ISA II devices must comply with the board design specifications for the ISA bus (see IEEE P996 Specification or the book, AT Bus Design by Edward Solari). The ISA bus specifies a maximum stub length of 2.5 inches and a maximum capacitive load of 15 pF on each signal line. The PCnet-ISA, PCnet-ISA$^+$, and PCnet-ISA II devices have a maximum bus signal pin capacitance of 10 pF. Hence, with typical printed circuit board trace dimensions and materials, a board that complies with the 2.5 inch stub length restriction should meet the 15 pF load specification when using the PCnet-ISA, PCnet-ISA$^+$, or PCnet-ISA II. The estimated load capacitance presented by the board can be calculated using the equations presented in the Estimated Printed Circuit Board Parameters section of this application note.

PCnet-32 SPECIFIC LAYOUT GUIDELINES

In addition to the general layout recommendations already mentioned, designs using the PCnet-32 device must comply with the VESA VL-bus specification, when the device is used in a VL-bus application. The VESA VL-bus specification places the following requirements on expansion boards:

- The maximum trace length is limited to 2 inches. If the trace branches on the add-in board then the total length of all branches is limited to 2 inches.
- Each signal coming from the VL-bus can be loaded by 25 pF on the add-in card.
- “Signal Impedance” should equal 50 Ω or less on each trace, where Signal Impedance is defined as:

$$Z_{signal} = \frac{Z_0}{\sqrt{\left(\frac{C_0}{C_{component}}\right)+1}}$$

where

Z_{signal}	=	signal loaded trace impedance
Z_0	=	the impedance of the board trace
C_0	=	the capacitance of the board trace
$C_{component}$	=	the load capacitance from components and connectors

The requirements mentioned above can be easily met by a design using the PCnet-32 because the device’s pin capacitance is specified at 10 pF maximum and the pinout of the device matches the VL-bus edge connector pin arrangement, allowing easy routing for short trace lengths. For equations and sample calculations of the printed circuit board parameters, see the Estimated Printed Circuit Board Parameters section of this application note.

Refer to the VESA VL-bus specification for additional details on these recommendations.

PCnet-PCI and PCnet-PCI II SPECIFIC LAYOUT GUIDELINES

In addition to the general layout recommendations already mentioned, designs using the PCnet-PCI and PCnet-PCI II devices must comply with the PCI specifications and the PCI compliance checklist. The PCI specification places the following requirements on expansion boards:

- The maximum trace length is limited to 1.5 inches.
- The CLK signal trace length must be 2.5 ± 0.1 inches and must be routed to only one load.
- The unloaded characteristic impedance (Z_0) of the printed circuit board traces shall be in the 60-100 Ω range. The trace velocity shall be between 150 and 190 ps/inch.
- Only one device load, with a maximum of 10 pF per pin (or 8 pF for IDSEL and 12 pF for CLK), is allowed on each pin per expansion card. NOTE: Multiple PCI devices may be placed on one expansion card only behind a PCI-PCI bridge.
- Pullup resistors or other discrete devices may not be connected to the PCI signals, unless they are placed behind a PCI-PCI bridge.
- Trace length from an edge connector power or ground pad to the expansion card V_{CC} or GND plane, respectively, is limited to 0.25 inches, assuming a 20 mil trace width.
- Power supply decoupling must average at least 0.01 pF (high speed) per V_{CC} pin.
- Trace length from pin pad to capacitor pad shall be no greater than 0.25 inches, using a trace width of at least 20 mils.
- The $\overline{\text{PRSNT}}$[1:2] pins must be connected to show correct power consumption.
- JTAG continuity must be maintained. TDI must be connected to TDO at the connector if JTAG is not used.
- All +3.3 V, unused +5 V, and +V I/O pins must be decoupled adequately.
- All GND fingers must be provided and bussed together.
- All RESERVED fingers must be no-connect and must not be bussed together.

The requirements mentioned above can be met by a design using the PCnet-PCI because the device’s pin capacitance is specified at 10 pF maximum and the pinout of the device follows the recommended pinout given in the PCI specification, allowing the trace length requirement to be met.

Refer to the PCI specification for complete recommendations on signal routing and power supply decoupling for both motherboard and adapter card designs.

ESTIMATING PRINTED CIRCUIT BOARD PARAMETERS

Characteristic impedance, trace velocity, and trace capacitance for printed circuit board traces can be estimated given the trace dimensions. This section will provide equations and examples for performing these calculations.

Note that software tools are available to perform these calculations automatically. These tools also calculate the effects of distributed loads and discontinuities caused by feedthroughs. Because of the tight tolerances of PCI designs, software aids are almost a necessity for designing PCI systems.

The Microstrip model can be used for a typical 4-layer board with signal traces on the outer layers. The microstrip model consists of a metal trace over an AC ground plane, with a dielectric in between. The model and its associated equations are given below.

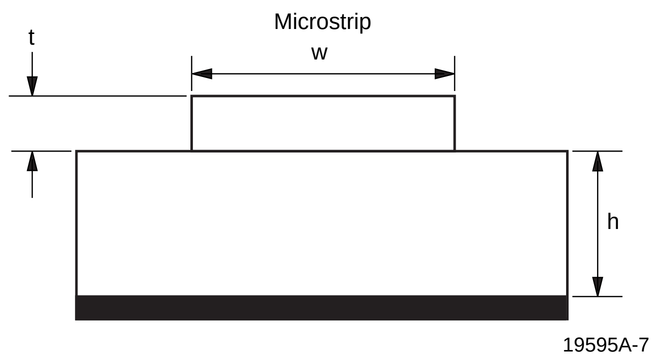

Figure 7. Microstrip Model

$$Z_0 = \frac{87}{\sqrt{(\varepsilon_R = 1.41)}} \text{ In } \frac{5.98\ h}{0.8\ w + t}\ \Omega$$

$$\tau = 1.017 \sqrt{0.457\ \varepsilon_R + 0.67}\ ns/ft$$

$$C_0 = 100\ \frac{\tau}{Z_0}\ pF/ft$$

where

Z_0	=	characteristic impedance of the board trace
τ	=	trace velocity
C_0	=	trace capacitance
ε_R	=	dielectric constant of the board material (e.g., ε_R = 5 for FR-4 material and ε_R = 4.8 for G-10)
t, w, and h	=	board dimensions as defined in Figure 7 above

From the above equations, typical values for a 4-layer board can be calculated. A few of these typical values are given below.

If h = 0.020 inch, t = 0.0015 inch, and ε_R = 4.7, then τ = 1.71 ns/ft and

for w = 0.008 inch (8 mil traces):	Z_0 = 129 Ω and C_0 = 3 pF/ft
for w = 0.010 inch (10 mil traces):	Z_0 = 89 Ω and C_0 = 19 pF/ft
for w = 0.020 inch (20 mil traces):	Z_0 = 67 Ω and C_0 = 26.5 pF/ft

The Stripline model can be used in multilayer boards in which a signal trace is between two AC ground planes.

The model and equations for the Stripline model are given below.

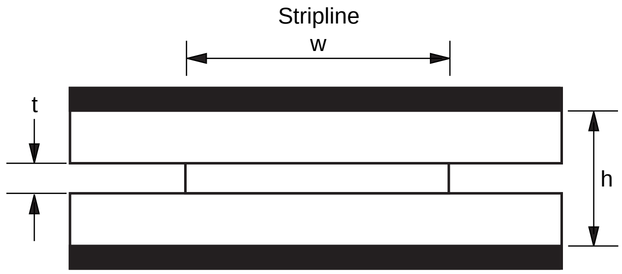

Figure 8. Stripline Model

$$Z_0 = \frac{60}{\sqrt{\varepsilon_R}} \ \mathrm{In} \ \frac{4\,h}{0.67\ \pi w \left(0.8 + \frac{t}{w}\right)} \ \Omega$$

$$\tau = 1.017 \sqrt{\varepsilon_R} \ ns/ft$$

$$C_0 = 1000 \ \frac{\tau}{Z_0} \ pF/ft$$

where

Z_0	=	characteristic impedance of the board trace
τ	=	trace velocity
C_0	=	trace capacitance
ε_R	=	dielectric constant of the board material (e.g., ε_R = 5 for FR-4 material and ε_R = 4.8 for G-10)
t, w, and h	=	board dimensions as defined in Figure 8 above

PCnet FAMILY ETHERNET AND SCSI BOARD LAYOUT CHECKLIST

This checklist covers all the key items which must be reviewed in a design using AMD PCnet™ or PCSCSI™ devices. For more information regarding the SCSI component board layout, please refer to Appendix C and E of the *PCnet-SCSI* data sheet (PID# 18681B) or the *PCSCSI II Technical Manual* (PID# 19113A).

A. PCnet Family General

A.1 Is the device oriented the correct way?

By carefully choosing the device orientation and placement in a design, signals can be kept short and routing can be optimized. Place the device as close as possible to the media connector, without violating the layout rules for the bus interface.

A.2 On motherboards, are noisy devices distant from PCnet device and its crystal?

Sources of noise such as the CPU, clock, cache controller, VGA controller, numeric coprocessor, and bus lines (high drive signals) should be placed some distance away from the Ethernet components.

A.3 Are all bus interface requirements for motherboards or expansion boards followed?

All designs using the PCnet family or PCSCSI devices should comply with the relevant and latest specification for the bus interface design and layout. (e.g., all PCI designs should follow the guidelines in the PCI Specification and the PCI Compliance Checklist.)

A.4 Are power and ground adequately decoupled?

Adequate decoupling of the power and ground pins and planes is required by all PCnet designs. This includes both low-frequency bulk capacitors and high frequency capacitors. It is recommended that at least one low-frequency bulk (e.g., 22 µF) decoupling capacitor be placed close to the PCnet device. The bulk capacitor(s) should be connected directly to the power and ground planes. In addition, at least 8 high frequency decoupling capacitors (e.g., 0.1 µF) should be used around the periphery of the PCnet device to prevent power and ground bounce from affecting device operation. Multilayer ceramic capacitors with a good quality dielectric such as NPO or X7R (avoid using Z5U) are recommended for the high frequency capacitors. To reduce the inductance between the power and ground pins and the capacitors, the pins should be connected directly to the capacitors rather than through the supply planes to the capacitors. Use traces of at least 15 mils width.

A.5 Is there a dedicated capacitor for the AVSS1 and AVDD3 pins?

The AVSS1 and AVDD3 pins are the supply pins for the transmit output drivers and should have a high frequency capacitor dedicated to them.

A.6 Are ferrite beads avoided for power supply decoupling?

Don't use ferrite beads for PCnet power supply decoupling. Because the supply current requirement for the PCnet device is so dynamic (it is a CMOS device) ferrite beads are not recommended for power supply decoupling.

A.7 Is the $\overline{\text{SLEEP}}$ pin connected?

The $\overline{\text{SLEEP}}$ pin should not be left floating. If the sleep function is not used, the $\overline{\text{SLEEP}}$ pin must be externally pulled up via a 2.2 k Ω or smaller resistor.

A.8 Are signals connected to RESERVED pins?

Do not connect the RESERVED pins to any signal.

B. Ethernet Practices

General:

B.1 Have signals been routed to avoid the analog corner of the PCnet device?

By avoiding routing non-network signals (address, data, control, etc.) directly beneath the analog corner of the PCnet (the corner near the XTAL1 pin), noise coupling into the PLL is minimized.

B.2 Is a low-pass filter for the Ethernet phase-lock loop (PLL) used?

To reduce bit error rates, a low-pass filter on the AVSS2 and AVDD2 pins is highly recommended (do not use ferrite beads). A good quality tantalum capacitor should be used. The RC value should be $\geq 88 * 10^{-6}$ sec.

When Using a Crystal for the Ethernet Clock:

B.3 Is the crystal of the correct frequency and tolerance?

A 20 MHz ± 50 ppm/0.005%, parallel resonant, AT-cut crystal is required (ESR < 35 Ω).

B.4 Is the load capacitance correct?

When selecting a crystal, the load capacitance requirement specified by the crystal manufacturer should be met. The total load seen by the crystal oscillator will include both the discrete load capacitance and all the trace parasitics.

B.5 Are the crystal placement and layout correct?

The crystal should be located as close as possible to the XTAL1 and XTAL2 inputs of the device to minimize parasitic capacitance. If possible, the connection should be done with a single layer trace (no vias). The layout should include a grounded cross-hatch area under the crystal. The case of the crystal should be connected to the cross-hatch to reduce EMI emissions.

When Using an External Oscillator for the Ethernet Clock:

B.6 Is the oscillator of the correct frequency, tolerance and drive level?

A 20 MHz 100 ppm/0.01% CMOS oscillator is required.

B.7 Is the oscillator connected correctly?

The oscillator drives the XTAL1 pin. The XTAL2 pin must be left unconnected.

Ethernet LEDs:

B.8 If an EEPROM is present, is the level on the EESK/$\overline{\text{LED1}}$ pin high after hardware reset?

The logic high is used to indicate an EEPROM is present. The pin can be pulled up either by LED circuitry or an external pull-up resistor.

B.9 If the EEDO/$\overline{\text{LED3}}$ pin is used to connect to both an LED and an EEPROM, does the EEPROM IOL specification meet the LED load?

Typically, the I_{OL} requirement of the LED exceeds the specification of the EEPROM and buffering circuitry is required.

10BASE-T Interface:

B.10 If the 10BASE-T interface is not used, are all related signals left unconnected?

B.11 Have unrelated signals and power and ground planes been removed beneath the filter/ transformer and RJ45 connector?

To prevent unrelated signals as well as power and ground noise from coupling into the network interface, there should be no unrelated signals, power, or ground plane present beneath the filter/transformer module and RJ45 connector.

B.12 Have the 10BASE-T signals been routed in pairs?

All differential network signals should be routed in pairs. Proximity to noisy signals should be avoided. Transmit and receive pairs should be routed separately from each other to avoid cross-talk.

B.13 Does the design use a common-mode choke?

Common-mode noise is the primary contributor to radiated energy from the 10BASE-T interface. The use of a common-mode choke is highly recommended to allow the design to pass EMI testing.

B.14 Is all 10BASE-T circuitry placed together at the perimeter of the board near the media connector?

To provide a 10BASE-T port, all that is needed is a network of resistors, a filter and isolation transformer, a common-mode choke, and an RJ45 connector. By keeping the 10BASE-T circuitry on the motherboard free from unrelated signal traces, interference from unrelated signals is minimized.

AUI Interface:

B.15 If the AUI port is not used, are all related pins left unconnected?

B.16 Are the DI± and CI± signals terminated properly?

The DI± and CI± pairs must be terminated with 40.2 Ω (or 39 Ω SIP) resistors. The optional 0.01 µF – 0.1 µF capacitors to ground may be used to reduce common mode voltage on the differential pairs.

B.17 Have the AUI signals been routed in pairs?

All differential network signals should be routed in pairs. Proximity to noisy signals should be avoided. Transmit and receive pairs should be routed separately from each other to avoid cross-talk.

B.18 Are the AUI signals connected to the AUI DB-15 connector through a transformer?

The IEEE 802.3 specification allows signals of up to 15V in amplitude on the AUI connector. An isolation transformer is required to protect the inputs of the PCnet device from such voltages since they exceed the operating conditions of the device.

B.19 Is all AUI circuitry placed together at the perimeter of the board near the media connector?

To provide an AUI port, all that is needed is the termination resistors, an isolation transformer, and a DB-15 AUI connector. By keeping the AUI circuitry on the motherboard free from unrelated signal traces, interference from unrelated signals is minimized.

10BASE2 Interface:

B.20 Are all AUI interface design rules met?

The 10BASE2 interface consists of an on-board transceiver that is connected via a transformer to the AUI port of the PCnet device. All AUI interface design rules apply also to the 10BASE2 interface.

B.21 Is the DO± pair terminated properly?

For an on-board transceiver design, the DO± pair must be terminated on the transceiver side of the transformer in a similar way to the DI± pair.

B.22 Have unrelated signals and power and ground planes been removed beneath the transceiver and associated components?

To prevent unrelated signals as well as power and ground noise from coupling into the network interface, to reduce parasitics, and also to meet isolation requirements, there should be no unrelated signals, power, or ground plane present beneath all of the 10BASE2 MAU circuitry.

B.23 Is all 10BASE2 circuitry placed together at the perimeter of the board near the media connector?

Place the 10BASE2 transceiver and external support components as close as possible to the BNC connector to minimize parasitic capacitance, especially on the RXD and TXD lines.

B.24 Is the transceiver soldered directly to the PCB without using a socket?

B.25 Is the transceiver configured to generate the SQE test message?

For testing of the collision logic, the SQE test message (nominal 10 MHz sequence) is returned on the CI± pair, by the transceiver, within a 40 network-bit-time period after DI± goes inactive. If not, the CERR collision error bit will be set in CSR0.

B.26 If an 8392 type transceiver is used, is there a 200 k Ω resistor between pin 1 and pin 2 of the BNC connector?

The resistor solves the driver hang problem when the BNC connector is unterminated. An alternative is to use the 8394 type transceiver.

C. SCSI Practices

C.1 Is a low pass filter for the SCSI clock used?

To reduce unwanted noise from the 40 MHz oscillator a 33 Ω resistor should be placed in series with the oscillator to form a low pass filter with the input capacitance (10pF) of the SCSI CLK1 pin.

C.2 Are SCSI-2 high density cables used?

SCSI-2 high density cables should be used, as the cable is shielded and signal wires are strategically placed for better signal travel.

C.3 Is active termination used for the SCSI interface?

The use of active or regulated termination is highly recommended.