



Designing 10/100 Mbps Ethernet Switches with the NetPHY™-4LP Device (Am79C875)

Application Note

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by Robert Hartman

This application note provides a design reference for customers implementing mixed 10BASE-T/100BASE-X switch systems, using the NetPHY-4LP device as the PHY. Included is an overview of the NetPHY-4LP functional blocks and outstanding features, guidelines on interfacing to repeaters and switches, and general high-speed design and layout rules. For further NetPHY-4LP device information, refer to the product data sheet, and for other sources of information for PHY layout and high-speed designs, consult the References section at the end.

INTRODUCTION

Using the new capabilities standardized in IEEE 802.3u, it is now possible to build an Ethernet network that freely mixes both 10 Mbps and 100 Mbps equipment. The switch now has the responsibility, through Auto-Negotiation, to determine the capabilities of the connected equipment and to configure the link appropriately to support that equipment. The Am79C875 NetPHY-4LP is a complete four-port implementation of the IEEE 802.3u PHY for 10 Mbps and 100 Mbps operation on both twisted pair and fiber optic media.

As the use of switched Ethernet has become more widespread, manufacturers have desired to increase the number of ports available on the switch. Using the MII standardized in IEEE 802.3u presents a problem in this regard, due to the large number of signals involved for each physical layer port. To address this problem, AMD joined with other companies desiring a smaller pin count solution and created the Reduced Media Independent Interface (RMII).

The RMII is functionally equivalent to the IEEE 802.3u MII but uses significantly fewer signals. This allows a single switch ASIC to increase the number of physical layer ports to which it can attach. The RMII is an industry standard interface for Ethernet switches that connects chips from different vendors. The NetPHY-4LP implements the RMII interface to connect to switch and other multi-MAC applications.

OVERVIEW

The NetPHY-4LP device offers both 10 Mbps and 100 Mbps operation. A summary of the functions in each PHY sublayer is provided here for reference.

Reduced Media Independent Interface

The RMII is designed to allow vendors of physical layer and switch fabric silicon to interoperate with minimal difficulty.

The RMII provides the same functions as the MII, only with fewer pins. The RMII has the following characteristics:

- Supports both 10 Mbps and 100 Mbps data rates
- Provides data delimiters that are synchronous to the clock reference
- Provides independent 2-bit wide transmit and receive data paths
- Uses TTL signal levels, compatible with common digital CMOS ASIC processes
- Uses a minimum number of pins to accomplish the task.

The RMII performs the same functions as the MII while reducing the number of pins to a minimum. It provides the same media independence as the MII, supports both 10 Mbps and 100 Mbps data rates, and is tailored for application in Ethernet switches. A single 50 MHz clock is the reference clock for all signal transitions. When used at 100 Mbps, information is transferred on the transmit and receive paths on every clock cycle. At 10 Mbps, the information on the transmit and receive paths is stable for 10 cycles of the reference clock.

The transmit path uses only three signals: TX_EN and TXD[1:0]. These signals are synchronous to the single, 50 MHz system reference clock (REF_CLK). Two bits (a di-bit) of information are transferred from the MAC to the PHY on TXD[1:0]. The receive path also uses only three signals: CRS_DV and RXD[1:0]. Again, a di-bit of information is transferred from the PHY to the MAC on RXD[1:0]. CRS_DV combines the functions of the MII signals CRS and RX_DV. Optionally, RX_ER may be added to signal physical layer errors. The signals of the receive path are also synchronous to the system reference clock.

Physical Coding Sublayer

The PCS lies below the MII/RMII interface. It performs the following functions as described in IEEE 802.3u (100BASE-X) standard:

- Encoding and decoding MII data nibbles to and from 5-bit code groups. This is accomplished by using the 4B/5B algorithms.
- Generating Carrier Sense and Collision Detection indications.
- Serializing and deserializing code groups for transmission and reception on the underlying PMA layer.
- Mapping of Transmit, Receive, Carrier Sense, and Collision Detection between the MII and the underlying PMA layer.

The NetPHY-4LP device implements the PCS layer as described in the IEEE 802.3u standard and also adds a scrambler/descrambler block to complete the PCS functions, as shown in Figure 1 and Figure 2.

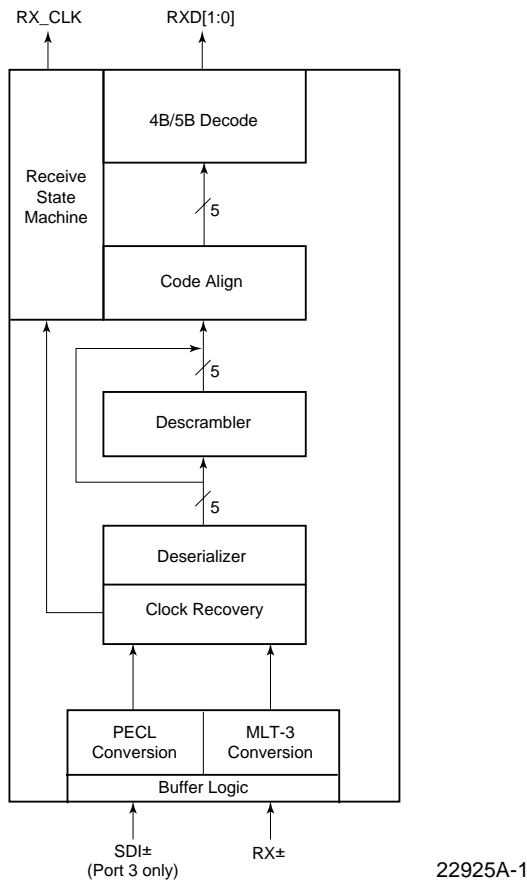


Figure 1. NetPHY-4LP 100BASE-X Receive Path

On receipt of data, after it has passed through the PMA layer, the serial data is deserialized and passed on as a 5-bit entity to the descrambler block. Scrambling and

descrambling is offered on the NetPHY-4LP device as a means of reducing EMI peaks in the radiated signal (data) caused by repetitive patterns of 0's and 1's. Scrambling is done by adding the output of a random number generator to the data signal. The descrambler is self-synchronizing and does the reverse process for received data. The scrambler/descrambler function can be set to minimize emissions as needed on the NetPHY-4LP device.

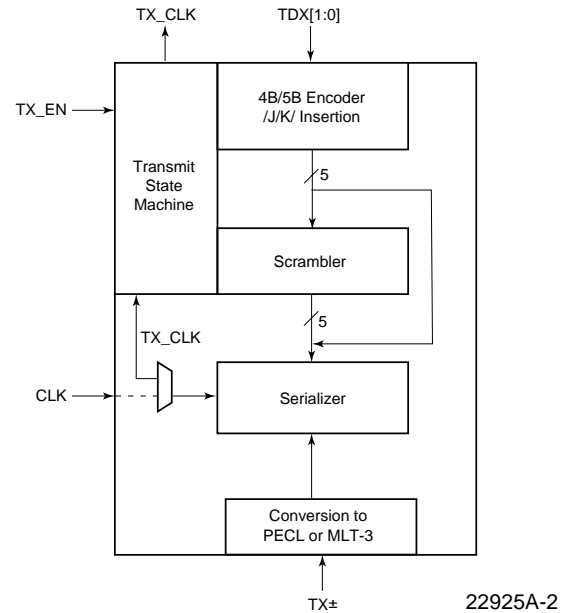


Figure 2. NetPHY-4LP 100BASE-X Transmit Path

Following the descrambler block, received data is aligned and decoded. Encoding and decoding is performed using the 4B/5B code-group algorithms. Decoding 5-bit PCS code groups into 4-bit MII groups or a pair of di-bit RMII groups effectively reduces the 125-Mbps physical channel rate to a 100-Mbps physical layer interface. The reverse happens for transmission. Here, JK and TR delimiter pairs are added (for transmission) or removed (for receive) from the packet when the data packet is aligned.

Refer to the IEEE 802.3u standard or the NetPHY-4LP device data sheet for the code-group mapping tables. The align/disalign and encode/decode features can be set as needed on the NetPHY-4LP device.

Once the data is decoded and converted into 4-bit nibbles, it is passed to the MII interface or as a pair of di-bits on RXD[1:0] of the RMII interface. All other RMII signals, such as RX_ER and CRS_DV, are set appropriately.

Figure 2 illustrates the transmission process through the NetPHY-4LP device from the RMII. Data is received on TXD[1:0], encoded into 5-bit PCS code groups,

aligned, scrambled (if necessary), and serialized for the PMA layer.

Physical Medium Attachment

The PMA layer lies below the PCS interface. It performs the following functions as described in the IEEE 802.3u (10BASE-X) standard:

- Clock recovery from the NRZI data provided by the PMD
- Mapping of transmit and receive code-bits between the PMA's client and the PMD
- Optionally, generating indication of carrier activity and carrier errors from the PMD
- Optionally, sensing receive channel failures, and detecting and transmitting the Far End Fault Indication (FEFI)

The NetPHY-4LP device uses an analog phase lock loop for clock recovery.

In transmit, after passing through the PCS, the 5-bit symbol is clocked into the APLL, serialized, converted to NRZI format, and shifted to the TX \pm outputs at PECL-compatible signal levels. The APLL uses the system CLK as the frequency and phase reference to generate the serial link data rate. The APLL requires a continuous external reference, from which it can derive its internal clock, and which is multiplied by 5 to generate the 125 Mbps channel rate. The external reference clock must meet IEEE 802.3u frequency and stability requirements (± 50 ppm).

When receiving, data coming into the RX \pm inputs is streamed into the APLL, which recovers the clock. This recovered clock is then used to recover the data. The data, in an unframed 5-bit symbol, is sent up to the PCS level for further operations. The APLL is capable of recovering data correctly within ± 1000 ppm of the 25 MHz clock signal.

Carrier Detect, Link Monitor, and Far End Fault Detect and Generate functions are also provided by the NetPHY-4LP device. Refer to the IEEE 802.3u standard for details on these functions.

10BASE-T MAU

Within the NetPHY-4LP device, there are four 10BASE-T blocks, connecting to a twisted pair network through an integrated Medium Access Unit (MAU). The NetPHY-4LP MAU meets transmitter and receiver requirements as specified in IEEE 802.3, Section 14, when properly terminated. The MAU performs the following functions:

- Transmit operation
- Receive operation
- Link Interface status
- Collision Detect

- Jabber function
- Reverse Polarity Detect

For transmit operations, data is Manchester Encoded from the repeater layer above and sent out to the TX driver in the NetPHY-4LP device. If there is no data to be sent, the MAU sends idle signals out on TX \pm . When receiving, the RX driver receives data that passes through the squelch circuit. The squelch circuit unsquelches the data and then AND's it with the original data, so that only the valid data signal peaks are passed onto the Manchester Decoder and out to the repeater. Refer to Figure 3 for the 10BASE-T transmit and receive paths.

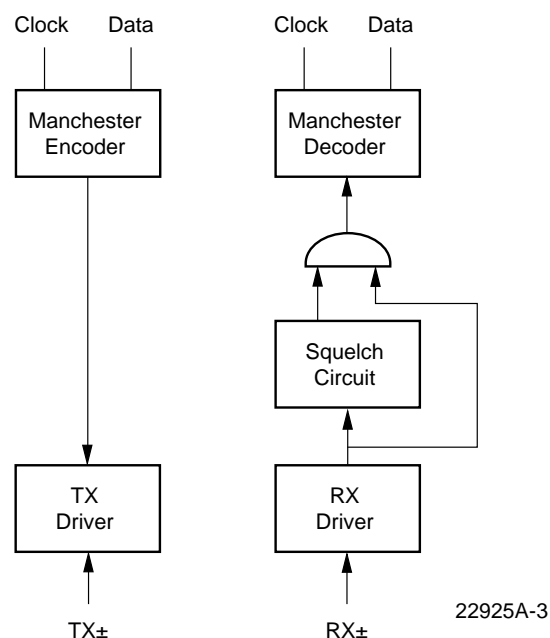


Figure 3. NetPHY-4LP 10BASE-T Transmit and Receive Data Paths

The MAU looks for valid link pulses and raises the Link signal to indicate valid Link. The NetPHY-4LP transceiver powers up in the Link fail state, and Auto-Negotiation determines if it will enter Link Pass. Once in Link Pass, any packets received will cause the PCS to raise Carrier Sense.

The MAU also provides a Collision Detect function. Collision is simultaneous activity on both RX \pm and the internal transmit function. This causes the PCS to assert the Collision signal on the MII.

The MAU supports Jabber and Reverse Polarity Detect. Jabber is asserted if an excessively long signal (long data frame) is transmitted for a period of 20-150 ms. The Collision signal is asserted by the PCS when Jabber is detected. Reverse Polarity

is in operation if the End-of-Packet (ETD) delimiter is detected upside-down. When two consecutive packets are received with the ETD delimiter upside-down, then the polarity will be locked. To change the polarity, the link must be brought down and back up again.

Physical Medium Dependent Sublayer

The PMD sublayer lies below the PMA and was originally derived from the FDDI standard. Thus, it has been defined to support 125-Mbps fiber and shielded and unshielded twisted pair media. The PMD translates the NRZI-coded data to and from signals suitable for the specified medium, which is either twisted pair or fiber. Data must be transmitted using at least Category 5 UTP for twisted pair applications.

MLT-3 transmission

For twisted pair, data translation is accomplished most often by using MLT-3 (Multilevel Transmission - 3 Level). MLT-3 is very similar to NRZI, except that it adds a third level of voltage to represent the data. Thus, where NRZI data falls between 0 V and a predetermined limit of volts, MLT-3 data can be any of three levels: 0, +V and -V. MLT-3 uses a fundamental frequency one-half that of NRZI. With that, MLT-3 achieves data transmission at the same data rate, but with lower spectral energy (e.g., lower EMI emissions) than NRZI. Often, MLT-3 is further combined with scrambling to eliminate repetitive patterns in the data that cause more peaks in the EMI spectrum.

When implementing MLT-3, the following several considerations must be attended to, due to the type of media being used:

- Adaptive equalization
- Baseline restoration
- Transmit conditioning

Adaptive equalization is a key feature in MLT-3. Data transmitted over twisted pair wire can suffer much attenuation (signal loss) or experience varying amounts of attenuation, due to different frequency components of the signal itself, as well as cable length. When the signal is received, the device has to reconstruct the original signal and somehow overcome this loss. Adaptive equalization enables the MLT-3 device to compensate for this loss and for varying cable lengths by analyzing the incoming signal and adjusting the equalizer accordingly.

Baseline restoration is another key feature required for MLT-3. A problem with data transmission is baseline wander, which is described as DC drifts in the incoming signal, and which may occur due to data pattern dependent DC shifts, the inherent low frequency bandwidth of the channel, and the AC coupling transformers. If not corrected, the droop component of the transformers dominate and “drag” the signal amplitude down below baseline causing data errors or link failure. Baseline restoration circuitry compensates for this wander by comparing the incoming signal with a reconstructed reference. The difference is filtered and used to affect low frequency compensation in order to maintain the equalized signal at the reference level.

Transmit conditioning includes providing the correct transmit amplitude at the TX outputs, as well as generating output waveforms synchronized in timing with minimal jitter effects.

The MLT-3 logic block with adaptive equalization, baseline restoration, and transmit conditioning has been integrated into the core four-port PHY logic of the NetPHY-4LP device. The MLT-3 block performs all the necessary functions required by the IEEE 802.3u standard without requiring any external glue logic. The MLT-3 logic is always enabled and when the Port 3 SDI± pins are pulled to V_{SS} .

The TX± and RX± differential signal pairs connect directly to the PMD as shown in Figure 4.

PMD Magnetics

As in 10BASE-T, magnetics solutions are still needed to provide isolation between the cable and the PHY layer. Most modules are comprised of any combination of filters, transformers, and chokes for common mode rejection, but filters and chokes are optional and can be obtained separately. They provide high voltage isolation (ESD protection @ 2 kV), wide bandwidth, and fast rise times.

An important point to note is to follow termination guidelines as recommended by the magnetics manufacturer. This is interpreted as a combination of resistors and decoupling capacitors and proper grounding on non-data lines (including center taps) used to reduce common mode noise, that provides significant reduction in EMI and noise susceptibility. Center tap connections can typically provide a 10-dB improvement in common mode rejection.

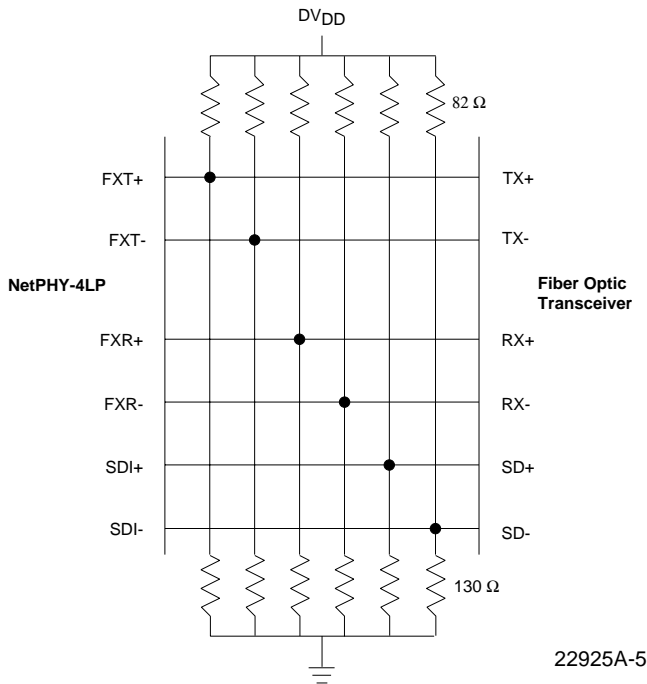


Figure 5. Interfacing the NetPHY-4LP Device Port 3 to a Fiber Optic Transceiver

Auto-Negotiation

The objective of Auto-Negotiation is to determine the abilities of the devices sharing a link. After exchanging abilities, the NetPHY-4LP device and remote link partner device acknowledge each other and make a choice of which advertised abilities to support. The Auto-Negotiation function facilitates an ordered resolution between exchanged abilities. This exchange allows both devices at either end of the link to take maximum advantage of their respective shared abilities.

The NetPHY-4LP device implements the transmit and receive Auto-Negotiation algorithm as defined in IEEE 802.3u, Section 28. The Auto-Negotiation algorithm uses a burst of link pulses called Fast Link Pulses (FLPs), which are spaced between 55 μs and 140 μs so as to be ignored by the standard 10BASE-T algorithm. The FLP burst conveys information about the abilities of the sending device. The receiver can accept and decode an FLP burst to learn the abilities of the sending device. The device can perform Auto-Negotiation with reverse polarity link pulses.

The NetPHY-4LP device uses the Auto-Negotiation algorithm to select the type connection to be established according to the following priority: 100BASE-TX full-duplex, 100BASE-T4 (not supported by NetPHY-4LP device), 100BASE-TX half-duplex, 10BASE-T full-duplex, and 10BASE-T half-duplex.

The Auto-Negotiation algorithm is initiated when one of the following events occurs: reset, transition to link fail

state, Auto-Negotiation restart bit is set, or the Auto-Negotiation enable bit is set. The result of the Auto-Negotiation process can be read from the status register for the port of interest.

The NetPHY-4LP device supports Parallel Detection for remote legacy devices, which do not support the Auto-Negotiation algorithm. In the case that a 100BASE-TX only device is connected to the remote end, the NetPHY-4LP device will see scrambled idle symbols and establish a 100BASE-TX only connection. If NLPs are seen, the NetPHY-4LP device will establish a 10BASE-T connection.

USING THE NETPHY-4LP DEVICE IN MIXED 10 MBPS AND 100 MBPS ETHERNET APPLICATIONS

Ethernet Switches

Because of the ability to create free bandwidth in an Ethernet network, Ethernet switching is one of the fastest growing segments of the Ethernet market. There has also been a significant cost premium associated with switches over repeaters. This is due to the enhanced functionality and additional bandwidth it brings to a network. While market forces have been acting to bring the cost of Ethernet switches down, the NetPHY-4LP device brings higher integration and increased functionality to an Ethernet switch to significantly reduce the cost and complexity of the PHY solution.

The NetPHY-4LP device provides a complete PHY solution for mixed 10 Mbps and 100 Mbps Ethernet switches. The RMII mode of operation of the NetPHY-4LP device allows the switch designer to increase the density and/or reduce the cost of the switch ASIC by requiring fewer signal pins per PHY port. Each link includes full support for Auto-Negotiation and full status reporting, including circuitry to report up to five different status conditions for display on LEDs.

Design and layout practices for Ethernet switches vary according to the chip set used. However, PHY design and layout using the NetPHY-4LP device is similar to that of repeater design, as both switches and repeaters are susceptible to similar noise and EMI effects. Thus, switch system designers should follow the rules for repeaters and general high-speed logic and interface design rules. Refer to the *General Circuit Design and Layout Guidelines* section for further information.

NetPHY-4LP Operation in an Ethernet Switch

The NetPHY-4LP device is an ideal PHY solution for an Ethernet switch in a mixed 10 Mbps and 100 Mbps environment. There is one port per RMII, which can be configured for half- or full-duplex operation. RMII operation minimizes the number of signals required between the NetPHY-4LP device and the switch ASIC.

The on-chip Auto-Negotiation logic automatically configures each link to operate at either 10 Mbps or 100 Mbps, depending on the abilities of the equipment sharing the link. By connecting each of the NetPHY-4LP RMII ports to a baseband switch engine, for as many NetPHY-4LP devices as are needed to fill out the required number of links, and by adding magnetics, connectors, and the appropriate passives for AC and DC termination, a complete Ethernet switch can be produced.

A switch application example is shown in Figure 6. Each NetPHY-4LP RMII port is directly to a corresponding MII port on the switch.

Ethernet Repeaters

Ethernet switches are the highest growing segment of the Ethernet market, and some applications continue to use repeaters. The NetPHY-4LP device is targeted at switches primarily, but optionally can be used for RMII repeaters. However, additional latency is incurred

which should be evaluated carefully when considering this mode.

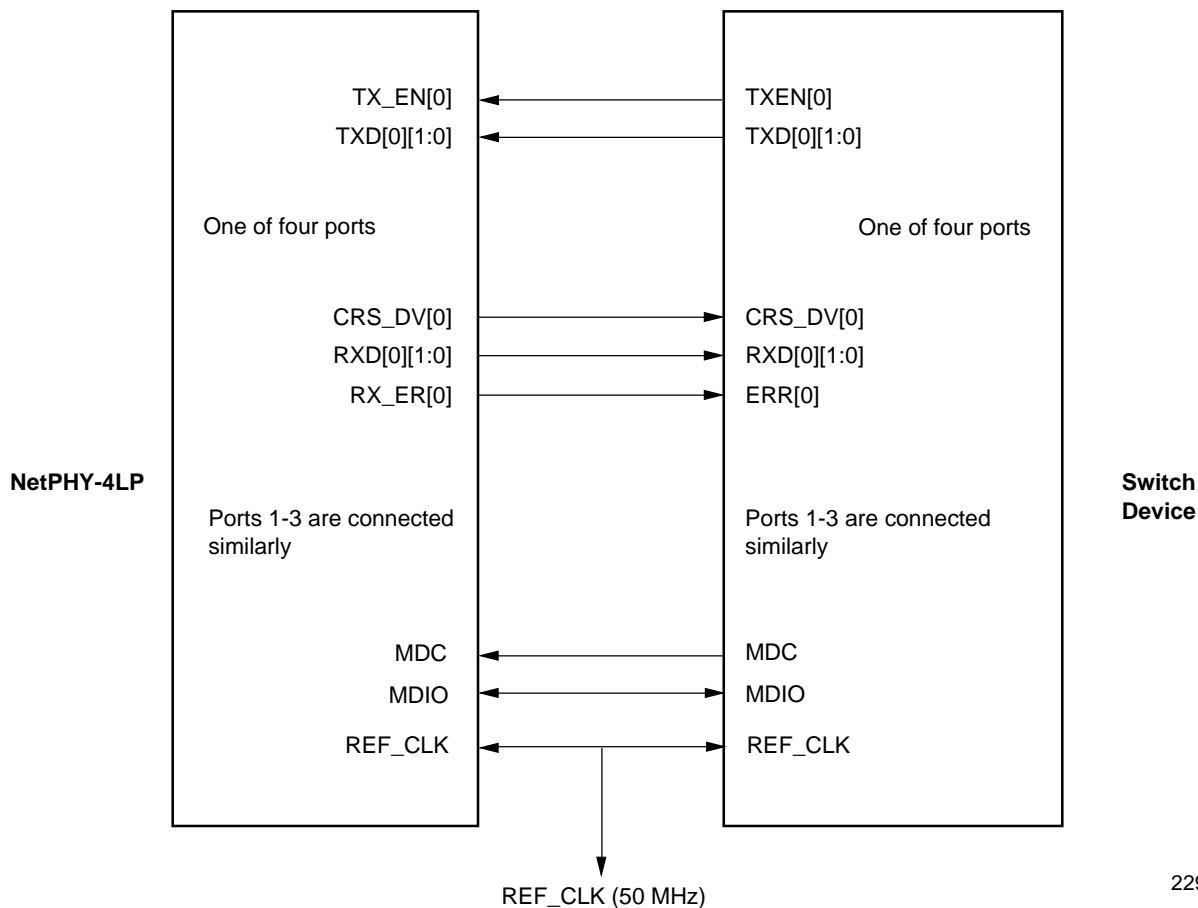
LED STATUS REPORTING

The NetPHY-4LP device provides extensive status reporting for each link through its LED port. The conditions reported through the LED port are link speed, full-/half-duplex operation, link up/down status, and indications of transmit and receive activity.

LED Port Configuration

The NetPHY-4LP device has several pins which are used both device configuration and LED drivers. These pins set the configuration of the device on the rising edge of \overline{RST} and thereafter indicate the state of the respective port.

The polarity of the LED drivers (Active-LOW or Active-HIGH) is set at the rising edge of \overline{RST} . If the pin is LOW at the rising edge of \overline{RST} , it becomes an active-HIGH driver. If it is HIGH at the rising edge of \overline{RST} , it becomes an active LOW driver.



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Figure 6. Application of the NetPHY-4LP Device in a 10/100 Mbps Ethernet Switch

Proper configuration requires external pull-up or pull-down resistors. If the LED corresponding to a pin is not used, the pin must be terminated via a resistor. The resistor value is not critical and can be in the range of 1 k Ω to 10 k Ω . If the corresponding LED is used, the terminating resistor must be placed in parallel with the

LED. Figure 7 illustrates the wiring of the LEDs for both configuration settings.

The value of the series resistor (R_L) should be selected to ensure sufficient illumination of the LED. It is dependent on the LED rating.

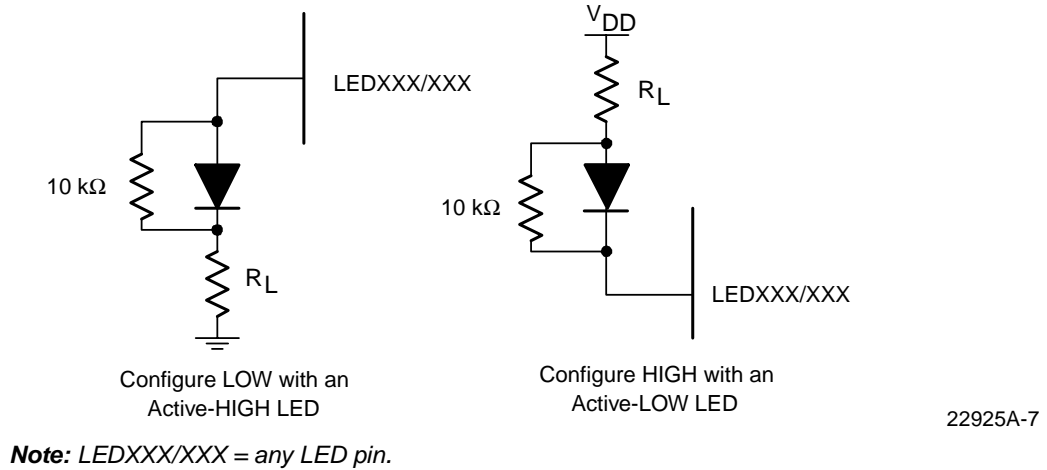


Figure 7. LED Port Configuration

MDC/MDIO CONSIDERATIONS

Ringling Effects

The serial management pins MDC and MDIO are the command interface to the system MAC/Switch/Repeater. Even though these signals are low speed (2.5 MHz) per the IEEE standard, certain effects like ringing and signal reflection can affect performance. To counter these random situations, we recommend adding a damping resistor of small value, in the range of 20 Ω to 40 Ω in series with the MDC pin. A shunt/0- Ω resistor can be used and if there are reflections/ringing, the shunt can be swapped out for the resistor.

Fast MDC/DMDIO Access

The NetPHY-4LP device supports MDC clock speeds of up to 25 MHz, 10 times faster than dictated by the standard. Providing a faster management clock allows

designers to speed up transactions to and from the PHY device.

However, much like high-speed system design, the faster MDC/MDIO signals must also be designed carefully to avoid typical high-speed design pitfalls, such as double clocking and glitches. Adhering to recommended design rules below will reduce the incidence of pitfalls and ensure proper PHY communication and configuration for the system.

Point-to-Point MDC Layout

When interfacing to a single MAC or quad MAC/switch, serial resistors are recommended when using faster MDC clock rates. The resistor value depends on the trace and driver source impedance, and 50 Ω is approximate. The resistor should be placed close to the MAC/Switch driver. Refer to Figure 8.

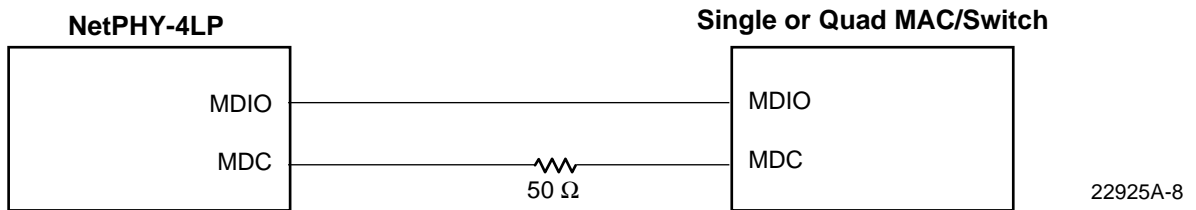


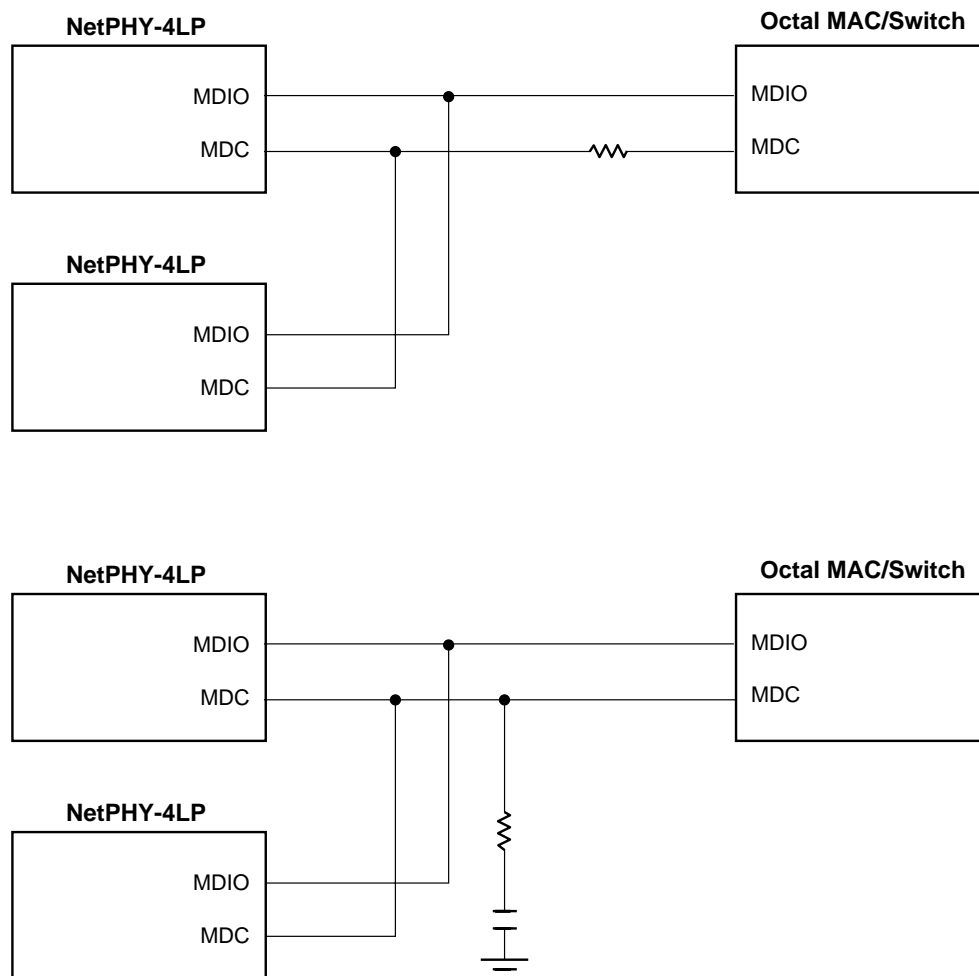
Figure 8. Point-to-Point MDC Connection

Octal MAC to PHY MDC Layout

With a faster MDC clock, high frequency noise is more prevalent. A serial or RC termination scheme on the MDC line can reduce the amount of high frequency noise. Again, the resistor choice is dependent on the trace and driver source impedance. The capacitor in the RC scheme is dependent on the MAC/Switch drive capability and AC loading of the MDC line. When using the RC termination, the termination should be placed midpoint between the PHY devices. Note that the distance between the NetPHY-4LP devices should be as short as possible. Refer to Figure 9.

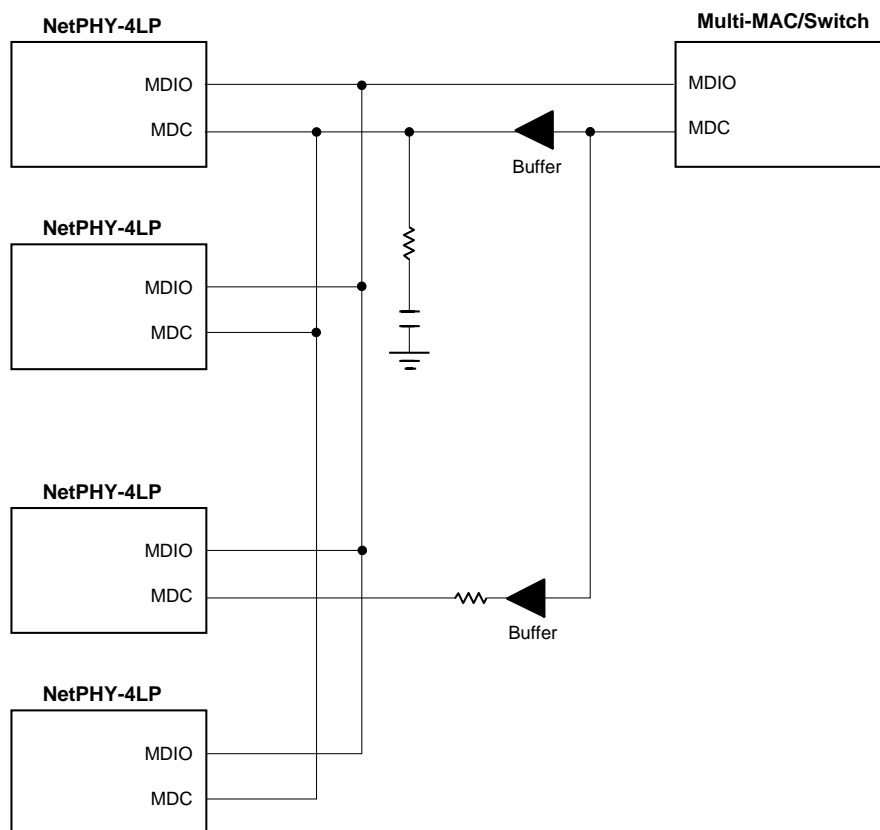
Multi-Port Switch/MAC to PHY MDC Layout

With multiple PHY devices connected to a single multi-MAC/Switch device, it is recommended to use a line driver or buffer (such as an FCT/ACT/ABT244) or other special clock driver for the MDC clock. Series or RC termination can be used if the rise/fall edges (10% - 90%) are less than the round trip delay of the signal. Again the resistor choice is dependent on the trace impedance. The capacitor in the RC scheme is dependent on the MAC/Switch drive capability and AC loading of the MDC line. When using the RC termination, the termination should be placed midpoint between the PHY devices. Note that the distance between the NetPHY-4LP devices should be as short as possible. Refer to Figure 10.



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Figure 9. Dual PHY MDC Layout



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Figure 10. Multi-PHY MDC Layout

GENERAL CIRCUIT DESIGN AND LAYOUT GUIDELINES

To optimize a design for the NetPHY-4LP device, designers must follow basic rules in layout and placement, decoupling and isolation, clock and oscillator considerations, general termination, power supply filtering and plane partitioning, and finally, EMI considerations. Following these rules will contribute greatly to a properly functioning repeater or switch system. In addition to and above all, suggestions from PHY and magnetics vendors should be followed when designing a specific solution.

Part Recommendations

- Resistors should be 1% tolerance.
- Capacitors:
 - For low frequency and large value decoupling, use electrolytic capacitors.
 - For high frequency and small value decoupling, use X7R and C0G capacitors.
- Recommended ferrite beads should be Fair Rite 274-3019-446.
- Fully Shielded RJ-45 8-position jacks should be used.

Placement and Layout

Placement and layout are the key components of board design. Much care, if given to performing these tasks properly, ensures a good design. Noise, ringing, transmission lines, and other factors have to be controlled. Data lines should have a controlled impedance and be properly terminated, and power supply pins should be protected by proper filtering techniques. All PC traces should be treated as transmission lines with continuous ground or power planes beneath each trace.

Placement of the NetPHY-4LP PHY should be symmetrical and as close as possible with respect to the switch and other devices. This will help to provide equal trace length to each PHY and counteract many timing/skew problems, especially with synchronization of the clock to all clock-based components.

When placing decoupling components, traces should be kept as short as possible, especially for the transceiver interface. Short traces minimize noise interference. These components, if using many transceivers, should be placed symmetrically across the board to avoid uneven parasitic loading. It is preferred to have decoupling components on the same side as the device, to avoid routing through different planes and having components on

the solder side, as well as absorbing noise from different planes.

Other general guidelines for signal trace routing include the following:

- Only differential pair signals (TX \pm and RX \pm) should be run parallel to each other, since they provide a canceling effect on noise. Non-differential parallel traces tend to induce crosstalk. Differential signal traces should be as short and direct as possible avoiding unnecessary vias.
- 90° trace corners should be minimized. Bevel them at a 45-degree angle or as appropriate (chamfered or radiused approach). Differential pairs will require equal trace length, even with 45-degree angle traces. Sharp edges add parasitic effects that translate into minute impedance mismatches.
- Minimize the number of vias for any one given signal trace. It is recommended that the signal trace remain only on one plane (component or solder) or go directly into the power or ground layer (if it is a power/ground signal). As vias pass through layers, the impedance of the trace changes and it is difficult to maintain constant impedance after the via.
- Traces carrying large amounts of current should be thicker than normal signal traces. Otherwise, the traces may be easily burned out by current overloads.

EMI Considerations

To reduce EMI emissions, the following rules should be observed for board layout:

- Avoid crossrouting of transmit and receive signals. This will result in crosstalk and interference as well as decreased EMI compliance.
- The PCB should be multilayer (4 to 6 layers), with individual power and ground sublayers for best high frequency and EMI performance. Component traces can be run on the component and solder sides, but preferably only on the component side, unless it is absolutely critical to place decoupling components underneath devices. The power and ground layers should be in the inner layers of the PCB.
- Proper ground and power plane partitioning should be followed.
- Use shielded RJ-45 jacks with contacts to chassis ground and terminate unused pairs.
- Proper termination of components and unused (high speed) pairs in their common mode impedance (to chassis ground) minimizes cable reflections and common mode standing waves.
- When adding spacers to elevate the system from the chassis, ensure that the screws are not placed symmetrically (either straight rows/columns or diagonals) throughout the board. The screws tend to act as antennae and create wave harmonics that

will affect the EMI testing. Optionally, Teflon screws can be used to support the board.

Clock/Oscillator Considerations

The clock is an important device in the design, since it is from the main clock that any reference clocks are derived. It is also used for the various PLLs. With a noisy clock signal, PLLs will have difficulty locking onto the data packets.

Oscillators are recommended, in the metal can package, due to the shielding. They should be decoupled as recommended by manufacturer's guidelines. Oscillators should meet ± 50 ppm over temperature with CMOS output.

Oscillators should be placed as close as possible to switch and NetPHY-4LP components. If this is not possible, they should be placed close to the switch component, and same-length traces should be used to the NetPHY-4LP devices. Extra care should be paid when using the NetPHY-4LP device in RMI mode because of the 50 MHz CLK_REF requirement. It is recommended that the clock trace not run parallel to other signal traces, particularly the RX \pm and TX \pm signals. Careful routing of the clock signal traces can minimize the clock noise coupled to other signal traces.

General Rules On Termination

Termination of signals is a requirement in switch design. Termination helps reduce ringing/cable reflections and impedance mismatching. A variety of termination networks are available, and manufacturer (NetPHY-4LP device, and magnetics) recommendations should be heeded.

AC termination is needed to minimize high-speed reflections. This can be accomplished by placing a resistor in series with a capacitor to digital ground or a series resistor on high speed data/control lines (47 Ω or lower can be used). The effect of the termination will also slow down any fast ramping CMOS signals and ease some undershoot/overshoot conditions.

Termination is also needed at the PECL level. Signal traces should be effective 50 Ω transmission lines. This can be achieved using Thevenin termination or other recommended schemes from transceiver and magnetics vendors. The unused pairs of the RJ-45 jacks should also be terminated to improve EMI performance. Consult magnetics vendor application notes.

Power Supply: Decoupling and Filtering

With a complicated high-speed design, noise can be picked up and propagated easily through the devices. If this noise is in the power supply lines, device and system performance is compromised. DV_{DD} signals should be decoupled as closely as possible to the IC. Ferrite beads can be used to isolate power planes, and

an appropriate selection of capacitors can be placed around the board to filter out other frequencies. In general, 10-100 μF tantalum or electrolytic capacitors filter line frequencies and act as high speed filters. An additional ferrite bead can be used to help the effectiveness of the capacitor on the power input. 0.1 μF capacitors will help filter out higher harmonics (100 MHz and higher). Other recommendations are as follows:

- 0.1 μF to 1.0 μF capacitors should be used for logic decoupling
- 0.1 μF capacitors should be used between each port's power/ground signals
- A 22 μF tantalum capacitor in parallel with a 22 μF ceramic capacitor should be used to decouple the power supply source for each device. See Table 1 to decouple NetPHY-4LP power and ground signals.

Table 1. Decoupling Guidelines for NetPHY-4LP Device

Signal Name	Function	Decoupling Capacitor Value	Notes
CV _{DD}	Core power supply	0.1 μF	Critical components
OV _{DD}	I/O power supply	0.1 μF	Critical components
AV _{DD}	10/100 Mbps analog PLL power supply	0.1 μF	Critical components
GA_V _{DD}	General power supply	0.1 μF	
OGND, CGND, AGND, GAGND	Ground		Grounds connected to DV _{SS} plane

Critical Components

Critical components are those components that should be placed as *close as possible* to the NetPHY-4LP device. The capacitors should be within 3 mm of the chip. The following guidelines should be followed:

- All ceramic-filtering capacitors should be X7R type.
- The primary critical capacitors needed (0.1 μF) are for the analog V_{DD} pins (AV_{DD}): pins 7, 8, 15, 16, 23, 24, 31, and 100.
- Of secondary importance are the capacitors for the Core V_{DD} pins (CV_{DD}): pins 54, 67, and 77.
- Of tertiary importance are the capacitors for the Digital I/O pins (OV_{DD}): pins 44, 62, and 80.

Other Power Supply Considerations

The NetPHY-4LP device uses a 3.3 V nominal power supply. Voltage tolerance should be $\pm 5\%$ over operating temperature range. An LT1117 3.3 V regulator from Linear Technology can be used.

Plane Partitioning and EMI Considerations

100BASE-TX uses MLT-3 line coding (with a fundamental frequency of 32.5 MHz) to shift 90 percent of spectral energy below 40 MHz. Without it, most systems, even with good system design, would not be able to pass standard EMI tests.

The NetPHY-4LP device is a four-port device with RMII interfaces and MLT-3, 10BASE-T, or PECL interfaces. The RMII interface lies in the digital portion of the board and, therefore, can be overlaid by a digital power and ground plane. PECL/MLT-3 ports can be overlaid by digital or PECL planes, but PECL planes are recommended so long as they are tied to a system or chassis ground of some sort to provide for return paths. The NetPHY-4LP device can have separate APLL planes to ensure a clean power signal is sent to the on-board PLLs.

In general, digital areas can be partitioned from analog areas, which are extremely sensitive to noise. Digital signals alone suffer greatly since the fast switching times of digital components cause a significant amount of energy to be dumped into power and ground layers, generating significant overshoots and undershoots on the line. Any analog circuitry on the same plane will also experience the energy fluctuation, which can improperly bias the transistors, possibly causing the circuits to malfunction.

A low pass filter combination of a ferrite bead (inductor) and capacitors provides a cleaner, filtered power plane for analog considerations. Ferrite beads are more effective than coils. At DC, the ferrite bead acts as a short, providing a low-resistance path for the power on the analog plane. The unwanted higher frequency AC noise sees the ferrites as inductors in a low pass filter. Ferrite beads generally allow an increase in impedance as the frequency increases. Ferrite beads are quite useful as filters. However, be aware that they do add extra inductance to the plane. Therefore, they should be used sparingly.

Ground plane layout, as well as power plane layout, should take into consideration the signal-return path for the AC current generated every time a signal switches. Once the signal has returned, the current loop has been completed. AC return signals have an entire plane in which to choose a path, but they take the path of least impedance (inductance and capacitance) to the current and not necessarily in a straight line. If there are physical breaks in the return signal plane, the signal has to circumvent the break, thereby, increasing

inductance and loop size. A ground plane layout involves a common digital ground plane, connecting with the remainder of the system beyond the MII interface. NetPHY-4LP evaluation kits have performed well using single power and ground planes, while adhering to strict design guidelines and EMI considerations.

The plane area under the magnetics is left void for optimum noise separation between the transmit/receive and chassis planes. The chassis plane connects directly to the RJ-45 jacks, which are recommended to be fully shielded. Additionally, 2 kV capacitors connected to chassis ground are required for ESD protection, per the IEEE 802.3u standard.

Other Placement and Layout Considerations

The following considerations should be made:

- Do not have power or ground planes beneath the differential pair traces in order to minimize common mode noise coupling and improve EMI performance.
- If high-speed clock speed/data signals are routed directly beneath the transceiver, there should be a power or ground plane between the signals and the NetPHY-4LP.
- Chassis Ground and Analog Ground should have a minimum of 45 mils of air gap separation. The separation is located between the primary side and the secondary side of the transformer, and there should be no power or ground planes beneath the primary or secondary sides.
- Power planes should not be segmented. Use a single, continuous power plane for the transceiver.
- Multiple power planes without proper coupling and decoupling can cause degradation in performance. If multiple power planes are used, place ferrite beads (impedance of 100 Ω at 250 MHz) between

planes for filtering and capacitors (0.1 μ F ceramic) to ground for coupling.

CONCLUSION

Mixed 10BASE-T and 100BASE-TX repeater or switch design is more intricate and requires a greater design effort than 10BASE-T design alone. However, there is a great amount of knowledge readily available to designers from the manufacturers of the components used in high speed designs.

Using the NetPHY-4LP device, it is relatively straightforward to design a mixed 10-Mbps and 100-Mbps switch system. With integrated MLT-3 and 10/100 Mbps four-port capability, the reduction in board space and related components (otherwise needed for single port PHYs), the NetPHY-4LP device provides an easier and more cost-effective design.

By using the recommendations in the application note for designs with the NetPHY-4LP device, mixed 10 Mbps and 100 Mbps repeater and switch designers should create highly efficient, cost-effective system designs with low part count, low power requirements, and value added features for their customers.

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