



# **Am79C901A HomePHY™ Board Design Guide**

*Application Note*

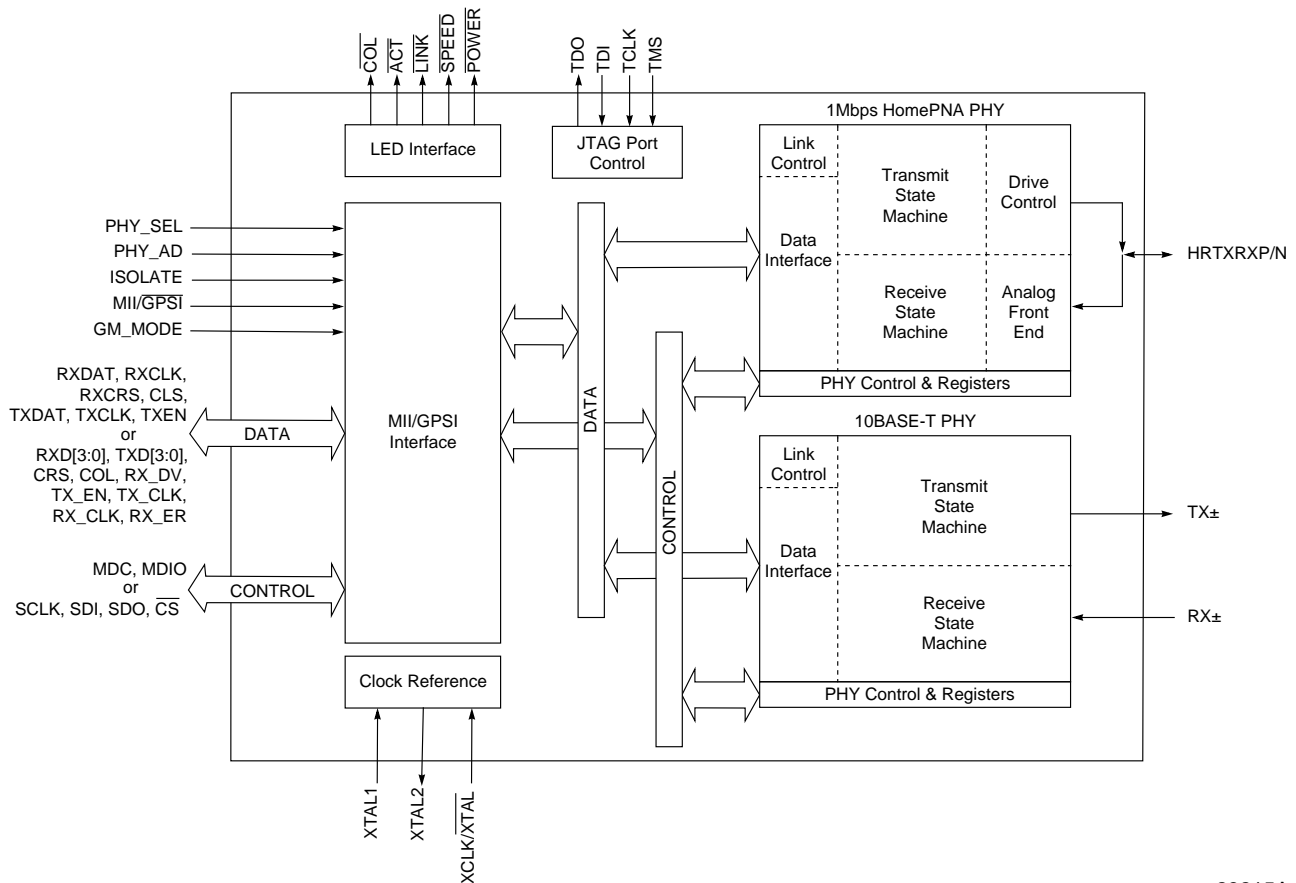
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## Application Note

This application note is intended to assist customers in using AMD's Am79C901A HomePHY device. Details concerning application information, circuit design, EMI, printed circuit layout techniques, and component selection are provided to help ensure first-pass success in implementing a functional design that has optimized signal quality. This document should be used in conjunction with the HomePHY Data Sheet (PID #22304) for functional descriptions and features of the device, as well as the schematics provided in the Evaluation Kit. Contact your local AMD Field Applications Engineer or Sales Office to discuss any questions that you may have.

## INTRODUCTION

The Am79C901A device is a highly integrated 1 Mbps home networking and 10BASE-T physical layer device (PHY) with MII-compatible and 7-wire GPSI interfaces. Figure 1 shows the block diagram of the device.



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Figure 1. HomePHY Block Diagram

## POWER SUPPLY

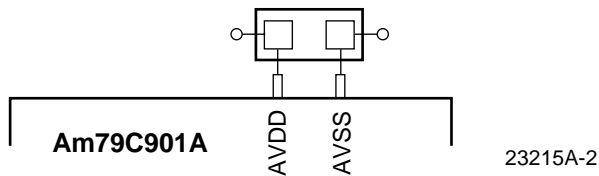
AMD's HomePHY device operates from a +3.3 V  $\pm 300$  mV power supply. However, some systems only have a +5 V supply. The best way to convert a +5 V supply to a +3.3 V is to use a linear regulator. The linear regulator also helps to optimize the receive sensitivity performance by providing a stable, quiet +3.3 V isolated from the possible noise of the +5 V system supply.

## DECOUPLING CAPACITORS

Great care should be given to the power distribution and decoupling of specific Am79C901A power pins. Poor power decoupling on these pins can cause degradation of the HomePNA small signal receive sensitivity by as much as 5 mV. The following pin pairs should have 0.1-0.2  $\mu$ F surface mount capacitors placed between them. To be effective, the capacitors should be placed as close as possible to the pins.

**Table 1. Pin Pairs Requiring Decoupling Capacitors**

68 PLCC	80 TQFP
Pin 16 AVDD and Pin 12 DVSS	Pin 9 AVDD and Pin 5 DVSS
Pin 58 AVDD and Pin 56 DVSS	Pin 57 AVDD and Pin 55 AVSS
Pin 54 AVDD and Pin 56 DVSS	Pin 53 AVDD and Pin 55 AVSS
Pin 50 AVDD and Pin 52 AVSS	Pin 49 AVDD and Pin 51 AVSS
Pin 48 AVDD and Pin 46 AVSS	Pin 47 AVDD and Pin 45 AVSS



**Figure 2. Recommended Bypass Capacitors**

## +3.3 V DIGITAL SIGNALS AND POWER DISTRIBUTION

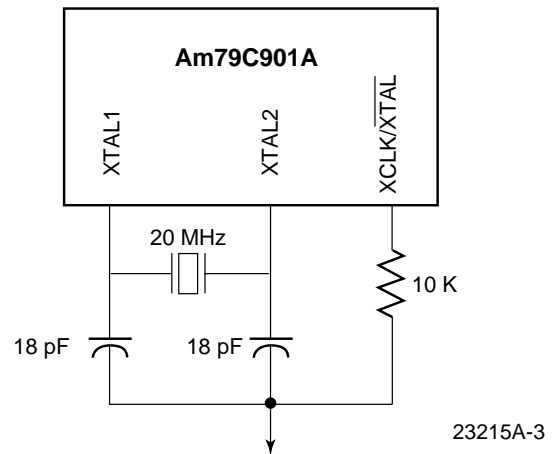
If a plane is used for +3.3 V power distribution, care should be given to avoid the routing of digital signals across the power plane boundaries, particularly in the area of the above pins. Generally, any digital signal traces traversing the +3.3 V plane boundary should be routed away from the above pins and should have small capacitors between the planes close to the trace to ensure a localized signal return path.

## CRYSTAL OSCILLATOR

The HomePHY device has an on-chip oscillator circuit allowing the use of an external 20-MHz crystal connected to the XTAL1 and XTAL2 pins with the XCLK/XTAL pin tied LOW.

Alternatively, a 60-MHz clock source can also be used to drive XTAL1. In this case, the XTAL2 pin must be left unconnected, with XCLK/XTAL tied HIGH.

The crystal should meet the 50 ppm, 18 pF standard load capacitors (or 33 pF), and 0.005% tolerance at 20 MHz.



**Figure 3. Crystal Clock Source**

Two crystal suppliers are listed below:

- Ecliptik Corporation: [www.ecliptik.com](http://www.ecliptik.com)
- Epson Corporation: [www.epson.com](http://www.epson.com).

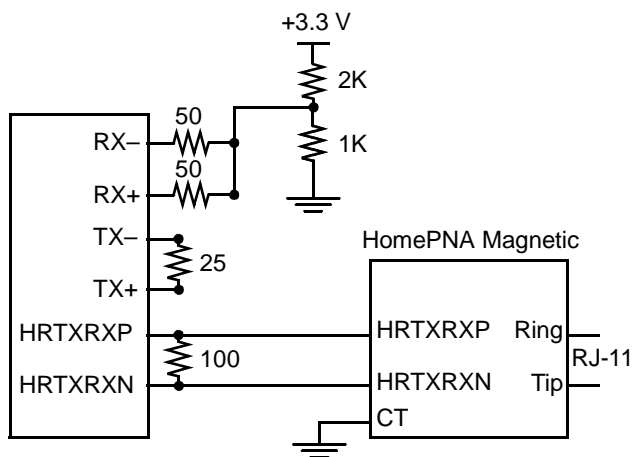
## MAGNETIC INTERFACE

The Am79C901A consists of an integrated 1 Mbps HomePNA PHY and a 10BASE-T Ethernet PHY. The designer may choose to implement the physical layer functionality of the Am79C901A in one of three possible ways: HomePNA only, 10BASE-T only, or HomePNA and 10BASE-T.

**Note:** All resistors must be of 1% or better accuracy.

### ■ HomePNA PHY Only

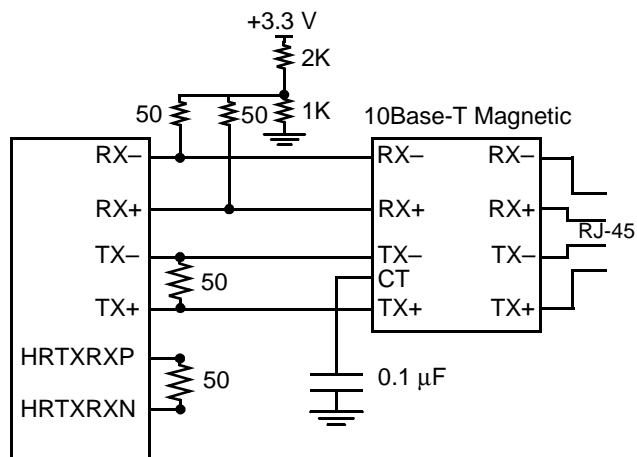
The 1 Mbps HomePNA PHY should be terminated with 100  $\Omega$  between the Am79C901A and a HomePNA-compatible magnetic. If only the 1 Mbps HomePNA PHY is to be used, the 10BASE-T transmit and receive signals should still be resistively terminated to reduce noise injected into the HomePNA analog section. Refer to Figure 4 for the proper termination of the HRTXRXN, TX $\pm$ , and RX $\pm$  differential signals.



**Figure 4. Magnetic Interface Using HomePNA-Only PHY**

### ■ 10BASE-T PHY Only

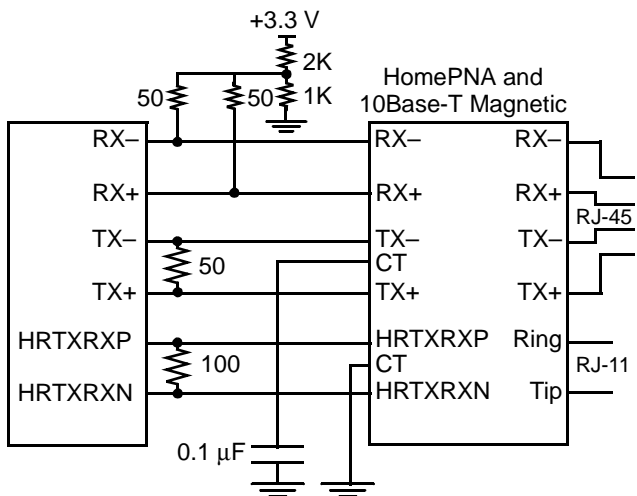
The 10BASE-T PHY transmit pair must be terminated with 50  $\Omega$ , and the receive pair must be terminated with 100  $\Omega$  (two 50  $\Omega$  resistors). The receive pair is also biased to 1.1 V using a 2 k $\Omega$ /1 k $\Omega$  voltage divider circuit connected between the two 50  $\Omega$  resistors. The 10BASE-T PHY also requires a magnetic with a 1:1.414 transmit turns ratio and a 1:1 receive turns ratio. Refer to Figure 5 for the proper termination of the HRTXRXN, TX $\pm$ , and RX $\pm$  differential signals.



**Figure 5. Magnetic Interface Using 10BASE-T-Only PHY**

### ■ HomePNA and 10BASE-T PHY

While it is not possible to use both the HomePNA PHY and 10BASE-T PHY simultaneously, the system's station management entity can selectively choose which PHY to use as needed. This is possible by using managed mode and choosing between PHY's by toggling bit 10 of the HPR0 and TBR0 registers. Refer to Figure 6 for the proper termination of the HRTXRXN, TX $\pm$ , and RX $\pm$  differential signals.



**Figure 6. Magnetic Interface Using HomePNA and 10BASE-T PHY's**

## MAGNETICS VENDORS

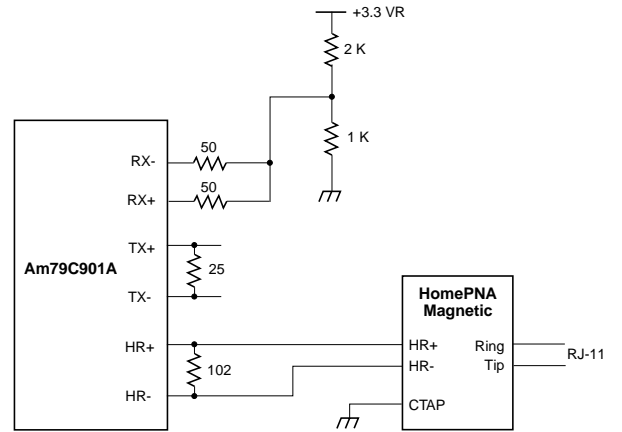
According to the data sheets from the vendors below, the following surface mount magnetics should work in 1 Mbps HomePNA and 10BASE-T applications. Only a few part numbers for each vendor are listed for brevity, and most vendors offer a number of suitable devices. This is not meant to be a comprehensive list. Magnetics vendors change their product offering very frequently, so please contact the vendor directly before finalizing any design.

**Table 2. Magnetics Vendors**

Magnetics Vendor	Part No. of HomePNA-Only Magnetic	Part No. of 10BASE-T and HomePNA Integrated Magnetic	Web URL
APC	APC76085	APC76160	<a href="http://www.apcisdn.com">www.apcisdn.com</a>
Belfuse	RS556-5000-05	RS556-5000-06	<a href="http://www.belfuse.com">www.belfuse.com</a>
Midcom (Nanopulse)	7074-37	7084-30	<a href="http://www.midcom-inc.com">www.midcom-inc.com</a>
PCA Electronics, Inc.	EPB5035G	EPB5036G	<a href="http://www.pcainc.com">www.pcainc.com</a>
Pulse Engineering	B6003L	B6006L	<a href="http://www.pulseeng.com">www.pulseeng.com</a>
YCL	FH166911	FH166901	<a href="http://www.ycl.com">www.ycl.com</a>

### HomePNA-ONLY MODE (NO 10BASE-T PORT CONNECTED)

If the internal 10BASE-T port is not utilized, appropriate 10BASE-T signals (TX± and RX±) should be resistively terminated. This termination helps to reduce the noise injected by the Ethernet link pulse back into the HomePNA analog section. In addition, “a HomePNA-only” magnetic should be used to prevent interference from the floating 10BASE-T magnetic section (if both 10BASE-T/HomePNA magnetics are used). It is also beneficial, but not mandatory, to disable the transmission of 10BASE-T link pulses by setting bit 12 of the TBR17 register. See Figure 7 for more details.



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**Figure 7. Recommended Termination for HomePNA-Only Mode**

## DEVICE PLACEMENT AND ROUTING

The Am79C901A HomePHY device pin location has been designed to allow for minimum length signal routing. Refer to the HomePHY evaluation board layout diagram (HomePHY-1\_mii\_1\_PCB.pdf) for an example of component placement. Short signal traces reduce the capacitive loading caused by the signal trace and noise from adjacent signals. It is also recommended to place the integrated magnetics near the RJ-11 connector for EMI prevention.

## PCB LAYOUT RECOMMENDATIONS

The following are some general guidelines that will ensure success of the HomePHY design.

- Component placement should be carefully considered in order to optimize and shorten the routing traces.
- Keep the decoupling capacitors as close as possible to the power pins, and provide enough capacitors for the analog power pins. A good rule of thumb is to have a 0.1  $\mu\text{F}$  capacitor for each analog power pin unless they are very close together.
- The traces of differential signal pairs from the device side to the magnetic side, such as TX/RX for 10BASE-T, and HRTXRXP and HRTXRXN for HomePNA, should be maintained at an equal length. They should also be on the same side of the PCB to minimize impedance mismatch.
- A 10 to 15 mils trace thickness is recommended with 8 to 10 mils space to maintain a 50- $\Omega$  impedance of the signal pair.
- Keep digital signals or other signals away from the differential signals to prevent any noise from injecting into the differential pairs.
- Keep the 20-MHz clock source away from the HomePNA differential signal pair to prevent coupling to the differential pair.
- Do not separate digital and analog ground planes. Keep them the same to maintain the same current return path.

## EMI AND FCC

Since the Am79C901A device utilizes the telephone or Ethernet cable, careful design techniques must be considered in order to ensure first-pass FCC requirement, Part 68 and Class B.

**Note:** For Part 68, not all telecommunication requirements need to be tested since the HomePHY only transfers data and has no voice support like a modem. Consult with your FCC testing house for more details.

- When routing the HomePNA pair with magnetics close to the RJ-11 port, follow Part 68 requirements. That is, there should be no power plane around the area, and all tip and ring traces must have enough clearance (at least 50 mils) to isolate potential power surges.
- Keep the AC ground return paths close to the signal paths. In AMD's design, the analog and digital grounds are on the same plane.
- Isolated planes (if any, i.e., +5 V to +3.3 V plane) should be avoided by capacitively coupling the planes together to prevent any discontinuities and provide a signal return path across the isolated planes. The capacitor used to tie the +3.3 V and +5 V planes together should be a good bypass capacitor (0.01  $\mu\text{F}$  or 0.1  $\mu\text{F}$ ), and it should be placed close to the center point of the signals that cross the boundary or on each side of the group.
- The chassis ground plane that is connected to the bracket/chassis should be isolated from the signal plane to prevent any radiation from leaking through and causing FCC requirements failure.

Additional information about PCB layout and how to reduce EMI may be found at:

<http://www.amd.com/products/npd/techdocs/techdocs.html>.

## CONCLUSION

Following the guidelines described in this document and referring to the evaluation board schematic and layout diagram will help ensure first-pass success. Contact your AMD local field applications and sales engineers for samples, schematics, and PCB layout reviews.

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