



# **AMD-761™ System Controller Revision Guide**

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## **Revision History**

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<b>Date</b>	<b>Rev</b>	<b>Description</b>
October 2002	F	Added errata #55
February 2002	E	Added errata #54
September 2001	D	Added B4 silicon information
May 2001	C	Initial public release

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# AMD-761™ System Controller Revision Guide

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The purpose of the *AMD-761™ System Controller Revision Guide* is to communicate updated product information on the AMD-761™ system controller to designers of computer systems and software developers. This guide consists of four major sections:

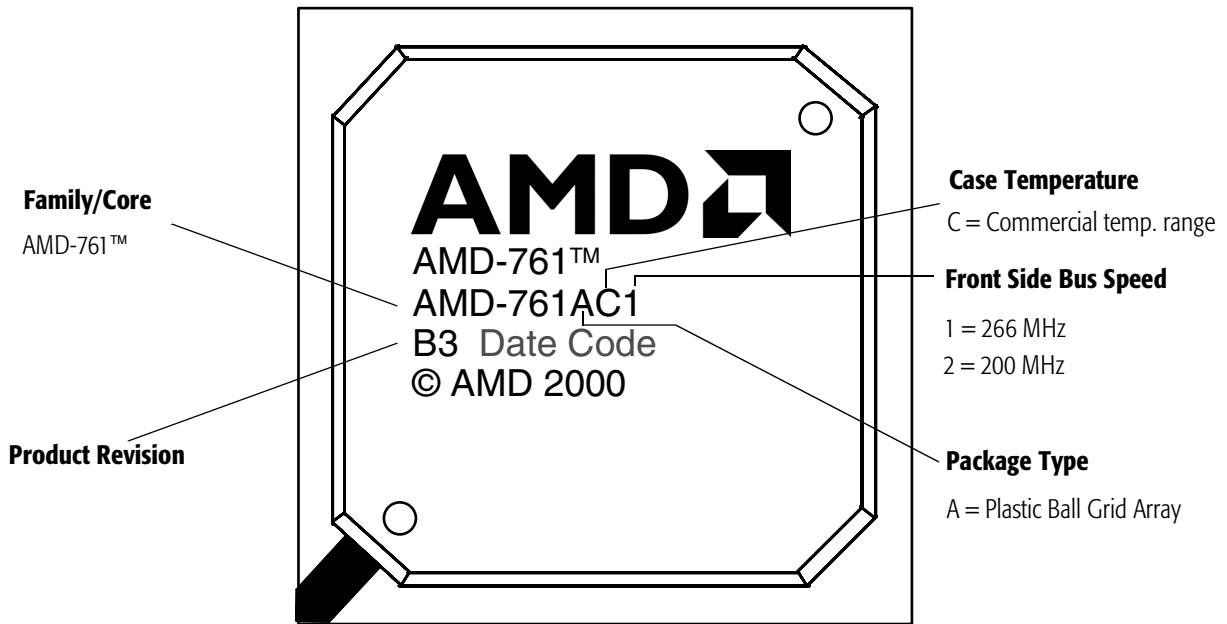
- **Product Marking Identification:** This section, which starts on page 5, provides product types, product revisions, OPNs (ordering part numbers), and product marking information.
- **Product Errata:** This section, which starts on page 6, provides a detailed description of product errata, including potential effects on system operation and suggested workarounds. An erratum is defined as a deviation from the product's specification. A product errata may cause the behavior of the AMD-761 system controller to deviate from the published specifications.
- **Revision Determination:** This section, which starts on page 17, describes the registers that identify the current revision of the part.
- **Technical and Documentation Support:** This section, which starts on page 18, provides a listing of available technical support resources.

## Revision Guide Policy

Occasionally, AMD identifies deviations from or changes to the specification of the AMD-761 system controller. These changes are documented in the *AMD-761™ System Controller Revision Guide* as errata. Descriptions are written to assist system and software designers in using the AMD-761 system controller, and corrections to AMD's documentation on the AMD-761 system controller are included. This release documents currently characterized product errata.

# 1 Product Marking Identification

## 1.1 Production Marking



**Table 1. Valid Combinations for Ordering Parts**

OPN	Package Type	Operating Voltage	Case Temperature
AMD-761AC1	569-pin PBGA	2.375V—2.625V	85°C
<b>Note:</b> Valid combinations are configurations that are or will be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.			

## 2 Product Errata

This section documents AMD-761 system controller product errata. A unique tracking number for each erratum has been assigned within this document for user convenience in tracking the errata within specific revision levels. Table 2 cross-references the revisions of the controller to each erratum. An “X” indicates that the erratum applies to the revision. The absence of an “X” indicates that the erratum does not apply to the revision.

*Note:* There can be missing errata numbers. Errata that have been resolved from early revisions of the controller have been deleted, and errata that have been reconsidered may have been deleted or renumbered.

**Table 2. Cross-Reference of Product Revision to Errata**

Erratum Number and Description	Revision				
	B0	B1	B2	B3	B4
4 GART Requestors Do Not Work with TLB Caches Off	X	X	X	X	X
7 AGP Ordering Problem	X	X			
31 External PCI Master to APC Target Resulted in an Extra Null Data Phase	X	X	X	X	X
37 Idle Cycle Limit Field Must be Non-Zero or ECC Scrubbing May Cause Failure	X	X	X	X	X
38 AGP Differential Strobe Inputs Must Be Controlled by AGP Command Register	X				
39 Writing to AGP Compensation Bypass Register Locks BIU Arbitration	X	X	X	X	X
41 AGP Failures During ACPI C1, C2 Power Management States	X	X			
43 Voltage Sensitivity on VDD_CORE Causes AGP Failures	X	X	X	X	X
44 SYSCLK/AGPCLK Clock Skew Causes AGP-2X Failures	X	X			
45 Timing Problem Prevents AGP Fast Writes Operation	X	X			
46 Setup Violation on AGP SBA Pins	X	X			
47 Extra Pulse on AGP Strobes	X	X			
48 Memory Read Modify Write Data Corruption from AGP When Entering Self-Refresh in C2/C3 Power Management States	X	X	X	X	X
49 Failure to Reconnect Following Exit From Self-Refresh			X		
51 Missed Refreshes When Burst Refresh is Enabled	X	X	X	X	X
52 False ACK When Switching from Two-Bit Time to Four-Bit Time Mode	X	X	X	X	X
53 Data Corruption Due to Switching Noise on Front-side Bus	X	X	X	X	X
54 AGP Compensation Cycle Causes Data Corruption During AGP Writes	X	X	X	X	X
55 System Hangs During Prefetches Into 640K-1M Segment	X	X	X	X	X

## 4 GART Requestors Do Not Work with TLB Caches Off

**Products Affected.** B0, B1, B2, B3, B4

**Description.** Only partial support exists for the mode where GART TLB caches are disabled. The ability to disable GART caches was intended primarily for performance evaluation, and is not supported.

**Potential Effect on System.** None

**Suggested Workaround.** The BIOS should set BAR1: Offset 02h bit 2.

**Resolution Status.** None required, proper operation.

## 7 AGP Ordering Problem

**Products Affected.** B0, B1

**Description.** A processor write to memory followed immediately by an AGP read may fail.

**Potential Effect on System.** It is extremely unlikely that this problem will occur in a single-processor system. Consider the two following scenarios:

- 1a) The processor writes data to memory, but the write waits in the AMD-761 system controller write queue for read traffic.
- 1b) The processor writes the associated flag in the AGP device.
- 1c) The AGP device writes to the same address in memory.
- 1d) The processor write completes, overwriting the AGP data memory.
- 2a) The processor writes data to memory, but the write waits in the AMD-761 system controller write queue for read traffic.
- 2b) The processor writes the associated flag in the AGP device.
- 2c) The AGP device reads memory getting incorrect data.
- 2d) The processor write completes.

Both scenario one and two are bugs. The timing of both makes them extremely unlikely to occur in a single processor system.

**Suggested Workaround.** The workaround requires that the write queue get flushed prior to steps 1B and 2B above. This is accomplished by performing a read of the last data written to memory prior to step 1B or 2B, which forces the queue to be flushed, thus ensuring coherency on the subsequent write or read by the AGP master.

**Resolution Status.** Fixed in revision B2.

### 31 External PCI Master to APC Target Resulted in an Extra Null Data Phase

**Products Affected.** B0, B1, B2, B3, B4

**Description.** A doubleword write from an external PCI bus master to external APC target (AGP device) results in an extra null data phase.

**Potential Effect on System.** No observed effect, except an additional null data phase. This will not be noticeable because it is only a 15 nS data phase, and PCI to APC writes are rare in most systems.

**Suggested Workaround.** None required, normal operation.

**Resolution Status.** None.

### 37 Idle Cycle Limit Field Must be Non-Zero or ECC Scrubbing May Cause Failure

**Products Affected.** B0, B1, B2, B3, B4

**Description.** The Idle Cycle Limit parameter defines how many idle cycles may occur before the memory controller will automatically precharge the open page. The AMD-761 system controller allows this field to be any binary value from 000b to 111b but a setting of 000b while ECC scrubbing is enabled can cause data corruption on the AMD system bus if a bypassed read occurs following the scrub cycle.

**Potential Effect on System.** Possible data corruption on the AMD system bus during bypassed memory read cycles.

**Suggested Workaround.** Always set the Idle\_Cyc\_Limit field in Device 0:F0:0x54 (DRAM Timing) to a non-zero value. The recommended safe configuration is 8 clocks which is a setting of 001b.

**Resolution Status.** Fix planned for a future silicon revision.

### 38 AGP Differential Strobe Inputs Must Be Controlled by AGP Command Register

**Products Affected.** B0

**Description.** When operating in AGP-4X mode the AGP strobe pins must be configured as differential inputs. Microsoft® Windows® and the software application determine whether to operate in AGP-4X mode, but the AGP pin configuration is currently controlled by a configuration register visible only to BIOS. This needs to be controlled directly by the AGP rate field in the AGP Command Register that gets written when the operating system determines which AGP speed to enable (1x, 2X, 4X).

**Potential Effect on System.** Improper configuration of the AGP strobe inputs could result in failures in 4X mode when the AGP card is driving the strobes to the AMD-761 system controller.

**Suggested Workaround.** A workaround in BIOS will be required in this silicon revision. This workaround allows the user to setup the AGP mode.

**Resolution Status.** Fixed in revision B1.

## 39 Writing to AGP Compensation Bypass Register Locks BIU Arbitration

**Products Affected.** B0, B1, B2, B3, B4

**Description.** In test conditions at low speeds (~10 MHz) the bus interface arbitration can potentially lock up when the processor writes to the AGP Compensation Bypass Register (Dev 0:F0:0xB8) when illegal (zero) values are programmed in the BIU Control Register (Dev 0:F0:0x60).

**Potential Effect on System.** The system may hard lock if incorrect values are programmed in the BIU Control Register. These fields include the following (Dev 0:F0:0x60):

- Xca\_Probe\_Cnt, bits [27:25]
- Xca\_Rd\_Cnt, bits [24:22]
- Xca\_Wr\_Cnt, bits [21:19]

**Suggested Workaround.** This scenario can be avoided by writing non-zero values to the Xca\_Probe\_Cnt, Xca\_Rd\_Cnt, and Xca\_Wr\_Cnt fields in the BIU Control Register (Dev 0:F0:0x60, bits [27:19]). A value of 0x6 is recommended in each of these fields.

**Resolution Status.** None.

## 41 AGP Failures During ACPI C1, C2 Power Management States

**Products Affected.** B0, B1

**Description.** Failures can occur during AGP reads if the AMD-761 system controller simultaneously attempts to enter either the C1 or C2 ACPI states and the system controller is programmed to perform a disconnect on Halt or Stop Grant. The failure occurs when a Halt or Stop Grant special cycle is generated by the processor while AGP SBA cycles are in progress, such as would be the case during the C1 or C2 states or when clock throttling is enabled. Disconnect on Stop Grant operation is functional for the S1 and S3 states because the peripheral driver places the device in the D3 (sleep) state before STPCLK# is asserted to the processor.

**Potential Effect on System.** Data corruption or failure to resume properly from C1 or C2 state.

**Suggested Workaround.** The following steps should be taken as a workaround for this problem:

1. The Disconnect on Halt feature should be disabled (bit 18 of the BIU Control Register, Dev 0:F0:0x60).
2. The BIOS must not report C2 or C3 capability in the ACPI table.
3. Clock throttling must be disabled.

Note that ACPI S1 and S3 states are still functional. The Disconnect on Stop Grant bit must be set if the system requires support of the S1 or S3 states (set bit 17 of the BIU Control Register, Dev 0:F0:0x60).

**Resolution Status.** Fixed in revision B2.

### 43 Voltage Sensitivity on VDD\_CORE Causes AGP Failures

**Products Affected.** B0, B1, B2, B3, B4

**Description.** A timing issue has been identified in the internal AGP logic. The resulting failure has been observed in 3DMark™ 2000 benchmarks as well as various games running with AGP. Most failures are seen in systems running with AGP-4X mode but failures have also been observed in 2X mode.

**Potential Effect on System.** Failures typically result in video corruption or system hard locks.

**Suggested Workaround.** Raising the AMD-761 system controller core voltage (VDD\_CORE) to 2.65V +/- 3% will correct this problem.

**Resolution Status.** Fix planned for a future silicon revision.

### 44 SYCLK/AGPCLK Clock Skew Causes AGP-2X Failures

**Products Affected.** B0, B1

**Description.** The specified clock skew between the SYCLK and AGPCLK pins is < 500 pS, but the AMD-761 system controller requires between 1–1.5 nS for proper operation.

**Potential Effect on System.** AGP failures such as video corruption and hard locks, when operating in AGP-2X mode.

**Suggested Workaround.** The motherboard must be modified to ensure that the AGPCLK signal is skewed between 1–1.5 nS from the SYCLK signal.

**Resolution Status.** Fixed in revision B2.

### 45 Timing Problem Prevents AGP Fast Writes Operation

**Products Affected.** B0, B1

**Description.** A timing problem internal to the AMD-761 system controller prevents proper operation of AGP Fast Writes. The problem is seen as a one clock delay in the ADSTB[1] signal during fast writes.

**Potential Effect on System.** Failures when AGP Fast Writes are enabled, resulting in AGP data corruption and system hard locks.

**Suggested Workaround.** AGP Fast Writes must be disabled by BIOS in the AGP Dynamic Compensation Register by writing a zero to bit 7 (Dev 0:F0:0xB4). This will cause the FW bit to be cleared in the AGP Status Register (Dev 0:F0:0xA4, bit 4).

**Resolution Status.** Fixed in revision B2.

## 46 Setup Violation on AGP SBA Pins

**Products Affected.** B0, B1

**Description.** A setup violation exists on some AGP Sideband Address pins, the worst is the SBA[6] pin.

**Potential Effect on System.** Failures when operating with AGP sideband addressing, including video corruption and system hard locks.

**Suggested Workaround.** Sideband addressing must not be used by the AGP card, the card should be programmed to operate only in PIPE operation mode.

**Resolution Status.** Fixed in revision B2.

## 47 Extra Pulse on AGP Strobes

**Products Affected.** B0, B1

**Description.** In some circumstances an additional pulse has been observed on the AGP strobe pins (ADSTB[1:0], ADSTB[1:0]#).

**Potential Effect on System.** Video corruption and hard lock failures when AGP writes are implemented by the AGP card.

1. An extra strobe pulse can be seen following AGP reads. This pulse does not affect the AMD-761 system controller but may affect some AGP cards that do not qualify the strobe signals.
2. The AMD-761 system controller's AGP read FIFO is corrupted when an AGP write (from the AGP card) occurs immediately after an AGP read, due to the additional pulse. This occurs only on cards that perform AGP writes to memory.

**Suggested Workaround.** AGP cards must not be configured by their respective drivers to perform AGP write cycles for proper operation.

**Resolution Status.** Fixed in revision B2.

## 48 Memory Read Modify Write Data Corruption from AGP When Entering Self-Refresh in C2/C3 Power Management States

**Products Affected.** B0, B1, B2, B3, B4

**Description.** A memory read-modify-write initiated on behalf of AGP results in corrupted data when the sequence is interrupted by a request to enter self-refresh mode by the AMD-761 system controller power management logic. The problem is a result of entering power management modes simultaneous with AGP traffic.

**Potential Effect on System.** Data corruption when the system exits self-refresh. The read-modify-write sequence is restarted after exiting self-refresh mode but it is to the wrong memory address.

**Suggested Workaround.** The problem can be avoided by disallowing AGP traffic simultaneous with entering power management states. The following steps should be taken as a workaround for this problem:

1. The BIOS must not report C2 or C3 capability in the ACPI table.
2. Clock throttling must be disabled.

Note that ACPI S1 and S3 states are still functional. The Disconnect on Stop Grant bit must be set if the system requires support of the S1 or S3 states (set bit 17 of the BIU Control Register, Dev 0:F0:0x60).

**Resolution Status.** Fix planned for a future silicon revision.

## 49 Failure to Reconnect Following Exit From Self-Refresh

**Products Affected.** B2 (Only)

**Description.** A logic fault in the DDR PDL calibration logic prevents the power management state machine from properly reconnecting the AMD system bus upon exiting self-refresh in ACPI C2, C3, S1, and S3 power management states. The calibration logic fails to properly acknowledge the exit from self-refresh, which locks up the disconnect state machine.

**Potential Effect on System.** The system hangs when exiting self-refresh during any of the stated ACPI power management sequences.

**Suggested Workaround.** Implement the following modified BIOS algorithm for DDR PDL calibration.

- a. Immediately after reset, set the Act\_Dly\_Inh bit in the DDR PDL Calibration Register in Dev 0:F1:0x40. The proper value to write to this register is 0x1X (lower nibble is still defined by system implementor). This bit should be set as soon as possible after reset to prevent any potential conflicts between the calibration logic and the power management state machines.
- b. Perform the normal initialization of the SW\_Cal\_Dly field in each of the 18 DDR PDL configuration registers in Dev 0:F1:0x44 through 0x8B. The recommended values are 0x69 for 100-MHz frontside bus, or 0x6B for 133-MHz bus. This initialization can be done at the same time it is currently done in the system BIOS, there are no new special requirements.
- c. Perform a single software-initiated calibration by setting the SW\_Recal bit in the DDR PDL Calibration Control Register in Dev 0:F1:0x40. This is accomplished by setting bit 7 of this register and waiting for the bit to be cleared automatically by the AMD-761 system controller. The AMD-761 system controller clears the bit when the calibration is completed. Note that the correct value to write is 0x9X (lower nibble defined by system designer).
- d. Copy the Cal\_Dly value to the Act\_Dly for all eighteen PDLs. This requires copying the value from bits [15:8] to bits [7:0] of each register from Dev 0:F1:0x44 through Dev 0:F1:0x88.
- e. Next, the PDLs must be updated with the Act\_Dly values just copied from Cal\_Dly. This is accomplished by writing to the Use\_Act\_Dly bit in the same register. This forces the values from the calibration logic to be written to the PDLs. The correct value to write to the DDR PDL Calibration Control Register (Dev 0:F1:0x40) is 0x5X. Afterwards, this bit should be reset by writing a 01X to this register.

Following power on reset, steps a through e above should be implemented before accessing the DDR memory subsystem.

Following exit from S3, steps c through e above should be implemented before setting the STR[1:0] bits in Dev 0:F0:0x58.

**Resolution Status.** Fix planned for a future silicon revision.

## 51 Missed Refreshes When Burst Refresh is Enabled

**Products Affected.** B0, B1, B2, B3, B4

**Description.** The DRAM refresh period may be violated in some cases when the burst refresh feature is enabled in the DRAM Mode/Status Register. The burst refresh feature allows multiple refresh requests to be queued up before holding off any memory requests, but the AMD-761 system controller may violate the maximum refresh rate under very heavy loading conditions. This occurs only when burst refresh is enabled.

**Potential Effect on System.** Data corruption or hard locks when running with burst refresh enabled. This has been observed only in very harsh memory testing, and has never been observed when running any Windows operating systems.

**Suggested Workaround.** Disable the burst refresh feature by writing a zero to bit 20 of the DRAM Mode/Status Register (Dev 0:F0:0x58).

**Resolution Status.** Fix planned for a future silicon revision.

## 52 False ACK When Switching from Two-Bit Time to Four-Bit Time Mode

**Products Affected.** B0, B1, B2, B3, B4

**Description.** The P0\_2BitPF (Two Bit Times Per Frame Enable) bit in the Extended BIU Control Register is specified to be set when running with an AMD Athlon™ processor, or cleared when running with an Alpha™ processor. Setting this bit (enabling 2-bit times per frame), and subsequently clearing the bit, can cause the AMD-761 system controller to return a false ACK to the processor, resulting in system failures.

Under normal conditions this bit should not be changed once it is initialized by the system BIOS. Changing the value of the bit from a zero to a one is considered normal operation and does not cause the failure.

**Potential Effect on System.** System may hard lock when changing the P0\_2BitPF bit in the Extended BIU Control Register from one to zero.

**Suggested Workaround.** Do not change the “Two Bit Times Per Frame Enable” bit (P0\_2BitPF, bit 3 of Dev 0:F0:0x44) from a one to a zero. BIOS should set this bit only when running with an AMD Athlon processor, and then not change the value. The bit should be left cleared when running with an Alpha processor.

**Resolution Status.** None required.

## 53 Data Corruption Due to Switching Noise on Front-side Bus

**Products Affected.** B0, B1, B2, B3, B4

**Description.** InClk signals are corrupted by noise induced by data transitions on the front-side bus, resulting in functional failures. Glitches can be seen on the various InClk signals, especially with higher processor clock multipliers (>10X FID), resulting in data corruption at the processor. This noise is resultant of inductance in the bond wires of the AMD-761 system controller wirebond package.

**Potential Effect on System.** Typical functional failures result in a system hang.

**Suggested Workaround.** The motherboard should be designed to incorporate special low-pass filters on the SDATAINCLK[3:0]# pins and must also adhere to specific board routing rules. The filter circuitry and routing rules are specified in the latest revision of the motherboard reference design files (schematics, gerbers, etc.) for the AMD-760™ chipset. For detailed background and solution information, refer to the following application note:

*Analysis of Crosstalk Noise on the System Bus INCLK Signals in the AMD-761™ System Controller, order# 24748A.*

Please contact your local AMD specialist for details.

**Resolution Status.** None.

## 54 AGP Compensation Cycle Causes Data Corruption During AGP Writes

**Products Affected.** B0, B1, B2, B3, B4

**Description.** A bug in the AGP compensation logic can cause the AMD-761 system controller to drive the AGP data bus while the AGP card has been granted the bus by the AGP arbiter. This occurs only during AGP write cycles and can result in data corruption on the AGP data bus.

**Potential Effect on System.** Data written to main memory by the AGP card can be corrupted when AGP compensation is enabled in the AMD-761 system controller. The AGP compensation circuitry is only enabled when configured for 1.5V signaling.

**Suggested Workaround.** The suggested workaround for cards that use 1.5V signaling is to configure the card's AGP driver to not allow the AGP card to perform AGP writes.

**Resolution Status.** No fix planned.

## 55 System Hangs During Prefetches Into 640K-1M Segment

**Products Affected.** B0, B1, B2, B3, B4

**Description.** A system hang occurs when a PCI bus master prefetches into the 640K-1M region while Dev 0:F0:0x84, bit 4 (EV6\_Mode) is set and VGA is enabled (Dev 1:F0:0x3C, bit 19). The AMD-761 system controller will forward writes to this region to the AGP card but reads are incorrectly terminated (accepted via DEVSEL# assertion but not forwarded to AGP or DRAM).

**Potential Effect on System.** System hangs when a PCI bus master prefetches into the 640K-1M region.

**Suggested Workaround.** BIOS should reserve the area directly below A0000h to prevent prefetching into the 640K-1M region.

**Resolution Status.** No fix planned.

### 3 Revision Determination

Table 3 summarizes the AMD-761 system controller configuration register offsets, devices, default values after reset, and access types. Access types are indicated as follows:

RW – Read/Write

RO – Read Only

**Table 3. Function 0, Device 0 Configuration Registers**

Offset	Cache Control	Reset	Access
01h–00h	Vendor ID (AMD)	1022h	RO
03h–02h	Device ID Single-Processor Device	700Eh	RO
08h	Revision ID	nn *	RO
<b>Note:</b>			
* nn changes for each device revision. For example, 00h = Revision A0; 01h = Revision A1; 10h = Revision B0; 21h = Revision C1; 25h = Revision C5 etc.			

#### Vendor ID Device 0 Offset 01h–00h

Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
Vendor ID															

Reset 0 0 0 1 0 0 0 0 0 0 1 0 0 0 1 0

This read-only value is defined as 1022h.

#### Device ID Device 0 Offset 03h–02h

Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
Device ID															

Reset 0 1 1 1 0 0 0 0 0 0 0 0 1 1 1 0

This read-only value of 700Eh represents the AMD-761 system controller single-processor device.

#### Revision ID Device 0 Offset 08h

Bit 7	6	5	4	3	2	1	Bit 0
AMD-761™ System Controller Chip Revision and Stepping Code							

Reset — — — — — — — —

#### Bits 7–0

**AMD-761 System Controller Revision Code (RO)** – The most-significant nibble indicates the die revision and the least-significant nibble represents the stepping. (For example, 00h = Revision A0, 01h = Revision A1, 10h = Revision B0, 21h = Revision C1, 25h = Revision C5, etc.)

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## 4 Technical and Documentation Support

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The following documents provide additional information regarding the operation of the AMD-761 system controller:

- *AMD-761™ System Controller Data Sheet*, order# 24088
- *AMD-761™ System Controller Software/BIOS Design Guide*, order# 24081
- *AMD-766™ Peripheral Bus Controller Data Sheet*, order# 23167
- *AMD Athlon™ System Bus Specification*, order# 21902
- *AMD Athlon™ Processor BIOS, Software, and Debug Tools Developers Guide*, order# 21656
- *AMD Athlon™ Processor Data Sheet*, order# 21016
- *Analysis of Crosstalk Noise on the System Bus INCLK Signals in the AMD-761™ System Controller*, order# 24748A

For the latest updates, refer to [www.amd.com](http://www.amd.com) and download the appropriate files. For documents under NDA, please contact your local sales representative for updates.