SLB INTERSECT® PERFORMANCE LEADERSHIP
RESERVOIR ENGINEERING SIMULATOR

Powered by 4th Gen AMD EPYC™ Processors

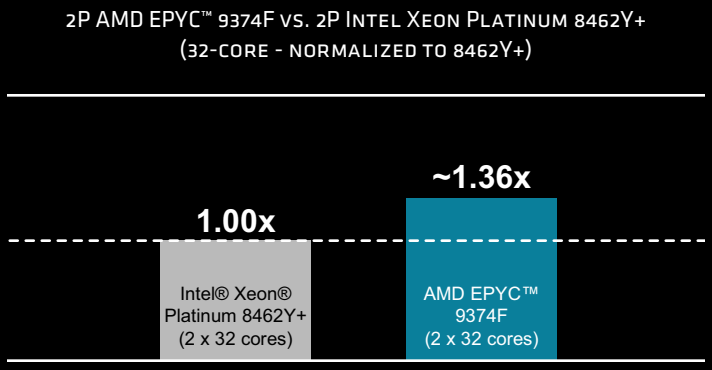
June 2023

AT A GLANCE

A 2P system powered by 32-core 4th Gen AMD EPYC™ 9374F CPUs technology demonstrate outstanding per-core competitive performance uplifts on SLB INTERSECT® versus a 2P system powered by 32-core Intel® Xeon® Platinum 8462Y+ CPUs.

PERFORMANCE HIGHLIGHTS

A single 2P 32-core 4th Gen AMD EPYC 9374F system demonstrates a ~1.36x uplift vs. a single 2P Intel® Xeon® Platinum 8462Y+ system on SLB INTERSECT.



KEY TAKEAWAYS

A 2P server powered by 4th Gen AMD EPYC 9374F (32-core) processors delivered an average SLB INTERSECT performance uplift of ~1.36x compared to a 2P server powered by Intel Xeon Platinum 8462Y+ (32-core) processors.

4th Gen AMD EPYC 9004 processors are available in 1P and 2P configurations and feature:

- Up to 384 MB L3 cache.
- Up to 4 links of Gen 3 Infinity Fabric™ at up to 32 Gbps.
- 12 memory channels that support up to 6TB of DDR5-4800 memory.
- Support for PCIe® Gen 5 at up to 32 Gbps.
- AVX-512 instruction support for enhanced HPC and ML performance.
- AMD Infinity Guard technology to defend your data.[2]

IN THIS BRIEF

SYSTEM CONFIGURATION

AMD SYSTEM CONFIGURATION	
CPUs	2 x AMD EPYC 9374F
Frequency: Base | Boost[3]	3.85 GHz | 4.10 GHz (up to)
Cores	32 cores/socket (64 threads)
L3 Cache	256 MB per CPU
Memory	1.5 TB (24x) Dual-Rank DDR5 4800 64 GB DIMMs 1 DPC
NIC	25 Gb Ethernet CCX512-A ConnectX-5 (fw 16.35.2000)
InfiniBand	200 Gb HDR ConnectX-6 VPI (fw 20.35.2000)
Storage: OS | Data	Samsung MZQL21T9HCJR-00A07 1.92 TB
BIOS Version	1007D
BIOS Settings	SMT=OFF; NPS=4; Determinism=Power
OS	RHEL 8.7 (kernel 4.18.0-425.3.1.el8.x86_64)
OS Settings	amd_iommu=ON; iommu=pt; mitigations=off; clear caches; NUMA balancing=0; THP=on; CPU governor=Performance; C2 states=disabled

Table 1: AMD system configurations

INTEL SYSTEM CONFIGURATION	
CPUs	2x Intel Xeon Platinum 8462Y+
Frequency: Base | Boost	2.40 GHz | 4.10 GHz (up to)
Cores	32 cores per socket (64 threads)
L3 Cache	60 MB per CPU
Memory	1.0 TB (16x) Dual-Rank DDR5 4800 64 GB DIMMs 2 DPC
NIC	25 Gb Ethernet CCX512-A ConnectX-5 (fw 16.35.2000)
InfiniBand	200 Gb HDR ConnectX-6 VPI (fw 20.35.2000)
Storage: OS | Data	Samsung MZQL21T9HCJR-00A07 1.92 TB
BIOS Version	ESE110Q-1.10
BIOS Settings	Hyperthreading=Off, Profile = Maximum Performance
OS	RHEL 8.7 (kernel 4.18.0-425.3.1.el8.x86_64)
OS Settings	processor.max_cstate=1; intel_idle.max_cstate=0; iommu=pt mitigations=off; clear caches; NUMA Balancing=0; randomize_va_space 0; THP=ON; CPU Governor=Performance

Table 2: Intel system configurations

TEST METHODOLOGY

SLB's INTERSECT High Resolution Reservoir Simulator provide a standard set of benchmarks that represent typical usage and cover a range of problem sizes that can be used to evaluate the performance of different platforms running INTERSECT. The uplift is calculated as the ratio of the systems under test (*sut*) to the reference system (*ref*). In this Performance Brief, the Intel Xeon Platinum 8462Y is the *ref* and the 4th Gen AMD EPYC 9374F processor is the *sut*. The total amount of variability between individual runs was < 1%. The systems tested were configured as shown in Tables 1 and 2, above.

FOR ADDITIONAL INFORMATION

Please see the following additional resources for more information about 4th Gen AMD EPYC features, architecture, and available models:

- AMD EPYC™ 9004 Series Processors
- AMD EPYC™ Tuning Guides
- AMD EPYC™ Products

REFERENCES

1. "Technical Computing" or "Technical Computing Workloads" as defined by AMD can include: electronic design automation, computational fluid dynamics, finite element analysis, seismic tomography, weather forecasting, quantum mechanics, climate research, molecular modeling, or similar workloads. GD-204
2. AMD Infinity Guard features vary by EPYC™ Processor generations. Infinity Guard security features must be enabled by server OEMs and/or Cloud Service Providers to operate. Check with your OEM or provider to confirm support of these features. Learn more about Infinity Guard at https://www.amd.com/en/technologies/infinity-guard. GD-183
3. Maximum boost for AMD EPYC processors is the maximum frequency achievable by any single core on the processor under normal operating conditions for server systems. EPYC-18

AUTHORS

Alvaro Fernandez and Ashok Manikonda contributed to this Performance Brief.

RELATED LINKS

- SLB INTERSECT*
- SLB ECLIPSE*
- SLB Delfi Petrotechnical Suite*
- AMD EPYC™ Processors
- AMD EPYC Technical Briefs

**Links to third party sites are provided for convenience and unless explicitly stated, AMD is not responsible for the contents of such linked sites and no endorsement is implied.*

BOOST PERFORMANCE WITH AMD EPYC

AMD EPYC™ processors are built to handle large scientific and engineering datasets - ideal for compute-intensive modeling and advanced analysis techniques. Leveraged by many of the world's largest, most scalable data centers and supercomputers, AMD EPYC™ enables fast time-to-results for HPC.

"ZEN 4" CORE & SECURITY FEATURES

Support for up to:

- 96 physical cores, 192 threads
- 1152 MB of L3 cache per CPU
- 96 MB of L3 cache per CCD
- 6 TB of DDR5-4800 memory
- Up to 128 1P, up to 160 2P PCIe® Gen 5 lanes

Infinity Guard security features[2]

- Secure Boot
- Encrypted memory with SME

SLB INTERSECT

The INTERSECT simulator combines physics and performance in a fit-for-purpose reservoir simulator that enables fast modeling at scale and a new approach to reservoir simulation that employs robust physics to support better field development decisions. INTERSECT includes completion configurations for complex wells, advanced production controls in terms of reservoir coupling and flexible field management, and completion configurations for complex wells.