SLB ECLIPSE® WITH AMD 3D V-CACHE™ TECHNOLOGY
RESERVOIR ENGINEERING SIMULATOR

Powered by 4th Gen AMD EPYC™ Processors with AMD 3D V-Cache™ technology

June 2023

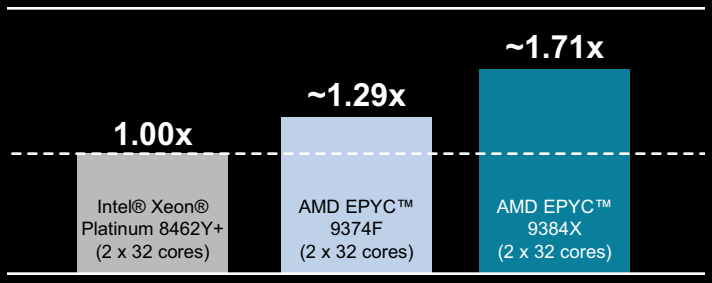
AT A GLANCE

2P systems powered by 32-core 4th Gen AMD EPYC™ processors with AMD 3D V-Cache™ technology demonstrate outstanding per-core competitive performance uplifts on SLB ECLIPSE®.

PERFORMANCE HIGHLIGHTS

A single 2P 32-core 4th Gen AMD EPYC 9384X system with AMD 3D V-Cache technology demonstrates a ~1.71 uplift vs. a single 2P 32-core Intel® Xeon® 8462Y+ system on SLB ECLIPSE.

2P AMD EPYC™ 9384X vs. 2P Intel Xeon Platinum 8462Y+
(32-core - normalized to 8462Y+)



KEY TAKEAWAYS

A 2P server powered by 4th Gen AMD EPYC 9384X processors delivered a SLB ECLIPSE competitive performance uplift of ~1.71x compared to a 2P server powered by a Intel Xeon Platinum 8462Y+ (32-core) processors. SLB ECLIPSE boundedness can take advantage of the large AMD 3D V-Cache sizes.

4th Gen AMD EPYC 9004X processors with AMD 3D V-Cache technology are available in 1P and 2P configurations and feature:

- Up to 1,152MB L3 cache vs. 384MB in standard 4th Gen AMD EPYC processors.
- Up to 4 links of Gen 3 Infinity Fabric™ at up to 32 Gbps.
- 12 memory channels that support up to 6TB of DDR5-4800 memory.
- Support for PCIe® Gen 5 at up to 32 Gbps.
- AVX-512 instruction support for enhanced HPC and ML performance.
- AMD Infinity Guard technology to defend your data.[2]

IN THIS BRIEF

AMD 3D V-CACHE™ TECHNOLOGY

Some AMD EPYC 9004 Series Processors include AMD 3D V-Cache™ die stacking technology that enables more efficient chiplet integration. AMD 3D Chiplet architecture stacks L3 cache tiles vertically to provide up to 96MB of L3 cache per die (and up to 1152 MB L3 Cache per socket) while still providing socket compatibility with standard AMD EPYC™ 9004 Series Processor models.

AMD EPYC 9004 Series Processors with AMD 3D V-Cache technology employ industry-leading logic stacking based on copper-to-copper hybrid bonding "bumpless" chip-on-wafer process to enable over 200X the interconnect densities of current 2D technologies (and over 15X the interconnect densities of other 3D technologies using solder bumps),[3,4] which can translate to lower latency, higher bandwidth, and greater power and thermal efficiencies.

SYSTEM CONFIGURATION

AMD SYSTEM CONFIGURATION		
CPUs	2 x AMD EPYC 9374F	2 x AMD EPYC 9384X
Frequency: Base | Boost[5]	3.85 GHz | 4.10 GHz (up to)	2.55 GHz | 3.70 GHz (up to)
Cores	32 cores/socket (64 threads)	
L3 Cache	256 MB per CPU	768 MB per CPU
Memory	1.5 TB (24x) Dual-Rank DDR5 4800 64 GB DIMMs 1 DPC	
NIC	25 Gb HDR Ethernet CCX512-A ConnectX-5 (fw 16.35.2000)	
InfiniBand	200 Gb ConnectX-6 VPI (fw 20.35.2000)	
Storage: OS | Data	Samsung MZQL21T9HCJR-00A07 1.92 TB	
BIOS Version	1007D	
BIOS Settings	SMT=OFF; NPS=4; Determinism=Power	
OS	RHEL 8.7 (kernel 4.18.0-425.3.1.el8.x86_64)	
OS Settings	amd_iommu=ON; iommu=pt; mitigations=off; clear caches; NUMA balancing=0; THP=on; CPU governor=Performance; C2 states=disabled	

Table 1: AMD system configurations

INTEL SYSTEM CONFIGURATION	
CPUs	2x Intel Xeon Platinum 8462Y+
Frequency: Base | Boost	2.40 GHz | 4.10 GHz (up to)
Cores	32 cores per socket (64 threads)
L3 Cache	60 MB per CPU
Memory	1.0 TB (16x) Dual-Rank DDR5 4800 64 GB DIMMs 2 DPC
NIC	25 Gb Ethernet CCX512-A ConnectX-5 (fw 16.35.2000)
InfiniBand	200 Gb HDR ConnectX-6 VPI (fw 20.35.2000)
Storage: OS | Data	Samsung MZQL21T9HCJR-00A07 1.92 TB
BIOS Version	ESE110Q-1.10
BIOS Settings	Hyperthreading=Off, Profile = Maximum Performance
OS	RHEL 8.7 (kernel 4.18.0-425.3.1.el8.x86_64)
OS Settings	processor.max_cstate=1; intel_idle.max_cstate=0; iommu=pt mitigations=off; clear caches; NUMA Balancing=0; randomize_va_space 0; THP=ON; CPU Governor=Performance

Table 2: Intel system configurations

TEST METHODOLOGY

SLB's ECLIPSE industry-reference simulator provide a standard set of benchmarks that represent typical usage and cover a range of problem sizes that can be used to evaluate the performance of different platforms running ECLIPSE. The uplift is calculated as the ratio of the systems under test (*sut*) to the reference system (*ref*). In this Summary Brief, the Intel Xeon 8462Y is the *ref* and the 4th Gen AMD EPYC 9384X with 3D V-Cache is the *sut*. The total amount of variability between individual runs was < 1%. The systems tested were configured as shown in Tables 1 and 2, above.

FOR ADDITIONAL INFORMATION

Please see the following additional resources for more information about 4th Gen AMD EPYC features, architecture, and available models:

- AMD EPYC™ 9004 Series Processors
- AMD EPYC™ Tuning Guides
- AMD EPYC™ Products

REFERENCES

1. "Technical Computing" or "Technical Computing Workloads" as defined by AMD can include: electronic design automation, computational fluid dynamics, finite element analysis, seismic tomography, weather forecasting, quantum mechanics, climate research, molecular modeling, or similar workloads. GD-204
2. AMD Infinity Guard features vary by EPYC™ Processor generations. Infinity Guard security features must be enabled by server OEMs and/or Cloud Service Providers to operate. Check with your OEM or provider to confirm support of these features. Learn more about Infinity Guard at https://www.amd.com/en/technologies/infinity-guard. GD-183
3. Based on calculated areal density and based on bump pitch between AMD hybrid bond AMD 3D V-Cache stacked technology compared to AMD 2D chiplet technology and Intel 3D stacked micro-bump technology. EPYC-026
4. Based on AMD internal simulations and published Intel data on "Foveros" technology specifications. EPYC-027
5. Maximum boost for AMD EPYC processors is the maximum frequency achievable by any single core on the processor under normal operating conditions for server systems. EPYC-18

AUTHORS

Alvaro Fernandez and Ashok Manikonda contributed to this Performance Brief.

RELATED LINKS

- SLB INTERSECT*
- SLB ECLIPSE*
- SLB Delfi Petrotechnical Suite*
- AMD EPYC™ Processors
- AMD EPYC Technical Briefs

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BOOST PERFORMANCE WITH AMD EPYC

AMD EPYC™ processors are built to handle large scientific and engineering datasets - ideal for compute-intensive modeling and advanced analysis techniques. Leveraged by many of the world's largest, most scalable data centers and supercomputers, AMD EPYC™ enables fast time-to-results for HPC.

"ZEN 4" CORE & SECURITY FEATURES

Support for up to:

- 96 physical cores, 192 threads
- 1152 MB of L3 cache per CPU
- 96 MB of L3 cache per CCD
- 6 TB of DDR5-4800 memory
- Up to 128 1P, up to 160 2P PCIe® Gen 5 lanes

Infinity Guard security features[2]

- Secure Boot
- Encrypted memory with SME

SLB ECLIPSE

The ECLIPSE industry-reference simulator is a feature-rich, comprehensive reservoir. ECLIPSE offers a complete and robust set of numerical solutions for fast and accurate prediction of dynamic behavior for all types of reservoirs and development schemes thanks to its extensive capabilities, robustness, speed, parallel scalability, and superb platform coverage.