SIMULIA® APPLICATIONS
TECHNICAL COMPUTING

Powered by 4th Gen AMD EPYC™ Processors

November 2022

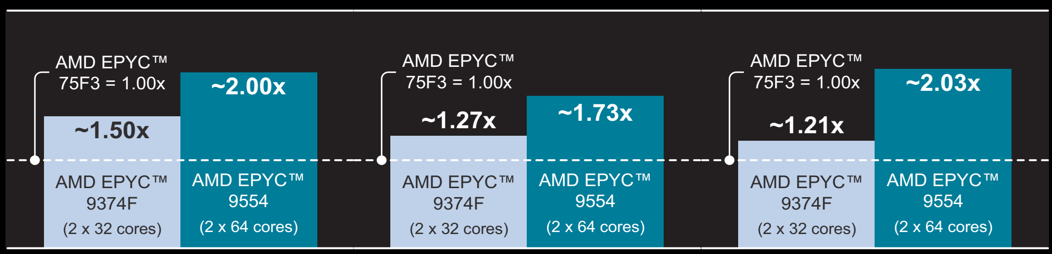
AT A GLANCE

Systems powered by dual 32-core and 64-core 4th Gen AMD EPYC™ processors demonstrate outstanding generational performance uplifts compared to dual 32-core 3rd Gen AMD EPYC processors on SIMULIA Abaqus and PowerFLOW.

PERFORMANCE HIGHLIGHTS

These charts show the average generational uplift provided by 32- and 64-core 4th Gen AMD EPYC processors across a variety of SIMULIA Abaqus and PowerFLOW benchmarks:

Up to ~2.00x on SIMULIA Abaqus Explicit | Up to ~1.73x on SIMULIA Abaqus Standard | Up to ~2.03x on SIMULIA PowerFLOW



KEY TAKEAWAYS

Comparing the performance of single-node servers powered by dual 4th Gen AMD EPYC 32-core 9374F and 64-core 9554 processors versus equivalent servers powered by prior-generation AMD EPYC 75F3 (32-core) processors yields the impressive generational performance uplifts shown above. These single-node uplifts ranging from ~1.21x to ~1.50x using the same number of cores demonstrate the real-world business value of the revolutionary technologies incorporated into 4th Gen AMD EPYC processors when running technical computing[1] workloads. Using 4th Gen AMD EPYC processors with higher core counts can achieve even higher performance uplifts of from ~1.73x to ~2.03x.

4th Gen AMD EPYC processors feature:

- 1MB L2 cache vs. 512 KB in "Zen 3."
- Up to 4 links of Gen 3 Infinity Fabric™ at up to 32 Gbps.
- 12 memory channels that support up to 6TB of DDR5-4800 memory.
- Support for PCIe® Gen 5 at up to 32 Gbps.
- AVX-512 instruction support for enhanced HPC and ML performance.
- AMD Infinity Guard technology to help protect your data.[2]

RELATED LINKS

- SIMULIA Abaqus*
- SIMULIA PowerFLOW*
- AMD EPYC™ Processors
- AMD EPYC Technical Briefs

FOR ADDITIONAL INFORMATION

Please see the following additional resources for more information about 4th Gen AMD EPYC features, architecture, and available models:

- AMD EPYC™ Tuning Guides
- AMD EPYC™ Products

TEST METHODOLOGY

SIMULIA provides a standard set of benchmarks that evaluate the performance of different platforms running SIMULIA applications.[3] These benchmark cases represent typical usage and cover a range of sizes. The uplift is calculated as the ratio of the systems under test (*sut*) to the reference system (*ref*). In this Summary Brief, the 3rd Gen AMD EPYC 75F3 processor is the *ref* and the 4th Gen AMD EPYC 9374F and 9554 processors are the *sut*.[4] The total amount of variability between individual runs was <1%.

REFERENCES

1. "Technical Computing" or "Technical Computing Workloads" as defined by AMD can include: electronic design automation, computational fluid dynamics, finite element analysis, seismic tomography, weather forecasting, quantum mechanics, climate research, molecular modeling, or similar workloads. GD-204
2. AMD Infinity Guard features vary by EPYC™ Processor generations. Infinity Guard security features must be enabled by server OEMs and/or Cloud Service Providers to operate. Check with your OEM or provider to confirm support of these features. Learn more about Infinity Guard at https://www.amd.com/en/technologies/infinity-guard. GD-183
3. The tests described in this Summary Brief used the following benchmarks and present the average performance across all benchmarks for each application (ABAQUS and PowerFLOW version is 2022 HF 4):
   -ABAQUS Explicit: e13 [Toyota Venza front crash simulation, 29 MM dof, explicit solver]; e14_droptest [phone drop from height, 7.4 MM dof, explicit solver]
   -ABAQUS Standard: s9 [Fuselage, 48 MM dof, direct linear solver]; s12 [Bearing, 6 Million dofs, direct linear solver];. s4e_direct_lm [Engine block model, 15 MM dof, direct linear solver, contact friction w Lagrange mults]; s4e_iter_lm [Engine block model, 15 MM dof, Iterative Algebraic Multigrid]; s4e_iter_penalty (Engine block, 15 MM dof, algebraic multigrid solver, contact friction w penalty]; s4e_iter_lm [Engine block, 15 MM dof, algebraic multigrid solver for indefinite systemsm hex, gasket & misc. elemm contact friction w/Lagrange Multipliers]
   -PowerFLOW: EV12-6-2021-r2 [low Mach regime isothermal car], EV12-6-2021-r2-nomeas-nomon [low Mach regime isothermal car, no I/O]
4. System configurations:
   -System 1: CPUs: 2 x AMD EPYC 9554 (64 cores/socket, 128 cores/node); Base Freq: 3.10 GHz; 256 MB L3; 1.5 TB (24x) Dual-Rank DDR5-4800 64GB DIMMs, 1DIMM per channel; 1 x 256 GB SATA (OS) | 1 x 1 TB NVMe (data); BIOS Version 1001C, SMT=off, Determinism=performance, NPS=4, TDP/PPT=400; RHEL 8.6; OS settings: Clear caches before every run, NUMA balancing 0, randomize_va_space 0
   -System 2: CPUs: 2 x AMD EPYC 9374F (32 cores/socket, 64 cores/node); Base Freq: 3.85 GHz; 256 MB L3; 1.5 TB (24x) Dual-Rank DDR5-4800 64GB DIMMs, 1DIMM per channel; 1 x 256 GB SATA (OS) | 1 x 1 TB NVMe (data); BIOS Version 1001C, SMT=off, Determinism=performance, NPS=4, TDP/PPT=400; RHEL 8.6; OS settings: Clear caches before every run, NUMA balancing 0, randomize_va_space 0
   -System 3: CPUs: 2 x AMD EPYC 75F3 (32 cores/socket, 64 cores/node); Base Freq: 2.95 GHz; 256 MB L3; 1 TB (16x) Dual-Rank DDR4-3200 64GB DIMMs, 1DIMM per channel; 1 x 256 GB SATA (OS) | 1 x 1 TB NVMe (data); BIOS Version 1009B, SMT=off, X2APIC=on, IOMMU=off, APBDIS=1, Fixed SOC P-state=0, Determinism=power, NPS=4, DF C-states=off, PIO, EPIO, TSME=off, PCIe 10 bit tag=on; RHEL 8.6; OS settings: Clear caches before every run, NUMA balancing 0, randomize_va_space 0

Alvaro Fernandez contributed to this Summary Brief.