

# **Processor Programming Reference (PPR) for AMD Family 1Ah Model 11h, Revision B0 Processors Volume 6 of 7**

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## 11 Fusion Controller Hub (FCH)

### 11.1 FCH Overview

#### 11.1.1 Acronyms

Table 177: List of Acronyms used in FCH

Acronym	Definition
ASF	Alert Standard Format.
ASL	ACPI Source Language. See <a href="#">docACPI</a> .
DASH	Desktop and mobile Architecture for System Hardware.
SCH	Server Controller Hub.
<a href="#">SSC</a>	Spread Spectrum Clocking.
TPM	Trusted Platform Module.

#### 11.1.2 Functional

This section describes the integrated [FCH](#), also known as the SCH. The SCH, which replaces the South Bridge Gasket (SBG), integrates the FCH with an interface to a standard Scalable Data Fabric Port (SDP). It also adapts additional DFX features such as the Remote System Management Unit (RSMU) and Remote Design-For-Test (RDFT) structures.

In terms of IO functions, the I2C, I3C, UART, and eSPI are available in the Family 1Ah Models 10h-1Fh Processors. In addition, ACPI Power management, basic low level system functions, boot, and clock generation (ClkGen) logic are provided by the processor.

The following is the list of IP blocks and functions:

AB/SB-SDP(SB Scalable Data Port): SDP is designed to meet Family 1Ah Models 10h-1Fh architecture and is the interface to Scalable Data Fabric (SDF).

SPI/eSPI – Serial peripheral interface: this is the bridge logic to the BIOS/firmware flash and SPI TPM. eSPI is multiplexed on the SPI bus to support an eSPI device such as embedded controller (ec).

Family 1Ah Models 10h-1Fh Processors have the following new features:

1. We have 2 sets of eSPI and SPI muxed pads. eSPI is the default function.
2. A second eSPI controller is added

UART – Universal Asynchronous Receiver/Transmitter: a low speed communication bus that is typically used for interfacing to serial ports. There are four UART ports and the speed can be upgraded to 4Mbps depending on availability of required reference clock. At least one UART is required to support legacy IO addresses (0x3F8:0x3FF). The UART doesn't support FIFO mode in legacy IO mode.

I2C - Inter-Integrated Circuit: a low level serial bus that is popular for connecting to external devices. Two I2Cs can be configured to be in secured mode. In secure mode, the two I2C blocks become inaccessible by the host CPU.

I3C - The I3C interface is intended to improve upon the features of the I2C interface, preserving backward compatibility. It provides more power efficiency and speed improvement over I2C.



**Clkgen – Clock Generation:** integrated clock generation function for the entire system. This block adds a non-spread display and more [PCIe®](#) GPP clock outputs. It also adds more internal reference clocks for various PHYs. In a multi-die configuration, Clkgen is configured to a different internal clock mode where the secondary dies use a 100MHz reference (coming from primary die) instead of a 48MHz crystal source. See 11.3.9.1 [Miscellaneous (MISC) Registers].

**SMBus – System Management Bus:** a low level serial bus used for communicating with on board devices. The SMBus Host Controller provides two independent control spaces, one for the SMBus and one for the Alert Standard Format (ASF) bus. For register definitions of these control spaces, see and for register descriptions.

**GPIO – General Purpose IO:** used as GPIO or interrupt inputs. See 11.3.10 [GPIO Pin control registers] for register descriptions.

**ACPI – Advanced Configuration and Power Interface:** power management and reset functions. This block also includes other system functions such as IOAPIC and various system timers. See 11.3.2 [I/O Advanced Programmable Interrupt Control] for register descriptions.

**Power Management (PM) Supervisory –** custom logic to manage iSCH (integrated server controller hub) clock and power gating to support AOAC. See 11.3.9.3 [Power Management (PM) Registers and Standard ACPI Registers] for register description.

### 11.1.3 MMIO Programming for Legacy Devices

The legacy devices, IOAPIC, TPM, ACPI, and Watchdog Timer, require the base address of the Memory Mapped IO registers to be assigned before these registers can be accessed. The Memory Mapped IO register base address and its entire range should be mapped to a non-posted memory region by programming the CPU register.

#### 11.1.3.1 Description for FCH::IO::PCIInterrupt Map

FCH::IO::PCI\_INTR\_INDEX bit [7] means PciIntrApic, set as 0 means IRQ routing to PIC, set as 1 means IRQ routing to IOAPIC.

FCH::IO::PCI\_INTR\_INDEX bit[6:0] are PCI interrupt index. Select which PCI interrupt to map. Following are detail description.

*Table 178: PCI interrupt index list of FCH::IO::PCI\_INTR\_INDEX bit[6:0]*

Bit[6:0]	Description
04h-00h	INT[E:A]#.
05h	INTF#/GENINT2.
06h	INTG#.
07h	INTH#.
08h	Misc.
0Bh-09h	Misc[2:0].
0Fh-0Ch	INT[D:A] from serial IRQ.
10h	SCI.
11h	SMBUS0.
12h	ASF.
15h-13h	Reserved.
16h	PerMon.
17h	SD.
18h	Reserved.

1Ah	SDIO.
1Fh-1Bh	Reserved.
20h	CIR, no IRQ connected
21h	GPIOa, from PAD_FANIN0
22h	GPIOb, PAD_FANOUT0
23h	GPIOc, no IRQ connected
4Fh-24h	Reserved.
53h-50h	GPPInt3/2/1/0.
5Fh-54h	Reserved.
60h	SCI Interrupt
61h	<a href="#">SMI</a> Interrupt
62h	GPIO controller interrupt.
6Fh-63h	Reserved.
70h	I2C0/I3C0.
71h	I2C1/I3C1.
72h	I2C2/I3C2.
73h	I2C3/I3C3.
75h-74h	UART1/UART0.
77h-76h	I2C5/I2C4.
79h-78h	UART3/UART2.
7Fh-7Ah	Reserved.

#### 11.1.4 ASF controller

The ASF controller may be used in a slave mode to support DASH clients. When the platform is configured for DASH the BIOS should set the following registers to ensure the ASF is configured in slave mode and the control commands are defined properly in the ASF tables:

When operating in Master mode,

BIOS programs FCH::PM::DECODEEN[asfsmasteren] = 1

BIOS programs FCH::PM::DECODEEN[asfsmasteren] back to 0 after the master operations are complete.

When operating in slave mode,

BIOS programs FCH::PM::DECODEEN[asfsmasteren] = 0

In addition to supporting remote DASH operations, BIOS should ensure that the ASF tables define the correct command codes and must be programmed with the same value reported in the ASF control data table.

The ASF controller can behave like a remote control device to accept commands from the client side to do the reset down and up power cycles. BIOS reports those in the ASF control data table. The command and command data are defined the below ASF Remote Control Commands table:

1. If Remote Control is rest, then control command is 50h, control data is 00h.
2. If Remote Control is Power Up, then control command is 51h, control data is 00h.
3. If Remote Control is Power Down, then control command is 52h, control data is 00h.
4. If Remote Control is Power Cycle, then control command is 53h, control data is 00h.

#### 11.1.5 A-Link Bridge

The A-link bridge (AB) sits behind the [FCH](#) gasket and acts as the bridge between the root complex and A-Link, B-Link bus.

Program the following sequence to detect upstream interrupts:

BIOS enables AB to detect upstream interrupts for the purpose of system management.

- Program with CPU interrupt delivery address [39:20].
- Program .

Program the following sequence to allow AB 32/64 Byte DMA writes:

1. Program .
2. .
3. Software ensures that SDP Upstream Control[Dma16ByteMode] == 0.

### 11.1.6 FCH Gasket

The FCH\_SDP replaces the FCH\_SBG and used to connect between the [FCH](#) and IO Hub.

The FCH\_SDP is responsible for converting between the protocols used by the SDP interface and the A-link bridge interface. BIOS programs FCH::PM::ABREGBAR to set up base address before accessing the AB configuration registers.

The SDP memory power saving list follows:

The following sequence enables SBG memory power saving:

1. Program FCH\_MISC\_MEMPWRSVCNTRL[sd\_bypass\_mem\_dsd] = 0 to enable SDP memory power savings.
2. Program SDP Misc Control[HostMemShutDownEn] = 1 to enable SDP host memory shutdown.
3. Program SDP Misc Control[DmaMemShutdownEn] = 1 to enable SDP DMA memory shutdown.

SBG internal clock gating list as below:

The following sequence enables the SBG internal clock gating:

1. Program SDP Misc Control[MedBCLKGateEnHost] = 1 to enable medium grain BCLK gating.
2. Program SDP Misc Control[DBG\_CLK\_GATE\_EN] = 1 to disable debug BCLK.

### 11.1.7 AOAC Function

#### 11.1.7.1 Wake Enable

The D3 cold and S3/S5 wake is triggered by GPIO. In order to enable the wake on specified GPIO pins, the corresponding GPIO registers need to be programmed to enable wake capability. See 11.1.14.1.2 [Wakeup GPIO] for GPIO wake up function.

For the S3 or S4 state, the wake goes through Pm1a and Gevent or the GPIO controller.

#### 11.1.7.2 WinBlue power button

Windows® 8.1 has redefined the power button. The power button connects to GPIO controller and can be programmed by the OS to trigger on both edges. In addition, the 4 second shutdown is changed to a 10 second shutdown. To support the 10 second shutdown, set FCH\_GPIO\_GPIO\_WAKE\_INTERRUPT\_MASTER\_SWITCH[enwinbluebtn] = 1.

### 11.1.8 ACPI

#### 11.1.8.1 Enable legacy IO access to DMA controller 1

To enable legacy IO access to FCH::IO::DMA\_CH\_0, program FCH\_PM\_LegacySS[LegacySS] to an unoccupied port address.

FCH\_PM\_LegacySS[LegacySS] used to define the IO base address of a function which is no longer used. It is defaulted

to be 0x0000 that conflicts with the legacy DMA BaseAddress register. Therefore software needs to program FCH\_PM\_LegacySS[LegacySS] to an unoccupied IO port address other than 0x0000.

### 11.1.9 SPI Bus Interface

This section describes the SPI Bus related programming requirements.

RomProtect applies to ROM, those ROM controls does not apply to eSPI bus as eSPI controller is another independent IP.

#### 11.1.9.1 Serial Peripheral Interface (SPI) ROM

##### 11.1.9.1.1 Introduction

Security is important to AMD. A feature called "ROM locking" enables platform developers to add a layer of security to their platforms. Regions of SPI ROM can be flagged as "Read" or "No-Read or Write" or "No-Write" ("Write-only" is not supported). Up to 64 MB of ROM can be managed through the ROM Protection regions.

The SPI ROM can be accessed by two methods or "modes" of operation: "Direct" and "Indexed".

- "Direct" is a program read or write to a memory location ([MMIO](#) in the Physical address range) which gets translated by HW to an SPI bus command behind the scene. This is the mode used for most ROM reads during boot.
- "Indexed" mode uses SPI bus commands to access the SPI device. This requires setting up the SPI command/control registers and issuing the command on the SPI bus. This mode is used for special operations like erasing a block and programming a block in the flash part. It can be used for reads; however, they are much slower. AMD recommends Index Mode not be used for reads.

When accessing the ROM in the various modes, it is important to keep in mind the addressing mechanisms in use. There are multiple places in the physical memory map where a ROM can be located.

- ROM1 – Traditionally a smaller ROM based at 1 MB.
- ROM2 – Typically located at the 4GB address boundary, supporting 16 MB ROMs, although larger ROMs may be used and paged into the 16 MB aperture.
- ROM3 – AMD supports a special address space which can support larger ROMs (up to 64 MB).

Also, when using Indexed mode, the address become a "relative" address. 0X0000 being the first storage in the device running up to ROM\_Size-1 being the last storage byte in the device. Multiple SPI devices can be present on the bus selected by the Alt\_SPI\_CS register as described in the PPR. Protection is applied identically to multiple ROMs.

AMD's architecture includes support for protection in all three ROM address spaces with the described ROM protection mechanisms.

##### 11.1.9.1.2 Normal Flash ROM on SPI Bus

This level of protection is characterized by having no added HW protection beyond that provided by the SPI ROM device or that is built into the platform.

This is the level most common for client PCs. Manufacturers use various schemes to prevent accidental erasure, and to ensure recovery from an update gone wrong.

SPI memory can be protected from being written to or read from by using the following sequence. This is optional and used as required.

##### 11.1.9.1.2.1 Steps to Prepare

Set the address(es) for the ROM(s) in the system. ROM Address\_Range registers are 16 bits => address [31:12]. These start and end registers contain the upper 20 bits of the start and end address of a ROM range. The lower 12 bits of a start address are 000h. The lower 12 bits of an end address are FFFh. These registers apply to SPI bus.

### 11.1.9.1.3 Standard HW Protection

This level is characterized by invoking hardware provided features for locking access to certain SPI registers. The PPR describes registers where the platform BIOS engineer can:

- Define Protection regions
- Set restricted commands (11.1.9.1.3.1.5 [Set the Block List])
- Invoke a hardware lock of protection registers

#### 11.1.9.1.3.1 Steps to Invoke HW Protection

##### 11.1.9.1.3.1.1 Prepare

Set the address(es) for the ROM(s) in the system. ROM Address\_Range registers are 16 bits => address [31:12]. These start and end registers contain the upper 20 bits of the start and end address of a ROM range. The lower 12 bits of a start address are 000h. The lower 12 bits of an end address are FFFh. These registers apply to SPI bus.

##### 11.1.9.1.3.1.2 Set the Protect Regions

There are four ROM\_PROTECT registers that allow you define up to 16 [MB](#) each of protected address space. Protection can be read-only, no-read-nor-write, or unprotected (write-only is not supported). It is considered an error to define a write-only area and SPI ROM Locking FW does not allow it. A summary of points of interest for these registers are described in the PPR:

- The 4 regions must not overlap.
- "Range" is 0-based (#blocks=N+1); max field value is 255, representing 256 RangeUnits.
- "RangeUnit" can be 4k (bit=0) or 64k (bit=1) in size.
- When programmed, all 4 protection registers must contain valid protection bits. If both protection bits are 0, the HW will not look at the range in a particular register.

##### 11.1.9.1.3.1.3 ROM2 Address Override

The developer must also ensure that the correct value for the ROM2\_ADDR\_OVERRIDE register is set in the same way as the ROM\_PROTECTx registers. Note that the HW only looks at unified addresses.

##### 11.1.9.1.3.1.4 SPI Bank Mapping

The PPR defines ROM2\_ADD\_OVERRIDE register that can be used to map banks of a large (up to 64M) ROM into a 16M window. This mapping is applied the ROM Physical address has been determined. This affects the protection setting chosen by the platform BIOS engineer. The protection regions must be aligned to the pre-paged physical addresses. When used in ROM2 space, the SPI Controller can address from the beginning to the end of the ROM subject to the ROM Protect registers. However, since the aperture is only 16MB, only the lower 16MB can be protected by HW mechanisms (Rom Protect registers) alone.

##### 11.1.9.1.3.1.5 Set the Block List

There are 2 SPI\_RestrictedCmd registers that allow for 8 commands to be in block list. List the hex command code(s) to be blocked. There are 5 commands (RestrictedCmdx) that restrict access when the OpCode matches and the address is above 512k. The 3 RestrictCmdWoAddrx entries restrict access with or without address parameters.

Note: For general protection from any/all SPI writes or erasures – include the WE (Write Enable) command in block list. The SPI protocol requires the WE command to be issued prior to any write or erase command.

#### 11.1.9.1.4 Set SPI ROM Protection

SPI memory can be protected from being written to or read from by using the following sequence. This is optional and used as required.

##### 11.1.9.1.4.1 Enable SPI ROM Protection

1. Program ROM\_PROTECT\_0 to enable protection for Read or Write memory accesses to SPI flash memory space. Up to eight ranges of memory can be protected.
2. Program FCH::LPCHOSTSPIREG::SPI\_RESTRICTEDCMD\_REGISTER or FCH::LPCHOSTSPIREG::SPI\_RESTRICTEDCMD2\_REGISTER with SPI commands that are required before doing write accesses to the SPI ROM. Use commands such as WR\_EN, WR\_Status and Erase when programming these restricted command registers.
3. Program FCH::LPCHOSTSPIREG::SPI\_CNTRL0\_REGISTER[spiaccessmacromen]= 0 or FCH::LPCHOSTSPIREG::SPI\_CNTRL0\_REGISTER[spihostaccessromen] = 0 to protect the registers above from being reprogrammed.

Accesses are now blocked by the SPI host preventing write accesses to the SPI ROM.

Notes:

Step 1 enables protection for direct memory access to SPI (Direct memory access is when Host access SPI memory using normal Read / Write commands these access are converted to SPI Read and Write commands by the SPI controller).

Step 2 enables protection for indirect memory access (a.k.a. Indexed mode) to the SPI controller. Indirect memory accesses (a.k.a. Indexed mode) are when the FCH::LPCHOSTSPIREG::CMDCODE is used to send SPI commands to the SPI ROM.

Step 3 By programming the FCH::LPCHOSTSPIREG::SPI\_CNTRL0\_REGISTER[spiaccessmacromen] = 0 or FCH::LPCHOSTSPIREG::SPI\_CNTRL0\_REGISTER[spihostaccessromen] = 0, all SPI commands (defined in register FCH::LPCHOSTSPIREG::SPI\_CMDVALUE1\_REGISTER and FCH::LPCHOSTSPIREG::SPI\_CMDVALUE2\_REGISTER) and Restricted commands (defined in FCH::LPCHOSTSPIREG::SPI\_RESTRICTEDCMD\_REGISTER and FCH::LPCHOSTSPIREG::SPI\_RESTRICTEDCMD2\_REGISTER) are protected.

##### 11.1.9.1.4.2 Disable SPI ROM Protection

1. Generate [SMI](#).
2. Program read\_protect and write\_protect to 0 to unprotect Read or Write memory access to the SPI flash memory space.
3. Program FCH::LPCHOSTSPIREG::SPI\_CNTRL0\_REGISTER[spiaccessmacromen] = 1 and FCH::LPCHOSTSPIREG::SPI\_CNTRL0\_REGISTER[spihostaccessromen] = 1 to unprotect the registers above from being reprogrammed.
4. Exit SMI mode.

#### 11.1.10 eSPI

eSPI is configured to run at 16.6MHz, 20MHz (default), 25MHz, 33MHz, 50MHz and 66MHz. See 11.3.8.2 [eSPI Registers] about how to program the speed.

### 11.1.11 UART

The UART is controlled by driver software. There are no programming requirements for the BIOS, except for pin configuration and enablement.

If Program UART0\_1p843MCLK\_EN=1, enable UART0 1.843MHz clock.

If Program UART1\_1p843MCLK\_EN=1, enable UART1 1.843MHz clock.

If Program UART2\_1p843MCLK\_EN=1, enable UART2 1.843MHz clock.

If Program UART3\_1p843MCLK\_EN=1, enable UART3 1.843MHz clock.

### 11.1.12 I2C Master

For I2C0~I2C3, the I2C pins interface pins can be either at 1.1V or 1.8V. I2C interface pins for I2C4 and I2C5 supports 1.8V. The following table lists the I2C PAD control registers.

*Table 179: I2C PAD Control Configuration*

I2C modules	Description	Register Location
I2C_0	Pad control Register	FCH::MISC::I2C0_PADCTRL
I2C_1	Pad control Register	FCH::MISC::I2C1_PADCTRL
I2C_2	Pad control Register	FCH::MISC::I2C2_PADCTRL
I2C_3	Pad control Register	FCH::MISC::I2C3_PADCTRL
I2C_4	Pad control Register	FCH::MISC::I2C4_PADCTRL
I2C_5	Pad control Register	FCH::MISC::I2C5_PADCTRL

### 11.1.13 I3C Master

The I3C interface is improved from I2C interface and preserves the backward compatibility with I2C.

Following are the supporting features:

1. Two wire serial interface up to 12.5MHz using Push-Pull
2. Legacy I2C Device co-existence on the same Bus (with some limitations)
3. Dynamic Addressing while supporting Static Addressing for Legacy I2C Devices
4. Broadcast and Direct Common Command Code ([CCC](#)) message
5. Legacy I2C messaging
6. Support Single Data Rate messaging ([SDR](#))
7. In-Band Interrupt support
8. Hot-Join support
9. Master mode only

For I3C0~I3C3, the I3C pins interface pins can be either at 1.1V or 1.8V

*Table 180: I3C PAD Control Configuration*

I3C modules	Description	Register Location
I3C_0	Pad control Register	FCH::MISC::I2C0_PADCTRL
I3C_1	Pad control Register	FCH::MISC::I2C1_PADCTRL
I3C_2	Pad control Register	FCH::MISC::I2C2_PADCTRL
I3C_3	Pad control Register	FCH::MISC::I2C3_PADCTRL

### 11.1.14 GPIO

There are three types of pads in [FCH](#): GPIO, I2C and I3C.

- For the GPIO pads, most of their functional connections are controlled by GPIO registers. When IOMUX is set to select the GPIO function, the pad is controlled by GPIO register, including the output enable, output value, pull-up and pull-down and driving strength functions.
- For the I2C pad, only the output enable comes from a GPIO register, as the pad output is an open drain output. Open drain outputs require an external (on-board) pull-up resistor. After programming the I2C pad to be GPIO (through the IOMUX register), drive the output enable high if you want the output PAD driven low. Conversely, drive the output enable low in order to allow the external pull-up resistor to pull the output PAD high.
- For the I3C pads, additional control ports are required. An additional 32-bit control register is available to control these GPIOs. After programming each I3C pad to be GPIO (through the IOMUX register), the register should be used to drive the GPIO accordingly.
  - I3C have more control ports than I2C. Besides one DWORD ACPI register, there is more GPIO register bits in use, the following is the details:
    - I2C0~3\_PadCtrl of MISC register
      - Bit31: SpikeRcSel1
      - Bit30: SpikeRcSel0
      - Bit29: Mode\_1p8\_1p1\_1
      - Bit28: Mode\_1p8\_1p1\_0
      - Bit27: Mode\_I3c\_I2c1
      - Bit26: Mode\_I3c\_I2c0
      - Bit25: Slewp1
      - Bit24: Slewp0
      - Bit23: ResBiasEn1
      - Bit22: ResBiasEn0
      - Bit21: CompSel1
      - Bit20: CompSel0
      - Bit19: Spare1
      - Bit18: Spare0
      - Bit17: BiasCrtEn1
      - Bit16: BiasCrtEn0
      - Bit15: RSel1p1
      - Bit14: RSel0p9
      - Bit13: CSel1p1
      - Bit12: CSel0p9
      - Bit11: SpikeRcEn1
      - Bit10: SpikeRcEn0
      - Bit9: FallSlewSel1
      - Bit8: FallSlewSel0
      - Bit7: Slewn1
      - Bit6: Slewn0
      - Bit5: RxSel1
      - Bit4: RxSel0
      - Bit3: OD\_Rp\_Sw3
      - Bit2: OD\_Rp\_Sw2
      - Bit1: OD\_Rp\_Sw1\_pre
      - Bit0: OD\_Rp\_Sw0\_pre
    - GPIO register bits
      - NG0\_SCL\_drv\_sel\_bit0



- NG1 SCL\_drv\_sel\_bit1
- NG2 SDA\_drv\_sel\_bit0
- NG3 SDA\_drv\_sel\_bit1
- DIN0 SCL\_IN\_DIN
- DIN1 SDA\_IN\_DIN
- OE0 SCL\_IN\_OE
- OE1 SDA\_IN\_OE
- PU0 SCL\_IN\_PU
- PU1 SDA\_IN\_PU
- PD0 SCL\_IN\_PD
- PD1 SDA\_IN\_PD

Table 181: GPIO capable pads

Bump Pin Name	Pad Macro
Power	
BP_PWR_BTN_L/AGPIO0	GPIO Pad
BP_SYS_RESET_L/AGPIO1	GPIO Pad
BP_WAKE_L/AGPIO2	GPIO Pad
BP_RSMRST_L	GPIO Pad
BP_SLP_S3_L	GPIO Pad
BP_SLP_S5_L	GPIO Pad
BP_PWR_GOOD	GPIO Pad
Clock	
BP_RTCCLK	GPIO Pad
GPIO S5	
BP_AGPIO3/SPD_HOST_CTRL_L	GPIO Pad
BP_AGPIO4/SATA_ACT_L	GPIO Pad
BP_AGPIO5/DEVSLP0/SATA_ZP0_L	GPIO Pad
BP_AGPIO6/DEVSLP1/SATA_ZP1_L	GPIO Pad
BP_AGPIO7	GPIO Pad
BP_AGPIO21	GPIO Pad
BP_AGPIO22	GPIO Pad
BP_SMERR_L/AGPIO24	GPIO Pad
BP_AGPIO256/SGPIO0_CLK	GPIO Pad
BP_AGPIO257/SGPIO1_CLK/CLK_REQ01_L	GPIO Pad
BP_AGPIO258/SGPIO2_CLK/CLK_REQ02_L	GPIO Pad
BP_AGPIO259/SGPIO3_CLK	GPIO Pad
BP_SGPIO_DATAOUT/AGPIO260	GPIO Pad
BP_SGPIO_LOAD/AGPIO261	GPIO Pad
BP_PWRGD_OUT/AGPIO12	GPIO Pad
BP_USB10_OC_L/AGPIO16	GPIO Pad
BP_USB11_OC_L/AGPIO17	GPIO Pad
BP_USB00_OC_L/AGPIO264	GPIO Pad
BP_USB01_OC_L/AGPIO265	GPIO Pad
I2C	
BP_I2C5_SCL/BMC_SCL/SMBUS1_SCL/AGPIO19	I2C Pad with SMBUS support
BP_I2C5_SDA/BMC_SDA/SMBUS1_SDA/AGPIO20	I2C Pad with SMBUS support
BP_I2C4_SCL/HP_SCL/UBM_SCL/AGPIO13	I2C Pad
BP_I2C4_SDA/HP_SDA/UBM_SDA/AGPIO14	I2C Pad

Legacy	
BP_PCIE_RST1_L/AGPIO26	GPIO Pad
BP_PCIE_RST0_L/AGPIO266	GPIO Pad
BP_SOCKET_ID[0]	GPIO Pad
BP_SOCKET_ID[1]	GPIO Pad
GPIO S0	
BP_AGPIO87	GPIO Pad
BP_AGPIO88	GPIO Pad
BP_GENINT_L/PM_INTR_L/AGPIO89	GPIO Pad
BP_AGPIO104	GPIO Pad
BP_AGPIO105	GPIO Pad
BP_AGPIO106	GPIO Pad
BP_AGPIO107	GPIO Pad
BP_AGPIO109	GPIO Pad
BP_AGPIO115/CLK_REQ11_L	GPIO Pad
BP_AGPIO116/CLK_REQ12_L	GPIO Pad
BP_NMI_SYNC_FLOOD_L	GPIO Pad
Thermal	
BP_THERMTRIP_L	GPIO Pad
SPI/ESPI	
BP_ESPI_CLK0/SPI_CLK0/AGPIO117	GPIO Pad
BP_ESPI0_ALERT_L_ESPI_IO1/AGPIO108	GPIO Pad
BP_ESPI_CLK1/SPI_CLK1/AGPIO75	GPIO Pad
BP_ESPI_CLK2/AGPIO74	GPIO Pad
BP_SPI_CS0_L/AGPIO118	GPIO Pad
BP_ESPI_CS0_L/AGPIO124	GPIO Pad
BP_ESPI_CS1_L/AGPIO125	GPIO Pad
BP_SPI_CS2_L/AGPIO126	GPIO Pad
BP_SPI_CS1_L/AGPIO119	GPIO Pad
BP_ESPI0_DAT0/SPI0_DAT0/AGPIO120	GPIO Pad
BP_ESPI0_DAT1/SPI0_DAT1/AGPIO121	GPIO Pad
BP_ESPI0_DAT2/SPI0_DAT2/AGPIO122	GPIO Pad
BP_ESPI0_DAT3/SPI0_DAT3/AGPIO123	GPIO Pad
BP_AGPIO76/SPI_TPM_CS_L	GPIO Pad
BP_ESPI_RSTIN_L/KBRST_L/AGPIO129	GPIO Pad
BP_ESPI1_DAT0/SPI1_DAT0/AGPIO131	GPIO Pad
BP_ESPI1_DAT1/SPI1_DAT1/AGPIO132	GPIO Pad
BP_ESPI1_DAT2/SPI1_DAT2/AGPIO133	GPIO Pad
BP_ESPI1_DAT3/SPI1_DAT3/AGPIO134	GPIO Pad
BP_ESPI1_ALERT_L/AGPIO110	GPIO Pad
BP_ESPI_RSTOUT_L/AGPIO23	GPIO Pad
UART	
BP_UART0_CTS_L/UART2_TXD/AGPIO135	GPIO Pad
BP_UART0_RXD/AGPIO136	GPIO Pad
BP_UART0_RTS_L/UART2_RXD/AGPIO137	GPIO Pad
BP_UART0_TXD/AGPIO138	GPIO Pad
BP_UART0_INTR/AGPIO139	GPIO Pad
BP_UART1_RXD/AGPIO141	GPIO Pad

BP_UART1_TXD/AGPIO142	GPIO Pad
I3C	
BP_I3C0_SCL/I2C0_SCL/SPD0_SCL/SMBUS0_SCL/AGPIO145	I3C Pad with SMBUS support
BP_I3C0_SDA/I2C0_SDA/SPD0_SDA/SMBUS0_SDA/AGPIO146	I3C Pad with SMBUS support
BP_I3C1_SCL/I2C1_SCL/SPD1_SCL/AGPIO147	I3C Pad
BP_I3C1_SDA/I2C1_SDA/SPD1_SDA/AGPIO148	I3C Pad
BP_I3C2_SCL/I2C2_SCL/SPD2_SCL/AGPIO149	I3C Pad
BP_I3C2_SDA/I2C2_SDA/SPD2_SDA/AGPIO150	I3C Pad
BP_I3C3_SCL/I2C3_SCL/SPD3_SCL/AGPIO151	I3C Pad
BP_I3C3_SDA/I2C3_SDA/SPD3_SDA/AGPIO152	I3C Pad

#### 11.1.14.1 Groups of GPIO

There are three groups of GPIO: GPIOBank0, GPIOBank1 and GPIOBank2, please refer to 11.3.10.2 [GPIO Registers]. To enable the GPIO controller, follow the programming steps below:

##### 11.1.14.1.1 Interrupt GPIO

All the configuration bits (Bit[x]) used in the following steps come from GPIOBank0, GPIOBank1 and GPIOBank2. If the pin is used as an interrupt, see 11.3.10.2 [GPIO Registers]:

1. The driver programs the DebounceTmrOut/DebounceTmrOutUnit/DebounceCntrl bits according to the data passed by BIOS through the ASL code.
2. Configure bit[10:8] according to the data passed by BIOS through ASL code.
3. Set bit[11] = 1 and bit[12] = 1 to enable interrupt delivery and interrupt status. Interrupt status is at bit[28] when the GPIO input is asserted.
4. Configure the GPIO controller interrupt. The GPIO controller interrupt is an active low level interrupt. The driver clears the interrupt status, then sets FCH::GPIO::GPIO\_WAKE\_INTERRUPT\_MASTER\_SWITCH[eoi] = 1 to deassert the interrupt request after acknowledging the interrupt.

##### 11.1.14.1.2 Wakeup GPIO

All the configuration bits (Bit[x]) used in the following steps come from GPIOBank0, GPIOBank1 and GPIOBank2. If the pin is used as wake, see 11.3.10.2 [GPIO Registers]:

1. BIOS programs bit[15:13] to enable wake in S3/S5 by BIOS. The wake status is bit[29]. BIOS/[MP1](#) reads the wake status to determine the wake source, then clears them after wake.
2. The driver programs DebounceTmrOut/DebounceTmrOutUnit/DebounceCntrl bits according the data from BIOS through the ASL code.
3. The driver sets bit[10:8] to configure assertion condition according to the data from BIOS through the ASL code.
4. Set bit[11] = 1 and bit[12] = 1 to enable interrupt delivery and interrupt status then its interrupt status is found at bit[28] when the GPIO input is asserted.
5. Configure the GPIO controller interrupt. The GPIO controller interrupt is an active low level interrupt. BIOS configures it and sets it to 0s. The driver clears the interrupt status then sets FCH::GPIO::GPIO\_WAKE\_INTERRUPT\_MASTER\_SWITCH[eoi] = 1 after the interrupt is acknowledged.

##### 11.1.14.1.3 Pure GPIO

All the configuration bits (Bit[x]) used in the following steps come from GPIOBank0, GPIOBank1 and GPIOBank2. If the pin is used as a GPIO, see 11.3.10.2 [GPIO Registers]:

1. Bit[23:17] provides the state of the control on pull-up, pull-down, drive strength, output enable, output value, and pin value through bit[16].

### 11.1.15 Sticky/non-sticky attribute of PMIO registers

The table below list the sticky/non-sticky attribute of all PMIO registers. Sticky/non-sticky attribute is directly related to the register's reset condition:

A "Sticky" register is reset in the following conditions:

- Resume Reset: This reset is asserted in G3 state, and deasserted during G3 to S5 transition.
- System Reset: From system reset button

A "Non-sticky" register is reset in the following conditions:

- Resume Reset: This reset is asserted in G3 state, and deasserted during G3 to S5 transition.
- System Reset: From system reset button.
- S0 Reset events: Some events that happen in S0 state, such as CF9 and Keyboard Reset.
- Traditional sleep: S3 and S5 states.

See 11.3.9.3 [Power Management (PM) Registers and Standard ACPI Registers] for PMIO register descriptions.

*Table 182: PMIO Register Sticky/Non-sticky Attributes*

Dword#	Offset	Sticky/Non-sticky
0	00h ~ 03h	Sticky
1	04h ~ 07h	Sticky
2	08h ~ 0Bh	Sticky
3	0Ch ~ 0Fh	Sticky
4	10h ~ 13h	Sticky
5	14h ~ 17h	Sticky
6	18h ~ 1Bh	Sticky
7	1Ch ~ 1Fh	Sticky
8	20h ~ 23h	Sticky
9	24h ~ 27h	Sticky
10	28h ~ 2Bh	Sticky
11	2Ch ~ 2Fh	Sticky
12	30h ~ 33h	Sticky
13	34h ~ 37h	Sticky
14	38h ~ 3Bh	Sticky
15	3Ch ~ 3Fh	Sticky
16	40h ~ 43h	Sticky
17	44h ~ 47h	[31] non-sticky [30] sticky [29] non-sticky [28:25] sticky [24:0] read-only
18	48h ~ 4Bh	Sticky
19	4Ch ~ 4Fh	Sticky
20	50h ~ 53h	Sticky
21	54h ~ 57h	[31:8] Sticky [7] Sticky when [14]=0, non-sticky when [14]=1 [6:0] Sticky
22	58h ~ 5Bh	[31:28] no reset (these bits are actually in RTC) [27:23] sticky

		[22] read-only [21] write-only, read always return 0 [20:19] sticky [18] read-only [17] sticky [16:0] sticky
23	5Ch ~ 5Fh	[31:24] no reset (these bits are actually in RTC) [23:11] sticky [10] reserved, read always return 1 [9:0] sticky
24	60h ~ 63h	Sticky
25	64h ~ 67h	Sticky
26	68h ~ 6Bh	Sticky
27	6Ch ~ 6Fh	Sticky
28	70h ~ 73h	Sticky
29	74h ~ 77h	[31:8] sticky [7] write-only, read always return 0 [6:0] sticky
30	78h ~ 7Bh	Non-sticky
31	7Ch ~ 7Fh	Non-sticky
32	80h ~ 83h	Sticky
33	84h ~ 87h	Non-sticky
34	88h ~ 8Bh	Non-sticky
35	8Ch ~ 8Fh	Sticky
36	90h ~ 93h	Sticky
37	94h ~ 97h	Sticky
38	98h ~ 9Bh	Sticky
39	9Ch ~ 9Fh	Read-only
40	A0h ~ A3h	[31:16] non-sticky [15:0] is read-only if 0xD0[23] is 1, otherwise it is non-sticky
41	A4h ~ A7h	[31] non-sticky [30:29] reserved, read always return 0 [28:0] is read-only if [31] is 1, otherwise it is non-sticky
42	A8h ~ Abh	Sticky
43	ACh ~ Afh	Reserved, read always return 0
44	B0h ~ B3h	[31:28] non-sticky [27:23] read-only [22:0] non-sticky
45	B4h ~ B7h	Sticky
46	B8h ~ BBh	[31:21] sticky [20] read-only [19:0] sticky
47	BCh ~ BFh	Sticky
48	C0h ~ C3h	[31:30] sticky [29:0] is sticky if 0xC4[2] is 1, otherwise it is read-only
49	C4h ~ C7h	[31:11] sticky [10] write-only, read always return 0 [9] sticky [8] reserved, read always return 0 [7:1] sticky [0] reserved, read always return 0
50	C8h ~ CBh	Sticky
51	CCh ~ CFh	Sticky

52	D0h ~ D3h	[31:16] sticky [15:8] sticky, but is indirect access to four 8-bit registers [7:0] sticky
53	D4h ~ D7h	Sticky
54	D8h ~ DBh	[31:16] sticky [15:0] is indirect access to a stack of registers, which are reset by Resume Reset only
55	DCh ~ DFh	Sticky
56	E0h ~ E3h	Sticky
57	E4h ~ E7h	Sticky
58	E8h ~ Ebh	Sticky
59	Ech ~ Efh	[31:20] sticky [19] read-only [18:0] sticky
60	F0h ~ F3h	Sticky
61	F4h ~ F7h	Sticky
62	F8h ~ FBh	Sticky
63	FCh ~ FFh	Sticky

### 11.1.16 CLK IP Overview

#### 11.1.16.1 iCLK/eCLK mode

There are two clocking modes in which the processor can be brought up based on the boot strap pin SPI\_CLK: iCLK and eCLK clocking modes. iCLK clocking mode means that chip takes an internal crystal generated clocks as reference clock while eCLK clocking mode means that chip takes an external clock as reference clock.

BIOS should read FCH::MISC::STRAPSTATUS[clkgenstrap] to determine the clocking mode.

#### 11.1.16.2 CGPLL SSC Enable/Disable

The CGPLL [SSC](#) is disabled by default.

In eCLK mode, Spread Spectrum Clocking (SSC) should remain disabled.

In iCLK mode, SSC can be enabled on the [BSP](#) (socket 0) CG1PLL only. The CGPLL default spread amount is -0.375%. Alternatively, the spread amount can be set to -0.3%.

SSC enable sequence only need be executed during initial boot-up sequence or reset sequence triggered by pushing reset button, that means, for example, this sequence should not be executed after system exit Sleep State.

Note: When spread spectrum is turned on, the effective clock frequency will be slowed down by the same amount. This is applicable to functions that derive clocks from this PLL. For example, the effective CPU core frequency will be slowed down approximately ½ of the spread amount.

##### 11.1.16.2.1 CG1PLL -0.375% SSC Programming

Software can enable the CG1PLL default -0.375% [SSC](#) setting by the following programming:

1. FCH::MISC::CGPLLCONFIG1[cg1\_spread\_spectrum\_enable] = 1

2. FCH::MISC::CGPLLCONFIG3[cg1pll\_fracn\_en\_override] = 1
3. FCH::MISC::MISCCLKCNTRL0[cg1\_cfg\_update\_req] = 1

Software can disable the CG1PLL default -0.375% SSC setting by the following programming:

1. FCH::MISC::CGPLLCONFIG1[cg1\_spread\_spectrum\_enable] = 0
2. FCH::MISC::CGPLLCONFIG3[cg1pll\_fracn\_en\_override] = 0
3. FCH::MISC::MISCCLKCNTRL0[cg1\_cfg\_update\_req] = 1

#### 11.1.16.2.2 CG1PLL -0.3% SSC Programming

Software can enable the CG1PLL -0.3% [SSC](#) setting by the following programming:

1. FCH::MISC::CGPLLCONFIG4[cg1pll\_fcw1\_frac\_override] = 0x1333
2. FCH::MISC::CGPLLCONFIG5[cg1pll\_fcw\_slew\_frac\_override] = 0x3A
3. FCH::MISC::CGPLLCONFIG1[cg1\_spread\_spectrum\_enable] = 1
4. FCH::MISC::CGPLLCONFIG3[cg1pll\_fracn\_en\_override] = 1
5. FCH::MISC::MISCCLKCNTRL0[cg1\_fbdiv\_loaden] = 1
6. FCH::MISC::MISCCLKCNTRL2[fch\_core\_400m\_switch\_maskoff] = 1
7. FCH::MISC::MISCCLKCNTRL0[cg1\_cfg\_update\_req] = 1

Software can disable the CG1PLL -0.3% SSC setting by the following programming:

1. FCH::MISC::CGPLLCONFIG4[cg1pll\_fcw1\_frac\_override] = 0
2. FCH::MISC::CGPLLCONFIG5[cg1pll\_fcw\_slew\_frac\_override] = 0
3. FCH::MISC::CGPLLCONFIG1[cg1\_spread\_spectrum\_enable] = 0
4. FCH::MISC::CGPLLCONFIG3[cg1pll\_fracn\_en\_override] = 0
5. FCH::MISC::MISCCLKCNTRL0[cg1\_fbdiv\_loaden] = 0
6. FCH::MISC::MISCCLKCNTRL2[fch\_core\_400m\_switch\_maskoff] = 1
7. FCH::MISC::MISCCLKCNTRL0[cg1\_cfg\_update\_req] = 1

#### 11.1.16.3 Global A-Link/B-Link Clock Gating

A-Link and B-Link clocks are 2 global clocks used inside [FCH](#) for most of sub-IPs.

Software enables the global A-Link clock gate off function by programming:

1. FCH::MISC::CLKGATEDCNTRL[alinkclk\_gateoffen] = 1
2. FCH::PM::ISACONTROL[abclkgateen] = 1

Software enables the global B-Link clock gate off function by programming:

1. FCH::MISC::CLKGATEDCNTRL[blinkclk\_gateoffen] = 1
2. FCH::PM::ISACONTROL[abclkgateen] = 1

FCH::MISC::CLKGATEDCNTRL[alinkclk\_gateoffen] and FCH::MISC::CLKGATEDCNTRL[blinkclk\_gateoffen] are sticky bits.

FCH::PM::ISACONTROL[abclkgateen] is a non-sticky bit that should be re-programmed to 1 after resets defined in 11.1.15 [Sticky/non-sticky attribute of PMIO registers] if global A-Link/B-Link gating functions been enabled.

Note: to enable FCH\_SDP disconnect to allow LCLK deep sleep.

### 11.1.16.4 GPP CLKREQB Mapping Table

Table 183: GPP ClkREQB Mapping

ClkReq Map Register	Package Pin Name
FCH::MISC::GPPCLKCONTROL[gpp_clk11_clock_request_mapping]	BP_AGPI0115/ CLK_REQ11_L
FCH::MISC::GPPCLKCONTROL[gpp_clk12_clock_request_mapping]	BP_AGPI0116/ CLK_REQ12_L
FCH::MISC2::RMT_CLKCNTL_0_REG[gpp_clk01_clock_request_mapping]	BP_AGPI0257/ SGPIO1_CLK/ CLK_REQ01_L
FCH::MISC2::RMT_CLKCNTL_0_REG[gpp_clk02_clock_request_mapping]	BP_AGPI0258/ SGPIO2_CLK/ CLK_REQ02_L

### 11.1.17 Reset Overview

Below is definition of all kind of reset types:

Type 0 reset (S5 Reset): RsmRst and UsrRstB

Type 1 reset (reset initiated by SW or system): CF9, KBRst, Sync\_flood, ASF\_remote\_reset, Fail\_boot, Watchdog timer reset, toggling of PwrGood (SLP\_S3#/SLP\_S5# remain deasserted at high), SHUTDOWN command, INIT/PORT92

Type 2 reset (Sleep Reset): S3/S4/S5 reset

Type 3 reset (Fatal\_error\_reset or reset caused by hw exception): 4s-shutdown, thermal trip, ASF\_remotePowerDown

Type 4 reset (any reset from above): Type 0 or Type 1 or Type 2 or Type 3

Table 184: Reset Type

Register block	Power domain	Reset source
PCI Configure	S0	Type 4
<a href="#">SMI</a> (11.3.3 [SMI Registers])	S5	Some register: Type 0 or Type 3 Some register: Type 4
PMIO (11.3.9.3 [Power Management (PM) Registers and Standard ACPI Registers])	S5	Some register: Type 0 Some register: Type 4
ACPI (11.3.9.3 [Power Management (PM) Registers and Standard ACPI Registers])	S5	Type 0 or Type 3
WatchDog (11.3.5 [Watchdog Timer (WDT) Registers])	S5	Type 0
HPET (11.3.4 [High Precision Event Timer (HPET) Registers])	S0	Type 4
IOMUX (11.3.10.1 [IOMUX Registers])	S5 (0-42) S0 (67-148)	S5-IoMux: Type 0 S0-IoMux: Type 4
MISC (11.3.9.1 [Miscellaneous (MISC) Registers])	S5	Most registers are Type 0 Some CLK register are Type 4, 0x4C, 0x94, ...
Serial Debug	S5	Type 0
Shadow System Counter	S5	Type 0 or Type 1
GPIO-0 (11.3.10.2 [GPIO Registers])	S5	Type 0 or Type 1
GPIO-1 (11.3.10.2 [GPIO Registers])	S0	Type 4
GPIO-2 (11.3.10.2 [GPIO Registers])	S0	Type 4
GPIO-3 (11.3.10.2 [GPIO Registers])	S0	Type 4



GPIO-4 (11.3.10.2 [GPIO Registers])	S0	Type 4
Wake Alarm (ACDC timer) (11.3.6 [Wake Alarm Device (AcDcTimer) Registers])	S5	Type 0
AOAC (11.3.7 [Always On Always Connected (AOAC) Registers])	S5	Type 0 or Type 1

Below are the simplified top level reset paths

When a reset is generated from acpi\_s5, all S0 logic within [FCH](#) are reset by it. Other IPs within SOC are not reset by it directly. Instead, they are being reset by [MP1](#). CpuPwrGood is connected to MP1 and MP1 treats it as an interrupt. Upon assertion of this signal, MP1 will proceed to do its "house cleaning" activities first; then it will issue resets to all other IPs that are not inside FCH. CpuPwrGood is the actual reset to MP1. When this signal is deasserted (to low), MP1 will propagate it reset to all IPs within SOC. We will define a warm reset as an assertion of CpuRstB and cold reset of toggling of both CpuRstB (low) and CpuPwrGood (low).

*Table 185: Reset Behavior Overview*

S5 reset	Behavior
RSMRST_L	Reset all logic (S0 and S5). In addition, SOC will go back to default power state (always-off, always-on, previous state).
SYS_RST_L	Reset all logic (S0 and S5).
Sleep induced reset	Behavior
SLEEP3/4/5	Sleep entry to S3/4/5 will assert cold reset to all S0 logic prior to assertion of SLP_S3_L/SLP_S5_L.
Pin included reset	Behavior
PWR_BTN_L	4 second override – unconditional shutdown (Sleep S5) → generates cold reset and will reset all S0 logic..
THERMTRIP_L	Over temperature indicator from CPU – unconditional shutdown (Sleep S5) → generates cold reset and will reset all S0 logic.
KBRST_L	Keyboard reset → reset to S0 logic; configurable to warm or cold reset.
PWR_GOOD	Deassertion of PWRGOOD will always generate cold reset to S0 logic.
SW induced reset	Behavior
CF9	Write to CF9 → reset S0 logic; configurable to warm or cold reset; or momentary S0 → S5 → S0 transition.
Port92	Write Port 92 (FAST_INIT) → reset S0 logic; configurable to warm or cold reset. Port92 function has been deprecated.
SW write to PMIO_Reg 0xC4[6], ResetAllAcpi	Generates reset to S0 and S5 logic.
HW based reset	Behavior
watchdog timer	watchdog timer → reset S0 logic; configurable to warm or cold reset.
AMD (boot_timer) watchdog timer	AMD defined watchdog timer → reset S0 logic; configurable to warm or cold reset.
Remote Command reset	Behavior
ASF – remote reset	Reset S0 logic; configurable to warm or cold reset.
ASF – remote sleep	Remote sleep S5 command – logic will sequence to S5 and assert cold reset to all S0 logic.
Internal events	Behavior
<a href="#">Shutdown</a> (message from CPU)	Triple faults in CPU will cause an internal SHUTDOWN message broadcasted. FCH will generate a reset to S0 logic; configurable to warm or cold reset.
SYNC_FLOOD (message)	Internal data fabric logic detects an error (eg. parity error) and broadcasts an internal SYNC_FLOOD message. FCH will generate a reset to S0 logic;

configurable to warm or cold reset.
-------------------------------------

### 11.1.18 ROM Address Mapping Support in FCH implementation

[FCH](#) needs to implement the following register bits.

1. spirom\_addr\_32 (FCH::LPCHOSTSPIREG::ADDR32CTRL0): 0: 24-bit SPI ROM address, default. 1: 32-bit SPI ROM address.
2. spirom\_page[31:24] (FCH::LPCHOSTSPIREG::ADDR32CTRL3[spirom\_page\_31\_24]): these bits will be used to control the address mapping, "XOR" will be used for spirom\_page[31:24] and HostMemAddr[31:24] to produce SPIROMAddr[31:24].

Following table shows the address mapping.

*Table 186: ROM Address Mapping Support in FCH implementation*

	ROM1 (1MB)	ROM2 (16MB)	ROM3 (64MB)
Default address space	0x0000_0000 - 0x000F_FFFF	0xFF00_0000 - 0xFFFF_FFFF	0xFD_0000_0000 - 0xFD_03FF_FFFF
SPI ROM, 24bit address	0xF0_0000 - 0xFF_FFFF (top 1MB of 16MB)	0x00_0000 – 0xFF_FFFF (16MB)	0x00_0000 – 0xFF_FFFF (16MB)
SPI ROM, 32bit address: Bit[31:24] are before XOR with SPIROM_page	0xFFF0_0000 – 0xFFFF_FFFF (top 1MB of 4GB)	0xFF00_0000 – 0xFFFF_FFFF (top 16MB of 4GB)	0xFC00_0000 – 0xFFFF_FFFF (top 64MB of 4GB)

### 11.1.19 RTC

#### 11.1.19.1 RTC Register

The value in Time/Alarm or CMOS registers or CMOS RAM is undefined/indeterministic when power up first time. It is highly recommended to add a checksum or CRC over CMOS RAM so BIOS can detect whether CMOS has been corrupted or erased.

You can see RTC registers at 11.3.1 [Legacy Block Configuration Registers (IO)]

#### 11.1.19.2 RTC Extended Register

The value in these RTC Extended registers is undefined/indeterministic when power up first time.

You can see RTC Extended registers at 11.3.9.4 [RTC External Registers]

#### 11.1.19.3 External RTC Decode

To support external RTC, using eSPI bus to decode RTC instead of using ACPI bus.

1. Program FCH::PM::RTCCONTROL[rtcdecodedis] to 1'b1 to disable the integrated RTC decoding. The default value for this bit is disable (1'b0) which means integrated RTC decode is working.
2. Config eSPI IO space to decode for RTC ports. Related registers:
  1. LEGACYIOx00000070: FCH::IO::NMI\_ENABLE
  2. LEGACYIOx00000071: FCH::IO::RTCDATAPORT
  3. LEGACYIOx00000072: FCH::IO::ALTERNATRTCADDRPORT
  4. LEGACYIOx00000073: FCH::IO::ALTERNATRTCDATAPORT

Note: the decode of FCH::IO::NMI\_ENABLE[nmienableb] is also blocked by FCH::PM::RTCCONTROL[rtcdecodedis]. Therefore, firmware has to config FCH::IO::NMI\_ENABLE[nmienableb] before disabling integrated RTC decoding.

### 11.1.20 Strap Definition

Table 187: Strap Pins/Function

Ball Name	Strap Name	Type	Default Value	Description
ESPI_CLK0	CLKGEN	II	NA	Defines clock generator "0" – Use 100MHz PCIE clock as reference clock and generate internal clocks only. Note a 48MHz crystal is still required in this configuration "1" – Use 48MHz crystal clock and generate both internal and external clocks External pull-up/Pull-down is required on the pin. (This strap does have a weak internal pull-down resistor (50K).)
UART1_TXD, AGPIO109	ROMTYPE[1:0]	II	NA	The strap pin should be configured to the corresponding state that matches the hardware ROM type installed. External pull-up/Pull-down is required on the pin. 00: Reserved 01: SPI ROM 10: eSPI with SAFS support 11: eSPI without SAFS support
ESPI_CLK1	AlternateImage	II	NA	Note this strap does not have any real hardware function. It only serves as a software bit for <a href="#">ASP</a> to read. This strap does have a weak internal pull-down resistor (50K). This strap has no meaning if the ROM is 16MB or less 1: ASP should modify SPI page register bits [25:24] to remap physical ROM to upper image 0: ASP should not modify SPI page register bits [25:24]
ESPI_CLK2	WAFL_TRAINING_DISABLE	II	0	Note this strap does not have any real hardware function. It only serves as a software bit to be read by ASP/ <a href="#">MP1</a> . This strap does have a weak internal pull-down resistor (50K). <ul style="list-style-type: none"> <li>WAFL_TRAINING_DISABLE = 0 (default) means WAFL link will be trained.</li> <li>WAFL_TRAINING_DISABLE = 1 means WAFL link will not be trained.</li> </ul>

Even though some of the pins may have integrated pull-up enabled, external pull-up/down are required on all strap pins except for the two pins explicitly mentioned above.

Type I strap: Use BP\_RSMRST\_L rising edge to latch the strap value. The strap pad can only locate in S5.

Type II strap: Use BP\_PWR\_GOOD as source and after S0 power up, count another counter (16 osc clock cycles), then latch the strap done. All straps on S0 pads use this type of strap.

*Table 188: Address Space Mapping under APB BUS*

Function name	Address Mapping
I2C_0	0xFEDC_2xxx
I2C_1	0xFEDC_3xxx
I2C_2	0xFEDC_4xxx
I2C_3	0xFEDC_5xxx
I2C_4	0xFEDC_6xxx
DMA_0	0xFEDC_7xxx
DMA_1	0xFEDC_8xxx
UART_0	0xFEDC_9xxx
UART_1	0xFEDC_Axxx
I2C_5	0xFEDC_Bxxx
DMA_2	0xFEDC_Cxxx
DMA_3	0xFEDC_Dxxx
UART_2	0xFEDC_Exxx
UART_3	0xFEDC_Fxxx
I3C_0	0xFEDD_2xxx
I3C_1	0xFEDD_3xxx
I3C_2	0xFEDD_4xxx
I3C_3	0xFEDD_6xxx
ACPI	0xFED8_0000 8KB memory Space
ACPI	0xFD_F95F_FF00 256B memory Space
SPI	0xFD_F95F_FE00 256B memory Space
SPI ROM	Top of 4G & 1M; 256B memory Space

## 11.2 FCH BTS Check Table

*Table 189: FCH BTS Common Table*

RegisterField	Type	Content
FCH::MISC::CLKGATEDCNTL[blinkclk_gateoffen]	Check	1b
FCH::MISC::CLKGATEDCNTL[alinkclk_gateoffen]	Check	1b

## 11.3 Registers

### 11.3.1 Legacy Block Configuration Registers (IO)

#### 11.3.1.1 Registers

**IOx00C01\_x00 [PCI INT[H#,G#,F#,E#,D#,C#,B#,A#] Map] (FCH::IO::PciIntMap)**

Read-write. Reset: 1Fh.

\_aliasIO; IOx00C01\_x00; IO=0000\_0000h; DataPortWrite=FCH::IO::PCI\_INTR\_INDEX

Bits	Description
7:5	Reserved.
4:0	<b>Pci2IntrMap</b> . Read-write. Reset: 1Fh. If (FCH::IO::PCI_INTR_INDEX[7] == 1) then Pci2IntrMap specifies mapping of INT[H#:A#] to APIC interrupt number. If (FCH::IO::PCI_INTR_INDEX[7] == 0) then Pci2IntrMap specifies mapping of INT[H#:A#] to PIC interrupt number.

**IOx00C01\_x08 [Intr\_Misc\_Map] (FCH::IO::IntrMiscMap)**

Read-write. Reset: 00h.

\_aliasIO; IOx00C01\_x08; IO=0000\_0000h; DataPortWrite=FCH::IO::PCI\_INTR\_INDEX

Bits	Description										
7:6	<b>Pci2Intr15Map</b> . Read-write. Reset: 0h. <b>ValidValues:</b> <table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>IRQ15 mapped to legacy IDE.</td></tr> <tr> <td>1h</td><td>IRQ15 mapped to SATA IDE.</td></tr> <tr> <td>2h</td><td>IRQ15 mapped to SATA2.</td></tr> <tr> <td>3h</td><td>IRQ15 come from Serial IRQ or PCI interrupt.</td></tr> </table>	Value	Description	0h	IRQ15 mapped to legacy IDE.	1h	IRQ15 mapped to SATA IDE.	2h	IRQ15 mapped to SATA2.	3h	IRQ15 come from Serial IRQ or PCI interrupt.
Value	Description										
0h	IRQ15 mapped to legacy IDE.										
1h	IRQ15 mapped to SATA IDE.										
2h	IRQ15 mapped to SATA2.										
3h	IRQ15 come from Serial IRQ or PCI interrupt.										
5:4	<b>Pci2Intr14Map</b> . Read-write. Reset: 0h. <b>ValidValues:</b> <table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>IRQ14 mapped to legacy IDE.</td></tr> <tr> <td>1h</td><td>IRQ14 mapped to SATA IDE.</td></tr> <tr> <td>2h</td><td>IRQ14 mapped to SATA2.</td></tr> <tr> <td>3h</td><td>IRQ14 mapped to Serial IRQ or PCI interrupt.</td></tr> </table>	Value	Description	0h	IRQ14 mapped to legacy IDE.	1h	IRQ14 mapped to SATA IDE.	2h	IRQ14 mapped to SATA2.	3h	IRQ14 mapped to Serial IRQ or PCI interrupt.
Value	Description										
0h	IRQ14 mapped to legacy IDE.										
1h	IRQ14 mapped to SATA IDE.										
2h	IRQ14 mapped to SATA2.										
3h	IRQ14 mapped to Serial IRQ or PCI interrupt.										
3	<b>PciIntrIrq12</b> . Read-write. Reset: 0. 0=IMC as IRQ12 input source. 1=Serial IRQ or PCI devices as IRQ12 input source.										
2	<b>PciIntrIrq8</b> . Read-write. Reset: 0. 0=RTC is IRQ8 input source. 1=Serial IRQ or PCI devices as IRQ8 input source.										
1	<b>PciIntrIrq1</b> . Read-write. Reset: 0. 0=IMC as IRQ1 input source. 1=Serial IRQ or PCI devices as IRQ1 input source.										
0	<b>PciIntrIrq0</b> . Read-write. Reset: 0. 0=8254 timer as IRQ0 input source. 1=Serial IRQ or PCI devices as IRQ0 input source.										

**IOx00C01\_x09 [Intr\_Misc0Map] (FCH::IO::IntrMisc0Map)**

Read-write. Reset: E7h.

\_aliasIO; IOx00C01\_x09; IO=0000\_0000h; DataPortWrite=FCH::IO::PCI\_INTR\_INDEX

Bits	Description
7	<b>IntrDelay.</b> Read-write. Reset: 1. INTR 600 ns delay.
6	<b>IRQ12FilterEnable.</b> Read-write. Reset: 1. IRQ12 filter enable.
5	<b>IRQ1FilterEnable.</b> Read-write. Reset: 1. IRQ1 filter enable.
4	<b>IrqInputEn.</b> Read-write. Reset: 0. 0=Mask off IRQ input. 1=Enable IRQ input.
3	<b>MaskIrq1Irq12.</b> Read-write. Reset: 0. 0=Enable IRQ1 and IRQ12. 1=Mask off IRQ1 and IRQ12.
2	<b>Merge_Ec_irq12.</b> Read-write. Reset: 1. 0=Route serial IRQ12 to USB IRQ12 input. 1=Route IMC IRQ12 to USB IRQ12 input.
1	<b>Merge_Ec_irq1.</b> Read-write. Reset: 1. 0=Route serial IRQ1 to USB IRQ1 input. 1=Route IMC IRQ1 to USB IRQ1 input.
0	<b>IntMap.</b> Read-write. Reset: 1. 0=INT0 in IOAPIC comes from IRQ0 in PIC, INT2 in IOAPIC comes from INTR in PIC. 1=INT2 in IOAPIC comes from IRQ0 in PIC, INT0 in IOAPIC comes from INTR in PIC.

**IOx00C01\_x0A [Intr\_Misc1Map] (FCH::IO::IntrMisc1Map)**

Read-write. Reset: 00h.

\_aliasIO; IOx00C01\_x0A; IO=0000\_0000h; DataPortWrite=FCH::IO::PCI\_INTR\_INDEX

Bits	Description
7:0	<b>HPET.</b> Read-write. Reset: 00h. Writes to this register update the bits in FCH::TMR::HPET::TMR0_CONF_CAP_H [7:0], FCH::TMR::HPET::TMR1_CONF_CAP_H [7:0] and FCH::TMR::HPET::TMR2_CONF_CAP_H [7:0]; All 3 registers, HPETx104[7:0], HPETx124[7:0], and HPETx144[7:0], are updated at the same time. FCH::IO::IntrMisc1Map updates the lower 8 bits. FCH::IO::IntrMisc2Map updates the upper 8 bits.

**IOx00C01\_x0B [Intr\_Misc2Map] (FCH::IO::IntrMisc2Map)**

Read-write. Reset: 00h.

\_aliasIO; IOx00C01\_x0B; IO=0000\_0000h; DataPortWrite=FCH::IO::PCI\_INTR\_INDEX

Bits	Description
7:0	<b>HPET.</b> Read-write. Reset: 00h. Writes to this register update this bits in FCH::TMR::HPET::TMR0_CONF_CAP_H [15:8], FCH::TMR::HPET::TMR1_CONF_CAP_H [15:8] and FCH::TMR::HPET::TMR2_CONF_CAP_H [15:8]; All 3 registers, HPETx104[15:8], HPETx124[15:8], and HPETx144[15:8], are updated at the same time. FCH::IO::IntrMisc1Map updates the lower 8 bits. FCH::IO::IntrMisc2Map updates the upper 8 bits.

**IOx00C01\_x0C [PCIInterruptMap] (FCH::IO::PCIInterruptMap)**

Read-write. Reset: 1Fh.

\_aliasIO; IOx00C01\_x0C; IO=0000\_0000h; DataPortWrite=FCH::IO::PCI\_INTR\_INDEX

Bits	Description
7:5	Reserved.
4:0	<b>Pci2IntrMap.</b> Read-write. Reset: 1Fh. If (FCH::IO::PCI_INTR_INDEX[7] == 1), then Pci2IntrMap specifies the APIC interrupt number that the corresponding PCI interrupt maps to. If (FCH::IO::PCI_INTR_INDEX[7] == 0), then Pci2IntrMap specifies the PIC interrupt number that the corresponding PCI interrupt maps to.

**LEGACYIOx00000000 (FCH::IO::DMA\_CH\_0)**

Read-write. Reset: 0000h.

Dma\_Ch 0 register

\_aliasHOSTLEGACY; LEGACYIOx00000000; LEGACYIO=FF00\_0000h

Bits	Description
15:0	<b>dma_ch_0.</b> Read-write. Reset: 0000h. DMA1 Ch0 Base and Current Address

**LEGACYIOx00000002 (FCH::IO::DMA\_CH\_1)**

Read-write. Reset: 0000h.

Dma\_Ch 1 register

\_aliasHOSTLEGACY; LEGACYIOx00000002; LEGACYIO=FF00\_0000h

**Bits Description**15:0 **dma\_ch\_1.** Read-write. Reset: 0000h. DMA1 Ch1 Base and Current Address**LEGACYIOx00000004 (FCH::IO::DMA\_CH\_2)**

Read-write. Reset: 0000h.

Dma\_Ch 2 register

\_aliasHOSTLEGACY; LEGACYIOx00000004; LEGACYIO=FF00\_0000h

**Bits Description**15:0 **dma\_ch\_2.** Read-write. Reset: 0000h. DMA2 Ch2 Base and Current Address**LEGACYIOx00000006 (FCH::IO::DMA\_CH\_3)**

Read-write. Reset: 0000h.

Dma\_Ch 3 register

\_aliasHOSTLEGACY; LEGACYIOx00000006; LEGACYIO=FF00\_0000h

**Bits Description**15:0 **dma\_ch\_3.** Read-write. Reset: 0000h. DMA1 Ch3 Base and Current Address**LEGACYIOx00000008 (FCH::IO::DMA\_STATUS)**

Read-write. Reset: 00h.

Dma\_Status register

\_aliasHOSTLEGACY; LEGACYIOx00000008; LEGACYIO=FF00\_0000h

**Bits Description**7:0 **dma\_status.** Read-write. Reset: 00h. Returns status when read command for write**LEGACYIOx00000009 (FCH::IO::DMA\_WRITEREQUEST)**

Read-write. Reset: 00h.

Dma\_WriteRequest register

\_aliasHOSTLEGACY; LEGACYIOx00000009; LEGACYIO=FF00\_0000h

**Bits Description**7:0 **dma\_writerequest.** Read-write. Reset: 00h. Request register.**LEGACYIOx0000000A (FCH::IO::DMA\_WRITEMASK)**

Read-write. Reset: 00h.

Dma\_WriteMask register

\_aliasHOSTLEGACY; LEGACYIOx0000000A; LEGACYIO=FF00\_0000h

**Bits Description**7:0 **dma\_writemask.** Read-write. Reset: 00h. Channel mask register.**LEGACYIOx0000000B (FCH::IO::DMA\_WRITEMODE)**

Read-write. Reset: 00h.

Dma\_WriteMode register

\_aliasHOSTLEGACY; LEGACYIOx0000000B; LEGACYIO=FF00\_0000h

**Bits Description**7:0 **dma\_writemode.** Read-write. Reset: 00h. Mode register.

**LEGACYIOx0000000C (FCH::IO::DMA\_CLEAR)**

Read-write. Reset: 00h.

Dma\_Clear register

\_aliasHOSTLEGACY; LEGACYIOx0000000C; LEGACYIO=FF00\_0000h

Bits	Description
7:0	<b>dma_clear.</b> Read-write. Reset: 00h. Channel 0-3 DMA clear byte pointer

**LEGACYIOx0000000D (FCH::IO::DMA\_MASTERCLR)**

Read-write. Reset: 00h.

Dma\_MasterClr register

\_aliasHOSTLEGACY; LEGACYIOx0000000D; LEGACYIO=FF00\_0000h

Bits	Description
7:0	<b>dma_masterclr.</b> Read-write. Reset: 00h. Intermediate register.

**LEGACYIOx0000000E (FCH::IO::DMA\_CLRMASK)**

Read-write. Reset: 00h.

Dma\_ClrMask register

\_aliasHOSTLEGACY; LEGACYIOx0000000E; LEGACYIO=FF00\_0000h

Bits	Description
7:0	<b>dma_clrmask.</b> Read-write. Reset: 00h. Channel 0-3 DMA Clear Mask

**LEGACYIOx0000000F (FCH::IO::DMA\_ALLMASK)**

Read-write. Reset: 00h.

Dma\_AllMask register

\_aliasHOSTLEGACY; LEGACYIOx0000000F; LEGACYIO=FF00\_0000h

Bits	Description
7:0	<b>dma_allmask.</b> Read-write. Reset: 00h. Mask register.

**LEGACYIOx00000020 (FCH::IO::INTRCNTRL1REG1)**

Read-write. Reset: 00h.

IntrCntrl1Reg1 register

\_aliasHOSTLEGACY; LEGACYIOx00000020; LEGACYIO=FF00\_0000h

Bits	Description
7:0	<b>intrcntrl1reg1.</b> Read-write. Reset: 00h. <b>Description:</b> IRQ0 IRQ7: Read IRR, ISR Write ICW1, OCW2, OCW3

**LEGACYIOx00000021 (FCH::IO::INTRCNTRL1REG2)**

Read-write. Reset: 00h.

IntrCntrl1Reg2 register

\_aliasHOSTLEGACY; LEGACYIOx00000021; LEGACYIO=FF00\_0000h

Bits	Description
7:0	<b>intrcntrl1reg2.</b> Read-write. Reset: 00h. <b>Description:</b> IRQ0 IRQ7: Read IMR Write ICW2, ICW3, ICW4, OCW1



**LEGACYIOx00000022 (FCH::IO::IMCR\_INDEX)**

Read-write. Reset: 00h.

IMCR\_Index register

\_aliasHOSTLEGACY; LEGACYIOx00000022; LEGACYIO=FF00\_0000h

Bits	Description
7:0	<b>imcr_index.</b> Read-write. Reset: 00h. The IMCR is supported by two read/writeable IO ports 22/23h which are used as index and data port respectively. The actual IMCR register is located at index 70h.

**LEGACYIOx00000023 (FCH::IO::IMCR\_DATA)**

Read-write. Reset: 00h.

IMCR\_Data register

\_aliasHOSTLEGACY; LEGACYIOx00000023; LEGACYIO=FF00\_0000h

Bits	Description
7:0	<b>imcr_data.</b> Read-write. Reset: 00h. The IMCR is supported by two read/writeable IO ports 22/23h which are used as index and data port respectively. The actual IMCR register is located at index 70h and it is at bit 0. The actual IMCR bit can only be accessed when bit port 22 is set to 70h. Default value of IMCR is 0.

**LEGACYIOx00000040 (FCH::IO::TIMERCH0)**

Read-write. Reset: 00h.

TimerCh0 register

\_aliasHOSTLEGACY; LEGACYIOx00000040; LEGACYIO=FF00\_0000h

Bits	Description
7:0	<b>timerch0.</b> Read-write. Reset: 00h. <b>Description:</b> 8254 Timer 1: Counter 0 Data Port This timer is known as the System Clock timer and it is always on. It is clocked internally by OSC/12 (1.19318MHz), and asserts IRQ0 every time the timer rolls over. This timer is used for time-of-day, diskette time-out, and other system timing functions.

**LEGACYIOx00000041 (FCH::IO::TIMERCH1)**

Read-write. Reset: 00h.

TimerCh1 register

\_aliasHOSTLEGACY; LEGACYIOx00000041; LEGACYIO=FF00\_0000h

Bits	Description
7:0	<b>timerch1.</b> Read-write. Reset: 00h. <b>Description:</b> 8254 Timer 1: Counter 1 Data Port This timer is normally used for ISA refresh cycles and is also clocked by OSC/12 (1.19818MHz). Since this refresh function is no longer needed (we don't have an external ISA bus), it can be used as a general purpose timing function.

**LEGACYIOx00000042 (FCH::IO::TIMERCH2)**

Read-write. Reset: 00h.

TimerCh2 register

\_aliasHOSTLEGACY; LEGACYIOx00000042; LEGACYIO=FF00\_0000h

Bits	Description
7:0	<b>timerch2.</b> Read-write. Reset: 00h. <b>Description:</b> 8254 Timer 1: Counter 2 Data Port This is the speaker tone generator and is enabled by IO port 61H. It is clocked by OSC/12 (1.19318MHz) and directly drives the output SPKR that goes to a speaker.

**LEGACYIOx00000043 (FCH::IO::TMR1CNTRLWORD)**

Write-only. Reset: 00h.

Tmr1CntrlWord register: This is the control word to access the 8254 timer 1. It is used to select which counter will be accessed and how it will be accessed. This register specifies the counter, the operating mode, the order and size of the count value, and whether it counts down in a 16 bit or [BCD](#) format.

If a counter is programmed to read or write two-byte counts, the following precaution applies: A program must not transfer control between writing the first and second byte to another routine which also writes into that same counter otherwise, the counter will be loaded with an incorrect value. The count must always be completely loaded with both bytes.

Tmr1CntrlWord is write-only. Read always returns FF.

\_aliasHOSTLEGACY; LEGACYIOx00000043; LEGACYIO=FF00\_0000h

Bits	Description
7:6	<b>counterselect.</b> Write-only. Reset: 0h. <b>Description:</b> 00: Select counter 0 01: Select counter 1 10: Select counter 2 11: Read back command
5:4	<b>cmmandselect.</b> Write-only. Reset: 0h. <b>Description:</b> 00: Counter latch command 01: Read/write least significant byte 10: Read/write most significant byte 11: Read/write least, and then most significant byte
3:1	<b>modeselect.</b> Write-only. Reset: 0h. <b>Description:</b> 000: Asserts OUT signal at end of count 001: Hardware re-triggerable one-shot 010: Rate generator 011: Square wave output 100: Software triggered strobe 101: Hardware triggered strobe 110 111: Not used
0	<b>cntdownselect.</b> Write-only. Reset: 0. <b>Description:</b> 0: Binary countdown 1: <a href="#">BCD</a> countdown

**LEGACYIOx00000060 (FCH::IO::IO\_PORT\_60)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; LEGACYIOx00000060; LEGACYIO=FF00\_0000h

Bits	Description
7:0	<b>io_port_60.</b> Read-write. Reset: 00h. This is for Legacy USB emulation, please refer to 4.25 USB Legacy register for detail

**LEGACYIOx00000061 (FCH::IO::NMI\_STATUS)**

Read-write.

Nmi\_Status register: Independent read and write registers will be accessed at this port. When writing to port 61H, bits[3:0] allow software to enable/disable parity error NMI's and control the speaker timer. When reading port 61H, status on parity errors, speaker count, speaker control and refresh cycles is returned.

\_aliasHOSTLEGACY; LEGACYIOx00000061; LEGACYIO=FF00\_0000h

Bits	Description
7	<b>parerr_nmi.</b> Read-write. Reset: X. NMI is caused by parity error (either PERR# or SERR#). [Read-only]
6	<b>iochk_nmi.</b> Read-write. Reset: X. NMI is triggered by serial IOCHK. [Read-only]
5	<b>spkrclk.</b> Read-write. Reset: X. The output of the counter 2. [Read-only]
4	<b>refclk.</b> Read-write. Reset: X. The output of the counter 1 (8254). [Read-only]
3	<b>iochk_nmi_en.</b> Read-write. Reset: 1. <b>Description:</b> 0: Enable IoChk to NMI generation 1: Disable IoChk to NMI generation
2	<b>parity_nmi_en.</b> Read-write. Reset: 1. <b>Description:</b> 0: Enable Parity Error to NMI generation (from SERR# or PERR#) 1: Disable Parity Error to NMI generation and clear bit 7
1	<b>spkrtmrenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Speaker timer off 1: Speaker timer on
0	<b>spkrenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable counter 2 1: Enable counter 2

**LEGACYIOx00000064 (FCH::IO::IO\_PORT\_64)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; LEGACYIOx00000064; LEGACYIO=FF00\_0000h

Bits	Description
7:0	<b>io_port_64.</b> Read-write. Reset: 00h. This is for Legacy USB emulation, please refer to 4.25 USB Legacy register for detail

**LEGACYIOx00000070 (FCH::IO::NMI\_ENABLE)**

Read-write. Reset: 80h.

Nmi\_Enable register

\_aliasHOSTLEGACY; LEGACYIOx00000070; LEGACYIO=FF00\_0000h

Bits	Description
7	<b>nmienableb.</b> Read-write. Reset: 1. <b>Description:</b> 0: NMI enable 1: NMI disable
6:0	<b>rtc_address_port.</b> Read-write. Reset: 00h. This is used with either internal RTC or external RTC

**LEGACYIOx00000071 (FCH::IO::RTCDATAPORT)**

Read-write. Reset: 00h.

RtcDataPort

\_aliasHOSTLEGACY; LEGACYIOx00000071; LEGACYIO=FF00\_0000h

Bits	Description
7:0	<b>rtc_data_port.</b> Read-write. Reset: 00h. This is used with either internal RTC or external RTC

**LEGACYIOx00000072 (FCH::IO::ALTERNATRTCADDRPORT)**

Read-write. Reset: 00h.

AlternatRtcAddrPort

\_aliasHOSTLEGACY; LEGACYIOx00000072; LEGACYIO=FF00\_0000h

Bits	Description
7:0	<b>alternatrtcaddrport</b> . Read-write. Reset: 00h. This is used with internal RTC. This port allows user to specify the full 8 bit address (instead of bank0/bank1 indexing) to access the 256 byte RTC RAM

**LEGACYIOx00000073 (FCH::IO::ALTERNATRTCdataport)**

Read-write. Reset: 00h.

AlternatRtcDataPort

\_aliasHOSTLEGACY; LEGACYIOx00000073; LEGACYIO=FF00\_0000h

Bits	Description
7:0	<b>alternatrtc_data_port</b> . Read-write. Reset: 00h. This is used with internal RTC in conjunction with port h72

**LEGACYIOx00000080 (FCH::IO::IO\_PORT\_80)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; LEGACYIOx00000080; LEGACYIO=FF00\_0000h

Bits	Description
7:0	<b>io_port_80</b> . Read-write. Reset: 00h. Write to this port will send data to be displayed on "POST Code display module"

**LEGACYIOx00000081 (FCH::IO::DMA\_PAGECH2)**

Read-write. Reset: 00h.

Dma\_PageCh2 register

\_aliasHOSTLEGACY; LEGACYIOx00000081; LEGACYIO=FF00\_0000h

Bits	Description
7:0	<b>dma_pagech2</b> . Read-write. Reset: 00h. DMA2 ch 2 page register

**LEGACYIOx00000082 (FCH::IO::DMA\_PAGECH3)**

Read-write. Reset: 00h.

Dma\_PageCh3 register

\_aliasHOSTLEGACY; LEGACYIOx00000082; LEGACYIO=FF00\_0000h

Bits	Description
7:0	<b>dma_pagech3</b> . Read-write. Reset: 00h. DMA2 ch 3 page register

**LEGACYIOx00000083 (FCH::IO::DMA\_PAGECH1)**

Read-write. Reset: 00h.

Dma\_PageCh1 register

\_aliasHOSTLEGACY; LEGACYIOx00000083; LEGACYIO=FF00\_0000h

Bits	Description
7:0	<b>dma_pagech1</b> . Read-write. Reset: 00h. DMA2 ch 1 page register

**LEGACYIOx00000084 (FCH::IO::DMA\_PAGE\_RESERVED1)**

Read-write. Reset: 00h.

Dma\_Page\_Reserved1 register

\_aliasHOSTLEGACY; LEGACYIOx00000084; LEGACYIO=FF00\_0000h

Bits	Description
7:0	<b>dma_page_reserved1</b> . Read-write. Reset: 00h. DMA Page Reserved1 register

**LEGACYIOx00000085 (FCH::IO::DMA\_PAGE\_RESERVED2)**

Read-write. Reset: 00h.

Dma\_Page\_Reserved2 register

\_aliasHOSTLEGACY; LEGACYIOx00000085; LEGACYIO=FF00\_0000h

Bits	Description
7:0	<b>dma_page_reserved2.</b> Read-write. Reset: 00h. DMA Page Reserved2 register

**LEGACYIOx00000086 (FCH::IO::DMA\_PAGE\_RESERVED3)**

Read-write. Reset: 00h.

Dma\_Page\_Reserved3 register

\_aliasHOSTLEGACY; LEGACYIOx00000086; LEGACYIO=FF00\_0000h

Bits	Description
7:0	<b>dma_page_reserved3.</b> Read-write. Reset: 00h. DMA Page Reserved3 register

**LEGACYIOx00000087 (FCH::IO::DMA\_PAGECH0)**

Read-write. Reset: 00h.

Dma\_PageCh0 register

\_aliasHOSTLEGACY; LEGACYIOx00000087; LEGACYIO=FF00\_0000h

Bits	Description
7:0	<b>dma_pagech0.</b> Read-write. Reset: 00h. DMA2 ch 0 page register

**LEGACYIOx00000088 (FCH::IO::DMA\_PAGE\_RESERVED4)**

Read-write. Reset: 00h.

Dma\_Page\_Reserved4 register

\_aliasHOSTLEGACY; LEGACYIOx00000088; LEGACYIO=FF00\_0000h

Bits	Description
7:0	<b>dma_page_reserved4.</b> Read-write. Reset: 00h. Dma Page Reserved4 register

**LEGACYIOx00000089 (FCH::IO::DMA\_PAGECH6)**

Read-write. Reset: 00h.

Dma\_PageCh6 register

\_aliasHOSTLEGACY; LEGACYIOx00000089; LEGACYIO=FF00\_0000h

Bits	Description
7:0	<b>dma_pagech6.</b> Read-write. Reset: 00h. DMA2 ch 6 page register

**LEGACYIOx0000008A (FCH::IO::DMA\_PAGECH7)**

Read-write. Reset: 00h.

Dma\_PageCh7 register

\_aliasHOSTLEGACY; LEGACYIOx0000008A; LEGACYIO=FF00\_0000h

Bits	Description
7:0	<b>dma_pagech7.</b> Read-write. Reset: 00h. DMA2 ch 7 page register

**LEGACYIOx0000008B (FCH::IO::DMA\_PAGECH5)**

Read-write. Reset: 00h.

Dma\_PageCh5 register

\_aliasHOSTLEGACY; LEGACYIOx0000008B; LEGACYIO=FF00\_0000h

Bits	Description
7:0	<b>dma_pagech5.</b> Read-write. Reset: 00h. DMA2 ch 5 page register

**LEGACYIOx0000008C (FCH::IO::DMA\_PAGE\_RESERVED5)**

Read-write. Reset: 00h.

Dma\_Page\_Reserved5 register

\_aliasHOSTLEGACY; LEGACYIOx0000008C; LEGACYIO=FF00\_0000h

Bits	Description
7:0	<b>dma_page_reserved5.</b> Read-write. Reset: 00h. Dma Page Reserved5 register

**LEGACYIOx0000008D (FCH::IO::DMA\_PAGE\_RESERVED6)**

Read-write. Reset: 00h.

Dma\_Page\_Reserved6 register

\_aliasHOSTLEGACY; LEGACYIOx0000008D; LEGACYIO=FF00\_0000h

Bits	Description
7:0	<b>dma_page_reserved6.</b> Read-write. Reset: 00h. Dma Page Reserved6 register

**LEGACYIOx0000008E (FCH::IO::DMA\_PAGE\_RESERVED7)**

Read-write. Reset: 00h.

Dma\_Page\_Reserved7 register

\_aliasHOSTLEGACY; LEGACYIOx0000008E; LEGACYIO=FF00\_0000h

Bits	Description
7:0	<b>dma_page_reserved7.</b> Read-write. Reset: 00h. Dma Page Reserved7 register

**LEGACYIOx0000008F (FCH::IO::DMA\_REFRESH)**

Read-write. Reset: 00h.

Dma\_Refresh register

\_aliasHOSTLEGACY; LEGACYIOx0000008F; LEGACYIO=FF00\_0000h

Bits	Description
7:0	<b>dma_refresh.</b> Read-write. Reset: 00h. DMA2 ch4 page register.

**LEGACYIOx00000092 (FCH::IO::FASTINIT)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; LEGACYIOx00000092; LEGACYIO=FF00\_0000h

Bits	Description
7:2	Reserved.
1	<b>a20enb.</b> Read-write. Reset: 0. <b>Description:</b> A20Enable Bar bit if set to 1 A20M# function is disabled.
0	<b>fastinit.</b> Read-write. Reset: 0. <b>Description:</b> FAST_INIT. This read/write bit provides a fast software executed processor reset function. Writing a 1 to this bit will cause the INIT assertion for approximately 4ms. Before another INIT pulse can be generated via this register, this bit must be written back to a 0.

**LEGACYIOx000000A0 (FCH::IO::INTRCNTRL2REG1)**

Read-write. Reset: 00h.

IntrCntrl2Reg1 register

\_aliasHOSTLEGACY; LEGACYIOx000000A0; LEGACYIO=FF00\_0000h

Bits	Description
7:0	<b>intrcntrl2reg1.</b> Read-write. Reset: 00h. <b>Description:</b> IRQ8 IRQ15: Read IRR, ISR Write ICW1, OCW2, OCW3

**LEGACYIOx000000A1 (FCH::IO::INTRCNTRL2REG2)**

Read-write. Reset: 00h.

IntrCntrl2Reg2 register

\_aliasHOSTLEGACY; LEGACYIOx000000A1; LEGACYIO=FF00\_0000h

Bits	Description
7:0	<b>intrcntrl2reg2.</b> Read-write. Reset: 00h. <b>Description:</b> IRQ8 IRQ15: Read IMR Write ICW2, ICW3, ICW4, OCW1

**LEGACYIOx000000C0 (FCH::IO::DMA2\_CH4ADDR)**

Read-write. Reset: 00h.

Dma2\_Ch4Addr register

\_aliasHOSTLEGACY; LEGACYIOx000000C0; LEGACYIO=FF00\_0000h

Bits	Description
7:0	<b>dma2_ch4addr.</b> Read-write. Reset: 00h. DMA2 Ch4 Base and Current Address

**LEGACYIOx000000C2 (FCH::IO::DMA2\_CH4CNT)**

Read-write. Reset: 00h.

Dma2\_Ch4Cnt register

\_aliasHOSTLEGACY; LEGACYIOx000000C2; LEGACYIO=FF00\_0000h

Bits	Description
7:0	<b>dma2_ch4cnt.</b> Read-write. Reset: 00h. DMA2 Ch4 Base and Current Count

**LEGACYIOx000000C4 (FCH::IO::DMA2\_CH5ADDR)**

Read-write. Reset: 00h.

Dma2\_Ch5Addr register

\_aliasHOSTLEGACY; LEGACYIOx000000C4; LEGACYIO=FF00\_0000h

Bits	Description
7:0	<b>dma2_ch5addr.</b> Read-write. Reset: 00h. DMA2 Ch5 Base and Current Address

**LEGACYIOx000000C6 (FCH::IO::DMA2\_CH5CNT)**

Read-write. Reset: 00h.

Dma2\_Ch5Cnt register

\_aliasHOSTLEGACY; LEGACYIOx000000C6; LEGACYIO=FF00\_0000h

Bits	Description
7:0	<b>dma2_ch5cnt.</b> Read-write. Reset: 00h. DMA2 Ch4 Base and Current Count

**LEGACYIOx000000C8 (FCH::IO::DMA2\_CH6ADDR)**

Read-write. Reset: 00h.

Dma2\_Ch6Addr register

\_aliasHOSTLEGACY; LEGACYIOx000000C8; LEGACYIO=FF00\_0000h

Bits	Description
7:0	<b>dma2_ch6addr.</b> Read-write. Reset: 00h. DMA2 Ch6 Base and Current Address

**LEGACYIOx000000CA (FCH::IO::DMA2\_CH6CNT)**

Read-write. Reset: 00h.

Dma2\_Ch6Cnt register

\_aliasHOSTLEGACY; LEGACYIOx000000CA; LEGACYIO=FF00\_0000h

Bits	Description
7:0	<b>dma2_ch6cnt.</b> Read-write. Reset: 00h. DMA2 Ch6 Base and Current Count

**LEGACYIOx000000CC (FCH::IO::DMA2\_CH7ADDR)**

Read-write. Reset: 00h.

Dma2\_Ch7Addr register

\_aliasHOSTLEGACY; LEGACYIOx000000CC; LEGACYIO=FF00\_0000h

Bits	Description
7:0	<b>dma2_ch7addr.</b> Read-write. Reset: 00h. DMA2 Ch5 Base and Current Address

**LEGACYIOx000000CE (FCH::IO::DMA2\_CH7CNT)**

Read-write. Reset: 00h.

Dma2\_Ch7Cnt register

\_aliasHOSTLEGACY; LEGACYIOx000000CE; LEGACYIO=FF00\_0000h

Bits	Description
7:0	<b>dma2_ch7cnt.</b> Read-write. Reset: 00h. Channel 7 DMA base and current count

**LEGACYIOx000000D0 (FCH::IO::DMA2\_STATUS)**

Read-write. Reset: 00h.

Dma\_Status register

\_aliasHOSTLEGACY; LEGACYIOx000000D0; LEGACYIO=FF00\_0000h

Bits	Description
7:0	<b>dma_status.</b> Read-write. Reset: 00h. DMA2 status register

**LEGACYIOx000000D2 (FCH::IO::DMA2\_WRITEREQUEST)**

Read-write. Reset: 00h.

Dma\_WriteRequest register

\_aliasHOSTLEGACY; LEGACYIOx000000D2; LEGACYIO=FF00\_0000h

Bits	Description
7:0	<b>dma_writerequest.</b> Read-write. Reset: 00h. DMA2 request register

**LEGACYIOx000000D4 (FCH::IO::DMA2\_WRITEMASK)**

Read-write. Reset: 00h.

Dma\_WriteMask register

\_aliasHOSTLEGACY; LEGACYIOx000000D4; LEGACYIO=FF00\_0000h

Bits	Description
7:0	<b>dma_writemask.</b> Read-write. Reset: 00h. DMA2 channel mask register

**LEGACYIOx000000D6 (FCH::IO::DMA2\_WRITEMODE)**

Read-write. Reset: 00h.

Dma\_WriteMode register

\_aliasHOSTLEGACY; LEGACYIOx000000D6; LEGACYIO=FF00\_0000h

Bits	Description
7:0	<b>dma_writemode.</b> Read-write. Reset: 00h. DMA2 mode register

**LEGACYIOx000000D8 (FCH::IO::DMA2\_CLEAR)**

Read-write. Reset: 00h.

Dma\_Clear register

\_aliasHOSTLEGACY; LEGACYIOx000000D8; LEGACYIO=FF00\_0000h

Bits	Description
7:0	<b>dma_clear.</b> Read-write. Reset: 00h. Channel 4-7 clear byte pointer



**LEGACYIOx000000DA (FCH::IO::DMA2\_MASTER\_CLEAR)**

Read-write. Reset: 00h.

Dma\_Clear register

\_aliasHOSTLEGACY; LEGACYIOx000000DA; LEGACYIO=FF00\_0000h

**Bits Description**7:0 **dma\_clear.** Read-write. Reset: 00h. Channel 4-7 DMA master clear**LEGACYIOx000000DC (FCH::IO::DMA2\_CLRMASK)**

Read-write. Reset: 00h.

Dma\_ClrMask register

\_aliasHOSTLEGACY; LEGACYIOx000000DC; LEGACYIO=FF00\_0000h

**Bits Description**7:0 **dma\_clrmask.** Read-write. Reset: 00h. Channel 4-7 DMA Clear Mask**LEGACYIOx000000DE (FCH::IO::DMA2\_ALLMASK)**

Read-write. Reset: 00h.

Dma\_AllMask register

\_aliasHOSTLEGACY; LEGACYIOx000000DE; LEGACYIO=FF00\_0000h

**Bits Description**7:0 **dma\_allmask.** Read-write. Reset: 00h. DMA2 mask register**LEGACYIOx000000F0 (FCH::IO::NCP\_ERROR)**

Read-write. Reset: 00h.

NCP\_Error register: In addition to the WarmBoot function, writing to this port will assert IGNNE# if FERR# is true. If FERR# is false, then write to this port will not assert IGNNE#.

\_aliasHOSTLEGACY; LEGACYIOx000000F0; LEGACYIO=FF00\_0000h

**Bits Description**

7 **warmboot.** Read-write. Reset: 0.  
**Description:** Warm or cold boot indicator  
 0: Cold  
 1: Warm, this bit is set when any value is written to this register

6:0 Reserved.

**LEGACYIOx000004D0 (FCH::IO::INTREDGECONTROL)**

Read-write. Reset: 0000h.

IntrEdgeControl register: This register programs each interrupt to be either edge or level sensitive.

\_aliasHOSTLEGACY; LEGACYIOx000004D0; LEGACYIO=FF00\_0000h

Bits	Description
15	<b>irq15control.</b> Read-write. Reset: 0. <b>Description:</b> 1: Level 0: Edge
14	<b>irq14control.</b> Read-write. Reset: 0. <b>Description:</b> 1: Level 0: Edge
13	Reserved.
12	<b>irq12control.</b> Read-write. Reset: 0. <b>Description:</b> 1: Level 0: Edge
11	<b>irq11control.</b> Read-write. Reset: 0. <b>Description:</b> 1: Level 0: Edge
10	<b>irq10control.</b> Read-write. Reset: 0. <b>Description:</b> 1: Level 0: Edge
9	<b>irq9control.</b> Read-write. Reset: 0. <b>Description:</b> 1: Level 0: Edge
8	<b>irq8control.</b> Read-write. Reset: 0. (Read Only) Always Edge
7	<b>irq7control.</b> Read-write. Reset: 0. <b>Description:</b> 1: Level 0: Edge
6	<b>irq6control.</b> Read-write. Reset: 0. <b>Description:</b> 1: Level 0: Edge
5	<b>irq5control.</b> Read-write. Reset: 0. <b>Description:</b> 1: Level 0: Edge
4	<b>irq4control.</b> Read-write. Reset: 0. <b>Description:</b> 1: Level 0: Edge
3	<b>irq3control.</b> Read-write. Reset: 0. <b>Description:</b> 1: Level 0: Edge
2	Reserved.
1	<b>irq1control.</b> Read-write. Reset: 0. <b>Description:</b> 1: Level 0: Edge
0	<b>irq0control.</b> Read-write. Reset: 0. <b>Description:</b> 1: Level 0: Edge

**LEGACYIOx00000C00 (FCH::IO::PCI\_INTR\_INDEX)**

Read-write. Reset: 00h.

Pci\_Intr\_Index register

\_aliasHOSTLEGACY; LEGACYIOx00000C00; LEGACYIO=FF00\_0000h

Bits	Description
7:0	<b>pci_intr_index.</b> Read-write. Reset: 00h. PCI interrupt index

**LEGACYIOx00000C01 (FCH::IO::PCI\_INTR\_DATA)**

Read-write. Reset: 1Fh.

Pci\_Intr\_Data register

\_aliasHOSTLEGACY; LEGACYIOx00000C01; LEGACYIO=FF00\_0000h

Bits	Description
7:0	<b>pci_intr_data.</b> Read-write. Reset: 1Fh. PCI redirection register

**LEGACYIOx00000C14 (FCH::IO::PCI\_ERROR)**

Read-write.

Pci\_Error register. This register is enabled/disabled by PM\_Reg:00[20].

\_aliasHOSTLEGACY; LEGACYIOx00000C14; LEGACYIO=FF00\_0000h

Bits	Description
7:4	Reserved.
3	<b>perr_nmi.</b> Read-write. Reset: 1. <b>Description:</b> Enable NMI generation from PERR# 0: Enable 1: Disable
2	<b>serr_nmi.</b> Read-write. Reset: 1. <b>Description:</b> Enable NMI generation from SERR# 0: Enable 1: Disable
1	<b>perr_nmi_status.</b> Read-write. Reset: X. Set to 1 when NMI generation is enabled and PERR# has been asserted due to a PCI data parity error. Cleared by writing a one to port 61h, bit 2. [Read-only]
0	<b>serr_nmi_status.</b> Read-write. Reset: X. Set to 1 when NMI generation is enabled and SERR# has been asserted due to a PCI error. Cleared by writing a one to port 61h, bit 2. [Read-only]

**LEGACYIOx00000CF9 (FCH::IO::IO\_PORT\_CF9)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; LEGACYIOx00000CF9; LEGACYIO=FF00\_0000h

Bits	Description
7:4	Reserved.
3:1	<b>io_port_cf9.</b> Read-write. Reset: 0h. <b>Description:</b> 010: do init, send INIT HT message 011: do reset, generate <a href="#">Warm reset</a> 111: do full reset, generate <a href="#">Cold reset</a> and place system in S5 state for 3 to 5 seconds All other values are reserved
0	Reserved.

**RTCHOSTx00000000 (FCH::IO::SECONDS)**

Read-write.

Seconds register

\_aliasHOSTLEGACY; RTCHOSTx00000000; RTCHOST=FED8\_0700h

Bits	Description
7:0	<b>seconds.</b> Read-write. Reset: XXXXXXXXb.
	<b>Description:</b> Binary-Code-Decimal format. Range:00 59 This register can be set by software (set bit of Register B = 1) or can be automatically updated by hardware every second. When set by software, hardware updating is disabled. Note: the value of this register is undefined/indeterministic when power up first time.

**RTCHOSTx00000001 (FCH::IO::SECONDS\_ALARM)**

Read-write.

Seconds Alarm register

\_aliasHOSTLEGACY; RTCHOSTx00000001; RTCHOST=FED8\_0700h

Bits	Description
7:0	<b>seconds_alarm.</b> Read-write. Reset: XXXXXXXXb.
	<b>Description:</b> Binary-Code-Decimal format. If set bit = 1, the Seconds Alarm Register will never match with Seconds Register, else If bits [7:6] = [11], the Seconds Alarm Register always matches with Seconds Register. Note: the value of this register is undefined/indeterministic when power up first time.

**RTCHOSTx00000002 (FCH::IO::MINUTES)**

Read-write.

Minutes register

\_aliasHOSTLEGACY; RTCHOSTx00000002; RTCHOST=FED8\_0700h

Bits	Description
7:0	<b>minutes.</b> Read-write. Reset: XXXXXXXXb.
	<b>Description:</b> Binary-Code-Decimal format. Range:00 59 This register can be set by software (set bit of Register B = 1) or can be automatically updated by hardware every minute. When set by software, hardware updating is disabled. Note: the value of this register is undefined/indeterministic when power up first time.

**RTCHOSTx00000003 (FCH::IO::MINUTES\_ALARM)**

Read-write.

Minutes Alarm register

\_aliasHOSTLEGACY; RTCHOSTx00000003; RTCHOST=FED8\_0700h

Bits	Description
7:0	<b>minutes_alarm.</b> Read-write. Reset: XXXXXXXXb.
	<b>Description:</b> Binary-Code-Decimal format. If set bit = 1, the Minutes Alarm Register will never match with Minutes Register, else If bits [7:6] = [11], the Minutes Alarm Register always matches with Minutes Register. Note: the value of this register is undefined/indeterministic when power up first time.

**RTCHOSTx00000004 (FCH::IO::HOURS)**

Read-write.

Hours register

\_aliasHOSTLEGACY; RTCHOSTx00000004; RTCHOST=FED8\_0700h

Bits	Description
7:0	<b>hours.</b> Read-write. Reset: XXXXXXXXb.
	<b>Description:</b> Binary-Code-Decimal format. Range:00 23 This register can be set by software (set bit of Register B = 1) or can be automatically updated by hardware every hour. When set by software, hardware updating is disabled. Note: the value of this register is undefined/indeterministic when power up first time.

**RTCHOSTx00000005 (FCH::IO::HOURS\_ALARM)**

Read-write.

Hours Alarm register

\_aliasHOSTLEGACY; RTCHOSTx00000005; RTCHOST=FED8\_0700h

Bits	Description
7:0	<b>hours_alarm.</b> Read-write. Reset: XXXXXXXXb.
	<b>Description:</b> Binary-Code-Decimal format. If set bit = 1, the Hours Alarm Register will never match with Hours Register, else If bits [7:6] = [11], the Hours Alarm Register always matches with Hours Register. Note: the value of this register is undefined/indeterministic when power up first time.

**RTCHOSTx00000006 (FCH::IO::DAY\_OF\_WEEK)**

Read-write.

Day of Week register

\_aliasHOSTLEGACY; RTCHOSTx00000006; RTCHOST=FED8\_0700h

Bits	Description
7:0	<b>day_of_week.</b> Read-write. Reset: XXXXXXXXb.
	<b>Description:</b> Binary-Code-Decimal format. Range: 01 07 (Sunday = 1). No leap year correction capability. Leap year correction has to be done by software. This register can be set by a software (set bit of Register B = 1) or can be automatically updated by hardware everyday. When set by software, hardware updating is disabled. Note: the value of this register is undefined/indeterministic when power up first time.

**RTCHOSTx00000007 (FCH::IO::DATE\_OF\_MONTH)**

Read-write.

Date of Month register

\_aliasHOSTLEGACY; RTCHOSTx00000007; RTCHOST=FED8\_0700h

Bits	Description
7:0	<b>date_of_month.</b> Read-write. Reset: XXXXXXXXb.
	<b>Description:</b> Binary-Code-Decimal format. Range: 01 28 for February and no leap year capability. Leap year correction has to be done by software. This register can be set by software (set bit of Register B = 1) or can be automatically updated by hardware everyday. When set by software, hardware updating is disabled. Note: the value of this register is undefined/indeterministic when power up first time.

**RTCHOSTx00000008 (FCH::IO::MONTH)**

Read-write.

Month register

\_aliasHOSTLEGACY; RTCHOSTx00000008; RTCHOST=FED8\_0700h

Bits	Description
7:0	<b>month.</b> Read-write. Reset: XXXXXXXXb. <b>Description:</b> Binary-Code-Decimal format. Range: 01 12. No leap year correction capability. Leap year correction has to be done by software. This register can be set by software (set bit of Register B = 1) or can be automatically updated by hardware every month. When set by software, hardware updating is disabled. Note: the value of this register is undefined/indeterministic when power up first time.

**RTCHOSTx00000009 (FCH::IO::YEAR)**

Read-write.

Year register

\_aliasHOSTLEGACY; RTCHOSTx00000009; RTCHOST=FED8\_0700h

Bits	Description
7:0	<b>year.</b> Read-write. Reset: XXXXXXXXb. <b>Description:</b> Binary-Code-Decimal format. Range: 00 99. No leap year correction capability. Leap year correction has to be done by software. This register can be set by software (set bit of Register B = 1) or can be automatically updated by hardware every year. When set by software, hardware updating is disabled. Note: the value of this register is undefined/indeterministic when power up first time.

**RTCHOSTx0000000A (FCH::IO::REGISTER\_A)**

Read-write.

Register A: Control register

\_aliasHOSTLEGACY; RTCHOSTx0000000A; RTCHOST=FED8\_0700h

Bits	Description
7	<b>update_in_progress_uip.</b> Read-write. Reset: X. <b>Description:</b> If set bit = 1, UIP is cleared. If UIP = 1, the update transfer will soon occur. If UIP = 0, the update transfer will not occur for at least 244us. [Read-only] Note: the value of this register is undefined/indeterministic when power up first time.
6:5	Reserved.
4	<b>bank_selection_dv0.</b> Read-write. Reset: X. <b>Description:</b> DV0 = 0 selects Bank 0 DV0 = 1 selects Bank 1. The SB800 has an alternate way to access the RAM without the use of bank select bit. Port 72/73 can be used as the index to access the full 256 bytes of RAM directly. Note: the value of this register is undefined/indeterministic when power up first time.
3	<b>rate_selection_rs3.</b> Read-write. Reset: X.
2	<b>rate_selection_rs2.</b> Read-write. Reset: X.
1	<b>rate_selection_rs1.</b> Read-write. Reset: X.
0	<b>rate_selection_rs0.</b> Read-write. Reset: X. <b>Description:</b> These four rate-selection bits select one of the 13 taps on the 15-stage frequency divider or disable the divider output (flat output signal). The tap selected can be used to generate a periodic interrupt. See the following table for the frequency selection. Note: the value of this register is undefined/indeterministic when power up first time.

**RTCHOSTx0000000B (FCH::IO::REGISTER\_B)**

Read-write.

Register B: Control register

\_aliasHOSTLEGACY; RTCHOSTx0000000B; RTCHOST=FED8\_0700h

Bits	Description
7	<b>set_new_time_set.</b> Read-write. Reset: X. <b>Description:</b> If set bit = 1, no internal updating for Time Registers is allowed. If set bit = 0, the Time Registers are updated every second. Note: the value of this register is undefined/indeterministic when power up first time.
6	<b>periodic_interrupt_enable_pie.</b> Read-write. Reset: X. <b>Description:</b> PIE enables the Periodic Interrupt Flag (PF) bit in Register C to assert IRQ. Note: the value of this register is undefined/indeterministic when power up first time.
5	<b>alarm_interrupt_enable_aie.</b> Read-write. Reset: X. <b>Description:</b> AIE enables the Alarm Flag (AF) bit in Register C to assert IRQ. Note: the value of this register is undefined/indeterministic when power up first time.
4	<b>update_ended_interrupt_enable_uie.</b> Read-write. Reset: X. <b>Description:</b> UIE enables the Update End Flag (UF) bit in Register C to assert IRQ. If set bit = 1, UIE is cleared. Note: the value of this register is undefined/indeterministic when power up first time.
3:2	Reserved.
1	<b>hourmode.</b> Read-write. Reset: X. <b>Description:</b> Hour mode 0: 12 hour mode 1: 24 hour mode Note: the value of this register is undefined/indeterministic when power up first time.
0	<b>daylight_saving_enable.</b> Read-write. Reset: X. <b>Description:</b> Both this bit and RtcExt_Reg: 00h bit[0] need to be set to 1 to enable RTC daylight saving feature. Note: the value of this register is undefined/indeterministic when power up first time.

**RTCHOSTx0000000C (FCH::IO::REGISTER\_C)**

Read-only.

Register C: Control register

\_aliasHOSTLEGACY; RTCHOSTx0000000C; RTCHOST=FED8\_0700h

Bits	Description
7	<b>interrupt_request_flag_irqf.</b> Read-only. Reset: X. <b>Description:</b> Logically, IRQF = (PF*PIE)+(AF*AIE)+(UF*UIE)+(WF*WIE) where WF and WIE are defined in Extended Control Register 4A and 4B. Reading Register C clears IRQF bit. Any time the IRQF bit is set to one, the #IRQ pin is driven low. Note: the value of this register is undefined/indeterministic when power up first time.
6	<b>xperiodic_interrupt_flag_pf.</b> Read-only. Reset: X. <b>Description:</b> This bit is set to one when an edge is detected on the selected tap (through RS3 to RS0) of the frequency divider. Reading Register C clears PF bit. Note: the value of this register is undefined/indeterministic when power up first time.
5	<b>alarm_interrupt_flag_af.</b> Read-only. Reset: X. <b>Description:</b> This bit is set to one if second, minute and hour time has matched the second, minute and hour alarm time. Reading Register C clears AF bit. Note: the value of this register is undefined/indeterministic when power up first time.
4	<b>update_ended_interrupt_flag_uf.</b> Read-only. Reset: X. <b>Description:</b> This bit is set to one after each update cycle. Reading Register C clears UF. Note: the value of this register is undefined/indeterministic when power up first time.
3:0	Reserved.

**RTCHOSTx0000000D (FCH::IO::DATEALARM)**

Read-write.

Date Alarm Register

\_aliasHOSTLEGACY; RTCHOSTx0000000D; RTCHOST=FED8\_0700h

Bits	Description
7	<b>vrt.</b> Read-write. Reset: X. <b>Description:</b> Valid RAM and Time refer to VRT_T1 and VRT_T2 registers (PMIO 3E/3F) Note: the value of this register is undefined/indeterministic when power up first time.
6	<b>scratchbit.</b> Read-write. Reset: X.
5:0	<b>datealarm.</b> Read-write. Reset: XXXXXXb. <b>Description:</b> DateAlarm in <a href="#">BCD</a> format and is considered when it is set to non-zero value. If this value is set to 0, then date is not compared for alarm generation. Note: the value of this register is undefined/indeterministic when power up first time.

**RTCHOSTx00000032 (FCH::IO::ALTCENTURY)**

Read-write.

AltCentury Register

\_aliasHOSTLEGACY; RTCHOSTx00000032; RTCHOST=FED8\_0700h

Bits	Description
7:0	<b>altcentury.</b> Read-write. Reset: XXXXXXXXb. <b>Description:</b> (This register is accessed only when DV0=0 and PM_Reg 56h Bit12=1.) Binary-Code-Decimal format. Leap year correction is done through hardware. This register can be set by software (set bit of Register B = 1) or can be automatically updated by hardware every century. When set by software, hardware updating is disabled. Note: the value of this register is undefined/indeterministic when power up first time.

**RTCHOSTx00000048 (FCH::IO::CENTURY)**

Read-write.

Century Register

\_aliasHOSTLEGACY; RTCHOSTx00000048; RTCHOST=FED8\_0700h

Bits	Description
7:0	<b>century.</b> Read-write. Reset: XXXXXXXXb. <b>Description:</b> (This register is accessed only when DV0=1) Binary-Code-Decimal format. Leap year correction is done through hardware. This register can be set by software (set bit of Register B = 1) or can be automatically updated by hardware every century. When set by software, hardware updating is disabled. Note: the value of this register is undefined/indeterministic when power up first time.

**RTCHOSTx00000050 (FCH::IO::EXTENDED\_RAM\_ADDRESS\_PORT)**

Read-write.

Extended RAM Address Port register: The address port to access Extended RAM.

\_aliasHOSTLEGACY; RTCHOSTx00000050; RTCHOST=FED8\_0700h

Bits	Description
7	Reserved.
6:0	<b>extendedramaddr.</b> Read-write. Reset: XXXXXXXb. <b>Description:</b> Because only 7 address bits are used in port x70, only lower 128 bytes are accessible through port x71. The Extended RAM (upper 128 bytes) are physically located at address 80H to FFH. In order to access these address, an address offset should be programmed into this register and access them through Extended RAMDataPort. (An offset of x80H will automatically add to this 7-bit address). Note: the value of this register is undefined/indeterministic when power up first time.



**RTCHOSTx00000053 (FCH::IO::EXTENDED\_RAM\_DATA\_PORT)**

Read-write.

Extended RAM Data Port register.

\_aliasHOSTLEGACY; RTCHOSTx00000053; RTCHOST=FED8\_0700h

Bits	Description
7:0	<b>extended_ram_data_port.</b> Read-write. Reset: XXXXXXXXb. There is no physical register corresponding to this data port but the data port address is used for decoding to generate appropriate internal control signals.

**RTCHOSTx0000007E (FCH::IO::RTC\_TIME\_CLEAR)**

Read-write.

RTC Time Clear register.

\_aliasHOSTLEGACY; RTCHOSTx0000007E; RTCHOST=FED8\_0700h

Bits	Description
7:1	Reserved.
0	<b>rtctimeclear.</b> Read-write. Reset: X. <b>Description:</b> Setting this bit '1' will clear the RTC second and RTC time will stop. When PSP_regxFC[9]=1, this bit can only be written '0'. Note: the value of this register is undefined/indeterministic when power up first time.

**RTCHOSTx0000007F (FCH::IO::RTC\_RAM\_ENABLE)**

Read-write.

RTC RAM Enable register.

\_aliasHOSTLEGACY; RTCHOSTx0000007F; RTCHOST=FED8\_0700h

Bits	Description
7:1	Reserved.
0	<b>rtcramenable.</b> Read-write. Reset: X. <b>Description:</b> Setting this bit will enable access to the RTC RAM Note: the value of this register is undefined/indeterministic when power up first time.

**11.3.2 I/O Advanced Programmable Interrupt Control****11.3.2.1 IOAPIC Registers****IOAPICx00000000 (FCH::IOAPIC::IO\_REGISTER\_SELECT\_REGISTER)**

Read-write.

Used to determine which register is manipulated during an IO Window Register read/write operation.

\_aliasHOSTLEGACY; IOAPICx00000000; IOAPIC=FEC0\_0000h

Bits	Description
31:8	Reserved.
7:0	<b>indirect_address_offset.</b> Read-write. Reset: 00h. Indirect Address Offset to IO Window Register, used to determine which register is manipulated during an IO Window Register read/write operation.

**IOAPICx00000010 (FCH::IOAPIC::IO\_WINDOW\_REGISTER)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; IOAPICx00000010; IOAPIC=FEC0\_0000h

Bits	Description
31:0	<b>io_window.</b> Read-write. Reset: 0000_0000h. <b>Description:</b> Mapped by the value in the IO Register Select Register to the designated indirect access register. Technically a RW register however, the read/write capability is determined by the indirect access register referenced by the IO Register Select Register.

**IOAPICx00000010\_indirectaddressoffset00 (FCH::IOAPIC::IOAPIC\_ID\_REGISTER)**

Read-write. Reset: 0000\_0000h.

Not used in XAPIC PCI bus delivery mode.

\_aliasHOSTLEGACY; IOAPICx00000010\_indirectaddressoffset00; IOAPIC=FEC0\_0000h;  
DataPortWrite=FCH::IOAPIC::IO\_REGISTER\_SELECT\_REGISTER[indirect\_address\_offset]

Bits	Description
31:24	<b>id.</b> Read-write. Reset: 00h. IOAPIC device ID for APIC serial bus delivery mode
23:0	Reserved.

**IOAPICx00000010\_indirectaddressoffset01 (FCH::IOAPIC::IOXAPIC\_VERSION\_REGISTER)**

Read-only. Reset: 0017\_8021h.

\_aliasHOSTLEGACY; IOAPICx00000010\_indirectaddressoffset01; IOAPIC=FEC0\_0000h;  
DataPortWrite=FCH::IOAPIC::IO\_REGISTER\_SELECT\_REGISTER[indirect\_address\_offset]

Bits	Description
31:24	Reserved.
23:16	<b>max_redirection_entries.</b> Read-only. Reset: 17h. 24 entries [23:0]
15	<b>prq.</b> Read-only. Reset: 1. IRQ pin assertion supported
14:8	Reserved.
7:0	<b>version.</b> Read-only. Reset: 21h. PCI 2.2 compliant

**IOAPICx00000010\_indirectaddressoffset02 (FCH::IOAPIC::IOAPIC\_ARBITRATION\_REGISTER)**

Read-only. Reset: 0000\_0000h.

Not used in XAPIC PCI bus delivery mode.

\_aliasHOSTLEGACY; IOAPICx00000010\_indirectaddressoffset02; IOAPIC=FEC0\_0000h;  
DataPortWrite=FCH::IOAPIC::IO\_REGISTER\_SELECT\_REGISTER[indirect\_address\_offset]

Bits	Description
31:28	Reserved.
27:24	<b>arbitration_id.</b> Read-only. Reset: 0h. Arbitration ID for APIC serial bus delivery mode
23:0	Reserved.

**IOAPICx00000010\_indirectaddressoffset10**  
**(FCH::IOAPIC::REDIRECTION\_TABLE\_ENTRY\_0\_LOW\_32BIT)**

Read-write. Reset: 0001\_0000h.

 \_aliasHOSTLEGACY; IOAPICx00000010\_indirectaddressoffset10; IOAPIC=FEC0\_0000h;  
 DataPortWrite=FCH::IOAPIC::IO\_REGISTER\_SELECT\_REGISTER[indirect\_address\_offset]

Bits	Description
31:17	Reserved.
16	<b>mask</b> . Read-write. Reset: 1. <b>Description:</b> Masks the interrupt injection at the input of this device. Write 0 to unmask
15	<b>trigger_mode</b> . Read-write. Reset: 0. <b>Description:</b> 0: Edge 1: Level
14	<b>remote_irr</b> . Read-write. Reset: 0. <b>Description:</b> Read Only. Used for level triggered interrupts only. Set when interrupt message delivered. Cleared by EOI special cycle transaction or write to EOI register
13	<b>interrupt_pin_polarity</b> . Read-write. Reset: 0. <b>Description:</b> 0: High 1: Low
12	<b>delivery_status</b> . Read-write. Reset: 0. <b>Description:</b> Read Only 0: Idle 1: Send Pending
11	<b>destination_mode</b> . Read-write. Reset: 0. <b>Description:</b> 0: Physical 1: Logical
10:8	<b>delivery_mode</b> . Read-write. Reset: 0h. <b>Description:</b> 000: Fixed 001: Lowest Priority 010: <a href="#">SMI</a> /PMI 011: Reserved 100: NMI 101: INIT 110: Reserved 111: ExtINT
7:0	<b>vector</b> . Read-write. Reset: 00h. The value of this field is the clock interrupt value when bit[22] (clkintrvectororden) of FCH::PM::MISC_PMIO register is 0.

**IOAPICx00000010\_indirectaddressoffset11**  
**(FCH::IOAPIC::REDIRECTION\_TABLE\_ENTRY\_0\_HIGH\_32BIT)**

Read-write. Reset: 0000\_0000h.

 \_aliasHOSTLEGACY; IOAPICx00000010\_indirectaddressoffset11; IOAPIC=FEC0\_0000h;  
 DataPortWrite=FCH::IOAPIC::IO\_REGISTER\_SELECT\_REGISTER[indirect\_address\_offset]

Bits	Description
31:24	<b>destination_id</b> . Read-write. Reset: 00h. Bits [19:12] of the address field of the interrupt message
23:0	Reserved.

### IOAPICx00000010\_indirectaddressoffset12 (FCH::IOAPIC::REDIRECTION\_TABLE\_ENTRY\_1\_LOW\_32BIT)

Read-write. Reset: 0001\_0000h.

\_aliasHOSTLEGACY; IOAPICx00000010\_indirectaddressoffset12; IOAPIC=FEC0\_0000h;  
DataPortWrite=FCH::IOAPIC::IO\_REGISTER\_SELECT\_REGISTER[indirect\_address\_offset]

Bits	Description
31:17	Reserved.
16	<b>mask.</b> Read-write. Reset: 1. <b>Description:</b> Masks the interrupt injection at the input of this device. Write 0 to unmask
15	<b>trigger_mode.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge 1: Level
14	<b>remote_irr.</b> Read-write. Reset: 0. <b>Description:</b> Read Only. Used for level triggered interrupts only. Set when interrupt message delivered. Cleared by EOI special cycle transaction or write to EOI register
13	<b>interrupt_pin_polarity.</b> Read-write. Reset: 0. <b>Description:</b> 0: High 1: Low
12	<b>delivery_status.</b> Read-write. Reset: 0. <b>Description:</b> Read Only 0: Idle 1: Send Pending
11	<b>destination_mode.</b> Read-write. Reset: 0. <b>Description:</b> 0: Physical 1: Logical
10:8	<b>delivery_mode.</b> Read-write. Reset: 0h. <b>Description:</b> 000: Fixed 001: Lowest Priority 010: <a href="#">SMI</a> /PMI 011: Reserved 100: NMI 101: INIT 110: Reserved 111: ExtINT
7:0	<b>vector.</b> Read-write. Reset: 00h. The value of this field is the clock interrupt value when bit[22] (clkintrvectororden) of FCH::PM::MISC_PMIO register is 0.

### IOAPICx00000010\_indirectaddressoffset13 (FCH::IOAPIC::REDIRECTION\_TABLE\_ENTRY\_1\_HIGH\_32BIT)

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; IOAPICx00000010\_indirectaddressoffset13; IOAPIC=FEC0\_0000h;  
DataPortWrite=FCH::IOAPIC::IO\_REGISTER\_SELECT\_REGISTER[indirect\_address\_offset]

Bits	Description
31:24	<b>destination_id.</b> Read-write. Reset: 00h. Bits [19:12] of the address field of the interrupt message
23:0	Reserved.

### IOAPICx00000010\_indirectaddressoffset14 (FCH::IOAPIC::REDIRECTION\_TABLE\_ENTRY\_2\_LOW\_32BIT)

Read-write. Reset: 0001\_0000h.

\_aliasHOSTLEGACY; IOAPICx00000010\_indirectaddressoffset14; IOAPIC=FEC0\_0000h;  
DataPortWrite=FCH::IOAPIC::IO\_REGISTER\_SELECT\_REGISTER[indirect\_address\_offset]

Bits	Description
31:17	Reserved.
16	<b>mask.</b> Read-write. Reset: 1. <b>Description:</b> Masks the interrupt injection at the input of this device. Write 0 to unmask
15	<b>trigger_mode.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge 1: Level
14	<b>remote_irr.</b> Read-write. Reset: 0. <b>Description:</b> Read Only. Used for level triggered interrupts only. Set when interrupt message delivered. Cleared by EOI special cycle transaction or write to EOI register
13	<b>interrupt_pin_polarity.</b> Read-write. Reset: 0. <b>Description:</b> 0: High 1: Low
12	<b>delivery_status.</b> Read-write. Reset: 0. <b>Description:</b> Read Only 0: Idle 1: Send Pending
11	<b>destination_mode.</b> Read-write. Reset: 0. <b>Description:</b> 0: Physical 1: Logical
10:8	<b>delivery_mode.</b> Read-write. Reset: 0h. <b>Description:</b> 000: Fixed 001: Lowest Priority 010: <a href="#">SMI</a> /PMI 011: Reserved 100: NMI 101: INIT 110: Reserved 111: ExtINT
7:0	<b>vector.</b> Read-write. Reset: 00h. The value of this field is the clock interrupt value when bit[22] (clkintrvectororden) of FCH::PM::MISC_PMIO register is 0.

### IOAPICx00000010\_indirectaddressoffset15 (FCH::IOAPIC::REDIRECTION\_TABLE\_ENTRY\_2\_HIGH\_32BIT)

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; IOAPICx00000010\_indirectaddressoffset15; IOAPIC=FEC0\_0000h;  
DataPortWrite=FCH::IOAPIC::IO\_REGISTER\_SELECT\_REGISTER[indirect\_address\_offset]

Bits	Description
31:24	<b>destination_id.</b> Read-write. Reset: 00h. Bits [19:12] of the address field of the interrupt message
23:0	Reserved.

**IOAPICx00000010\_indirectaddressoffset16**  
**(FCH::IOAPIC::REDIRECTION\_TABLE\_ENTRY\_3\_LOW\_32BIT)**

Read-write. Reset: 0001\_0000h.

\_aliasHOSTLEGACY; IOAPICx00000010\_indirectaddressoffset16; IOAPIC=FEC0\_0000h;  
 DataPortWrite=FCH::IOAPIC::IO\_REGISTER\_SELECT\_REGISTER[indirect\_address\_offset]

Bits	Description
31:17	Reserved.
16	<b>mask.</b> Read-write. Reset: 1. <b>Description:</b> Masks the interrupt injection at the input of this device. Write 0 to unmask
15	<b>trigger_mode.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge 1: Level
14	<b>remote_irr.</b> Read-write. Reset: 0. <b>Description:</b> Read Only. Used for level triggered interrupts only. Set when interrupt message delivered. Cleared by EOI special cycle transaction or write to EOI register
13	<b>interrupt_pin_polarity.</b> Read-write. Reset: 0. <b>Description:</b> 0: High 1: Low
12	<b>delivery_status.</b> Read-write. Reset: 0. <b>Description:</b> Read Only 0: Idle 1: Send Pending
11	<b>destination_mode.</b> Read-write. Reset: 0. <b>Description:</b> 0: Physical 1: Logical
10:8	<b>delivery_mode.</b> Read-write. Reset: 0h. <b>Description:</b> 000: Fixed 001: Lowest Priority 010: <a href="#">SMI</a> /PMI 011: Reserved 100: NMI 101: INIT 110: Reserved 111: ExtINT
7:0	<b>vector.</b> Read-write. Reset: 00h. The value of this field is the clock interrupt value when bit[22] (clkintrvectororden) of FCH::PM::MISC_PMIO register is 0.

**IOAPICx00000010\_indirectaddressoffset17**  
**(FCH::IOAPIC::REDIRECTION\_TABLE\_ENTRY\_3\_HIGH\_32BIT)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; IOAPICx00000010\_indirectaddressoffset17; IOAPIC=FEC0\_0000h;  
 DataPortWrite=FCH::IOAPIC::IO\_REGISTER\_SELECT\_REGISTER[indirect\_address\_offset]

Bits	Description
31:24	<b>destination_id.</b> Read-write. Reset: 00h. Bits [19:12] of the address field of the interrupt message
23:0	Reserved.

**IOAPICx00000010\_indirectaddressoffset18**  
**(FCH::IOAPIC::REDIRECTION\_TABLE\_ENTRY\_4\_LOW\_32BIT)**

Read-write. Reset: 0001\_0000h.

\_aliasHOSTLEGACY; IOAPICx00000010\_indirectaddressoffset18; IOAPIC=FEC0\_0000h;  
 DataPortWrite=FCH::IOAPIC::IO\_REGISTER\_SELECT\_REGISTER[indirect\_address\_offset]

Bits	Description
31:17	Reserved.
16	<b>mask.</b> Read-write. Reset: 1. <b>Description:</b> Masks the interrupt injection at the input of this device. Write 0 to unmask
15	<b>trigger_mode.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge 1: Level
14	<b>remote_irr.</b> Read-write. Reset: 0. <b>Description:</b> Read Only. Used for level triggered interrupts only. Set when interrupt message delivered. Cleared by EOI special cycle transaction or write to EOI register
13	<b>interrupt_pin_polarity.</b> Read-write. Reset: 0. <b>Description:</b> 0: High 1: Low
12	<b>delivery_status.</b> Read-write. Reset: 0. <b>Description:</b> Read Only 0: Idle 1: Send Pending
11	<b>destination_mode.</b> Read-write. Reset: 0. <b>Description:</b> 0: Physical 1: Logical
10:8	<b>delivery_mode.</b> Read-write. Reset: 0h. <b>Description:</b> 000: Fixed 001: Lowest Priority 010: <a href="#">SMI</a> /PMI 011: Reserved 100: NMI 101: INIT 110: Reserved 111: ExtINT
7:0	<b>vector.</b> Read-write. Reset: 00h. The value of this field is the clock interrupt value when bit[22] (clkintrvectororden) of FCH::PM::MISC_PMIO register is 0.

**IOAPICx00000010\_indirectaddressoffset19**  
**(FCH::IOAPIC::REDIRECTION\_TABLE\_ENTRY\_4\_HIGH\_32BIT)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; IOAPICx00000010\_indirectaddressoffset19; IOAPIC=FEC0\_0000h;  
 DataPortWrite=FCH::IOAPIC::IO\_REGISTER\_SELECT\_REGISTER[indirect\_address\_offset]

Bits	Description
31:24	<b>destination_id.</b> Read-write. Reset: 00h. Bits [19:12] of the address field of the interrupt message
23:0	Reserved.

**IOAPICx00000010\_indirectaddressoffset1A**  
**(FCH::IOAPIC::REDIRECTION\_TABLE\_ENTRY\_5\_LOW\_32BIT)**

Read-write. Reset: 0001\_0000h.

\_aliasHOSTLEGACY; IOAPICx00000010\_indirectaddressoffset1A; IOAPIC=FEC0\_0000h;  
 DataPortWrite=FCH::IOAPIC::IO\_REGISTER\_SELECT\_REGISTER[indirect\_address\_offset]

Bits	Description
31:17	Reserved.
16	<b>mask.</b> Read-write. Reset: 1. <b>Description:</b> Masks the interrupt injection at the input of this device. Write 0 to unmask
15	<b>trigger_mode.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge 1: Level
14	<b>remote_irr.</b> Read-write. Reset: 0. <b>Description:</b> Read Only. Used for level triggered interrupts only. Set when interrupt message delivered. Cleared by EOI special cycle transaction or write to EOI register
13	<b>interrupt_pin_polarity.</b> Read-write. Reset: 0. <b>Description:</b> 0: High 1: Low
12	<b>delivery_status.</b> Read-write. Reset: 0. <b>Description:</b> Read Only 0: Idle 1: Send Pending
11	<b>destination_mode.</b> Read-write. Reset: 0. <b>Description:</b> 0: Physical 1: Logical
10:8	<b>delivery_mode.</b> Read-write. Reset: 0h. <b>Description:</b> 000: Fixed 001: Lowest Priority 010: <a href="#">SMI</a> /PMI 011: Reserved 100: NMI 101: INIT 110: Reserved 111: ExtINT
7:0	<b>vector.</b> Read-write. Reset: 00h. The value of this field is the clock interrupt value when bit[22] (clkintrvectororden) of FCH::PM::MISC_PMIO register is 0.

**IOAPICx00000010\_indirectaddressoffset1B**  
**(FCH::IOAPIC::REDIRECTION\_TABLE\_ENTRY\_5\_HIGH\_32BIT)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; IOAPICx00000010\_indirectaddressoffset1B; IOAPIC=FEC0\_0000h;  
 DataPortWrite=FCH::IOAPIC::IO\_REGISTER\_SELECT\_REGISTER[indirect\_address\_offset]

Bits	Description
31:24	<b>destination_id.</b> Read-write. Reset: 00h. Bits [19:12] of the address field of the interrupt message
23:0	Reserved.



**IOAPICx00000010\_indirectaddressoffset1C**  
**(FCH::IOAPIC::REDIRECTION\_TABLE\_ENTRY\_6\_LOW\_32BIT)**

Read-write. Reset: 0001\_0000h.

\_aliasHOSTLEGACY; IOAPICx00000010\_indirectaddressoffset1C; IOAPIC=FEC0\_0000h;  
 DataPortWrite=FCH::IOAPIC::IO\_REGISTER\_SELECT\_REGISTER[indirect\_address\_offset]

Bits	Description
31:17	Reserved.
16	<b>mask.</b> Read-write. Reset: 1. <b>Description:</b> Masks the interrupt injection at the input of this device. Write 0 to unmask
15	<b>trigger_mode.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge 1: Level
14	<b>remote_irr.</b> Read-write. Reset: 0. <b>Description:</b> Read Only. Used for level triggered interrupts only. Set when interrupt message delivered. Cleared by EOI special cycle transaction or write to EOI register
13	<b>interrupt_pin_polarity.</b> Read-write. Reset: 0. <b>Description:</b> 0: High 1: Low
12	<b>delivery_status.</b> Read-write. Reset: 0. <b>Description:</b> Read Only 0: Idle 1: Send Pending
11	<b>destination_mode.</b> Read-write. Reset: 0. <b>Description:</b> 0: Physical 1: Logical
10:8	<b>delivery_mode.</b> Read-write. Reset: 0h. <b>Description:</b> 000: Fixed 001: Lowest Priority 010: <a href="#">SMI</a> /PMI 011: Reserved 100: NMI 101: INIT 110: Reserved 111: ExtINT
7:0	<b>vector.</b> Read-write. Reset: 00h. The value of this field is the clock interrupt value when bit[22] (clkintrvectororden) of FCH::PM::MISC_PMIO register is 0.

**IOAPICx00000010\_indirectaddressoffset1D**  
**(FCH::IOAPIC::REDIRECTION\_TABLE\_ENTRY\_6\_HIGH\_32BIT)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; IOAPICx00000010\_indirectaddressoffset1D; IOAPIC=FEC0\_0000h;  
 DataPortWrite=FCH::IOAPIC::IO\_REGISTER\_SELECT\_REGISTER[indirect\_address\_offset]

Bits	Description
31:24	<b>destination_id.</b> Read-write. Reset: 00h. Bits [19:12] of the address field of the interrupt message
23:0	Reserved.

**IOAPICx00000010\_indirectaddressoffset1E  
(FCH::IOAPIC::REDIRECTION\_TABLE\_ENTRY\_7\_LOW\_32BIT)**

Read-write. Reset: 0001\_0000h.

\_aliasHOSTLEGACY; IOAPICx00000010\_indirectaddressoffset1E; IOAPIC=FEC0\_0000h;  
DataPortWrite=FCH::IOAPIC::IO\_REGISTER\_SELECT\_REGISTER[indirect\_address\_offset]

Bits	Description
31:17	Reserved.
16	<b>mask</b> . Read-write. Reset: 1. <b>Description:</b> Masks the interrupt injection at the input of this device. Write 0 to unmask
15	<b>trigger_mode</b> . Read-write. Reset: 0. <b>Description:</b> 0: Edge 1: Level
14	<b>remote_irr</b> . Read-write. Reset: 0. <b>Description:</b> Read Only. Used for level triggered interrupts only. Set when interrupt message delivered. Cleared by EOI special cycle transaction or write to EOI register
13	<b>interrupt_pin_polarity</b> . Read-write. Reset: 0. <b>Description:</b> 0: High 1: Low
12	<b>delivery_status</b> . Read-write. Reset: 0. <b>Description:</b> Read Only 0: Idle 1: Send Pending
11	<b>destination_mode</b> . Read-write. Reset: 0. <b>Description:</b> 0: Physical 1: Logical
10:8	<b>delivery_mode</b> . Read-write. Reset: 0h. <b>Description:</b> 000: Fixed 001: Lowest Priority 010: <a href="#">SMI</a> /PMI 011: Reserved 100: NMI 101: INIT 110: Reserved 111: ExtINT
7:0	<b>vector</b> . Read-write. Reset: 00h. The value of this field is the clock interrupt value when bit[22] (clkintrvectororden) of FCH::PM::MISC_PMIO register is 0.

**IOAPICx00000010\_indirectaddressoffset1F  
(FCH::IOAPIC::REDIRECTION\_TABLE\_ENTRY\_7\_HIGH\_32BIT)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; IOAPICx00000010\_indirectaddressoffset1F; IOAPIC=FEC0\_0000h;  
DataPortWrite=FCH::IOAPIC::IO\_REGISTER\_SELECT\_REGISTER[indirect\_address\_offset]

Bits	Description
31:24	<b>destination_id</b> . Read-write. Reset: 00h. Bits [19:12] of the address field of the interrupt message
23:0	Reserved.

**IOAPICx00000010\_indirectaddressoffset20**  
**(FCH::IOAPIC::REDIRECTION\_TABLE\_ENTRY\_8\_LOW\_32BIT)**

Read-write. Reset: 0001\_0000h.

 \_aliasHOSTLEGACY; IOAPICx00000010\_indirectaddressoffset20; IOAPIC=FEC0\_0000h;  
 DataPortWrite=FCH::IOAPIC::IO\_REGISTER\_SELECT\_REGISTER[indirect\_address\_offset]

Bits	Description
31:17	Reserved.
16	<b>mask</b> . Read-write. Reset: 1. <b>Description:</b> Masks the interrupt injection at the input of this device. Write 0 to unmask
15	<b>trigger_mode</b> . Read-write. Reset: 0. <b>Description:</b> 0: Edge 1: Level
14	<b>remote_irr</b> . Read-write. Reset: 0. <b>Description:</b> Read Only. Used for level triggered interrupts only. Set when interrupt message delivered. Cleared by EOI special cycle transaction or write to EOI register
13	<b>interrupt_pin_polarity</b> . Read-write. Reset: 0. <b>Description:</b> 0: High 1: Low
12	<b>delivery_status</b> . Read-write. Reset: 0. <b>Description:</b> Read Only 0: Idle 1: Send Pending
11	<b>destination_mode</b> . Read-write. Reset: 0. <b>Description:</b> 0: Physical 1: Logical
10:8	<b>delivery_mode</b> . Read-write. Reset: 0h. <b>Description:</b> 000: Fixed 001: Lowest Priority 010: <a href="#">SMI</a> /PMI 011: Reserved 100: NMI 101: INIT 110: Reserved 111: ExtINT
7:0	<b>vector</b> . Read-write. Reset: 00h. The value of this field is the clock interrupt value when bit[22] (clkintrvectororden) of FCH::PM::MISC_PMIO register is 0.

**IOAPICx00000010\_indirectaddressoffset21**  
**(FCH::IOAPIC::REDIRECTION\_TABLE\_ENTRY\_8\_HIGH\_32BIT)**

Read-write. Reset: 0000\_0000h.

 \_aliasHOSTLEGACY; IOAPICx00000010\_indirectaddressoffset21; IOAPIC=FEC0\_0000h;  
 DataPortWrite=FCH::IOAPIC::IO\_REGISTER\_SELECT\_REGISTER[indirect\_address\_offset]

Bits	Description
31:24	<b>destination_id</b> . Read-write. Reset: 00h. Bits [19:12] of the address field of the interrupt message
23:0	Reserved.

### IOAPICx00000010\_indirectaddressoffset22 (FCH::IOAPIC::REDIRECTION\_TABLE\_ENTRY\_9\_LOW\_32BIT)

Read-write. Reset: 0001\_0000h.

\_aliasHOSTLEGACY; IOAPICx00000010\_indirectaddressoffset22; IOAPIC=FEC0\_0000h;  
DataPortWrite=FCH::IOAPIC::IO\_REGISTER\_SELECT\_REGISTER[indirect\_address\_offset]

Bits	Description
31:17	Reserved.
16	<b>mask.</b> Read-write. Reset: 1. <b>Description:</b> Masks the interrupt injection at the input of this device. Write 0 to unmask
15	<b>trigger_mode.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge 1: Level
14	<b>remote_irr.</b> Read-write. Reset: 0. <b>Description:</b> Read Only. Used for level triggered interrupts only. Set when interrupt message delivered. Cleared by EOI special cycle transaction or write to EOI register
13	<b>interrupt_pin_polarity.</b> Read-write. Reset: 0. <b>Description:</b> 0: High 1: Low
12	<b>delivery_status.</b> Read-write. Reset: 0. <b>Description:</b> Read Only 0: Idle 1: Send Pending
11	<b>destination_mode.</b> Read-write. Reset: 0. <b>Description:</b> 0: Physical 1: Logical
10:8	<b>delivery_mode.</b> Read-write. Reset: 0h. <b>Description:</b> 000: Fixed 001: Lowest Priority 010: <a href="#">SMI</a> /PMI 011: Reserved 100: NMI 101: INIT 110: Reserved 111: ExtINT
7:0	<b>vector.</b> Read-write. Reset: 00h. The value of this field is the clock interrupt value when bit[22] (clkintrvectororden) of FCH::PM::MISC_PMIO register is 0.

### IOAPICx00000010\_indirectaddressoffset23 (FCH::IOAPIC::REDIRECTION\_TABLE\_ENTRY\_9\_HIGH\_32BIT)

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; IOAPICx00000010\_indirectaddressoffset23; IOAPIC=FEC0\_0000h;  
DataPortWrite=FCH::IOAPIC::IO\_REGISTER\_SELECT\_REGISTER[indirect\_address\_offset]

Bits	Description
31:24	<b>destination_id.</b> Read-write. Reset: 00h. Bits [19:12] of the address field of the interrupt message
23:0	Reserved.

### IOAPICx00000010\_indirectaddressoffset24 (FCH::IOAPIC::REDIRECTION\_TABLE\_ENTRY\_10\_LOW\_32BIT)

Read-write. Reset: 0001\_0000h.

\_aliasHOSTLEGACY; IOAPICx00000010\_indirectaddressoffset24; IOAPIC=FEC0\_0000h;  
DataPortWrite=FCH::IOAPIC::IO\_REGISTER\_SELECT\_REGISTER[indirect\_address\_offset]

Bits	Description
31:17	Reserved.
16	<b>mask.</b> Read-write. Reset: 1. <b>Description:</b> Masks the interrupt injection at the input of this device. Write 0 to unmask
15	<b>trigger_mode.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge 1: Level
14	<b>remote_irr.</b> Read-write. Reset: 0. <b>Description:</b> Read Only. Used for level triggered interrupts only. Set when interrupt message delivered. Cleared by EOI special cycle transaction or write to EOI register
13	<b>interrupt_pin_polarity.</b> Read-write. Reset: 0. <b>Description:</b> 0: High 1: Low
12	<b>delivery_status.</b> Read-write. Reset: 0. <b>Description:</b> Read Only 0: Idle 1: Send Pending
11	<b>destination_mode.</b> Read-write. Reset: 0. <b>Description:</b> 0: Physical 1: Logical
10:8	<b>delivery_mode.</b> Read-write. Reset: 0h. <b>Description:</b> 000: Fixed 001: Lowest Priority 010: <a href="#">SMI</a> /PMI 011: Reserved 100: NMI 101: INIT 110: Reserved 111: ExtINT
7:0	<b>vector.</b> Read-write. Reset: 00h. The value of this field is the clock interrupt value when bit[22] (clkintrvectororden) of FCH::PM::MISC_PMIO register is 0.

### IOAPICx00000010\_indirectaddressoffset25 (FCH::IOAPIC::REDIRECTION\_TABLE\_ENTRY\_10\_HIGH\_32BIT)

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; IOAPICx00000010\_indirectaddressoffset25; IOAPIC=FEC0\_0000h;  
DataPortWrite=FCH::IOAPIC::IO\_REGISTER\_SELECT\_REGISTER[indirect\_address\_offset]

Bits	Description
31:24	<b>destination_id.</b> Read-write. Reset: 00h. Bits [19:12] of the address field of the interrupt message
23:0	Reserved.

**IOAPICx00000010\_indirectaddressoffset26**  
**(FCH::IOAPIC::REDIRECTION\_TABLE\_ENTRY\_11\_LOW\_32BIT)**

Read-write. Reset: 0001\_0000h.

 \_aliasHOSTLEGACY; IOAPICx00000010\_indirectaddressoffset26; IOAPIC=FEC0\_0000h;  
 DataPortWrite=FCH::IOAPIC::IO\_REGISTER\_SELECT\_REGISTER[indirect\_address\_offset]

Bits	Description
31:17	Reserved.
16	<b>mask.</b> Read-write. Reset: 1. <b>Description:</b> Masks the interrupt injection at the input of this device. Write 0 to unmask
15	<b>trigger_mode.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge 1: Level
14	<b>remote_irr.</b> Read-write. Reset: 0. <b>Description:</b> Read Only. Used for level triggered interrupts only. Set when interrupt message delivered. Cleared by EOI special cycle transaction or write to EOI register
13	<b>interrupt_pin_polarity.</b> Read-write. Reset: 0. <b>Description:</b> 0: High 1: Low
12	<b>delivery_status.</b> Read-write. Reset: 0. <b>Description:</b> Read Only 0: Idle 1: Send Pending
11	<b>destination_mode.</b> Read-write. Reset: 0. <b>Description:</b> 0: Physical 1: Logical
10:8	<b>delivery_mode.</b> Read-write. Reset: 0h. <b>Description:</b> 000: Fixed 001: Lowest Priority 010: <a href="#">SMI</a> /PMI 011: Reserved 100: NMI 101: INIT 110: Reserved 111: ExtINT
7:0	<b>vector.</b> Read-write. Reset: 00h. The value of this field is the clock interrupt value when bit[22] (clkintrvectororden) of FCH::PM::MISC_PMIO register is 0.

**IOAPICx00000010\_indirectaddressoffset27**  
**(FCH::IOAPIC::REDIRECTION\_TABLE\_ENTRY\_11\_HIGH\_32BIT)**

Read-write. Reset: 0000\_0000h.

 \_aliasHOSTLEGACY; IOAPICx00000010\_indirectaddressoffset27; IOAPIC=FEC0\_0000h;  
 DataPortWrite=FCH::IOAPIC::IO\_REGISTER\_SELECT\_REGISTER[indirect\_address\_offset]

Bits	Description
31:24	<b>destination_id.</b> Read-write. Reset: 00h. Bits [19:12] of the address field of the interrupt message
23:0	Reserved.

**IOAPICx00000010\_indirectaddressoffset28**  
**(FCH::IOAPIC::REDIRECTION\_TABLE\_ENTRY\_12\_LOW\_32BIT)**

Read-write. Reset: 0001\_0000h.

\_aliasHOSTLEGACY; IOAPICx00000010\_indirectaddressoffset28; IOAPIC=FEC0\_0000h;  
 DataPortWrite=FCH::IOAPIC::IO\_REGISTER\_SELECT\_REGISTER[indirect\_address\_offset]

Bits	Description
31:17	Reserved.
16	<b>mask.</b> Read-write. Reset: 1. <b>Description:</b> Masks the interrupt injection at the input of this device. Write 0 to unmask
15	<b>trigger_mode.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge 1: Level
14	<b>remote_irr.</b> Read-write. Reset: 0. <b>Description:</b> Read Only. Used for level triggered interrupts only. Set when interrupt message delivered. Cleared by EOI special cycle transaction or write to EOI register
13	<b>interrupt_pin_polarity.</b> Read-write. Reset: 0. <b>Description:</b> 0: High 1: Low
12	<b>delivery_status.</b> Read-write. Reset: 0. <b>Description:</b> Read Only 0: Idle 1: Send Pending
11	<b>destination_mode.</b> Read-write. Reset: 0. <b>Description:</b> 0: Physical 1: Logical
10:8	<b>delivery_mode.</b> Read-write. Reset: 0h. <b>Description:</b> 000: Fixed 001: Lowest Priority 010: <a href="#">SMI</a> /PMI 011: Reserved 100: NMI 101: INIT 110: Reserved 111: ExtINT
7:0	<b>vector.</b> Read-write. Reset: 00h. The value of this field is the clock interrupt value when bit[22] (clkintrvectororden) of FCH::PM::MISC_PMIO register is 0.

**IOAPICx00000010\_indirectaddressoffset29**  
**(FCH::IOAPIC::REDIRECTION\_TABLE\_ENTRY\_12\_HIGH\_32BIT)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; IOAPICx00000010\_indirectaddressoffset29; IOAPIC=FEC0\_0000h;  
 DataPortWrite=FCH::IOAPIC::IO\_REGISTER\_SELECT\_REGISTER[indirect\_address\_offset]

Bits	Description
31:24	<b>destination_id.</b> Read-write. Reset: 00h. Bits [19:12] of the address field of the interrupt message
23:0	Reserved.

**IOAPICx00000010\_indirectaddressoffset2A**  
**(FCH::IOAPIC::REDIRECTION\_TABLE\_ENTRY\_13\_LOW\_32BIT)**

Read-write. Reset: 0001\_0000h.

\_aliasHOSTLEGACY; IOAPICx00000010\_indirectaddressoffset2A; IOAPIC=FEC0\_0000h;  
 DataPortWrite=FCH::IOAPIC::IO\_REGISTER\_SELECT\_REGISTER[indirect\_address\_offset]

Bits	Description
31:17	Reserved.
16	<b>mask.</b> Read-write. Reset: 1. <b>Description:</b> Masks the interrupt injection at the input of this device. Write 0 to unmask
15	<b>trigger_mode.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge 1: Level
14	<b>remote_irr.</b> Read-write. Reset: 0. <b>Description:</b> Read Only. Used for level triggered interrupts only. Set when interrupt message delivered. Cleared by EOI special cycle transaction or write to EOI register
13	<b>interrupt_pin_polarity.</b> Read-write. Reset: 0. <b>Description:</b> 0: High 1: Low
12	<b>delivery_status.</b> Read-write. Reset: 0. <b>Description:</b> Read Only 0: Idle 1: Send Pending
11	<b>destination_mode.</b> Read-write. Reset: 0. <b>Description:</b> 0: Physical 1: Logical
10:8	<b>delivery_mode.</b> Read-write. Reset: 0h. <b>Description:</b> 000: Fixed 001: Lowest Priority 010: <a href="#">SMI</a> /PMI 011: Reserved 100: NMI 101: INIT 110: Reserved 111: ExtINT
7:0	<b>vector.</b> Read-write. Reset: 00h. The value of this field is the clock interrupt value when bit[22] (clkintrvectororden) of FCH::PM::MISC_PMIO register is 0.

**IOAPICx00000010\_indirectaddressoffset2B**  
**(FCH::IOAPIC::REDIRECTION\_TABLE\_ENTRY\_13\_HIGH\_32BIT)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; IOAPICx00000010\_indirectaddressoffset2B; IOAPIC=FEC0\_0000h;  
 DataPortWrite=FCH::IOAPIC::IO\_REGISTER\_SELECT\_REGISTER[indirect\_address\_offset]

Bits	Description
31:24	<b>destination_id.</b> Read-write. Reset: 00h. Bits [19:12] of the address field of the interrupt message
23:0	Reserved.



**IOAPICx00000010\_indirectaddressoffset2C**  
**(FCH::IOAPIC::REDIRECTION\_TABLE\_ENTRY\_14\_LOW\_32BIT)**

Read-write. Reset: 0001\_0000h.

\_aliasHOSTLEGACY; IOAPICx00000010\_indirectaddressoffset2C; IOAPIC=FEC0\_0000h;  
 DataPortWrite=FCH::IOAPIC::IO\_REGISTER\_SELECT\_REGISTER[indirect\_address\_offset]

Bits	Description
31:17	Reserved.
16	<b>mask.</b> Read-write. Reset: 1. <b>Description:</b> Masks the interrupt injection at the input of this device. Write 0 to unmask
15	<b>trigger_mode.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge 1: Level
14	<b>remote_irr.</b> Read-write. Reset: 0. <b>Description:</b> Read Only. Used for level triggered interrupts only. Set when interrupt message delivered. Cleared by EOI special cycle transaction or write to EOI register
13	<b>interrupt_pin_polarity.</b> Read-write. Reset: 0. <b>Description:</b> 0: High 1: Low
12	<b>delivery_status.</b> Read-write. Reset: 0. <b>Description:</b> Read Only 0: Idle 1: Send Pending
11	<b>destination_mode.</b> Read-write. Reset: 0. <b>Description:</b> 0: Physical 1: Logical
10:8	<b>delivery_mode.</b> Read-write. Reset: 0h. <b>Description:</b> 000: Fixed 001: Lowest Priority 010: <a href="#">SMI</a> /PMI 011: Reserved 100: NMI 101: INIT 110: Reserved 111: ExtINT
7:0	<b>vector.</b> Read-write. Reset: 00h. The value of this field is the clock interrupt value when bit[22] (clkintrvectororden) of FCH::PM::MISC_PMIO register is 0.

**IOAPICx00000010\_indirectaddressoffset2D**  
**(FCH::IOAPIC::REDIRECTION\_TABLE\_ENTRY\_14\_HIGH\_32BIT)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; IOAPICx00000010\_indirectaddressoffset2D; IOAPIC=FEC0\_0000h;  
 DataPortWrite=FCH::IOAPIC::IO\_REGISTER\_SELECT\_REGISTER[indirect\_address\_offset]

Bits	Description
31:24	<b>destination_id.</b> Read-write. Reset: 00h. Bits [19:12] of the address field of the interrupt message
23:0	Reserved.

**IOAPICx00000010\_indirectaddressoffset2E  
(FCH::IOAPIC::REDIRECTION\_TABLE\_ENTRY\_15\_LOW\_32BIT)**

Read-write. Reset: 0001\_0000h.

 \_aliasHOSTLEGACY; IOAPICx00000010\_indirectaddressoffset2E; IOAPIC=FEC0\_0000h;  
DataPortWrite=FCH::IOAPIC::IO\_REGISTER\_SELECT\_REGISTER[indirect\_address\_offset]

Bits	Description
31:17	Reserved.
16	<b>mask.</b> Read-write. Reset: 1. <b>Description:</b> Masks the interrupt injection at the input of this device. Write 0 to unmask
15	<b>trigger_mode.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge 1: Level
14	<b>remote_irr.</b> Read-write. Reset: 0. <b>Description:</b> Read Only. Used for level triggered interrupts only. Set when interrupt message delivered. Cleared by EOI special cycle transaction or write to EOI register
13	<b>interrupt_pin_polarity.</b> Read-write. Reset: 0. <b>Description:</b> 0: High 1: Low
12	<b>delivery_status.</b> Read-write. Reset: 0. <b>Description:</b> Read Only 0: Idle 1: Send Pending
11	<b>destination_mode.</b> Read-write. Reset: 0. <b>Description:</b> 0: Physical 1: Logical
10:8	<b>delivery_mode.</b> Read-write. Reset: 0h. <b>Description:</b> 000: Fixed 001: Lowest Priority 010: <a href="#">SMI</a> /PMI 011: Reserved 100: NMI 101: INIT 110: Reserved 111: ExtINT
7:0	<b>vector.</b> Read-write. Reset: 00h. The value of this field is the clock interrupt value when bit[22] (clkintrvectororden) of FCH::PM::MISC_PMIO register is 0.

**IOAPICx00000010\_indirectaddressoffset2F  
(FCH::IOAPIC::REDIRECTION\_TABLE\_ENTRY\_15\_HIGH\_32BIT)**

Read-write. Reset: 0000\_0000h.

 \_aliasHOSTLEGACY; IOAPICx00000010\_indirectaddressoffset2F; IOAPIC=FEC0\_0000h;  
DataPortWrite=FCH::IOAPIC::IO\_REGISTER\_SELECT\_REGISTER[indirect\_address\_offset]

Bits	Description
31:24	<b>destination_id.</b> Read-write. Reset: 00h. Bits [19:12] of the address field of the interrupt message
23:0	Reserved.

**IOAPICx00000010\_indirectaddressoffset30  
(FCH::IOAPIC::REDIRECTION\_TABLE\_ENTRY\_16\_LOW\_32BIT)**

Read-write. Reset: 0001\_0000h.

\_aliasHOSTLEGACY; IOAPICx00000010\_indirectaddressoffset30; IOAPIC=FEC0\_0000h;  
DataPortWrite=FCH::IOAPIC::IO\_REGISTER\_SELECT\_REGISTER[indirect\_address\_offset]

Bits	Description
31:17	Reserved.
16	<b>mask.</b> Read-write. Reset: 1. <b>Description:</b> Masks the interrupt injection at the input of this device. Write 0 to unmask
15	<b>trigger_mode.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge 1: Level
14	<b>remote_irr.</b> Read-write. Reset: 0. <b>Description:</b> Read Only. Used for level triggered interrupts only. Set when interrupt message delivered. Cleared by EOI special cycle transaction or write to EOI register
13	<b>interrupt_pin_polarity.</b> Read-write. Reset: 0. <b>Description:</b> 0: High 1: Low
12	<b>delivery_status.</b> Read-write. Reset: 0. <b>Description:</b> Read Only 0: Idle 1: Send Pending
11	<b>destination_mode.</b> Read-write. Reset: 0. <b>Description:</b> 0: Physical 1: Logical
10:8	<b>delivery_mode.</b> Read-write. Reset: 0h. <b>Description:</b> 000: Fixed 001: Lowest Priority 010: <a href="#">SMI</a> /PMI 011: Reserved 100: NMI 101: INIT 110: Reserved 111: ExtINT
7:0	<b>vector.</b> Read-write. Reset: 00h. The value of this field is the clock interrupt value when bit[22] (clkintrvectororden) of FCH::PM::MISC_PMIO register is 0.

**IOAPICx00000010\_indirectaddressoffset31  
(FCH::IOAPIC::REDIRECTION\_TABLE\_ENTRY\_16\_HIGH\_32BIT)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; IOAPICx00000010\_indirectaddressoffset31; IOAPIC=FEC0\_0000h;  
DataPortWrite=FCH::IOAPIC::IO\_REGISTER\_SELECT\_REGISTER[indirect\_address\_offset]

Bits	Description
31:24	<b>destination_id.</b> Read-write. Reset: 00h. Bits [19:12] of the address field of the interrupt message
23:0	Reserved.

**IOAPICx00000010\_indirectaddressoffset32**  
**(FCH::IOAPIC::REDIRECTION\_TABLE\_ENTRY\_17\_LOW\_32BIT)**

Read-write. Reset: 0001\_0000h.

 \_aliasHOSTLEGACY; IOAPICx00000010\_indirectaddressoffset32; IOAPIC=FEC0\_0000h;  
 DataPortWrite=FCH::IOAPIC::IO\_REGISTER\_SELECT\_REGISTER[indirect\_address\_offset]

Bits	Description
31:17	Reserved.
16	<b>mask.</b> Read-write. Reset: 1. <b>Description:</b> Masks the interrupt injection at the input of this device. Write 0 to unmask
15	<b>trigger_mode.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge 1: Level
14	<b>remote_irr.</b> Read-write. Reset: 0. <b>Description:</b> Read Only. Used for level triggered interrupts only. Set when interrupt message delivered. Cleared by EOI special cycle transaction or write to EOI register
13	<b>interrupt_pin_polarity.</b> Read-write. Reset: 0. <b>Description:</b> 0: High 1: Low
12	<b>delivery_status.</b> Read-write. Reset: 0. <b>Description:</b> Read Only 0: Idle 1: Send Pending
11	<b>destination_mode.</b> Read-write. Reset: 0. <b>Description:</b> 0: Physical 1: Logical
10:8	<b>delivery_mode.</b> Read-write. Reset: 0h. <b>Description:</b> 000: Fixed 001: Lowest Priority 010: <a href="#">SMI</a> /PMI 011: Reserved 100: NMI 101: INIT 110: Reserved 111: ExtINT
7:0	<b>vector.</b> Read-write. Reset: 00h. The value of this field is the clock interrupt value when bit[22] (clkintrvectororden) of FCH::PM::MISC_PMIO register is 0.

**IOAPICx00000010\_indirectaddressoffset33**  
**(FCH::IOAPIC::REDIRECTION\_TABLE\_ENTRY\_17\_HIGH\_32BIT)**

Read-write. Reset: 0000\_0000h.

 \_aliasHOSTLEGACY; IOAPICx00000010\_indirectaddressoffset33; IOAPIC=FEC0\_0000h;  
 DataPortWrite=FCH::IOAPIC::IO\_REGISTER\_SELECT\_REGISTER[indirect\_address\_offset]

Bits	Description
31:24	<b>destination_id.</b> Read-write. Reset: 00h. Bits [19:12] of the address field of the interrupt message
23:0	Reserved.

### IOAPICx00000010\_indirectaddressoffset34 (FCH::IOAPIC::REDIRECTION\_TABLE\_ENTRY\_18\_LOW\_32BIT)

Read-write. Reset: 0001\_0000h.

\_aliasHOSTLEGACY; IOAPICx00000010\_indirectaddressoffset34; IOAPIC=FEC0\_0000h;  
DataPortWrite=FCH::IOAPIC::IO\_REGISTER\_SELECT\_REGISTER[indirect\_address\_offset]

Bits	Description
31:17	Reserved.
16	<b>mask.</b> Read-write. Reset: 1. <b>Description:</b> Masks the interrupt injection at the input of this device. Write 0 to unmask
15	<b>trigger_mode.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge 1: Level
14	<b>remote_irr.</b> Read-write. Reset: 0. <b>Description:</b> Read Only. Used for level triggered interrupts only. Set when interrupt message delivered. Cleared by EOI special cycle transaction or write to EOI register
13	<b>interrupt_pin_polarity.</b> Read-write. Reset: 0. <b>Description:</b> 0: High 1: Low
12	<b>delivery_status.</b> Read-write. Reset: 0. <b>Description:</b> Read Only 0: Idle 1: Send Pending
11	<b>destination_mode.</b> Read-write. Reset: 0. <b>Description:</b> 0: Physical 1: Logical
10:8	<b>delivery_mode.</b> Read-write. Reset: 0h. <b>Description:</b> 000: Fixed 001: Lowest Priority 010: <a href="#">SMI</a> /PMI 011: Reserved 100: NMI 101: INIT 110: Reserved 111: ExtINT
7:0	<b>vector.</b> Read-write. Reset: 00h. The value of this field is the clock interrupt value when bit[22] (clkintrvectororden) of FCH::PM::MISC_PMIO register is 0.

### IOAPICx00000010\_indirectaddressoffset35 (FCH::IOAPIC::REDIRECTION\_TABLE\_ENTRY\_18\_HIGH\_32BIT)

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; IOAPICx00000010\_indirectaddressoffset35; IOAPIC=FEC0\_0000h;  
DataPortWrite=FCH::IOAPIC::IO\_REGISTER\_SELECT\_REGISTER[indirect\_address\_offset]

Bits	Description
31:24	<b>destination_id.</b> Read-write. Reset: 00h. Bits [19:12] of the address field of the interrupt message
23:0	Reserved.

**IOAPICx00000010\_indirectaddressoffset36**  
**(FCH::IOAPIC::REDIRECTION\_TABLE\_ENTRY\_19\_LOW\_32BIT)**

Read-write. Reset: 0001\_0000h.

\_aliasHOSTLEGACY; IOAPICx00000010\_indirectaddressoffset36; IOAPIC=FEC0\_0000h;  
 DataPortWrite=FCH::IOAPIC::IO\_REGISTER\_SELECT\_REGISTER[indirect\_address\_offset]

Bits	Description
31:17	Reserved.
16	<b>mask.</b> Read-write. Reset: 1. <b>Description:</b> Masks the interrupt injection at the input of this device. Write 0 to unmask
15	<b>trigger_mode.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge 1: Level
14	<b>remote_irr.</b> Read-write. Reset: 0. <b>Description:</b> Read Only. Used for level triggered interrupts only. Set when interrupt message delivered. Cleared by EOI special cycle transaction or write to EOI register
13	<b>interrupt_pin_polarity.</b> Read-write. Reset: 0. <b>Description:</b> 0: High 1: Low
12	<b>delivery_status.</b> Read-write. Reset: 0. <b>Description:</b> Read Only 0: Idle 1: Send Pending
11	<b>destination_mode.</b> Read-write. Reset: 0. <b>Description:</b> 0: Physical 1: Logical
10:8	<b>delivery_mode.</b> Read-write. Reset: 0h. <b>Description:</b> 000: Fixed 001: Lowest Priority 010: <a href="#">SMI</a> /PMI 011: Reserved 100: NMI 101: INIT 110: Reserved 111: ExtINT
7:0	<b>vector.</b> Read-write. Reset: 00h. The value of this field is the clock interrupt value when bit[22] (clkintrvectororden) of FCH::PM::MISC_PMIO register is 0.

**IOAPICx00000010\_indirectaddressoffset37**  
**(FCH::IOAPIC::REDIRECTION\_TABLE\_ENTRY\_19\_HIGH\_32BIT)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; IOAPICx00000010\_indirectaddressoffset37; IOAPIC=FEC0\_0000h;  
 DataPortWrite=FCH::IOAPIC::IO\_REGISTER\_SELECT\_REGISTER[indirect\_address\_offset]

Bits	Description
31:24	<b>destination_id.</b> Read-write. Reset: 00h. Bits [19:12] of the address field of the interrupt message
23:0	Reserved.

**IOAPICx00000010\_indirectaddressoffset38**  
**(FCH::IOAPIC::REDIRECTION\_TABLE\_ENTRY\_20\_LOW\_32BIT)**

Read-write. Reset: 0001\_0000h.

\_aliasHOSTLEGACY; IOAPICx00000010\_indirectaddressoffset38; IOAPIC=FEC0\_0000h;  
 DataPortWrite=FCH::IOAPIC::IO\_REGISTER\_SELECT\_REGISTER[indirect\_address\_offset]

Bits	Description
31:17	Reserved.
16	<b>mask.</b> Read-write. Reset: 1. <b>Description:</b> Masks the interrupt injection at the input of this device. Write 0 to unmask
15	<b>trigger_mode.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge 1: Level
14	<b>remote_irr.</b> Read-write. Reset: 0. <b>Description:</b> Read Only. Used for level triggered interrupts only. Set when interrupt message delivered. Cleared by EOI special cycle transaction or write to EOI register
13	<b>interrupt_pin_polarity.</b> Read-write. Reset: 0. <b>Description:</b> 0: High 1: Low
12	<b>delivery_status.</b> Read-write. Reset: 0. <b>Description:</b> Read Only 0: Idle 1: Send Pending
11	<b>destination_mode.</b> Read-write. Reset: 0. <b>Description:</b> 0: Physical 1: Logical
10:8	<b>delivery_mode.</b> Read-write. Reset: 0h. <b>Description:</b> 000: Fixed 001: Lowest Priority 010: <a href="#">SMI</a> /PMI 011: Reserved 100: NMI 101: INIT 110: Reserved 111: ExtINT
7:0	<b>vector.</b> Read-write. Reset: 00h. The value of this field is the clock interrupt value when bit[22] (clkintrvectororden) of FCH::PM::MISC_PMIO register is 0.

**IOAPICx00000010\_indirectaddressoffset39**  
**(FCH::IOAPIC::REDIRECTION\_TABLE\_ENTRY\_20\_HIGH\_32BIT)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; IOAPICx00000010\_indirectaddressoffset39; IOAPIC=FEC0\_0000h;  
 DataPortWrite=FCH::IOAPIC::IO\_REGISTER\_SELECT\_REGISTER[indirect\_address\_offset]

Bits	Description
31:24	<b>destination_id.</b> Read-write. Reset: 00h. Bits [19:12] of the address field of the interrupt message
23:0	Reserved.

**IOAPICx00000010\_indirectaddressoffset3A**  
**(FCH::IOAPIC::REDIRECTION\_TABLE\_ENTRY\_21\_LOW\_32BIT)**

Read-write. Reset: 0001\_0000h.

\_aliasHOSTLEGACY; IOAPICx00000010\_indirectaddressoffset3A; IOAPIC=FEC0\_0000h;  
 DataPortWrite=FCH::IOAPIC::IO\_REGISTER\_SELECT\_REGISTER[indirect\_address\_offset]

Bits	Description
31:17	Reserved.
16	<b>mask.</b> Read-write. Reset: 1. <b>Description:</b> Masks the interrupt injection at the input of this device. Write 0 to unmask
15	<b>trigger_mode.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge 1: Level
14	<b>remote_irr.</b> Read-write. Reset: 0. <b>Description:</b> Read Only. Used for level triggered interrupts only. Set when interrupt message delivered. Cleared by EOI special cycle transaction or write to EOI register
13	<b>interrupt_pin_polarity.</b> Read-write. Reset: 0. <b>Description:</b> 0: High 1: Low
12	<b>delivery_status.</b> Read-write. Reset: 0. <b>Description:</b> Read Only 0: Idle 1: Send Pending
11	<b>destination_mode.</b> Read-write. Reset: 0. <b>Description:</b> 0: Physical 1: Logical
10:8	<b>delivery_mode.</b> Read-write. Reset: 0h. <b>Description:</b> 000: Fixed 001: Lowest Priority 010: <a href="#">SMI</a> /PMI 011: Reserved 100: NMI 101: INIT 110: Reserved 111: ExtINT
7:0	<b>vector.</b> Read-write. Reset: 00h. The value of this field is the clock interrupt value when bit[22] (clkintrvectororden) of FCH::PM::MISC_PMIO register is 0.

**IOAPICx00000010\_indirectaddressoffset3B**  
**(FCH::IOAPIC::REDIRECTION\_TABLE\_ENTRY\_21\_HIGH\_32BIT)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; IOAPICx00000010\_indirectaddressoffset3B; IOAPIC=FEC0\_0000h;  
 DataPortWrite=FCH::IOAPIC::IO\_REGISTER\_SELECT\_REGISTER[indirect\_address\_offset]

Bits	Description
31:24	<b>destination_id.</b> Read-write. Reset: 00h. Bits [19:12] of the address field of the interrupt message
23:0	Reserved.



**IOAPICx00000010\_indirectaddressoffset3C**  
**(FCH::IOAPIC::REDIRECTION\_TABLE\_ENTRY\_22\_LOW\_32BIT)**

Read-write. Reset: 0001\_0000h.

\_aliasHOSTLEGACY; IOAPICx00000010\_indirectaddressoffset3C; IOAPIC=FEC0\_0000h;  
 DataPortWrite=FCH::IOAPIC::IO\_REGISTER\_SELECT\_REGISTER[indirect\_address\_offset]

Bits	Description
31:17	Reserved.
16	<b>mask.</b> Read-write. Reset: 1. <b>Description:</b> Masks the interrupt injection at the input of this device. Write 0 to unmask
15	<b>trigger_mode.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge 1: Level
14	<b>remote_irr.</b> Read-write. Reset: 0. <b>Description:</b> Read Only. Used for level triggered interrupts only. Set when interrupt message delivered. Cleared by EOI special cycle transaction or write to EOI register
13	<b>interrupt_pin_polarity.</b> Read-write. Reset: 0. <b>Description:</b> 0: High 1: Low
12	<b>delivery_status.</b> Read-write. Reset: 0. <b>Description:</b> Read Only 0: Idle 1: Send Pending
11	<b>destination_mode.</b> Read-write. Reset: 0. <b>Description:</b> 0: Physical 1: Logical
10:8	<b>delivery_mode.</b> Read-write. Reset: 0h. <b>Description:</b> 000: Fixed 001: Lowest Priority 010: <a href="#">SMI</a> /PMI 011: Reserved 100: NMI 101: INIT 110: Reserved 111: ExtINT
7:0	<b>vector.</b> Read-write. Reset: 00h. The value of this field is the clock interrupt value when bit[22] (clkintrvectororden) of FCH::PM::MISC_PMIO register is 0.

**IOAPICx00000010\_indirectaddressoffset3D**  
**(FCH::IOAPIC::REDIRECTION\_TABLE\_ENTRY\_22\_HIGH\_32BIT)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; IOAPICx00000010\_indirectaddressoffset3D; IOAPIC=FEC0\_0000h;  
 DataPortWrite=FCH::IOAPIC::IO\_REGISTER\_SELECT\_REGISTER[indirect\_address\_offset]

Bits	Description
31:24	<b>destination_id.</b> Read-write. Reset: 00h. Bits [19:12] of the address field of the interrupt message
23:0	Reserved.

**IOAPICx00000010\_indirectaddressoffset3E  
(FCH::IOAPIC::REDIRECTION\_TABLE\_ENTRY\_23\_LOW\_32BIT)**

Read-write. Reset: 0001\_0000h.

\_aliasHOSTLEGACY; IOAPICx00000010\_indirectaddressoffset3E; IOAPIC=FEC0\_0000h;  
DataPortWrite=FCH::IOAPIC::IO\_REGISTER\_SELECT\_REGISTER[indirect\_address\_offset]

Bits	Description
31:17	Reserved.
16	<b>mask.</b> Read-write. Reset: 1. <b>Description:</b> Masks the interrupt injection at the input of this device. Write 0 to unmask
15	<b>trigger_mode.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge 1: Level
14	<b>remote_irr.</b> Read-write. Reset: 0. <b>Description:</b> Read Only. Used for level triggered interrupts only. Set when interrupt message delivered. Cleared by EOI special cycle transaction or write to EOI register
13	<b>interrupt_pin_polarity.</b> Read-write. Reset: 0. <b>Description:</b> 0: High 1: Low
12	<b>delivery_status.</b> Read-write. Reset: 0. <b>Description:</b> Read Only 0: Idle 1: Send Pending
11	<b>destination_mode.</b> Read-write. Reset: 0. <b>Description:</b> 0: Physical 1: Logical
10:8	<b>delivery_mode.</b> Read-write. Reset: 0h. <b>Description:</b> 000: Fixed 001: Lowest Priority 010: <a href="#">SMI</a> /PMI 011: Reserved 100: NMI 101: INIT 110: Reserved 111: ExtINT
7:0	<b>vector.</b> Read-write. Reset: 00h. The value of this field is the clock interrupt value when bit[22] (clkintrvectororden) of FCH::PM::MISC_PMIO register is 0.

**IOAPICx00000010\_indirectaddressoffset3F  
(FCH::IOAPIC::REDIRECTION\_TABLE\_ENTRY\_23\_HIGH\_32BIT)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; IOAPICx00000010\_indirectaddressoffset3F; IOAPIC=FEC0\_0000h;  
DataPortWrite=FCH::IOAPIC::IO\_REGISTER\_SELECT\_REGISTER[indirect\_address\_offset]

Bits	Description
31:24	<b>destination_id.</b> Read-write. Reset: 00h. Bits [19:12] of the address field of the interrupt message
23:0	Reserved.

**IOAPICx00000020 (FCH::IOAPIC::IRQ\_PIN\_ASSERTION\_REGISTER)**

Read-write. Reset: 0000\_0000h.

Write to this register will trigger an interrupt associated with the redirection table entry referenced by the IRQ number. Currently the redirection table has 24 entries. Write with IRQ number greater than 17H has no effect.

\_aliasHOSTLEGACY; IOAPICx00000020; IOAPIC=FEC0\_0000h

Bits	Description
31:8	Reserved.
7:0	<b>input_irq</b> . Read-write. Reset: 00h. IRQ number for the requested interrupt

**IOAPICx00000040 (FCH::IOAPIC::EOI\_REGISTER)**

Write-only. Reset: 0000\_0000h.

Write to this register will clear the remote IRR bit in the redirection table entry found matching the interrupt vector. This provides an alternate mechanism other than PCI special cycle for EOI to reach IOXAPIC.

\_aliasHOSTLEGACY; IOAPICx00000040; IOAPIC=FEC0\_0000h

Bits	Description
31:8	Reserved.
7:0	<b>vector</b> . Write-only. Reset: 00h. Interrupt vector. Write 1 to clear the interrupt in REDIRECTION_TABLE_ENTRY_<0~23>_LOW_32BIT registers.

**11.3.3 SMI Registers**

[SMI](#) register space is accessed through the AcpiMmio region. The SMI registers range from FED8\_0000h+200h to FED8\_0000h+2FFh. See FCH::PM::ISACONTROL[mmioen].

**SMIx00000000 (FCH::SMI::EVENT\_STATUS)**

Read-write.

\_aliasHOSTLEGACY; SMIx00000000; SMI=FED8\_0200h

Bits	Description
31:0	<b>eventstatus</b> . Read-write. Reset: XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXb. <b>Description:</b> This is a mirror register of the standard ACPI EVENT_STATUS register. Writing 1 to each bit clears the corresponding status bit. Each Event status is set when the selected event input equals to the corresponding value in SciTrig.

**SMIx00000004 (FCH::SMI::EVENT\_ENABLE)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; SMIx00000004; SMI=FED8\_0200h

Bits	Description
31:0	<b>eventenable</b> . Read-write. Reset: 0000_0000h. This is the mirror register of the standard ACPI EVENT_ENABLE register. Each bit controls whether ACP should generate wakeup and Sci interrupt.

**SMIx00000008 (FCH::SMI::SCITRIG)**

Read-write. Reset: FFFF\_FFFFh.

\_aliasHOSTLEGACY; SMIx00000008; SMI=FED8\_0200h

Bits	Description
31	<b>scitrig31.</b> Read-write. Reset: 1. <b>Description:</b> The bit controls the way to set Event_Status bit 31 0: Active low 1: Active high
30	<b>scitrig30.</b> Read-write. Reset: 1. <b>Description:</b> The bit controls the way to set Event_Status bit 30 0: Active low 1: Active high
29	<b>scitrig29.</b> Read-write. Reset: 1. <b>Description:</b> The bit controls the way to set Event_Status bit 29 0: Active low 1: Active high
28	<b>scitrig28.</b> Read-write. Reset: 1. <b>Description:</b> The bit controls the way to set Event_Status bit 28 0: Active low 1: Active high
27	<b>scitrig27.</b> Read-write. Reset: 1. <b>Description:</b> The bit controls the way to set Event_Status bit 27 0: Active low 1: Active high
26	<b>scitrig26.</b> Read-write. Reset: 1. <b>Description:</b> The bit controls the way to set Event_Status bit 26 0: Active low 1: Active high
25	<b>scitrig25.</b> Read-write. Reset: 1. <b>Description:</b> The bit controls the way to set Event_Status bit 25 0: Active low 1: Active high
24	<b>scitrig24.</b> Read-write. Reset: 1. <b>Description:</b> The bit controls the way to set Event_Status bit 24 0: Active low 1: Active high
23	<b>scitrig23.</b> Read-write. Reset: 1. <b>Description:</b> The bit controls the way to set Event_Status bit 23 0: Active low 1: Active high
22	<b>scitrig22.</b> Read-write. Reset: 1. <b>Description:</b> The bit controls the way to set Event_Status bit 22 0: Active low 1: Active high
21	<b>scitrig21.</b> Read-write. Reset: 1. <b>Description:</b> The bit controls the way to set Event_Status bit 21 0: Active low 1: Active high
20	<b>scitrig20.</b> Read-write. Reset: 1.

	<b>Description:</b> The bit controls the way to set Event_Status bit 20 0: Active low 1: Active high
19	<b>scitrig19.</b> Read-write. Reset: 1. <b>Description:</b> The bit controls the way to set Event_Status bit 19 0: Active low 1: Active high
18	<b>scitrig18.</b> Read-write. Reset: 1. <b>Description:</b> The bit controls the way to set Event_Status bit 18 0: Active low 1: Active high
17	<b>scitrig17.</b> Read-write. Reset: 1. <b>Description:</b> The bit controls the way to set Event_Status bit 17 0: Active low 1: Active high
16	<b>scitrig16.</b> Read-write. Reset: 1. <b>Description:</b> The bit controls the way to set Event_Status bit 16 0: Active low 1: Active high
15	<b>scitrig15.</b> Read-write. Reset: 1. <b>Description:</b> The bit controls the way to set Event_Status bit 15 0: Active low 1: Active high
14	<b>scitrig14.</b> Read-write. Reset: 1. <b>Description:</b> The bit controls the way to set Event_Status bit 14 0: Active low 1: Active high
13	<b>scitrig13.</b> Read-write. Reset: 1. <b>Description:</b> The bit controls the way to set Event_Status bit 13 0: Active low 1: Active high
12	<b>scitrig12.</b> Read-write. Reset: 1. <b>Description:</b> The bit controls the way to set Event_Status bit 12 0: Active low 1: Active high
11	<b>scitrig11.</b> Read-write. Reset: 1. <b>Description:</b> The bit controls the way to set Event_Status bit 11 0: Falling edge 1: Active high
10	<b>scitrig10.</b> Read-write. Reset: 1. <b>Description:</b> The bit controls the way to set Event_Status bit 10 0: Active low 1: Active high
9	<b>scitrig9.</b> Read-write. Reset: 1. <b>Description:</b> The bit controls the way to set Event_Status bit 9 0: Active low 1: Active high
8	<b>scitrig8.</b> Read-write. Reset: 1. <b>Description:</b> The bit controls the way to set Event_Status bit 8 0: Active low 1: Active high

7	<b>scitrig7.</b> Read-write. Reset: 1. <b>Description:</b> The bit controls the way to set Event_Status bit 7 0: Active low 1: Active high
6	<b>scitrig6.</b> Read-write. Reset: 1. <b>Description:</b> The bit controls the way to set Event_Status bit 6 0: Active low 1: Active high
5	<b>scitrig5.</b> Read-write. Reset: 1. <b>Description:</b> The bit controls the way to set Event_Status bit 5 0: Active low 1: Active high
4	<b>scitrig4.</b> Read-write. Reset: 1. <b>Description:</b> The bit controls the way to set Event_Status bit 4 0: Active low 1: Active high
3	<b>scitrig3.</b> Read-write. Reset: 1. <b>Description:</b> The bit controls the way to set Event_Status bit 3 0: Active low 1: Active high
2	<b>scitrig2.</b> Read-write. Reset: 1. <b>Description:</b> The bit controls the way to set Event_Status bit 2 0: Active low 1: Active high
1	<b>scitrig1.</b> Read-write. Reset: 1. <b>Description:</b> The bit controls the way to set Event_Status bit 1 0: Active low 1: Active high
0	<b>scitrig0.</b> Read-write. Reset: 1. <b>Description:</b> The bit controls the way to set Event_Status bit 0 0: Active low 1: Active high

**SMIx0000000C (FCH::SMI::SCILEVL)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; SMIx0000000C; SMI=FED8\_0200h

Bits	Description
31	<b>scilevl31.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
30	<b>scilevl30.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
29	<b>scilevl29.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
28	<b>scilevl28.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
27	<b>scilevl27.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
26	<b>scilevl26.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
25	<b>scilevl25.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
24	<b>scilevl24.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
23	<b>scilevl23.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
22	<b>scilevl22.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
21	<b>scilevl21.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
20	<b>scilevl20.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
19	<b>scilevl19.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
18	<b>scilevl18.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
17	<b>scilevl17.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
16	<b>scilevl16.</b> Read-write. Reset: 0.

	<b>Description:</b> 0: Edge trigger 1: Level trigger
15	<b>scilevl15.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
14	<b>scilevl14.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
13	<b>scilevl13.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
12	<b>scilevl12.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
11	<b>scilevl11.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
10	<b>scilevl10.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
9	<b>scilevl9.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
8	<b>scilevl8.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>scilevl7.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
6	<b>scilevl6.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
5	<b>scilevl5.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
4	<b>scilevl4.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
3	<b>scilevl3.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
2	<b>scilevl2.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
1	<b>scilevl1.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
0	<b>scilevl0.</b> Read-write. Reset: 0.



	<b>Description:</b> This register defines the trigger mode for each of the Event_Status: 0: Edge trigger 1: Level trigger
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**SMIx00000010 (FCH::SMI::SMISCISTATUS)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; SMIx00000010; SMI=FED8\_0200h

Bits	Description
31:0	<b>smiscistatus.</b> Read-write. Reset: 0000_0000h. <b>Description:</b> Each bit indicates the corresponding SmiSci status. The input of each bit is controlled by the corresponding SciTrig bit. Each status bit can be cleared to 0 by writing 1. Note this function can be considered as a superset of Event_Status. When one of this bit is set (and its SmiSciEn is also set), it will trigger a <a href="#">SMI</a> to call the BIOS. After the BIOS has serviced the <a href="#">SMM</a> and clears its status, the internal logic will automatically set the corresponding Event_Status bit and thereby triggering a SCI.

**SMIx00000014 (FCH::SMI::SMISCIENT)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; SMIx00000014; SMI=FED8\_0200h

Bits	Description
31:0	<b>smiscien.</b> Read-write. Reset: 0000_0000h. <b>Description:</b> Each bit controls if <a href="#">SMI</a> message will be generated when the corresponding SmiSciStatus bit is set to 1. 0: Not to send SMI message when the corresponding SmiSciStatus bit is set 1: Send SMI message when the corresponding SmiSciStatus bit is set

**SMIx00000018 (FCH::SMI::SOFTWARESCIEN)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; SMIx00000018; SMI=FED8\_0200h

Bits	Description
31:0	<b>softwarescien.</b> Read-write. Reset: 0000_0000h. When set, software can write to softwareSciData and set the corresponding Event_Status bit (note the setting of this bit will need to match with SciTrig and SciLevl in order to set the status bit). This register is meant as a software mechanism to trigger SCI.

**SMIx0000001C (FCH::SMI::SOFTWARESCIDATA)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; SMIx0000001C; SMI=FED8\_0200h

Bits	Description
31:0	<b>softwarescidata.</b> Read-write. Reset: 0000_0000h. This is the software data path to set the corresponding Event_Status when softwareSciEn is set

**SMIx00000020 (FCH::SMI::SCISLEEPDISABLE)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; SMIx00000020; SMI=FED8\_0200h

Bits	Description
31:0	<b>scisleepdisable.</b> Read-write. Reset: 0000_0000h. When set, the corresponding Event_Status bit will be masked off whenever the system goes to S3 or higher sleep state. This is meant for ignoring EVENT pins that are powered in the main power domain (instead of aux. power domain).

**SMIx00000030 (FCH::SMI::CAPTUREDDATA)**

Read-only.

\_aliasHOSTLEGACY; SMIx00000030; SMI=FED8\_0200h

Bits	Description
31:0	<b>captureddata.</b> Read-only. Reset: XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXb. This is the buffer to capture write data for the last transaction that caused an <a href="#">SMI</a> #. Note: this buffer has no meaning for a read trap

**SMIx00000034 (FCH::SMI::CAPTUREDVALID)**

Read-only.

\_aliasHOSTLEGACY; SMIx00000034; SMI=FED8\_0200h

Bits	Description
7:4	Reserved.
3:0	<b>capturedvalid.</b> Read-only. Reset: XXXXb. This is the byte valid buffer to signal which byte is captured for the last transaction that caused the <a href="#">SMI</a> . Bit 0 for byte 0, 1 for byte 1, 2 for byte 2, 3 for byte 3

**SMIx00000038 (FCH::SMI::EPBIF\_AER\_STRAPS)**

Read-write. Reset: 07FE\_FFEh.

\_aliasHOSTLEGACY; SMIx00000038; SMI=FED8\_0200h

Bits	Description
31:28	Reserved.
27	<b>strap_bif_internal_err_en_sb.</b> Read-write. Reset: 0. Internal error enable.
26	<b>strap_bif_poisoned_advisory_nonfatal_a_sb.</b> Read-write. Reset: 1. Poisoned TLP as advisory nonfatal.
25	<b>strap_bif_acs_direct_translated_p2p_sb.</b> Read-write. Reset: 1. ACS direct translated P2P enable.
24	<b>strap_bif_acs_upstream_forwarding_sb.</b> Read-write. Reset: 1. ACS upstream forwarding enable.
23	<b>strap_bif_acs_p2p_completion_redirect_sb.</b> Read-write. Reset: 1. ACS P2P completion redirect enable.
22	<b>strap_bif_acs_p2p_request_redirect_sb.</b> Read-write. Reset: 1. ACS P2P request redirect enable.
21	<b>strap_bif_acs_translation_blocking_sb.</b> Read-write. Reset: 1. ACS translation blocking enable.
20	<b>strap_bif_acs_source_validation_sb.</b> Read-write. Reset: 1. ACS source validation enable.
19	<b>strap_bif_acs_en_sb.</b> Read-write. Reset: 1. ACS enable.
18	<b>strap_bif_first_rcvd_err_log_sb.</b> Read-write. Reset: 1. First received error log.
17	<b>strap_bif_ecrc_check_en_sb.</b> Read-write. Reset: 1. ECRC check enable.
16	<b>strap_bif_ecrc_gen_en_sb.</b> Read-write. Reset: 0. ECRC generate enable.
15	<b>strap_bif_cpl_abort_err_en_sb.</b> Read-write. Reset: 1. Completer abort error enable.
14	<b>strap_bif_rx_ignore_vend0_ur_sb.</b> Read-write. Reset: 1. Ignore Vendor 0 error.
13	<b>strap_bif_rx_ignore_tc_err_sb.</b> Read-write. Reset: 1. Ignore traffic class error.
12	<b>strap_bif_rx_ignore_msg_err_sb.</b> Read-write. Reset: 1. Ignore message error.
11	<b>strap_bif_rx_ignore_max_payload_err_sb.</b> Read-write. Reset: 1. Ignore maximum payload error.
10	<b>strap_bif_rx_ignore_len_mismatch_err_sb.</b> Read-write. Reset: 1. Ignore length mismatch error.
9	<b>strap_bif_rx_ignore_io_ur_err_sb.</b> Read-write. Reset: 1. Ignore IO UR error.
8	<b>strap_bif_rx_ignore_io_err_sb.</b> Read-write. Reset: 1. Ignore IO error.
7	<b>strap_bif_rx_ignore_ep_err_sb.</b> Read-write. Reset: 1. Ignore poisoned TLP error.
6	<b>strap_bif_rx_ignore_cpl_err_sb.</b> Read-write. Reset: 1. Ignore completion error.
5	<b>strap_bif_rx_ignore_cfg_ur_sb.</b> Read-write. Reset: 1. Ignore config. UR error.
4	<b>strap_bif_rx_ignore_cfg_err_sb.</b> Read-write. Reset: 1. Ignore configuration error.
3	<b>strap_bif_rx_ignore_be_err_sb.</b> Read-write. Reset: 1. Ignore byte enable error.
2	<b>strap_bif_err_reporting_dis_sb.</b> Read-write. Reset: 1. Error reporting disable.
1	<b>strap_bif_aer_en_sb.</b> Read-write. Reset: 1. AER enable.
0	<b>strap_bif_sticky_override_s5.</b> Read-write. Reset: 0. When set to 1, values in this register would override straps loaded from EEPROM.

**SMIx0000003C (FCH::SMI::DATAERRORSTATUS)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; SMIx0000003C; SMI=FED8\_0200h

Bits	Description
31:8	Reserved.
7	<b>sirq_iochk</b> . Read-write. Reset: 0. Serial Iochk error write 1 to clear it to 0
6	<b>sataperr</b> . Read-write. Reset: 0. SATA controller internal parity error status write 1 to clear it to 0.
5	<b>umi_uncorrectable_err</b> . Read-write. Reset: 0. <a href="#">UMI</a> uncorrectable error status write 1 to clear it to 0.
4	<b>umi_correctable_err</b> . Read-write. Reset: 0. <a href="#">UMI</a> correctable error status write 1 to clear it to 0.
3	<b>abumigppperr</b> . Read-write. Reset: 0. AB/ <a href="#">UMI</a> /GPP parity error status write 1 to clear it to 0.
2	<b>internalgppserr</b> . Read-write. Reset: 0. Internal error status: <a href="#">FCH</a> has detected an internal error from upstream bridge write 1 to clear it to 0.
1	<b>internalperr</b> . Read-write. Reset: 0. Internal devices Perr error status write 1 to clear it to 0.
0	<b>internalserr</b> . Read-write. Reset: 0. Internal devices serr error status write 1 to clear it to 0.

**SMIx00000040 (FCH::SMI::SCIMAP0)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; SMIx00000040; SMI=FED8\_0200h

Bits	Description
31:21	Reserved.
20:16	<b>scimap_2</b> . Read-write. Reset: 00h. <b>Description:</b> Mapping of AGPIO3 to one of 32 Event_Status. 00000: map event source 2 to the input of Event_Status bit 0 00001: map event source 2 to the input of Event_Status bit 1 11111: map event source 2 to the input of Event_Status bit 31
15:13	Reserved.
12:8	<b>scimap_1</b> . Read-write. Reset: 00h. <b>Description:</b> Mapping of GENINT2_L to one of 32 Event_Status. 00000: map event source 1 to the input of Event_Status bit 0 00001: map event source 1 to the input of Event_Status bit 1 11111: map event source 1 to the input of Event_Status bit 31
7:5	Reserved.
4:0	<b>scimap_0</b> . Read-write. Reset: 00h. <b>Description:</b> Mapping of GENINT1_L to one of 32 Event_Status. 00000: map event source 0 to the input of Event_Status bit 0 00001: map event source 0 to the input of Event_Status bit 1 11111: map input event0 to the input of Event_Status bit 31

**SMIx00000044 (FCH::SMI::SCIMAP1)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; SMIx000000044; SMI=FED8\_0200h

Bits	Description
31:29	Reserved.
28:24	<b>scimap_7.</b> Read-write. Reset: 00h.
	<b>Description:</b> Mapping of AGPIO5 to one of 32 Event_Status. 00000: map event source 7 to the input of Event_Status bit 0 00001: map event source 7 to the input of Event_Status bit 1 11111: map event source 7 to the input of Event_Status bit 31
23:21	Reserved.
20:16	<b>scimap_6.</b> Read-write. Reset: 00h.
	<b>Description:</b> Mapping of SPKR to one of 32 Event_Status. 00000: map event source 6 to the input of Event_Status bit 0 00001: map event source 6 to the input of Event_Status bit 1 11111: map event source 6 to the input of Event_Status bit 31
15:5	Reserved.
4:0	<b>scimap_4.</b> Read-write. Reset: 00h.
	<b>Description:</b> Mapping of AGPIO4 to one of 32 Event_Status. 00000: map event source 4 to the input of Event_Status bit 0 00001: map event source 4 to the input of Event_Status bit 1 11111: map event source 4 to the input of Event_Status bit 31

**SMIx00000048 (FCH::SMI::SCIMAP2)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; SMIx000000048; SMI=FED8\_0200h

Bits	Description
31:29	Reserved.
28:24	<b>scimap_11.</b> Read-write. Reset: 00h.
	<b>Description:</b> Mapping of AGPIO76 to one of 32 Event_Status. 00000: map event source 11 to the input of Event_Status bit 0 00001: map event source 11 to the input of Event_Status bit 1 11111: map event source 11 to the input of Event_Status bit 31
23:21	Reserved.
20:16	<b>scimap_10.</b> Read-write. Reset: 00h.
	<b>Description:</b> Mapping of AGPIO6 to one of 32 Event_Status. 00000: map event source 10 to the input of Event_Status bit 0 00001: map event source 10 to the input of Event_Status bit 1 11111: map event source 10 to the input of Event_Status bit 31
15:5	Reserved.
4:0	<b>scimap_8.</b> Read-write. Reset: 00h.
	<b>Description:</b> Mapping of WAKE_L to one of 32 Event_Status. 00000: map event source 8 to the input of Event_Status bit 0 00001: map event source 8 to the input of Event_Status bit 1 11111: map event source 8 to the input of Event_Status bit 31

**SMIx0000004C (FCH::SMI::SCIMAP3)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; SMIx0000004C; SMI=FED8\_0200h

Bits	Description
31:29	Reserved.
28:24	<b>scimap_15.</b> Read-write. Reset: 00h.
	<b>Description:</b> Mapping of USB_OC3_L to one of 32 Event_Status. 00000: map event source 15 to the input of Event_Status bit 0 00001: map event source 15 to the input of Event_Status bit 1 11111: map event source 15 to the input of Event_Status bit 31
23:21	Reserved.
20:16	<b>scimap_14.</b> Read-write. Reset: 00h.
	<b>Description:</b> Mapping of USB_OC2_L to one of 32 Event_Status. 00000: map event source 14 to the input of Event_Status bit 0 00001: map event source 14 to the input of Event_Status bit 1 11111: map event source 14 to the input of Event_Status bit 31
15:13	Reserved.
12:8	<b>scimap_13.</b> Read-write. Reset: 00h.
	<b>Description:</b> Mapping of USB_OC1_L to one of 32 Event_Status. 00000: map event source 13 to the input of Event_Status bit 0 00001: map event source 13 to the input of Event_Status bit 1 11111: map event source 13 to the input of Event_Status bit 31
7:5	Reserved.
4:0	<b>scimap_12.</b> Read-write. Reset: 00h.
	<b>Description:</b> Mapping of USB_OC0_L to one of 32 Event_Status. 00000: map event source 12 to the input of Event_Status bit 0 00001: map event source 12 to the input of Event_Status bit 1 11111: map event source 12 to the input of Event_Status bit 31

**SMIx00000050 (FCH::SMI::SCIMAP4)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; SMIx00000050; SMI=FED8\_0200h

Bits	Description
31:29	Reserved.
28:24	<b>scimap_19.</b> Read-write. Reset: 00h.
	<b>Description:</b> Mapping of SYS_RESET_L to one of 32 Event_Status. 00000: map event source 19 to the input of Event_Status bit 0 00001: map event source 19 to the input of Event_Status bit 1 11111: map event source 19 to the input of Event_Status bit 31
23:21	Reserved.
20:16	<b>scimap_18.</b> Read-write. Reset: 00h.
	<b>Description:</b> Mapping of FANIN0 to one of 32 Event_Status. 00000: map event source 18 to the input of Event_Status bit 0 00001: map event source 18 to the input of Event_Status bit 1 11111: map event source 18 to the input of Event_Status bit 31
15:13	Reserved.
12:8	<b>scimap_17.</b> Read-write. Reset: 00h.
	<b>Description:</b> Mapping of ESPI_RESET_L to one of 32 Event_Status. 00000: map event source 17 to the input of Event_Status bit 0 00001: map event source 17 to the input of Event_Status bit 1 11111: map event source 17 to the input of Event_Status bit 31
7:5	Reserved.
4:0	<b>scimap_16.</b> Read-write. Reset: 00h.
	<b>Description:</b> Mapping of AGPIO23 to one of 32 Event_Status. 00000: map event source 16 to the input of Event_Status bit 0 00001: map event source 16 to the input of Event_Status bit 1 11111: map event source 16 to the input of Event_Status bit 31

**SMIx00000054 (FCH::SMI::SCIMAP5)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; SMIx00000054; SMI=FED8\_0200h

Bits	Description
31:29	Reserved.
28:24	<b>scimap_23.</b> Read-write. Reset: 00h.
	<b>Description:</b> Mapping of AGPIO8 to one of 32 Event_Status. 00000: map event source 23 to the input of Event_Status bit 0 00001: map event source 23 to the input of Event_Status bit 1 11111: map event source 23 to the input of Event_Status bit 31
23:21	Reserved.
20:16	<b>scimap_22.</b> Read-write. Reset: 00h.
	<b>Description:</b> Mapping of AGPIO9 to one of 32 Event_Status. 00000: map event source 22 to the input of Event_Status bit 0 00001: map event source 22 to the input of Event_Status bit 1 11111: map event source 22 to the input of Event_Status bit 31
15:13	Reserved.
12:8	<b>scimap_21.</b> Read-write. Reset: 00h.
	<b>Description:</b> Mapping of PWR_BTN_L to one of 32 Event_Status. 00000: map event source 21 to the input of Event_Status bit 0 00001: map event source 21 to the input of Event_Status bit 1 11111: map event source 21 to the input of Event_Status bit 31
7:5	Reserved.
4:0	<b>scimap_20.</b> Read-write. Reset: 00h.
	<b>Description:</b> Mapping of AGPIO40 to one of 32 Event_Status. 00000: map event source 20 to the input of Event_Status bit 0 00001: map event source 20 to the input of Event_Status bit 1 11111: map event source 20 to the input of Event_Status bit 31

**SMIx00000058 (FCH::SMI::SCIMAP6)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; SMIx00000058; SMI=FED8\_0200h

Bits	Description
31:29	Reserved.
28:24	<b>scimap_27.</b> Read-write. Reset: 00h. <b>Description:</b> Mapping of eSPI_WAKE_PME (~eSPI_WAKE_PME_B, active high) to one of 32 Event_Status. 00000: map event source 27 to the input of Event_Status bit 0 00001: map event source 27 to the input of Event_Status bit 1 11111: map event source 27 to the input of Event_Status bit 31
23:21	Reserved.
20:16	<b>scimap_26.</b> Read-write. Reset: 00h. <b>Description:</b> Mapping of eSPI system event (~eSPI_SYS_EVT_B, Active high) to one of 32 Event_Status. 00000: map event source 26 to the input of Event_Status bit 0 00001: map event source 26 to the input of Event_Status bit 1 11111: map event source 26 to the input of Event_Status bit 31
15:13	Reserved.
12:8	<b>scimap_25.</b> Read-write. Reset: 00h. <b>Description:</b> Mapping of MP2 GPIO[0] to one of 32 Event_Status. 00000: map event source 25 to the input of Event_Status bit 0 00001: map event source 25 to the input of Event_Status bit 1 11111: map event source 25 to the input of Event_Status bit 31
7:5	Reserved.
4:0	<b>scimap_24.</b> Read-write. Reset: 00h. <b>Description:</b> Mapping of MP2 wakeup event to one of 32 Event_Status. 00000: map event source 24 to the input of Event_Status bit 0 00001: map event source 24 to the input of Event_Status bit 1 11111: map event source 24 to the input of Event_Status bit 31

**SMIx0000005C (FCH::SMI::SCIMAP7)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; SMIx0000005C; SMI=FED8\_0200h

Bits	Description
31:21	Reserved.
20:16	<b>scimap_30.</b> Read-write. Reset: 00h. <b>Description:</b> Mapping of NB GPP Hot Plug to one of 32 Event_Status. 00000: map event source 30 to the input of Event_Status bit 0 00001: map event source 30 to the input of Event_Status bit 1 11111: map event source 30 to the input of Event_Status bit 31
15:13	Reserved.
12:8	<b>scimap_29.</b> Read-write. Reset: 00h. <b>Description:</b> Mapping of NB GPP_PME to one of 32 Event_Status. 00000: map event source 29 to the input of Event_Status bit 0 00001: map event source 29 to the input of Event_Status bit 1 11111: map event source 29 to the input of Event_Status bit 31
7:5	Reserved.
4:0	<b>scimap_28.</b> Read-write. Reset: 00h. <b>Description:</b> Mapping of MP2 GPIO[1] to one of 32 Event_Status. 00000: map event source 28 to the input of Event_Status bit 0 00001: map event source 28 to the input of Event_Status bit 1 11111: map event source 28 to the input of Event_Status bit 31



**SMIx00000060 (FCH::SMI::SCIMAP8)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; SMIx00000060; SMI=FED8\_0200h

Bits	Description
31:29	Reserved.
28:24	<b>scimap_35.</b> Read-write. Reset: 00h.
	<b>Description:</b> Mapping of PM FakeSts2 to one of 32 Event_Status. 00000: map event source 35 to the input of Event_Status bit 0 00001: map event source 35 to the input of Event_Status bit 1 11111: map event source 35 to the input of Event_Status bit 31
23:21	Reserved.
20:16	<b>scimap_34.</b> Read-write. Reset: 00h.
	<b>Description:</b> Mapping of FakeSts1 to one of 32 Event_Status. 00000: map event source 34 to the input of Event_Status bit 0 00001: map event source 34 to the input of Event_Status bit 1 11111: map event source 34 to the input of Event_Status bit 31
15:13	Reserved.
12:8	<b>scimap_33.</b> Read-write. Reset: 00h.
	<b>Description:</b> Mapping of FakeSts0 to one of 32 Event_Status. 00000: map event source 33 to the input of Event_Status bit 0 00001: map event source 33 to the input of Event_Status bit 1 11111: map event source 33 to the input of Event_Status bit 31
7:5	Reserved.
4:0	<b>scimap_32.</b> Read-write. Reset: 00h.
	<b>Description:</b> Mapping of WAKE_L to one of 32 Event_Status. 00000: map event source 33 to the input of Event_Status bit 0 00001: map event source 33 to the input of Event_Status bit 1 11111: map event source 33 to the input of Event_Status bit 31

**SMIx00000064 (FCH::SMI::SCIMAP9)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; SMIx00000064; SMI=FED8\_0200h

Bits	Description
31:29	Reserved.
28:24	<b>scimap_39.</b> Read-write. Reset: 00h.
	<b>Description:</b> Mapping of Azalia PME to one of 32 Event_Status. 00000: map event source 39 to the input of Event_Status bit 0 00001: map event source 39 to the input of Event_Status bit 1 11111: map event source 39 to the input of Event_Status bit 31
23:21	Reserved.
20:16	<b>scimap_38.</b> Read-write. Reset: 00h.
	<b>Description:</b> Mapping of eSPI1_WAKE_PME (~eSPI1_WAKE_PME_B, active high) to one of 32 Event_Status. 00000: map event source 38 to the input of Event_Status bit 0 00001: map event source 38 to the input of Event_Status bit 1 11111: map event source 38 to the input of Event_Status bit 31
15:13	Reserved.
12:8	<b>scimap_37.</b> Read-write. Reset: 00h.
	<b>Description:</b> Mapping of eSPI1 system event (~eSPI1_SYS_EVT_B, Active high) to one of 32 Event_Status. 00000: map event source 37 to the input of Event_Status bit 0 00001: map event source 37 to the input of Event_Status bit 1 11111: map event source 37 to the input of Event_Status bit 31
7:5	Reserved.
4:0	<b>scimap_36.</b> Read-write. Reset: 00h.
	<b>Description:</b> Mapping of ESPI SCI (~eSPI_SCI_B, active high) to one of 32 Event_Status. 00000: map event source 36 to the input of Event_Status bit 0 00001: map event source 36 to the input of Event_Status bit 1 11111: map event source 36 to the input of Event_Status bit 31

**SMIx00000068 (FCH::SMI::SCIMAP10)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; SMIx00000068; SMI=FED8\_0200h

Bits	Description
31:29	Reserved.
28:24	<b>scimap_43.</b> Read-write. Reset: 00h.
	<b>Description:</b> Mapping of AltHPET timer event to one of 32 Event_Status. 00000: map event source 43 to the input of Event_Status bit 0 00001: map event source 43 to the input of Event_Status bit 1 11111: map event source 43 to the input of Event_Status bit 31
23:21	Reserved.
20:16	<b>scimap_42.</b> Read-write. Reset: 00h.
	<b>Description:</b> Mapping of ESPI1 SCI (~eSPI1_SCI_B, active high) to one of 32 Event_Status. 00000: map event source 42 to the input of Event_Status bit 0 00001: map event source 42 to the input of Event_Status bit 1 11111: map event source 42 to the input of Event_Status bit 31
15:13	Reserved.
12:8	<b>scimap_41.</b> Read-write. Reset: 00h.
	<b>Description:</b> Mapping of Gpio Interrupt to one of 32 Event_Status. 00000: map event source 41 to the input of Event_Status bit 0 00001: map event source 41 to the input of Event_Status bit 1 11111: map event source 41 to the input of Event_Status bit 31
7:5	Reserved.
4:0	<b>scimap_40.</b> Read-write. Reset: 00h.
	<b>Description:</b> Mapping of USB PD I2C4 INTR (~USB_PD_I2C4_intrB, active high) to one of 32 Event_Status. 00000: map event source 41 to the input of Event_Status bit 0 00001: map event source 41 to the input of Event_Status bit 1 11111: map event source 41 to the input of Event_Status bit 31

**SMIx0000006C (FCH::SMI::SCIMAP11)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; SMIx0000006C; SMI=FED8\_0200h

Bits	Description
31:29	Reserved.
28:24	<b>scimap_47.</b> Read-write. Reset: 00h.
	<b>Description:</b> Mapping of SMBUS0 Interrupt event to one of 32 Event_Status. 00000: map event source 47 to the input of Event_Status bit 0 00001: map event source 47 to the input of Event_Status bit 1 11111: map event source 47 to the input of Event_Status bit 31
23:21	Reserved.
20:16	<b>scimap_46.</b> Read-write. Reset: 00h.
	<b>Description:</b> Mapping of I2S wake event to one of 32 Event_Status. 00000: map event source 46 to the input of Event_Status bit 0 00001: map event source 46 to the input of Event_Status bit 1 11111: map event source 46 to the input of Event_Status bit 31
15:13	Reserved.
12:8	<b>scimap_45.</b> Read-write. Reset: 00h.
	<b>Description:</b> Mapping of ASF Master and Slave Interrupt event to one of 32 Event_Status. 00000: map event source 45 to the input of Event_Status bit 0 00001: map event source 45 to the input of Event_Status bit 1 11111: map event source 45 to the input of Event_Status bit 31
7:5	Reserved.
4:0	<b>scimap_44.</b> Read-write. Reset: 00h.
	<b>Description:</b> Mapping of internal FAN/THERMAL event to one of 32 Event_Status. 00000: map event source 44 to the input of Event_Status bit 0 00001: map event source 44 to the input of Event_Status bit 1 11111: map event source 44 to the input of Event_Status bit 31

**SMIx00000070 (FCH::SMI::SCIMAP12)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; SMIx00000070; SMI=FED8\_0200h

Bits	Description
31:29	Reserved.
28:24	<b>scimap_51.</b> Read-write. Reset: 00h.
	<b>Description:</b> Mapping of power button event to one of the 32 Event_Status bits. 00000: map event source 50 to the input of Event_Status bit 0 00001: map event source 50 to the input of Event_Status bit 1 11111: map event source 50 to the input of Event_Status bit 31
23:21	Reserved.
20:16	<b>scimap_50.</b> Read-write. Reset: 00h.
	<b>Description:</b> Mapping of LLB# to one of the 32 Event_Status bits. 00000: map event source 50 to the input of Event_Status bit 0 00001: map event source 50 to the input of Event_Status bit 1 11111: map event source 50 to the input of Event_Status bit 31
15:13	Reserved.
12:8	<b>scimap_49.</b> Read-write. Reset: 00h.
	<b>Description:</b> Mapping of internal traffic monitor to one of 32 Event_Status. 00000: map event source 49 to the input of Event_Status bit 0 00001: map event source 49 to the input of Event_Status bit 1 11111: map event source 49 to the input of Event_Status bit 31
7:5	Reserved.
4:0	<b>scimap_48.</b> Read-write. Reset: 00h.
	<b>Description:</b> Mapping of TWARN pin to one of 32 Event_Status. 00000: map event source 48 to the input of Event_Status bit 0 00001: map event source 48 to the input of Event_Status bit 1 11111: map event source 48 to the input of Event_Status bit 31

**SMIx00000074 (FCH::SMI::SCIMAP13)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; SMIx00000074; SMI=FED8\_0200h

Bits	Description
31:29	Reserved.
28:24	<b>scimap_55.</b> Read-write. Reset: 00h.
	<b>Description:</b> Mapping of RAS_event status to one of the 32 Event_Status bits. 00000: map event source 55 to the input of Event_Status bit 0 00001: map event source 55 to the input of Event_Status bit 1 11111: map event source 55 to the input of Event_Status bit 31
23:21	Reserved.
20:16	<b>scimap_54.</b> Read-write. Reset: 00h.
	<b>Description:</b> Mapping of "SCI assertion message from APU" to one of the 32 Event_Status bits. 00000: map event source 54 to the input of Event_Status bit 0 00001: map event source 54 to the input of Event_Status bit 1 11111: map event source 54 to the input of Event_Status bit 31
15:13	Reserved.
12:8	<b>scimap_53.</b> Read-write. Reset: 00h.
	<b>Description:</b> Mapping of "HW assertion message from APU" to one of the 32 Event_Status bits. 00000: map event source 53 to the input of Event_Status bit 0 00001: map event source 53 to the input of Event_Status bit 1 11111: map event source 53 to the input of Event_Status bit 31
7:5	Reserved.
4:0	<b>scimap_52.</b> Read-write. Reset: 00h.
	<b>Description:</b> Mapping of PROHOT# pin to one of the 32 Event_Status bits. 00000: map event source 52 to the input of Event_Status bit 0 00001: map event source 52 to the input of Event_Status bit 1 11111: map event source 52 to the input of Event_Status bit 31

**SMIx00000078 (FCH::SMI::SCIMAP14)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; SMIx00000078; SMI=FED8\_0200h

Bits	Description
31:21	Reserved.
20:16	<b>scimap_58.</b> Read-write. Reset: 00h.
	<b>Description:</b> Mapping of AC/DC timer event to one of the 32 Event_Status bits. 00000: map event source 57 to the input of Event_Status bit 0 00001: map event source 57 to the input of Event_Status bit 1 11111: map event source 57 to the input of Event_Status bit 31
15:13	Reserved.
12:8	<b>scimap_57.</b> Read-write. Reset: 00h.
	<b>Description:</b> Mapping of XHC-1 PME event to one of the 32 Event_Status bits. 00000: map event source 57 to the input of Event_Status bit 0 00001: map event source 57 to the input of Event_Status bit 1 11111: map event source 57 to the input of Event_Status bit 31
7:5	Reserved.
4:0	<b>scimap_56.</b> Read-write. Reset: 00h.
	<b>Description:</b> Mapping of XHC-0 PME event to one of the 32 Event_Status bits. 00000: map event source 56to the input of Event_Status bit 0 00001: map event source 56to the input of Event_Status bit 1 11111: map event source 56 to the input of Event_Status bit 31

**SMIx00000080 (FCH::SMI::SMISTATUS0)**

Read, Write-1-to-clear. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; SMIx00000080; SMI=FED8\_0200h

Bits	Description
31	Reserved.
30	<b>nbgpphp_event30</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of NB Hot Plug event
29	<b>nbgpppme_event29</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of NB GPP PME
28	<b>smi_event28</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of MP2 GPIO[1]
27	<b>espi_wake_pme_event27</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of ESPI WAKE/PME event
26	<b>smi_event26</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of ~eSPI_SYS_EVT_B
25	<b>smi_event25</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of MP2 GPIO[0]
24	<b>smi_event24</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of MP2 wakeup event
23	<b>gevent23status_event23</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of AGPIO106
22	<b>gevent22status_event22</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of AGPIO105
21	<b>gevent21status_event21</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of PWR_BTN_L
20	<b>gevent20status_event20</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of AGPIO104
19	<b>gevent19status_event19</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of SYS_RESET_L
18	<b>gevent18status_event18</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of X48M_OUT
17	<b>gevent17status_event17</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of ESPI_RSTIN_L
16	<b>gevent16status_event16</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of ESPI_RSTOUT_L
15	<b>gevent15status_event15</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of PCIE_RST1_L
14	<b>gevent14status_event14</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of SMERR_L
13	<b>gevent13status_event13</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of USB_OC1_L
12	<b>gevent12status_event12</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of USB_OC0_L
11	<b>gevent11status_event11</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of AGPIO76
10	<b>gevent10status_event10</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of AGPIO6
9	<b>gevent9status_event9</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of NMI_SYNC_FLOOD
8	<b>gevent8status_event8</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of WAKE_L
7	<b>gevent7status_event7</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of AGPIO5
6	<b>gevent6status_event6</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of AGPIO116
5	<b>gevent5status_event5</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of AGPIO21
4	<b>gevent4status_event4</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of AGPIO4
3	<b>gevent3status_event3</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of AGPIO22
2	<b>gevent2status_event2</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of AGPIO3
1	<b>gevent1status_event1</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of AGPIO115
0	<b>gevent0status_event0</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of GENINT1_L

**SMIx00000084 (FCH::SMI::SMISTATUS1)**

Read, Write-1-to-clear. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; SMIx00000084; SMI=FED8\_0200h

Bits	Description
31:27	Reserved.
26	<b>acdctimerevent_event58.</b> Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of AcDcTimer wake up event (Wake Alarm Device)
25	<b>xhc1pme_event57.</b> Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of XHC1 PME
24	<b>xhc0pme_event56.</b> Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of XHC0 PME
23	<b>ras_event55.</b> Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Internal devices SERR error status
22	<b>apusciasrtion_event54.</b> Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of APU SCI request
21	<b>apuhwassrtion_event53.</b> Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of APU Hw assertion
20	<b>prochot_event52.</b> Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of Prochot event
19	<b>pwrbutton_event51.</b> Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of PwrButton (rising edge) writing 1 to clear it to 0.
18	<b>illb_event50.</b> Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of iLLB# assertion
17	<b>trafficmonitorintr_event49.</b> Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of <a href="#">FCH</a> Traffic Monitor Interrupt
16	<b>twarn_event48.</b> Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of <a href="#">FCH</a> TWARN
15	<b>smbus0_event47.</b> Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of <a href="#">FCH</a> SMBUS0 Master interrupt
14	<b>i2swake_event46.</b> Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of I2S wake event
13	<b>asfrintr_event45.</b> Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of <a href="#">FCH</a> ASF Master and Slave interrupt
12	<b>fanthermalgevent_event44.</b> Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of <a href="#">FCH</a> FanThermal
11	<b>altmmtimersts_event43.</b> Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of AltMmTimer Alarm
10	<b>smi_event42.</b> Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of ~eSPI1_SCI_B
9	<b>gpointr_event41.</b> Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of GPIO interrupt
8	<b>smi_event40.</b> Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of ~USB_PD_I2C4_intrB
7	<b>azpme_event39.</b> Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of Azaila wake event
6	<b>espi1_wake_pme_event38.</b> Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of ESPI1 WAKE/PME event
5	<b>smi_event37.</b> Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of ~eSPI1_SYS_EVT_B
4	<b>smi_event36.</b> Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of ~eSPI_SCI_B
3	<b>fakests2_event35.</b> Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of Fake2
2	<b>fakests1_event34.</b> Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of Fake1
1	<b>fakests0_event33.</b> Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of Fake0
0	<b>smi_event32.</b> Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of WAKE_L



**SMIx00000088 (FCH::SMI::SMISTATUS2)**

Read,Write-1-to-clear. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; SMIx00000088; SMI=FED8\_0200h

Bits	Description
31:27	Reserved.
26	<b>emulate64_event90</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of Emulation Io Port 60/64h
25:21	Reserved.
20	<b>pciserr_event84</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of Serr assertion on Pci bus
19	<b>prothot_event83</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of ProtHot event
18	<b>vbatlow_event82</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of VBAT low
17	<b>sim_event81</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of Intruder Alert Status
16:15	Reserved.
14	<b>smbus0intr_event78</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of SMBUS0 interrupt request
13	<b>serialirqsmi_event77</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of Smi request from Serial IRQ
12	<b>usbsmi_event76</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of Usb Smi request
11	<b>smicmdport_event75</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of Writing Smi Command Port
10	<b>pwrbtn_event74</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of Power Button being pressed
9	<b>bios_rls_event73</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of BIOS_RLS
8	<b>gbl_rls_event72</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of GBL event
7:3	Reserved.
2	<b>ial2h_acpi_assertion_event66</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of iAL2H_ACPI_Assertion
1	<b>slp_type_event65</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status is set when ACPI SLP_TYP register bit 2 is programmed
0	<b>smi_event64</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of KBRst

**SMIx00000090 (FCH::SMI::SMISTATUS4)**

Read,Write-1-to-clear. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; SMIx00000090; SMI=FED8\_0200h

Bits	Description
31:29	Reserved.
28	<b>cfgtrapping0_event156</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of Pci configuration cycle Trapping0 Smi request
27:25	Reserved.
24	<b>memtrapping0_event152</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of memory Trapping0 Smi request
23	<b>iotrapping3_event151</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of Io Trapping3 Smi request
22	<b>iotrapping2_event150</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of Io Trapping2 Smi request
21	<b>iotrapping1_event149</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of Io Trapping1 Smi request
20	<b>iotrapping0_event148</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of Io Trapping0 Smi request
19	<b>espi1_smi_event147</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of eSPI1 <a href="#">SMI</a> event
18	<b>espi_smi_event146</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of eSPI <a href="#">SMI</a> event
17	Reserved.
16	<b>absmitrap_event144</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of AB Smi trapping request
15	<b>longtimer_event143</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of Long Timer Smi request
14	<b>shorttimer_event142</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of Short Timer Smi request
13	<b>cf9write_event141</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 1: Cf9 bit 2 has been written to 1. 0: Cf9 bit 2 is not written to 1.
12:6	Reserved.
5	<b>fanin0sts_event133</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Status of FanIn0 event
4:0	Reserved.

**SMIx00000094 (FCH::SMI::SMIPointer)**

Read-only.

This register is meant as a faster mechanism to locate the [SMI](#) source. BIOS can examine this register to find out the SMI source instead of reading SmiStatus0 through SmiStatus4 individually

\_aliasHOSTLEGACY; SMIx00000094; SMI=FED8\_0200h

Bits	Description
15:6	Reserved.
5	<b>smistatussource4.</b> Read-only. Reset: 0. Indicate whether the <a href="#">SMI</a> source is from SmiStatus4[31:0] if the corresponding SMI enable is selected.
4	<b>smistatussource3.</b> Read-only. Reset: 0. Indicate whether the <a href="#">SMI</a> source is from SmiStatus3[31:0] if the corresponding SMI enable is selected.
3	<b>smistatussource2.</b> Read-only. Reset: 0. Indicates whether the <a href="#">SMI</a> source is from SmiStatus2[31:0] if the corresponding SMI enable is selected.
2	<b>smistatussource1.</b> Read-only. Reset: 0. Indicates whether the <a href="#">SMI</a> source is from SmiStatus1[31:0] if the corresponding SMI enable is selected.
1	<b>smistatussource0.</b> Read-only. Reset: 0. Indicates whether the <a href="#">SMI</a> source is from SmiStatus0[31:0] if the corresponding SMI enable is selected.
0	<b>smiscisource.</b> Read-only. Reset: 0. Indicates whether the <a href="#">SMI</a> source is from SMISCI.

**SMIx00000096 (FCH::SMI::SMI\_SHORT\_LONG\_TIMER)**

Read-write. Reset: 0000h.

\*Note: This register 96h can be either "SmiShortTimer" or "SmiLongTimer," depending on the select bit "SmiTimerSel" in SMI\_Reg 98[29]. The default setting (SmiTimerSel=0) selects this register as "SmiShortTimer" software needs to set the "SmiTimerSel=1" to select this register as "SmiLongTimer".

\_aliasHOSTLEGACY; SMIx00000096; SMI=FED8\_0200h

Bits	Description
15	<b>timeren.</b> Read-write. Reset: 0. <b>Description:</b> Enable the <a href="#">SMI</a> short Timer or long timer, which is selected by SmiTimerEn (PMIO_98[29]). 0 = Disable 1 = Enable
14:0	<b>smitimercount.</b> Read-write. Reset: 0000h. <b>Description:</b> Actual timer duration = (TimerTime + 1) * 2us (Short Timer) Actual timer duration = (TimerTime + 1) * 1ms (Long Timer)

**SMIx00000098 (FCH::SMI::SMITRIG0)**

Read-write. Reset: 8FFF\_FFFFh.

\_aliasHOSTLEGACY; SMIx00000098; SMI=FED8\_0200h

Bits	Description
31	<b>smienb.</b> Read-write. Reset: 1. <b>Description:</b> Enable <a href="#">SMI</a> function. 0: Enable 1: Disable
30	Reserved.
29	<b>smitimersel.</b> Read-write. Reset: 0. <b>Description:</b> 0: Selects the SMI_Reg 96h to be SMIShortTimer register. 1: Selects the SMI_Reg 96h to be SMILongTimer register.
28	<b>eos.</b> Read-write. Reset: 0. This bit is set to 1 by SW to enable <a href="#">SMI</a> generation. It is cleared by hardware after a SMI event has occurred. When Eos is clear, subsequent pending SMI event will be blocked.
27	<b>fakests2.</b> Read-write. Reset: 1. Program the value to emulate an <a href="#">SMI</a> input event.
26	<b>fakests1.</b> Read-write. Reset: 1. Program the value to emulate an <a href="#">SMI</a> input event.
25	<b>fakests0.</b> Read-write. Reset: 1. Program the value to emulate an <a href="#">SMI</a> input event.
24	<b>trappingirqonpic.</b> Read-write. Reset: 1. <b>Description:</b> <a href="#">SMI</a> will be generated when 0: Trapping Irq0 ~ 15 of IoAPIC 1: Trapping Irq0 ~ 15 of PIC
23	<b>smitrig23.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
22	<b>smitrig22.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
21	<b>smitrig21.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
20	<b>smitrig20.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
19	<b>smitrig19.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
18	<b>smitrig18.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
17	<b>smitrig17.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
16	<b>smitrig16.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
15	<b>smitrig15.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
14	<b>smitrig14.</b> Read-write. Reset: 1.

	<b>Description:</b> 1: Active high 0: Active low
13	<b>smitrig13.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
12	<b>smitrig12.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
11	<b>smitrig11.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
10	<b>smitrig10.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
9	<b>smitrig9.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
8	<b>smitrig8.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
7	<b>smitrig7.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
6	<b>smitrig6.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
5	<b>smitrig5.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
4	<b>smitrig4.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
3	<b>smitrig3.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
2	<b>smitrig2.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
1	<b>smitrig1.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
0	<b>smitrig0.</b> Read-write. Reset: 1. <b>Description:</b> This defines the trigger mode for SmiStatus0[23:0]. Note these are different from SciTrig 0: Active low 1: Active high

**SMIx0000009C (FCH::SMI::SMITRIG1)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; SMIx0000009C; SMI=FED8\_0200h

Bits	Description
31	<b>smiirq31trig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Active low 1: Active high
30	<b>smiirq30trig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Active low 1: Active high
29	<b>smiirq29trig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Active low 1: Active high
28	<b>smiirq28trig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Active low 1: Active high
27	<b>smiirq27trig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Active low 1: Active high
26	<b>smiirq26trig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Active low 1: Active high
25	<b>smiirq25trig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Active low 1: Active high
24	<b>smiirq24trig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Active low 1: Active high
23	<b>smiirq23trig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Active low 1: Active high
22	<b>smiirq22trig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Active low 1: Active high
21	<b>smiirq21trig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Active low 1: Active high
20	<b>smiirq20trig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Active low 1: Active high
19	<b>smiirq19trig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Active low 1: Active high
18	<b>smiirq18trig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Active low 1: Active high
17	<b>smiirq17trig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Active low 1: Active high
16	<b>smiirq16trig.</b> Read-write. Reset: 0.

	<b>Description:</b> 0: Active low 1: Active high
15	<b>smiirq15trig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Active low 1: Active high
14	<b>smiirq14trig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Active low 1: Active high
13	<b>smiirq13trig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Active low 1: Active high
12	<b>smiirq12trig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Active low 1: Active high
11	<b>smiirq11trig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Active low 1: Active high
10	<b>smiirq10trig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Active low 1: Active high
9	<b>smiirq9trig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Active low 1: Active high
8	<b>smiirq8trig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Active low 1: Active high
7	<b>smiirq7trig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Active low 1: Active high
6	<b>smiirq6trig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Active low 1: Active high
5	<b>smiirq5trig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Active low 1: Active high
4	<b>smiirq4trig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Active low 1: Active high
3	<b>smiirq3trig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Active low 1: Active high
2	<b>smiirq2trig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Active low 1: Active high
1	<b>smiirq1trig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Active low 1: Active high
0	<b>smiirq0trig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Active low 1: Active high

**SMIx000000A0 (FCH::SMI::SMICONTROL0)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; SMIx000000A0; SMI=FED8\_0200h

Bits	Description
31:30	<b>smicontrol_15.</b> Read-write. Reset: 0h. <b>Description:</b> Control for GEVENT15 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
29:28	<b>smicontrol_14.</b> Read-write. Reset: 0h. <b>Description:</b> Control for GEVENT14 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
27:26	<b>smicontrol_13.</b> Read-write. Reset: 0h. <b>Description:</b> Control for GEVENT13 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
25:24	<b>smicontrol_12.</b> Read-write. Reset: 0h. <b>Description:</b> Control for GEVENT12 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
23:22	<b>smicontrol_11.</b> Read-write. Reset: 0h. <b>Description:</b> Control for GEVENT11 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
21:20	<b>smicontrol_10.</b> Read-write. Reset: 0h. <b>Description:</b> Control for GEVENT10 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
19:18	<b>smicontrol_9.</b> Read-write. Reset: 0h. <b>Description:</b> Control for GEVENT9 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
17:16	<b>smicontrol_8.</b> Read-write. Reset: 0h.

	<b>Description:</b> Control for GEVENT8 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
15:14	<b>smicontrol_7.</b> Read-write. Reset: 0h. <b>Description:</b> Control for GEVENT7 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
13:12	<b>smicontrol_6.</b> Read-write. Reset: 0h. <b>Description:</b> Control for GEVENT6 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
11:10	<b>smicontrol_5.</b> Read-write. Reset: 0h. <b>Description:</b> Control for GEVENT5 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
9:8	<b>smicontrol_4.</b> Read-write. Reset: 0h. <b>Description:</b> Control for GEVENT4 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
7:6	<b>smicontrol_3.</b> Read-write. Reset: 0h. <b>Description:</b> Control for GEVENT3 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
5:4	<b>smicontrol_2.</b> Read-write. Reset: 0h. <b>Description:</b> Control for GEVENT2 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
3:2	<b>smicontrol_1.</b> Read-write. Reset: 0h. <b>Description:</b> Control for GEVENT1 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
1:0	<b>smicontrol_0.</b> Read-write. Reset: 0h.



	<div><div><b>Description:</b> Control for GEVENT0</div><div>00: Disable</div><div>01: <a href="#">SMI</a></div><div>10: NMI</div><div>11: IRQ13</div></div>
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**SMIx000000A4 (FCH::SMI::SMICONTROL1)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; SMIx000000A4; SMI=FED8\_0200h

Bits	Description
31:30	<b>smicontrol_31.</b> Read-write. Reset: 0h. <b>Description:</b> Control for GPP_PME (device 21, function3) 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
29:28	<b>smicontrol_30.</b> Read-write. Reset: 0h. <b>Description:</b> Control for GPP_PME (device 21, function2) 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
27:26	<b>smicontrol_29.</b> Read-write. Reset: 0h. <b>Description:</b> Control for GPP_PME (device 21, function1) 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
25:24	<b>smicontrol_28.</b> Read-write. Reset: 0h. <b>Description:</b> Control for GPP_PME (device 21, function0~3) 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
23:22	<b>smicontrol_27.</b> Read-write. Reset: 0h. <b>Description:</b> Control for eSPI_WAKE_PME_B 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
21:20	<b>smicontrol_26.</b> Read-write. Reset: 0h. <b>Description:</b> Control for eSPI_SYS_EVT_B 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
19:18	Reserved.
17:16	<b>smicontrol_24.</b> Read-write. Reset: 0h. <b>Description:</b> Control for USB_PME (device 18) 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
15:14	<b>smicontrol_23.</b> Read-write. Reset: 0h.

	<b>Description:</b> Control for GEVENT23 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
13:12	<b>smicontrol_22.</b> Read-write. Reset: 0h. <b>Description:</b> Control for GEVENT22 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
11:10	<b>smicontrol_21.</b> Read-write. Reset: 0h. <b>Description:</b> Control for GEVENT21 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
9:8	<b>smicontrol_20.</b> Read-write. Reset: 0h. <b>Description:</b> Control for GEVENT20 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
7:6	<b>smicontrol_19.</b> Read-write. Reset: 0h. <b>Description:</b> Control for GEVENT19 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
5:4	<b>smicontrol_18.</b> Read-write. Reset: 0h. <b>Description:</b> Control for GEVENT18 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
3:2	<b>smicontrol_17.</b> Read-write. Reset: 0h. <b>Description:</b> Control for GEVENT17 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
1:0	<b>smicontrol_16.</b> Read-write. Reset: 0h. <b>Description:</b> Control for GEVENT16 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13

**SMIx000000A8 (FCH::SMI::SMICONTROL2)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; SMIx000000A8; SMI=FED8\_0200h

Bits	Description
31:30	<b>smicontrol_47.</b> Read-write. Reset: 0h. <b>Description:</b> Control for SMBUS0 interrupt 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
29:28	<b>smicontrol_46.</b> Read-write. Reset: 0h. <b>Description:</b> Control for ASF Slave interrupt 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
27:26	<b>smicontrol_45.</b> Read-write. Reset: 0h. <b>Description:</b> Control for ASF Master interrupt 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
25:24	<b>smicontrol_44.</b> Read-write. Reset: 0h. <b>Description:</b> Control for FanThermal Gevent 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
23:22	<b>smicontrol_43.</b> Read-write. Reset: 0h. <b>Description:</b> Control for ALTHPET_TimerSts 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
21:20	<b>smicontrol_42.</b> Read-write. Reset: 0h. <b>Description:</b> Control for eSPI1_SCI_B 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
19:18	<b>smicontrol_41.</b> Read-write. Reset: 0h. <b>Description:</b> Control for GPIO interrupt 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
17:16	<b>smicontrol_40.</b> Read-write. Reset: 0h.

	<b>Description:</b> Control for Ec Gevent0 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
15:14	Reserved.
13:12	<b>smicontrol_38.</b> Read-write. Reset: 0h. <b>Description:</b> Control for eSPI1_WAKE_PME_B 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
11:10	<b>smicontrol_37.</b> Read-write. Reset: 0h. <b>Description:</b> Control for eSPI1_SYS_EVT_B 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
9:8	<b>smicontrol_36.</b> Read-write. Reset: 0h. <b>Description:</b> Control for eSPI_SCI_B 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
7:6	<b>smicontrol_35.</b> Read-write. Reset: 0h. <b>Description:</b> Control for FakeSts2 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
5:4	<b>smicontrol_34.</b> Read-write. Reset: 0h. <b>Description:</b> Control for FakeSts1 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
3:2	<b>smicontrol_33.</b> Read-write. Reset: 0h. <b>Description:</b> Control for FakeSts0 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
1:0	<b>smicontrol_32.</b> Read-write. Reset: 0h. <b>Description:</b> Control for GPP_HotPlug (device 21, function 0~3) 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13

**SMIx000000AC (FCH::SMI::SMICONTROL3)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; SMIx000000AC; SMI=FED8\_0200h

Bits	Description
31:30	<b>smicontrol_63.</b> Read-write. Reset: 0h. <b>Description:</b> Control for TempTsi event 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
29:28	<b>smicontrol_62.</b> Read-write. Reset: 0h. <b>Description:</b> Control for DSM Cross Trigger event 3 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
27:26	<b>smicontrol_61.</b> Read-write. Reset: 0h. <b>Description:</b> Control for DSM Cross Trigger event 2 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
25:24	<b>smicontrol_60.</b> Read-write. Reset: 0h. <b>Description:</b> Control for DSM Cross Trigger event 1 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
23:22	<b>smicontrol_59.</b> Read-write. Reset: 0h. <b>Description:</b> Control for DSM Cross Trigger event 0 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
21:20	<b>smicontrol_58.</b> Read-write. Reset: 0h. <b>Description:</b> Control for AcDcTimer wake up event (Wake Device in ACPI4.0) 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
19:18	<b>smicontrol_57.</b> Read-write. Reset: 0h. <b>Description:</b> Control for XHC1 (dev 16, func 1) PME 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
17:16	<b>smicontrol_56.</b> Read-write. Reset: 0h.

	<b>Description:</b> Control for XHC0 (dev 16, func 0) PME 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
15:14	<b>smicontrol_55.</b> Read-write. Reset: 0h. <b>Description:</b> Control for Internal devices SERR error status 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
13:12	<b>smicontrol_54.</b> Read-write. Reset: 0h. <b>Description:</b> Control for APU SCI request 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
11:10	<b>smicontrol_53.</b> Read-write. Reset: 0h. <b>Description:</b> Control for APU Hw assertion 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
9:8	<b>smicontrol_52.</b> Read-write. Reset: 0h. <b>Description:</b> Control for Prochot event 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
7:6	<b>smicontrol_51.</b> Read-write. Reset: 0h. <b>Description:</b> Control for Power button event 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
5:4	<b>smicontrol_50.</b> Read-write. Reset: 0h. <b>Description:</b> Control for iLLB# 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
3:2	<b>smicontrol_49.</b> Read-write. Reset: 0h. <b>Description:</b> Control for internal Traffic monitor interrupt 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
1:0	<b>smicontrol_48.</b> Read-write. Reset: 0h.

	<b>Description:</b> Control for TWARN# 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
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**SMIx000000B0 (FCH::SMI::SMICONTROL4)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; SMIx000000B0; SMI=FED8\_0200h

Bits	Description
31:30	<b>smicontrol_79.</b> Read-write. Reset: 0h. <b>Description:</b> Control for Ec Smi request0 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
29:28	<b>smicontrol_78.</b> Read-write. Reset: 0h. <b>Description:</b> Control for SMBUS0 interrupt 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
27:26	<b>smicontrol_77.</b> Read-write. Reset: 0h. <b>Description:</b> Control for Smi request form serial Irq 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
25:24	<b>smicontrol_76.</b> Read-write. Reset: 0h. <b>Description:</b> Control for Usb Smi request 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
23:22	<b>smicontrol_75.</b> Read-write. Reset: 0h. <b>Description:</b> Control for writing Smi command port 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
21:20	<b>smicontrol_74.</b> Read-write. Reset: 0h. <b>Description:</b> Control for power button being pressed 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
19:18	<b>smicontrol_73.</b> Read-write. Reset: 0h. <b>Description:</b> Control for writing BIOS_RLS 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
17:16	<b>smicontrol_72.</b> Read-write. Reset: 0h.

	<b>Description:</b> Control for writing GBL_RLS 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
15:8	Reserved.
7:6	<b>smicontrol_67.</b> Read-write. Reset: 0h. <b>Description:</b> Control for Sata AHCI event 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
5:4	<b>smicontrol_66.</b> Read-write. Reset: 0h. <b>Description:</b> Control for iAL2H_ACPI_Assertion 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
3:2	<b>smicontrol_65.</b> Read-write. Reset: 0h. <b>Description:</b> Control for writing SLP_TYP to put the system in S state. 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
1:0	<b>smicontrol_64.</b> Read-write. Reset: 0h. <b>Description:</b> Control for Keyboard Reset event. 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13

**SMIx000000B4 (FCH::SMI::SMICONTROL5)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; SMIx000000B4; SMI=FED8\_0200h

Bits	Description
31:28	Reserved.
27:26	<b>smicontrol_93.</b> Read-write. Reset: 0h. <b>Description:</b> Control for HD audio FLR 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
25:24	<b>smicontrol_92.</b> Read-write. Reset: 0h. <b>Description:</b> Control for Sata FLR 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
23:22	<b>smicontrol_91.</b> Read-write. Reset: 0h. <b>Description:</b> Control for Usb FLR 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
21:20	<b>smicontrol_90.</b> Read-write. Reset: 0h. <b>Description:</b> Control for Emulation64 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
19:18	<b>smicontrol_89.</b> Read-write. Reset: 0h. <b>Description:</b> Control for ThermalTrip# assertion 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
17:12	Reserved.
11:10	<b>smicontrol_85.</b> Read-write. Reset: 0h. <b>Description:</b> Control for SB GPP Serr#(device 21, function 0~3) 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
9:8	<b>smicontrol_84.</b> Read-write. Reset: 0h. <b>Description:</b> Control for SERR# 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
7:6	<b>smicontrol_83.</b> Read-write. Reset: 0h.

	<b>Description:</b> Control for ProcHot 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
5:4	<b>smicontrol_82.</b> Read-write. Reset: 0h. <b>Description:</b> Control for VBAT low 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
3:2	<b>smicontrol_81.</b> Read-write. Reset: 0h. <b>Description:</b> Control for Intruder event. 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
1:0	<b>smicontrol_80.</b> Read-write. Reset: 0h. <b>Description:</b> Control for Ec Smi request1 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13

#### SMIx000000B8 (FCH::SMI::SMICONTROL6)

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; SMIx000000B8; SMI=FED8\_0200h

Bits	Description
31:0	Reserved.

#### SMIx000000BC (FCH::SMI::SMICONTROL7)

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; SMIx000000BC; SMI=FED8\_0200h

Bits	Description
31:0	Reserved.

**SMIx000000C0 (FCH::SMI::SMICONTROL8)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; SMIx000000C0; SMI=FED8\_0200h

Bits	Description
31:30	<b>smicontrol_143.</b> Read-write. Reset: 0h. <b>Description:</b> Control for Long timer 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
29:28	<b>smicontrol_142.</b> Read-write. Reset: 0h. <b>Description:</b> Control for Short timer 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
27:26	<b>smicontrol_141.</b> Read-write. Reset: 0h. <b>Description:</b> Control for Cf9 Io write 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
25:24	<b>smicontrol_140.</b> Read-write. Reset: 0h. <b>Description:</b> Control for FakeSts2 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13 Note: FakeSts2 defined in PMIO can be programmed to generate SMI/NMI/IRQ13 specified in those two bits.
23:22	<b>smicontrol_139.</b> Read-write. Reset: 0h. <b>Description:</b> Control for FakeSts1 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13 Note: FakeSts1 defined in PMIO can be programmed to generate SMI/NMI/IRQ13 specified in those two bits.
21:20	<b>smicontrol_138.</b> Read-write. Reset: 0h. <b>Description:</b> Control for FakeSts0 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13 Note: FakeSts0 defined in PMIO can be programmed to generate SMI/NMI/IRQ13 specified in those two bits.
19:12	Reserved.
11:10	<b>smicontrol_133.</b> Read-write. Reset: 0h. <b>Description:</b> Control for Fan Tach 0 too slow event 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
9:0	Reserved.

**SMIx000000C4 (FCH::SMI::SMICONTROL9)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; SMIx000000C4; SMI=FED8\_0200h

Bits	Description
31:26	Reserved.
25:24	<b>smicontrol_156.</b> Read-write. Reset: 0h. <b>Description:</b> Control for configuration cycle trapping 0 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
23:18	Reserved.
17:16	<b>smicontrol_152.</b> Read-write. Reset: 0h. <b>Description:</b> Control for memory trapping 0 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
15:14	<b>smicontrol_151.</b> Read-write. Reset: 0h. <b>Description:</b> Control for Io trapping 3 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
13:12	<b>smicontrol_150.</b> Read-write. Reset: 0h. <b>Description:</b> Control for Io trapping 2 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
11:10	<b>smicontrol_149.</b> Read-write. Reset: 0h. <b>Description:</b> Control for Io trapping 1 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
9:8	<b>smicontrol_148.</b> Read-write. Reset: 0h. <b>Description:</b> Control for Io trapping 0 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
7:6	<b>smicontrol_147.</b> Read-write. Reset: 0h. <b>Description:</b> Control for eSPI1_SMI_B 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
5:4	<b>smicontrol_146.</b> Read-write. Reset: 0h.

	<b>Description:</b> Control for eSPI_SMI_B 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
3:2	<b>smicontrol_145.</b> Read-write. Reset: 0h. <b>Description:</b> Control for P state message 0 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13
1:0	<b>smicontrol_144.</b> Read-write. Reset: 0h. <b>Description:</b> Control for AB Smi trapping request 00: Disable 01: <a href="#">SMI</a> 10: NMI 11: IRQ13

**SMIx000000C8 (FCH::SMI::SMILEVEL0)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; SMIx000000C8; SMI=FED8\_0200h

Bits	Description
31	<b>smilevel31.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
30	<b>smilevel30.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
29	<b>smilevel29.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
28	<b>smilevel28.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
27	<b>smilevel27.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
26	<b>smilevel26.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
25	<b>smilevel25.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
24	<b>smilevel24.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
23	<b>smilevel23.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
22	<b>smilevel22.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
21	<b>smilevel21.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
20	<b>smilevel20.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
19	<b>smilevel19.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
18	<b>smilevel18.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
17	<b>smilevel17.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
16	<b>smilevel16.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
15	<b>smilevel15.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
14	<b>smilevel14.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
13	<b>smilevel13.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
12	<b>smilevel12.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
11	<b>smilevel11.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
10	<b>smilevel10.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
9	<b>smilevel9.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
8	<b>smilevel8.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
7	<b>smilevel7.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
6	<b>smilevel6.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
5	<b>smilevel5.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
4	<b>smilevel4.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
3	<b>smilevel3.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
2	<b>smilevel2.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
1	<b>smilevel1.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
0	<b>smilevel0.</b> Read-write. Reset: 0. <b>Description:</b> This defines the edge/level trigger mode for SmiLevel[31:0]. Note these are different from SciLevl 0: Edge trigger mode, 1: Level trigger mode



**SMIx000000CC (FCH::SMI::SMILEVELTRIG0)**

Read-write. Reset: FFFF\_FFFFh.

\_aliasHOSTLEGACY; SMIx000000CC; SMI=FED8\_0200h

Bits	Description
31	<b>smitrig31.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
30	<b>smitrig30.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
29	<b>smitrig29.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
28	<b>smitrig28.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
27	<b>smitrig27.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
26	<b>smitrig26.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
25	<b>smitrig25.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
24	<b>smitrig24.</b> Read-write. Reset: 1. <b>Description:</b> This defines the trigger mode for SmiTrig[31:24]. 1: Active high 0: Active low
23:0	Reserved.

**SMIx000000D0 (FCH::SMI::SMILEVEL1)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; SMIx000000D0; SMI=FED8\_0200h

Bits	Description
31	<b>smilevel63.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
30	<b>smilevel62.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
29	<b>smilevel61.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
28	<b>smilevel60.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
27	<b>smilevel59.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
26	<b>smilevel58.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
25	<b>smilevel57.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
24	<b>smilevel56.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
23	<b>smilevel55.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
22	<b>smilevel54.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
21	<b>smilevel53.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
20	<b>smilevel52.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
19	<b>smilevel51.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
18	<b>smilevel50.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
17	<b>smilevel49.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
16	<b>smilevel48.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
15	<b>smilevel47.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
14	<b>smilevel46.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
13	<b>smilevel45.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
12	<b>smilevel44.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
11	<b>smilevel43.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
10	<b>smilevel42.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
9	<b>smilevel41.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
8	<b>smilevel40.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
7	<b>smilevel39.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
6	<b>smilevel38.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
5	<b>smilevel37.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
4	<b>smilevel36.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
3	<b>smilevel35.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
2	<b>smilevel34.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
1	<b>smilevel33.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
0	<b>smilevel32.</b> Read-write. Reset: 0. <b>Description:</b> This defines the edge/level trigger mode for SmiLevel[63:32]. Note these are different from SciLevl 0: Edge trigger mode, 1: Level trigger mode

**SMIx000000D4 (FCH::SMI::SMILEVEL2)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; SMIx000000D4; SMI=FED8\_0200h

Bits	Description
31	<b>smilevel95.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
30	<b>smilevel94.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
29	<b>smilevel93.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
28	<b>smilevel92.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
27	<b>smilevel91.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
26	<b>smilevel90.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
25	<b>smilevel89.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
24	<b>smilevel88.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
23	<b>smilevel87.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
22	<b>smilevel86.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
21	<b>smilevel85.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
20	<b>smilevel84.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
19	<b>smilevel83.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
18	<b>smilevel82.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
17	<b>smilevel81.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
16	<b>smilevel80.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
15	<b>smilevel79.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
14	<b>smilevel78.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
13	<b>smilevel77.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
12	<b>smilevel76.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
11	<b>smilevel75.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
10	<b>smilevel74.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
9	<b>smilevel73.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
8	<b>smilevel72.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
7	<b>smilevel71.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
6	<b>smilevel70.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
5	<b>smilevel69.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
4	<b>smilevel68.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
3	<b>smilevel67.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
2	<b>smilevel66.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
1	<b>smilevel65.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
0	<b>smilevel64.</b> Read-write. Reset: 0. <b>Description:</b> This defines the edge/level trigger mode for SmiLevel[95:64]. Note these are different from SciLevl 0: Edge trigger mode, 1: Level trigger mode

**SMIx000000D8 (FCH::SMI::SMILEVEL3)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; SMIx000000D8; SMI=FED8\_0200h

Bits	Description
31	<b>smilevel127.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
30	<b>smilevel126.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
29	<b>smilevel125.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
28	<b>smilevel124.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
27	<b>smilevel123.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
26	<b>smilevel122.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
25	<b>smilevel121.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
24	<b>smilevel120.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
23	<b>smilevel119.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
22	<b>smilevel118.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
21	<b>smilevel117.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
20	<b>smilevel116.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
19	<b>smilevel115.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
18	<b>smilevel114.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
17	<b>smilevel113.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
16	<b>smilevel112.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
15	<b>smilevel111.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
14	<b>smilevel110.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
13	<b>smilevel109.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
12	<b>smilevel108.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
11	<b>smilevel107.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
10	<b>smilevel106.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
9	<b>smilevel105.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
8	<b>smilevel104.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
7	<b>smilevel103.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
6	<b>smilevel102.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
5	<b>smilevel101.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
4	<b>smilevel100.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
3	<b>smilevel99.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
2	<b>smilevel98.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
1	<b>smilevel97.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
0	<b>smilevel96.</b> Read-write. Reset: 0. <b>Description:</b> This defines the edge/level trigger mode for SmiLevel[127:96]. Note these are different from SciLevel 0: Edge trigger mode, 1: Level trigger mode

**SMIx000000DC (FCH::SMI::SMILEVEL4)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; SMIx000000DC; SMI=FED8\_0200h

Bits	Description
31	<b>smilevel159.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
30	<b>smilevel158.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
29	<b>smilevel157.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
28	<b>smilevel156.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
27	<b>smilevel155.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
26	<b>smilevel154.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
25	<b>smilevel153.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
24	<b>smilevel152.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
23	<b>smilevel151.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
22	<b>smilevel150.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
21	<b>smilevel149.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
20	<b>smilevel148.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
19	<b>smilevel147.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
18	<b>smilevel146.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
17	<b>smilevel145.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
16	<b>smilevel144.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
15	<b>smilevel143.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
14	<b>smilevel142.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
13	<b>smilevel141.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
12	<b>smilevel140.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
11	<b>smilevel139.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
10	<b>smilevel138.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
9	<b>smilevel137.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
8	<b>smilevel136.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
7	<b>smilevel135.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
6	<b>smilevel134.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
5	<b>smilevel133.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
4	<b>smilevel132.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
3	<b>smilevel131.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
2	<b>smilevel130.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
1	<b>smilevel129.</b> Read-write. Reset: 0. 0: Edge trigger mode, 1: Level trigger mode
0	<b>smilevel128.</b> Read-write. Reset: 0. <b>Description:</b> This defines the edge/level trigger mode for SmiLevel[159:128]. Note these are different from SciLevel 0: Edge trigger mode, 1: Level trigger mode

**SMIx000000E0 (FCH::SMI::SMITRIG2)**

Read-write. Reset: FFFF\_FFFh.

\_aliasHOSTLEGACY; SMIx000000E0; SMI=FED8\_0200h

Bits	Description
31	<b>smitrig63.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
30	<b>smitrig62.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
29	<b>smitrig61.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
28	<b>smitrig60.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
27	<b>smitrig59.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
26	<b>smitrig58.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
25	<b>smitrig57.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
24	<b>smitrig56.</b> Read-write. Reset: 1. <b>Description:</b> 1: Active high 0: Active low
23	<b>smitrig55.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
22	<b>smitrig54.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
21	<b>smitrig53.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
20	<b>smitrig52.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
19	<b>smitrig51.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
18	<b>smitrig50.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
17	<b>smitrig49.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
16	<b>smitrig48.</b> Read-write. Reset: 1.

	<b>Description:</b> 0: Active low 1: Active high
15	<b>smitrig47.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
14	<b>smitrig46.</b> Read-write. Reset: 1. <b>Description:</b> 1: Active high 0: Active low
13	<b>smitrig45.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
12	<b>smitrig44.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
11	<b>smitrig43.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
10	<b>smitrig42.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
9	<b>smitrig41.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
8	<b>smitrig40.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
7	<b>smitrig39.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
6	<b>smitrig38.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
5	<b>smitrig37.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
4	<b>smitrig36.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
3	<b>smitrig35.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
2	<b>smitrig34.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
1	<b>smitrig33.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
0	<b>smitrig32.</b> Read-write. Reset: 1.

	<b>Description:</b> This defines the trigger mode for SmiTrig[63:32]. 0: Active low 1: Active high
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**SMIx000000E4 (FCH::SMI::SMITRIG3)**

Read-write. Reset: FFFF\_FFFFh.

\_aliasHOSTLEGACY; SMIx000000E4; SMI=FED8\_0200h

Bits	Description
31	<b>smitrig95.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
30	<b>smitrig94.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
29	<b>smitrig93.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
28	<b>smitrig92.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
27	<b>smitrig91.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
26	<b>smitrig90.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
25	<b>smitrig89.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
24	<b>smitrig88.</b> Read-write. Reset: 1. <b>Description:</b> 1: Active high 0: Active low
23	<b>smitrig87.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
22	<b>smitrig86.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
21	<b>smitrig85.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
20	<b>smitrig84.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
19	<b>smitrig83.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
18	<b>smitrig82.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
17	<b>smitrig81.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
16	<b>smitrig80.</b> Read-write. Reset: 1.

	<b>Description:</b> 0: Active low 1: Active high
15	<b>smitrig79.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
14	<b>smitrig78.</b> Read-write. Reset: 1. <b>Description:</b> 1: Active high 0: Active low
13	<b>smitrig77.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
12	<b>smitrig76.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
11	<b>smitrig75.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
10	<b>smitrig74.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
9	<b>smitrig73.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
8	<b>smitrig72.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
7	<b>smitrig71.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
6	<b>smitrig70.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
5	<b>smitrig69.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
4	<b>smitrig68.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
3	<b>smitrig67.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
2	<b>smitrig66.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
1	<b>smitrig65.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
0	<b>smitrig64.</b> Read-write. Reset: 1.

	<b>Description:</b> This defines the trigger mode for SmiTrig[95:64]. 0: Active low 1: Active high
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**SMIx000000E8 (FCH::SMI::SMITRIG4)**

Read-write. Reset: FFFF\_FFFFh.

\_aliasHOSTLEGACY; SMIx000000E8; SMI=FED8\_0200h

Bits	Description
31	<b>smitrig159.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
30	<b>smitrig158.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
29	<b>smitrig157.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
28	<b>smitrig156.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
27	<b>smitrig155.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
26	<b>smitrig154.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
25	<b>smitrig153.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
24	<b>smitrig152.</b> Read-write. Reset: 1. <b>Description:</b> 1: Active high 0: Active low
23	<b>smitrig151.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
22	<b>smitrig150.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
21	<b>smitrig149.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
20	<b>smitrig148.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
19	<b>smitrig147.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
18	<b>smitrig146.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
17	<b>smitrig145.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
16	<b>smitrig144.</b> Read-write. Reset: 1.

	<b>Description:</b> 0: Active low 1: Active high
15	<b>smitrig143.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
14	<b>smitrig142.</b> Read-write. Reset: 1. <b>Description:</b> 1: Active high 0: Active low
13	<b>smitrig141.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
12	<b>smitrig140.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
11	<b>smitrig139.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
10	<b>smitrig138.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
9	<b>smitrig137.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
8	<b>smitrig136.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
7	<b>smitrig135.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
6	<b>smitrig134.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
5	<b>smitrig133.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
4	<b>smitrig132.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
3	<b>smitrig131.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
2	<b>smitrig130.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
1	<b>smitrig129.</b> Read-write. Reset: 1. <b>Description:</b> 0: Active low 1: Active high
0	<b>smitrig128.</b> Read-write. Reset: 1.

	<b>Description:</b> This defines the trigger mode for SmiTrig[159:128]. 0: Active low 1: Active high
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### 11.3.4 High Precision Event Timer (HPET) Registers

HPET registers are accessed through two methods:

- Memory access to HPET memory address range from FED0\_0000h to FED0\_01FFh. Program PMx00[HpetEn]=1 to enable HPET decoding.
- Memory mapped access through the AcpiMmio region. The HPET registers range from FED8\_0000h+C00h to FED8\_0000h+CFFh. See PMx04[MmioEn].

All registers in this block are reset by PciRstB, which will be asserted in the following conditions:

- Resume Reset: This reset is asserted in G3 state and deasserted during G3 to S5 transition.
- System Reset: From system reset button.
- S0 Reset events: some events that happen in S0 state, such as CF9 and Keyboard Reset.
- Sleep states: S3, S5 and Power saving mode states.

HPETx00000000 (FCH::TMR::HPET::ID)	
Read-only. Reset: 1022_8201h.	
_aliasHOSTLEGACY; HPETx00000000; HPET=FED0_0000h	
Bits	Description
31:16	<b>vendorid.</b> Read-only. Reset: 1022h. AMD vendor ID.
15	<b>legacy_cap.</b> Read-only. Reset: 1. Legacy replacement interrupt is supported.
14	Reserved.
13	<b>counter_size_cap.</b> Read-only. Reset: 0. <b>Description:</b> Main counter is 32-bits wide or 64-bit mode. The read only register value depend on the HPET_width_sel register bit: When HPET_width_sel is 0, Counter_Size_Cap=0, means 32-bits wide When HPET_width_sel is 1, Counter_Size_Cap=1, means 64-bits wide
12:8	<b>num_tmr_cap.</b> Read-only. Reset: 02h. Three timers are supported.
7:0	<b>revid.</b> Read-only. Reset: 01h. Revision ID.

HPETx00000004 (FCH::TMR::HPET::CLKPERIOD)	
Read-only. Reset: 0429_B17Eh.	
_aliasHOSTLEGACY; HPETx00000004; HPET=FED0_0000h	
Bits	Description
31:0	<b>counter_clk_period.</b> Read-only. Reset: 0429_B17Eh. Specifies the clock period of each HPET timer tick. HPET main counter runs at 14.31818/48 MHz. The unit is femptoseconds ( $10^{-15}$ seconds). Note: The value of this register can be modified through MISC_Reg: 34h.

**HPETx00000010 (FCH::TMR::HPET::HPETCONFIG)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; HPETx00000010; HPET=FED0\_0000h

Bits	Description
31:9	Reserved.
8	<b>rst_sync_pingpong.</b> Read-write. Reset: 0. There is sync ping-pong logic to read timer value in Host clock domain, if this sync ping-pong logic stopped, timer value can no longer be read. Writing '1' to this bit will reset the logic to start sync ping-pong again, writing '0' will do nothing. This bit is write only.
7:2	Reserved.
1	<b>legacyen.</b> Read-write. Reset: 0. <b>Description:</b> If LegacyEn is set to 1b then: Timer0 interrupt goes to IRQ0 of PIC controller, INT2 of IoAPIC Timer1 interrupt goes to IRQ8 of PIC controller, INT8 of IoAPIC.
0	<b>tmren.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pause main counter and disable all timer interrupts. 1: Allow main counter to run and allow timer interrupts if enabled.

**HPETx00000020 (FCH::TMR::HPET::INTERRUPT\_STATUS)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; HPETx00000020; HPET=FED0\_0000h

Bits	Description
31:3	Reserved.
2	<b>tmr2intrsts.</b> Read-write. Reset: 0. <b>Description:</b> 0: Timer2 interrupt is not active. 1: Timer2 interrupt is active. Write 1 to clear if timer2 is set to level-triggered mode. When set to edge-triggered mode, software should ignore this bit and always write 0b to this bit.
1	<b>tmr1intrsts.</b> Read-write. Reset: 0. <b>Description:</b> 0: Timer1 interrupt is not active. 1: Timer1 interrupt is active. Write 1 to clear if timer1 is set to level-triggered mode. When set to edge-triggered mode, software should ignore this bit and always write 0b to this bit.
0	<b>tmr0intrsts.</b> Read-write. Reset: 0. <b>Description:</b> 0: Timer0 interrupt is not active. 1: Timer0 interrupt is active. Write 1 to clear if timer0 is set to level-triggered mode. When set to edge-triggered mode, software should ignore this bit and always write 0b to this bit.

**HPETx000000F0 (FCH::TMR::HPET::MAIN\_COUNTER\_L)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; HPETx000000F0; HPET=FED0\_0000h

Bits	Description
31:0	<b>maincounter_l.</b> Read-write. Reset: 0000_0000h. <b>Description:</b> HPET main counter, increment by 1 on every clock. Counter should be written to only when halted. The width of main counter depends on HPET_width_sel register bit: 0: HPET main counter is 32-bit. MainCounter_L is the valid counter bits. MainCounter_H is not valid. 1: HPET main counter is 64-bit. Both MainCounter_L and MainCounter_H are valid.

**HPETx000000F4 (FCH::TMR::HPET::MAIN\_COUNTER\_H)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; HPETx000000F4; HPET=FED0\_0000h

Bits	Description
31:0	<b>maincounter_h.</b> Read-write. Reset: 0000_0000h. <b>Description:</b> HPET main counter, increment by 1 on every clock. Counter should be written to only when halted. The width of main counter depends on HPET_width_sel register bit: 0: HPET main counter is 32-bit. MainCounter_L is the valid counter bits. MainCounter_H is not valid. 1: HPET main counter is 64-bit. Both MainCounter_L and MainCounter_H are valid.

**HPETx00000100 (FCH::TMR::HPET::TMR0\_CONF\_CAP\_L)**

Read-write. Reset: 0000\_8010h.

Hardware supports 3 timers, &lt;N&gt; is 0, 1 or 2.

\_aliasHOSTLEGACY; HPETx00000100; HPET=FED0\_0000h

Bits	Description
31:16	Reserved.
15	<b>tmrfsbcap.</b> Read-write. Reset: 1. FSB delivery is supported. Read only.
14	<b>tmrfsben.</b> Read-write. Reset: 0. Set to 1 to enable FSB (Front Side Bus) delivery of interrupt.
13:9	<b>tmrintroute.</b> Read-write. Reset: 00h. These 5 bits specify which INT entry of IoAPIC the timer is routed to when LegacyEn is not set.
8	<b>tmr32modeen.</b> Read-write. Reset: 0. Timer n 32-bit Mode: (where n is the timer number: 0 to 2). Software can set this read/write bit to force a 64-bit timer to behave as a 32-bit timer. This is typically needed if the software is not willing to halt the main counter to read or write a particular timer, and the software is not capable of doing an atomic 64-bit read to the timer. If the timer is not 64 bits wide, then this bit will always be read as 0 and writes will have no effect.
7	Reserved.
6	<b>tmrsetper.</b> Read-write. Reset: 0. <b>Description:</b> Set to 1 to allow software to set the timer's accumulator if the timer is set to periodic mode. The bit is automatically cleared when 'Comparator' is written by software.
5	<b>tmrsizecap.</b> Read-write. Reset: 0. <b>Description:</b> The timer is 32-bits wide/or 64bit wide. This read only register value depend on the HPET_width_sel register bit: When HPET_width_sel is 0, TmrSizeCap =0, means 32-bits wide When HPET_width_sel is 1, TmrSizeCap =1, means 64-bits wide
4	<b>tmrtypcap.</b> Read-write. Reset: 1. The timer supports periodic interrupt delivery mode. Read only.
3	<b>tmrtyp.</b> Read-write. Reset: 0. <b>Description:</b> Select the timer interrupt type: 0: Non-periodic 1: Periodic
2	<b>tmrinten.</b> Read-write. Reset: 0. Set to 1 to enable timer interrupt.
1	<b>tmrinttyp.</b> Read-write. Reset: 0. <b>Description:</b> Control timer interrupt polarity: 0: Edge triggered 1: Level triggered
0	Reserved.



**HPETx00000104 (FCH::TMR::HPET::TMR0\_CONF\_CAP\_H)**

Read-only. Reset: 00C0\_0000h.

Hardware supports 3 timers, &lt;N&gt; is 0, 1 or 2.

\_aliasHOSTLEGACY; HPETx00000104; HPET=FED0\_0000h

Bits	Description
31:0	<b>tmrintroutecap.</b> Read-only. Reset: 00C0_0000h. Indicates which INT entry of IoAPIC can be assigned to the timer interrupt. Read only.

**HPETx00000108 (FCH::TMR::HPET::TMR0\_COMP\_L)**

Read-write. Reset: FFFF\_FFFFh.

Hardware supports 3 timers, &lt;N&gt; is 0, 1 or 2.

\_aliasHOSTLEGACY; HPETx00000108; HPET=FED0\_0000h

Bits	Description
31:0	<b>comparator_l.</b> Read-write. Reset: FFFF_FFFFh. <b>Description:</b> The timer comparator. In non-periodic mode: 'Comparator' is writeable. In periodic mode: 'Comparator' can be modified after TmrSetPer is set to 1. 'Comparator' is periodically incremented by the value last written to this register. By default, value is incremented by 0xFFFFFFFF for 32-bit mode or 0xFFFFFFFFFFFFFFFF for 64-bit mode. The width of Comparator depends on HPET_width_sel register bit: 0: The Comparator is 32-bit. Comparator_L is the valid bits. Comparator_H is not valid. 1: The Comparator is 64-bit. Both Comparator_L and Comparator_H are valid.

**HPETx0000010C (FCH::TMR::HPET::TMR0\_COMP\_H)**

Read-write. Reset: 0000\_0000h.

Hardware supports 3 timers, &lt;N&gt; is 0, 1 or 2.

Note1: The HPET spec requires different default values for 32-bit and 64-bit HPET. For 32-bit HPET, Comparator\_H default should be 00000000h. For 64-bit HPET, Comparator\_H default should be FFFFFFFFh. Our HPET can be configured as 32-bit or 64-bit by HPET\_width\_sel register bit. By default, HPET is 32-bit, so the default of Comparator\_H is 00000000h.

\_aliasHOSTLEGACY; HPETx0000010C; HPET=FED0\_0000h

Bits	Description
31:0	<b>comparator_h.</b> Read-write. Reset: 0000_0000h. <b>Description:</b> The timer comparator. In non-periodic mode: 'Comparator' is writeable. In periodic mode: 'Comparator' can be modified after TmrSetPer is set to 1. 'Comparator' is periodically incremented by the value last written to this register. By default, value is incremented by 0xFFFFFFFF for 32-bit mode or 0xFFFFFFFFFFFFFFFF for 64-bit mode. The width of Comparator depends on HPET_width_sel register bit: 0: The Comparator is 32-bit. Comparator_L is the valid bits. Comparator_H is not valid. 1: The Comparator is 64-bit. Both Comparator_L and Comparator_H are valid.

**HPETx00000110 (FCH::TMR::HPET::TMR0\_FSBINTVAL)**

Read-write. Reset: 0000\_0000h.

Hardware supports 3 timers, &lt;N&gt; is 0, 1 or 2.

\_aliasHOSTLEGACY; HPETx00000110; HPET=FED0\_0000h

Bits	Description
31:0	<b>tn_fsb_int_val.</b> Read-write. Reset: 0000_0000h. Software sets this 32-bit field to specify the write data of FSB Interrupt Message.

**HPETx00000114 (FCH::TMR::HPET::TMR0\_FSBINTADDR)**

Read-write. Reset: 0000\_0000h.

Hardware supports 3 timers, &lt;N&gt; is 0, 1 or 2.

\_aliasHOSTLEGACY; HPETx00000114; HPET=FED0\_0000h

Bits	Description
31:0	<b>tn_fsb_int_addr.</b> Read-write. Reset: 0000_0000h. <b>Description:</b> Software sets this 32-bit field to specify the address of FSB interrupt Message.

**HPETx00000120 (FCH::TMR::HPET::TMR1\_CONF\_CAP\_L)**

Read-write. Reset: 0000\_8010h.

Hardware supports 3 timers, &lt;N&gt; is 0, 1 or 2.

\_aliasHOSTLEGACY; HPETx00000120; HPET=FED0\_0000h

Bits	Description
31:16	Reserved.
15	<b>tmrfsbcap.</b> Read-write. Reset: 1. FSB delivery is supported. Read only.
14	<b>tmrfsben.</b> Read-write. Reset: 0. Set to 1 to enable FSB (Front Side Bus) delivery of interrupt.
13:9	<b>tmrintroute.</b> Read-write. Reset: 00h. These 5 bits specify which INT entry of IoAPIC the timer is routed to when LegacyEn is not set.
8	<b>tmr32modeen.</b> Read-write. Reset: 0. Timer n 32-bit Mode: (where n is the timer number: 0 to 2). Software can set this read/write bit to force a 64-bit timer to behave as a 32-bit timer. This is typically needed if the software is not willing to halt the main counter to read or write a particular timer, and the software is not capable of doing an atomic 64-bit read to the timer. If the timer is not 64 bits wide, then this bit will always be read as 0 and writes will have no effect.
7	Reserved.
6	<b>tmrsetper.</b> Read-write. Reset: 0. <b>Description:</b> Set to 1 to allow software to set the timer's accumulator if the timer is set to periodic mode. The bit is automatically cleared when 'Comparator' is written by software.
5	<b>tmrsizecap.</b> Read-write. Reset: 0. <b>Description:</b> The timer is 32-bits wide/or 64bit wide. This read only register value depend on the HPET_width_sel register bit: When HPET_width_sel is 0, TmrSizeCap =0, means 32-bits wide When HPET_width_sel is 1, TmrSizeCap =1, means 64-bits wide
4	<b>tmrtypcap.</b> Read-write. Reset: 1. The timer supports periodic interrupt delivery mode. Read only.
3	<b>tmrtyp.</b> Read-write. Reset: 0. <b>Description:</b> Select the timer interrupt type: 0: Non-periodic 1: Periodic
2	<b>tmrinten.</b> Read-write. Reset: 0. Set to 1 to enable timer interrupt.
1	<b>tmrinttyp.</b> Read-write. Reset: 0. <b>Description:</b> Control timer interrupt polarity: 0: Edge triggered 1: Level triggered
0	Reserved.

**HPETx00000124 (FCH::TMR::HPET::TMR1\_CONF\_CAP\_H)**

Read-only. Reset: 00C0\_0000h.

Hardware supports 3 timers, &lt;N&gt; is 0, 1 or 2.

\_aliasHOSTLEGACY; HPETx00000124; HPET=FED0\_0000h

Bits	Description
31:0	<b>tmrintroutecap.</b> Read-only. Reset: 00C0_0000h. Indicates which INT entry of IoAPIC can be assigned to the timer interrupt. Read only.

**HPETx00000128 (FCH::TMR::HPET::TMR1\_COMP\_L)**

Read-write. Reset: FFFF\_FFFFh.

Hardware supports 3 timers, &lt;N&gt; is 0, 1 or 2.

\_aliasHOSTLEGACY; HPETx00000128; HPET=FED0\_0000h

Bits	Description
31:0	<b>comparator_l.</b> Read-write. Reset: FFFF_FFFFh. <b>Description:</b> The timer comparator. In non-periodic mode: 'Comparator' is writeable. In periodic mode: 'Comparator' can be modified after TmrSetPer is set to 1. 'Comparator' is periodically incremented by the value last written to this register. By default, value is incremented by 0xFFFFFFFF for 32-bit mode or 0xFFFFFFFFFFFFFFFF for 64-bit mode. The width of Comparator depends on HPET_width_sel register bit: 0: The Comparator is 32-bit. Comparator_L is the valid bits. Comparator_H is not valid. 1: The Comparator is 64-bit. Both Comparator_L and Comparator_H are valid.

**HPETx0000012C (FCH::TMR::HPET::TMR1\_COMP\_H)**

Read-write. Reset: 0000\_0000h.

Hardware supports 3 timers, &lt;N&gt; is 0, 1 or 2.

Note1: The HPET spec requires different default values for 32-bit and 64-bit HPET. For 32-bit HPET, Comparator\_H default should be 00000000h. For 64-bit HPET, Comparator\_H default should be FFFFFFFFh. Our HPET can be configured as 32-bit or 64-bit by HPET\_width\_sel register bit. By default, HPET is 32-bit, so the default of Comparator\_H is 00000000h.

\_aliasHOSTLEGACY; HPETx0000012C; HPET=FED0\_0000h

Bits	Description
31:0	<b>comparator_h.</b> Read-write. Reset: 0000_0000h. <b>Description:</b> The timer comparator. In non-periodic mode: 'Comparator' is writeable. In periodic mode: 'Comparator' can be modified after TmrSetPer is set to 1. 'Comparator' is periodically incremented by the value last written to this register. By default, value is incremented by 0xFFFFFFFF for 32-bit mode or 0xFFFFFFFFFFFFFFFF for 64-bit mode. The width of Comparator depends on HPET_width_sel register bit: 0: The Comparator is 32-bit. Comparator_L is the valid bits. Comparator_H is not valid. 1: The Comparator is 64-bit. Both Comparator_L and Comparator_H are valid.

**HPETx00000130 (FCH::TMR::HPET::TMR1\_FSBINTVAL)**

Read-write. Reset: 0000\_0000h.

Hardware supports 3 timers, &lt;N&gt; is 0, 1 or 2.

\_aliasHOSTLEGACY; HPETx00000130; HPET=FED0\_0000h

Bits	Description
31:0	<b>tn_fsb_int_val.</b> Read-write. Reset: 0000_0000h. Software sets this 32-bit field to specify the write data of FSB Interrupt Message.

**HPETx00000134 (FCH::TMR::HPET::TMR1\_FSBINTADDR)**

Read-write. Reset: 0000\_0000h.

Hardware supports 3 timers, &lt;N&gt; is 0, 1 or 2.

\_aliasHOSTLEGACY; HPETx00000134; HPET=FED0\_0000h

Bits	Description
31:0	<b>tn_fsb_int_addr.</b> Read-write. Reset: 0000_0000h. <b>Description:</b> Software sets this 32-bit field to specify the address of FSB interrupt Message.

**HPETx00000140 (FCH::TMR::HPET::TMR2\_CONF\_CAP\_L)**

Read-write. Reset: 0000\_8010h.

Hardware supports 3 timers, &lt;N&gt; is 0, 1 or 2.

\_aliasHOSTLEGACY; HPETx00000140; HPET=FED0\_0000h

Bits	Description
31:16	Reserved.
15	<b>tmrfsbcap.</b> Read-write. Reset: 1. FSB delivery is supported. Read only.
14	<b>tmrfsben.</b> Read-write. Reset: 0. Set to 1 to enable FSB (Front Side Bus) delivery of interrupt.
13:9	<b>tmrintroute.</b> Read-write. Reset: 00h. These 5 bits specify which INT entry of IoAPIC the timer is routed to when LegacyEn is not set.
8	<b>tmr32modeen.</b> Read-write. Reset: 0. Timer n 32-bit Mode: (where n is the timer number: 0 to 2). Software can set this read/write bit to force a 64-bit timer to behave as a 32-bit timer. This is typically needed if the software is not willing to halt the main counter to read or write a particular timer, and the software is not capable of doing an atomic 64-bit read to the timer. If the timer is not 64 bits wide, then this bit will always be read as 0 and writes will have no effect.
7	Reserved.
6	<b>tmrsetper.</b> Read-write. Reset: 0. <b>Description:</b> Set to 1 to allow software to set the timer's accumulator if the timer is set to periodic mode. The bit is automatically cleared when 'Comparator' is written by software.
5	<b>tmrsizecap.</b> Read-write. Reset: 0. <b>Description:</b> The timer is 32-bits wide/or 64bit wide. This read only register value depend on the HPET_width_sel register bit: When HPET_width_sel is 0, TmrSizeCap =0, means 32-bits wide When HPET_width_sel is 1, TmrSizeCap =1, means 64-bits wide
4	<b>tmrtypcap.</b> Read-write. Reset: 1. The timer supports periodic interrupt delivery mode. Read only.
3	<b>tmrtyp.</b> Read-write. Reset: 0. <b>Description:</b> Select the timer interrupt type: 0: Non-periodic 1: Periodic
2	<b>tmrinten.</b> Read-write. Reset: 0. Set to 1 to enable timer interrupt.
1	<b>tmrinttyp.</b> Read-write. Reset: 0. <b>Description:</b> Control timer interrupt polarity: 0: Edge triggered 1: Level triggered
0	Reserved.

**HPETx00000144 (FCH::TMR::HPET::TMR2\_CONF\_CAP\_H)**

Read-only. Reset: 00C0\_0000h.

Hardware supports 3 timers, &lt;N&gt; is 0, 1 or 2.

\_aliasHOSTLEGACY; HPETx00000144; HPET=FED0\_0000h

Bits	Description
31:0	<b>tmrintroutecap.</b> Read-only. Reset: 00C0_0000h. Indicates which INT entry of IoAPIC can be assigned to the timer interrupt. Read only.

**HPETx00000148 (FCH::TMR::HPET::TMR2\_COMP\_L)**

Read-write. Reset: FFFF\_FFFFh.

Hardware supports 3 timers, &lt;N&gt; is 0, 1 or 2.

\_aliasHOSTLEGACY; HPETx00000148; HPET=FED0\_0000h

Bits	Description
31:0	<b>comparator_l.</b> Read-write. Reset: FFFF_FFFFh.  <b>Description:</b> The timer comparator. In non-periodic mode: 'Comparator' is writeable. In periodic mode: 'Comparator' can be modified after TmrSetPer is set to 1. 'Comparator' is periodically incremented by the value last written to this register. By default, value is incremented by 0xFFFFFFFF for 32-bit mode or 0xFFFFFFFFFFFFFFFF for 64-bit mode. The width of Comparator depends on HPET_width_sel register bit: 0: The Comparator is 32-bit. Comparator_L is the valid bits. Comparator_H is not valid. 1: The Comparator is 64-bit. Both Comparator_L and Comparator_H are valid.

**HPETx0000014C (FCH::TMR::HPET::TMR2\_COMP\_H)**

Read-write. Reset: 0000\_0000h.

Hardware supports 3 timers, &lt;N&gt; is 0, 1 or 2.

Note1: The HPET spec requires different default values for 32-bit and 64-bit HPET. For 32-bit HPET, Comparator\_H default should be 00000000h. For 64-bit HPET, Comparator\_H default should be FFFFFFFFh. Our HPET can be configured as 32-bit or 64-bit by HPET\_width\_sel register bit. By default, HPET is 32-bit, so the default of Comparator\_H is 00000000h.

\_aliasHOSTLEGACY; HPETx0000014C; HPET=FED0\_0000h

Bits	Description
31:0	<b>comparator_h.</b> Read-write. Reset: 0000_0000h.  <b>Description:</b> The timer comparator. In non-periodic mode: 'Comparator' is writeable. In periodic mode: 'Comparator' can be modified after TmrSetPer is set to 1. 'Comparator' is periodically incremented by the value last written to this register. By default, value is incremented by 0xFFFFFFFF for 32-bit mode or 0xFFFFFFFFFFFFFFFF for 64-bit mode. The width of Comparator depends on HPET_width_sel register bit: 0: The Comparator is 32-bit. Comparator_L is the valid bits. Comparator_H is not valid. 1: The Comparator is 64-bit. Both Comparator_L and Comparator_H are valid.

**HPETx00000150 (FCH::TMR::HPET::TMR2\_FSBINTVAL)**

Read-write. Reset: 0000\_0000h.

Hardware supports 3 timers, &lt;N&gt; is 0, 1 or 2.

\_aliasHOSTLEGACY; HPETx00000150; HPET=FED0\_0000h

Bits	Description
31:0	<b>tn_fsb_int_val.</b> Read-write. Reset: 0000_0000h. Software sets this 32-bit field to specify the write data of FSB Interrupt Message.

**HPETx00000154 (FCH::TMR::HPET::TMR2\_FSBINTADDR)**

Read-write. Reset: 0000\_0000h.

Hardware supports 3 timers, &lt;N&gt; is 0, 1 or 2.

\_aliasHOSTLEGACY; HPETx00000154; HPET=FED0\_0000h

Bits	Description
31:0	<b>tn_fsb_int_addr.</b> Read-write. Reset: 0000_0000h. <b>Description:</b> Software sets this 32-bit field to specify the address of FSB interrupt Message.

**HPETx000001B0 (FCH::TMR::HPET::TMR0\_COMP\_BASE\_SHADOW\_L)**

Read-write. Reset: FFFF\_FFFFh.

\_aliasHOSTLEGACY; HPETx000001B0; HPET=FED0\_0000h

Bits	Description
31:0	<b>tmr0_comp_base_shadow_l.</b> Read-write. Reset: FFFF_FFFFh. <b>Description:</b> This is shadow of the base value of Tmr0 Comparator (HPET_Reg:108h). Reading this register returns the base value of Timer 0 Comparator. Writing the register will change the base value of Timer 0 Comparator.

**HPETx000001B4 (FCH::TMR::HPET::TMR0\_COMP\_BASE\_SHADOW\_H)**

Read-write. Reset: 0000\_0000h.

Note1: The HPET spec requires different default values for 32-bit and 64-bit HPET. For 32-bit HPET, Comparator\_H default should be 00000000h. For 64-bit HPET, Comparator\_H default should be FFFFFFFFh. Our HPET can be configured as 32-bit or 64-bit by HPET\_width\_sel register bit. By default, HPET is 32-bit, so the default of Comparator\_H is 00000000h.

\_aliasHOSTLEGACY; HPETx000001B4; HPET=FED0\_0000h

Bits	Description
31:0	<b>tmr0_comp_base_shadow_h.</b> Read-write. Reset: 0000_0000h. <b>Description:</b> This is shadow of the base value of Tmr0 Comparator (HPET_Reg:108h). Reading this register returns the base value of Timer 0 Comparator. Writing the register will change the base value of Timer 0 Comparator.

**HPETx000001B8 (FCH::TMR::HPET::TMR0\_COMP\_SHADOW\_L)**

Read-write. Reset: FFFF\_FFFFh.

\_aliasHOSTLEGACY; HPETx000001B8; HPET=FED0\_0000h

Bits	Description
31:0	<b>tmr0_comp_shadow_l.</b> Read-write. Reset: FFFF_FFFFh. <b>Description:</b> This is shadow of the current value of Tmr0 Comparator (HPET_Reg:108h). Reading this register returns the base value of Timer 0 Comparator. Writing the register will change the base value of Timer 0 Comparator.

**HPETx000001BC (FCH::TMR::HPET::TMR0\_COMP\_SHADOW\_H)**

Read-write. Reset: 0000\_0000h.

Note1: The HPET spec requires different default values for 32-bit and 64-bit HPET. For 32-bit HPET, Comparator\_H default should be 00000000h. For 64-bit HPET, Comparator\_H default should be FFFFFFFFh. Our HPET can be configured as 32-bit or 64-bit by HPET\_width\_sel register bit. By default, HPET is 32-bit, so the default of Comparator\_H is 00000000h.

\_aliasHOSTLEGACY; HPETx000001BC; HPET=FED0\_0000h

Bits	Description
31:0	<b>tmr0_comp_shadow_h.</b> Read-write. Reset: 0000_0000h. <b>Description:</b> This is shadow of the current value of Tmr0 Comparator (HPET_Reg:108h). Reading this register returns the base value of Timer 0 Comparator. Writing the register will change the base value of Timer 0 Comparator.

**HPETx000001C0 (FCH::TMR::HPET::TMR1\_COMP\_BASE\_SHADOW\_L)**

Read-write. Reset: FFFF\_FFFFh.

\_aliasHOSTLEGACY; HPETx000001C0; HPET=FED0\_0000h

Bits	Description
31:0	<b>tmr1_comp_base_shadow_l.</b> Read-write. Reset: FFFF_FFFFh. <b>Description:</b> This is shadow of the base value of Tmr1 Comparator (HPET_Reg:108h). Reading this register returns the base value of Timer 1 Comparator. Writing the register will change the base value of Timer 1 Comparator.

**HPETx000001C4 (FCH::TMR::HPET::TMR1\_COMP\_BASE\_SHADOW\_H)**

Read-write. Reset: 0000\_0000h.

Note1: The HPET spec requires different default values for 32-bit and 64-bit HPET. For 32-bit HPET, Comparator\_H default should be 00000000h. For 64-bit HPET, Comparator\_H default should be FFFFFFFFh. Our HPET can be configured as 32-bit or 64-bit by HPET\_width\_sel register bit. By default, HPET is 32-bit, so the default of Comparator\_H is 00000000h.

\_aliasHOSTLEGACY; HPETx000001C4; HPET=FED0\_0000h

Bits	Description
31:0	<b>tmr1_comp_base_shadow_h.</b> Read-write. Reset: 0000_0000h. <b>Description:</b> This is shadow of the base value of Tmr1 Comparator (HPET_Reg:108h). Reading this register returns the base value of Timer 1 Comparator. Writing the register will change the base value of Timer 1 Comparator.

**HPETx000001C8 (FCH::TMR::HPET::TMR1\_COMP\_SHADOW\_L)**

Read-write. Reset: FFFF\_FFFFh.

\_aliasHOSTLEGACY; HPETx000001C8; HPET=FED0\_0000h

Bits	Description
31:0	<b>tmr1_comp_shadow_l.</b> Read-write. Reset: FFFF_FFFFh. <b>Description:</b> This is shadow of the current value of Tmr1 Comparator (HPET_Reg:108h). Reading this register returns the base value of Timer 1 Comparator. Writing the register will change the base value of Timer 1 Comparator.

**HPETx000001CC (FCH::TMR::HPET::TMR1\_COMP\_SHADOW\_H)**

Read-write. Reset: 0000\_0000h.

Note1: The HPET spec requires different default values for 32-bit and 64-bit HPET. For 32-bit HPET, Comparator\_H default should be 00000000h. For 64-bit HPET, Comparator\_H default should be FFFFFFFFh. Our HPET can be configured as 32-bit or 64-bit by HPET\_width\_sel register bit. By default, HPET is 32-bit, so the default of Comparator\_H is 00000000h.

\_aliasHOSTLEGACY; HPETx000001CC; HPET=FED0\_0000h

Bits	Description
31:0	<b>tmr1_comp_shadow_h.</b> Read-write. Reset: 0000_0000h. <b>Description:</b> This is shadow of the current value of Tmr1 Comparator (HPET_Reg:108h). Reading this register returns the base value of Timer 1 Comparator. Writing the register will change the base value of Timer 1 Comparator.

**HPETx000001D0 (FCH::TMR::HPET::TMR2\_COMP\_BASE\_SHADOW\_L)**

Read-write. Reset: FFFF\_FFFFh.

\_aliasHOSTLEGACY; HPETx000001D0; HPET=FED0\_0000h

Bits	Description
31:0	<b>tmr2_comp_base_shadow_l.</b> Read-write. Reset: FFFF_FFFFh. <b>Description:</b> This is shadow of the base value of Tmr2 Comparator (HPET_Reg:108h). Reading this register returns the base value of Timer 2 Comparator. Writing the register will change the base value of Timer 2 Comparator.

**HPETx000001D4 (FCH::TMR::HPET::TMR2\_COMP\_BASE\_SHADOW\_H)**

Read-write. Reset: 0000\_0000h.

Note1: The HPET spec requires different default values for 32-bit and 64-bit HPET. For 32-bit HPET, Comparator\_H default should be 00000000h. For 64-bit HPET, Comparator\_H default should be FFFFFFFFh. Our HPET can be configured as 32-bit or 64-bit by HPET\_width\_sel register bit. By default, HPET is 32-bit, so the default of Comparator\_H is 00000000h.

\_aliasHOSTLEGACY; HPETx000001D4; HPET=FED0\_0000h

Bits	Description
31:0	<b>tmr2_comp_base_shadow_h.</b> Read-write. Reset: 0000_0000h. <b>Description:</b> This is shadow of the base value of Tmr2 Comparator (HPET_Reg:108h). Reading this register returns the base value of Timer 2 Comparator. Writing the register will change the base value of Timer 2 Comparator.

**HPETx000001D8 (FCH::TMR::HPET::TMR2\_COMP\_SHADOW\_L)**

Read-write. Reset: FFFF\_FFFFh.

\_aliasHOSTLEGACY; HPETx000001D8; HPET=FED0\_0000h

Bits	Description
31:0	<b>tmr2_comp_shadow_l.</b> Read-write. Reset: FFFF_FFFFh. <b>Description:</b> This is shadow of the current value of Tmr2 Comparator (HPET_Reg:108h). Reading this register returns the base value of Timer 2 Comparator. Writing the register will change the base value of Timer 2 Comparator.

**HPETx000001DC (FCH::TMR::HPET::TMR2\_COMP\_SHADOW\_H)**

Read-write. Reset: 0000\_0000h.

Note1: The HPET spec requires different default values for 32-bit and 64-bit HPET. For 32-bit HPET, Comparator\_H default should be 00000000h. For 64-bit HPET, Comparator\_H default should be FFFFFFFFh. Our HPET can be configured as 32-bit or 64-bit by HPET\_width\_sel register bit. By default, HPET is 32-bit, so the default of Comparator\_H is 00000000h.

\_aliasHOSTLEGACY; HPETx000001DC; HPET=FED0\_0000h

Bits	Description
31:0	<b>tmr2_comp_shadow_h.</b> Read-write. Reset: 0000_0000h. <b>Description:</b> This is shadow of the current value of Tmr2 Comparator (HPET_Reg:108h). Reading this register returns the base value of Timer 2 Comparator. Writing the register will change the base value of Timer 2 Comparator.

**HPETx000001E0 (FCH::TMR::HPET::MAIN\_COUNTER\_RTC\_L)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; HPETx000001E0; HPET=FED0\_0000h

Bits	Description
31:0	<b>main_counter_rtc_l.</b> Read-write. Reset: 0000_0000h. <b>Description:</b> This is a shadow of Main_Counter register. It samples the value of Main_Counter at every falling edge of Rtc 32kHz clock for SW to read. When SW writes this register, Main_Counter (offset F0) will be updated with the same value written to this register, and then enabled counting at the next RtcClk falling edge. The purpose of this register is for the convenience of SW save/restore HPET. For 32-bit HPET mode, only Main_Counter_rtc_L is valid. For 64-bit HPET mode, both Main_Counter_rtc_L and Main_Counter_rtc_H are valid.



**HPETx000001E4 (FCH::TMR::HPET::MAIN\_COUNTER\_RTC\_H)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; HPETx000001E4; HPET=FED0\_0000h

Bits	Description
31:0	<b>main_counter_rtc_h.</b> Read-write. Reset: 0000_0000h. <b>Description:</b> This is a shadow of Main_Counter register. It samples the value of Main_Counter at every falling edge of Rtc 32kHz clock for SW to read. When SW writes this register, Main_Counter (offset F0) will be updated with the same value written to this register, and then enabled counting at the next RtcClk falling edge. The purpose of this register is for the convenience of SW save/restore HPET. For 32-bit HPET mode, only Main_Counter_rtc_L is valid. For 64-bit HPET mode, both Main_Counter_rtc_L and Main_Counter_rtc_H are valid.

**HPETx000001E8 (FCH::TMR::HPET::NXTTMRREMAIN\_L)**

Read-write. Reset: FFFF\_FFFFh.

\_aliasHOSTLEGACY; HPETx000001E8; HPET=FED0\_0000h

Bits	Description
31:0	<b>nxttmrremain_l.</b> Read-write. Reset: FFFF_FFFFh. <b>Description:</b> Read-only. This register tells SW how many timer ticks remain before the next enabled comparator interrupt. For 32-bit HPET mode, only NxtTmrRemain_L is valid. For 64-bit HPET mode, both NxtTmrRemain_L and NxtTmrRemain_H are valid.

**HPETx000001EC (FCH::TMR::HPET::NXTTMRREMAIN\_H)**

Read-write. Reset: FFFF\_FFFFh.

\_aliasHOSTLEGACY; HPETx000001EC; HPET=FED0\_0000h

Bits	Description
31:0	<b>nxttmrremain_h.</b> Read-write. Reset: FFFF_FFFFh. <b>Description:</b> Read-only. This register tells SW how many timer ticks remain before the next enabled comparator interrupt. For 32-bit HPET mode, only NxtTmrRemain_L is valid. For 64-bit HPET mode, both NxtTmrRemain_L and NxtTmrRemain_H are valid.

**11.3.5 Watchdog Timer (WDT) Registers**

Watchdog timer registers are accessed through two methods:

- Memory access to Watchdog Timer memory address range from FEB0\_0000h to FEB0\_000Fh. Program FCH::PM::DECODEEN[watchdogtmren]=1 to enable Watchdog Timer decoding.
- Memory mapped access through the AcpiMmio region. The Watchdog Timer registers start from FED8\_0000h+B00h. See FCH::PM::ISACONTROL[mmioen].

**WDTx00000000 (FCH::TMR::WDT::WATCHDOGCONTROL)**

Read-write.

\_aliasHOSTLEGACY; WDTx00000000; WDT=FED8\_0B00h

Bits	Description
31:8	Reserved.
7	<b>watchdogtrigger_wo.</b> Read-write. Reset: 0. <b>Description:</b> Write only. Setting this bit triggers the watchdog to start a new count interval, counting down from the value that was last written to the Watchdog Count Register. This bit is always read as zero. Setting this bit has no effect if the watchdog is disabled or stopped.
6:5	Reserved.
4	<b>watchdogactionen.</b> Read-write. Reset: 1. <b>Description:</b> This bit is reset when enter Power saving mode. It can only be set after system enter POWER SAVING MODE and recover back. It is set by <a href="#">MP1</a> . When this bit is high, the actions in bit2 can be implemented. When this bit is low, although WatchDogFired is set, the actions will still be suppressed.
3	<b>watchdogdisable.</b> Read-write. Reset: 1. <b>Description:</b> This bit reflects the state of PMIO_Reg:00[7]. Writing to this bit has no effect. 0: Enable 1: Disable
2	<b>watchdogaction.</b> Read-write. Reset: 0. <b>Description:</b> This bit determines the action to be taken when the watchdog timer expires. 0: System reset 1: System power off The bit is only valid when the watchdog is enabled.
1	<b>watchdogfired.</b> Read-write. Reset: 0. A value of "1" indicates that the watchdog timer has expired and caused the current restart. The bit is cleared by writing a "1" to bit 1 in the Watchdog Control register. Writing a "0" has no effect. The bit is cleared by a power cycle or by the operating system and it must remain cleared for any restart that is not caused by the watchdog timer firing. The bit is only valid when the watchdog is enabled.
0	<b>watchdogrunstopb.</b> Read-write. Reset: 0. <b>Description:</b> This bit is used to control or indicate whether the watchdog is in the Running and Stopped states. 1: Watchdog is in the Running state 0: Watchdog is in the Stopped state If the watchdog is in the Stopped state and a 1 is written to bit [0], the watchdog moves to the Running state, but a count interval is not started until a 1 is written to bit [7]. If the watchdog is in the Running state, writing a 1 to bit 0 has no effect. The bit is only valid when the watchdog is enabled.

**WDTx00000004 (FCH::TMR::WDT::WATCHDOGCOUNT)**

Read-write.

\_aliasHOSTLEGACY; WDTx00000004; WDT=FED8\_0B00h

Bits	Description
31:16	Reserved.
15:0	<b>watchdogcount.</b> Read-write. Reset: XXXXXXXXXXXXXXXXb. <b>Description:</b> This defines the countdown time for the counter. The units are defined in the Units field in the Watchdog Resource Table (WDRT). The maximum value is defined in the Max Count field in the WDRT. Reading this register returns in the current counter value.

**11.3.6 Wake Alarm Device (AcDcTimer) Registers**

In Family 1Ah Models , signal iBatteryModeB is not tied off, it connects to BP\_AC\_PRESENCE or BP\_AGPIOWAKE.

The AC/DC timer registers are used to control the wake alarm device. They are accessed through the AcpiMmio region. The AC DC timer registers range from FED8\_0000h+1D00h to FED8\_0000h+1DFFh.

#### ACDCx00000000 (FCH::TMR::ACDC::AC\_TIMER\_VALUE)

Read-write. Reset: FFFF\_FFFFh.

\_aliasHOSTLEGACY; ACDCx00000000; ACDC=FED8\_1D00h

Bits	Description
31:0	<p><b>ac_timer_value.</b> Read-write. Reset: FFFF_FFFFh.</p> <p><b>Description:</b> Writing the register to a value other than FFFFFFFFh will start the AC timer:  Reading this register returns the current value of AC timer.  When AC or DC Timer generate wake up event, this register will be reset to FFFFFFFFh by hardware.  FFFFFFFh: Disable AC timer.  FFFFFFFEh ~ 00000001h: The value indicates the number of seconds between the time when the AC timer is programmed and the time when it expires.  00000000h: The AC timer will wake up the system instantly.</p>

#### ACDCx00000004 (FCH::TMR::ACDC::AC\_EXPIRED\_TIMER\_POLICY)

Read-write. Reset: FFFF\_FFFFh.

\_aliasHOSTLEGACY; ACDCx00000004; ACDC=FED8\_1D00h

Bits	Description
31:0	<p><b>ac_expired_timer_policy.</b> Read-write. Reset: FFFF_FFFFh.</p> <p><b>Description:</b> If AC timer expired when current power source is DC, the wake signal won't be asserted. If the power source is switched back to AC when the AC timer is already expired, we will wait for the number of seconds defined in this register and then wake up the system.  When AC or DC Timer generate wake up event, this register will be reset to FFFFFFFFh by hardware.  FFFFFFFh: Disable AC expired timer policy.  FFFFFFFEh ~ 00000001h: The value indicates the number of seconds between the time when the power is switched to AC and the time when it generates the wake-up event.  00000000h: The expired AC timer will wake up the system instantly once the power source is switched to AC.</p>

#### ACDCx00000008 (FCH::TMR::ACDC::AC\_TIMER\_STATUS)

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; ACDCx00000008; ACDC=FED8\_1D00h

Bits	Description
31:2	Reserved.
1	<p><b>ac_timer_wakeup.</b> Read-write. Reset: 0.</p> <p><b>Description:</b> 1: Wake-up was caused by AC timer expiration  0: Wake-up was not caused by AC timer expiration  Write 1 clear</p>
0	<p><b>ac_timer_expired.</b> Read-write. Reset: 0.</p> <p><b>Description:</b> 1: AC timer expired  0: AC timer not expired  Write 1 clear</p>

**ACDCx00000010 (FCH::TMR::ACDC::DC\_TIMER\_VALUE)**

Read-write. Reset: FFFF\_FFFFh.

\_aliasHOSTLEGACY; ACDCx00000010; ACDC=FED8\_1D00h

Bits	Description
31:0	<p><b>dc_timer_value.</b> Read-write. Reset: FFFF_FFFFh.</p> <p><b>Description:</b> Writing the register to a value other than FFFFFFFFh will start the DC timer: Reading this register returns the current value of DC timer. When AC or DC Timer generate wake up event, this register will be reset to FFFFFFFFh by hardware. FFFFFFFFh: Disable DC timer. FFFFFFFFEh ~ 00000001h: The value indicates the number of seconds between the time when the DC timer is programmed and the time when it expires. 00000000h: The DC timer will wake up the system instantly.</p>

**ACDCx00000014 (FCH::TMR::ACDC::DC\_EXPIRED\_TIMER\_POLICY)**

Read-write. Reset: FFFF\_FFFFh.

\_aliasHOSTLEGACY; ACDCx00000014; ACDC=FED8\_1D00h

Bits	Description
31:0	<p><b>dc_expired_timer_policy.</b> Read-write. Reset: FFFF_FFFFh.</p> <p><b>Description:</b> If DC timer expired when current power source is AC, the wake signal won't be asserted. If the power source is switched back to DC when the DC timer is already expired, we will wait for the number of seconds defined in this register and then wake up the system. When AC or DC Timer generate wake up event, this register will be reset to FFFFFFFFh by hardware. FFFFFFFFh: Disable DC expired timer policy. FFFFFFFFEh ~ 00000001h: The value indicates the number of seconds between the time when the power is switched to DC and the time when it generates the wake-up event. 00000000h: The expired DC timer will wake up the system instantly once the power source is switched to DC.</p>

**ACDCx00000018 (FCH::TMR::ACDC::DC\_TIMER\_STATUS)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; ACDCx00000018; ACDC=FED8\_1D00h

Bits	Description
31:2	Reserved.
1	<p><b>dc_timer_wakeup.</b> Read-write. Reset: 0.</p> <p><b>Description:</b> 1: Wake-up was caused by DC timer expiration 0: Wake-up was not caused by DC timer expiration Write 1 clear</p>
0	<p><b>dc_timer_expired.</b> Read-write. Reset: 0.</p> <p><b>Description:</b> 1: DC timer expired 0: DC timer not expired Write 1 clear</p>

**ACDCx00000020 (FCH::TMR::ACDC::ACDCTIMER\_CTRL)**

Read-write. Reset: 0000\_1000h.

\_aliasHOSTLEGACY; ACDCx00000020; ACDC=FED8\_1D00h

Bits	Description
31:13	Reserved.
12	<b>no_event_in_g0</b> . Read-write. Reset: 1. Debug purpose. Please don't change it.
11:10	<b>sel_wake_rst_1_0</b> . Read-write. Reset: 0h. Debug purpose. Please don't change it.
9	<b>dc_timer_event_en</b> . Read-write. Reset: 0. <b>Description:</b> 1: Disable AC Timer to wake up system 0: Disable
8	<b>ac_timer_event_en</b> . Read-write. Reset: 0. <b>Description:</b> 1: Enable AC Timer to wake up system 0: Disable
7:1	Reserved.
0	<b>busy</b> . Read-write. Reset: 0. <b>Description:</b> Read only. Right after AC_TIMER_VALUE or DC_TIMER_VALUE is programmed, the hardware will set Busy bit to 1. The hardware will clear Busy bit once the programming is done and the corresponding timer is started properly. Before the software write the AC_TIMER_VALUE or DC_TIMER_VALUE registers, it has to read the Busy bit and make sure it is 0, otherwise, the hardware will just ignore the programming action from software. For the registers other than AC_TIMER_VALUE and DC_TIMER_VALUE, there is no such limitation.

**11.3.7 Always On Always Connected (AOAC) Registers***Table 190: FCH Device D3 control/status mapping*

Controller Block	<a href="#">FCH</a> Power Group	D3 Control Register	D3 Status Register	ClkOk (From block to ACPI)	AOACtrl (From ACPI to block)
Clk Gen	PG1	DevCtrl 0	DevSts 0	Tied high	Connected PllRstB and PllLock
AB	PG1	DevCtrl 1	DevSts 1	Tied high	Connected
ACPI S0 (fch_acpismbus)	PG1	DevCtrl 2	DevSts 2	Tied high	Connected
ACPI S5 (fch_acpi_s5)	S5	DevCtrl 3	DevSts 3	Tied high	Not used
I2C0	PG1a	DevCtrl 5	DevSts 5	Tied high	Connected
I2C1	PG2	DevCtrl 6	DevSts 6	Tied high	Connected
I2C2	PG2	DevCtrl 7	DevSts 7	Tied high	Connected
I2C3	PG2	DevCtrl 8	DevSts 8	Tied high	Connected
I2C4	PG2	DevCtrl 9	DevSts 9	Tied high	Connected
I2C5	PG2	DevCtrl 10	DevSts 10	Tied high	Connected
UART0	PG2	DevCtrl 11	DevSts 11	Tied high	Connected
UART1	PG2	DevCtrl 12	DevSts 12	Tied high	Connected
I3C1	PG2	DevCtrl 13	DevSts 13	Tied high	Connected
I3C2	PG2	DevCtrl 14	DevSts 14	Tied high	Connected
I3C3	PG2	DevCtrl 15	DevSts 15	Tied high	Connected
UART2	PG2	DevCtrl 16	DevSts 16	Tied high	Connected
AMBA	PG1	DevCtrl 17	DevSts 17	Tied high	Connected
UART4	PG2	DevCtrl 20	DevSts 20	Tied high	Connected

I3C0	PG1a	DevCtrl 21	DevSts 21	Tied high	Connected
eSPI1	PG1	DevCtrl 22	DevSts 22	Tied high	Connected
UART3	PG2	DevCtrl 26	DevSts 26	Tied high	Connected
eSPI0	PG1	DevCtrl 27	DevSts 27	Tied high	Connected
CPU	PG1	DevCtrl 31	DevSts 31	Connected	FCH pin name FCH_SOC_RESETn and FCH_SOC_PWROK

**AOACx00000000 (FCH::AOAC::PERFMON\_CONTROL)**

Read-write. Reset: 0000\_0000h.

**NOTE 1:**

Each block's busy signal has a traffic counter. The traffic counter keeps track of the amount of traffic in a specified timer interval. Each time interval consists of 65280 time slots. We can change the length of the time slot and time interval by changing the MonPeriodSel[1:0] register. If the busy signal from a block has asserted during a time slot, the counter will increase by 1 no matter how long the busy signal was during that time slot. At the end of the time interval, the counter value will be scaled by a weight and updated to the output of the traffic counter.

Each block has a traffic counter and software can read the weighted counter values of each block (TrafficCount\_00 ~ 07). Hardware also provides a sum of those weighted counter values through register TrafficCount\_All.

\_aliasHOSTLEGACY; AOACx00000000; AOAC=FED8\_1E00h

Bits	Description
31:30	Reserved.
29	<b>trafficsts.</b> Read-write. Reset: 0. <b>Description:</b> Write-1-clear 1: There are less (TrafficLess=1) or more (TrafficLess=0) traffic than the threshold defined in BusyTimeThreshold. 0: There are more (TrafficLess=1) or less (TrafficLess=0) traffic than the threshold defined in BusyTimeThreshold.
28	<b>intrsts.</b> Read-write. Reset: 0. <b>Description:</b> Write-1-clear 1: There are less (IntrLess=1) or more (IntrLess=0) traffic than the threshold defined in IntrTimeThreshold. 0: There are more (IntrLess=1) or less (IntrLess=0) traffic than the threshold defined in IntrTimeThreshold.
27	<b>cnt1source.</b> Read-write. Reset: 0. <b>Description:</b> 1: Assign traffic_cnt01 to Sata traffic. 0: Assign traffic_cnt01 to Sata Port 1 active (not in partial/slumber).
26	<b>cnt0source.</b> Read-write. Reset: 0. <b>Description:</b> 1: Assign traffic_cnt00 to "AnyBusy". 0: Assign traffic_cnt00 to Sata Port 0 active (not in partial/slumber). (See NOTE 2)
25	<b>checkinterrupt.</b> Read-write. Reset: 0. Enable interrupt counter (IntrCount)
24	<b>checkc3.</b> Read-write. Reset: 0. <b>Description:</b> 1: Check C3 state when counting "AnyBusy" in traffic_cnt00. 0: Don't check C3. (See NOTE 2)
23:8	Reserved.
7:6	<b>monperiodsel_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Time slot = 15 ns Time interval = 979.2 us 01: Time slot = 240 ns Time interval = 15.667 ms 10: Time slot = 1.92 us Time interval = 125.34 ms 11: Time slot = 15.36 us Time interval = 1 s (See NOTE 1)
5	Reserved.
4	<b>intrless.</b> Read-write. Reset: 0. <b>Description:</b> 1: Generate interrupt status (IntrSts) when there is less interrupt than the specified threshold (IntrTimeThreshold) 0: Generate interrupt status (IntrSts) when there is more traffic than the specified threshold (IntrTimeThreshold)
3	<b>trafficless.</b> Read-write. Reset: 0. <b>Description:</b> 1: Generate traffic status (TrafficSts) when there is less traffic than the specified threshold (BusyTimeThreshold) 0: Generate traffic status (TrafficSts) when there is more traffic than the specified threshold (BusyTimeThreshold)

2	<b>interruptscien.</b> Read-write. Reset: 0. <b>Description:</b> 1: Generate SCI when there is interrupt status (IntrSts) 0: Disable
1	<b>trafficscien.</b> Read-write. Reset: 0. <b>Description:</b> 1: Generate SCI when there is traffic status (TrafficSts) 0: Disable
0	<b>perfmoneenable.</b> Read-write. Reset: 0. Global enable of Performance Monitor

**AOACx00000004 (FCH::AOAC::PERFMON\_TIME\_LIMIT)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; AOACx00000004; AOAC=FED8\_1E00h

Bits	Description
31:16	<b>intrtimethreshold.</b> Read-write. Reset: 0000h. Specify the counter threshold for generating Interrupt SCI.
15:0	<b>busytimethreshold.</b> Read-write. Reset: 0000h. Specify the counter threshold for generating Traffic SCI.

**AOACx00000008 (FCH::AOAC::PERFMON\_WEIGHT\_3\_2\_1\_0)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; AOACx00000008; AOAC=FED8\_1E00h

Bits	Description
31:0	Reserved.

**AOACx0000000C (FCH::AOAC::PERFMON\_WEIGHT\_7\_6\_5\_4)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; AOACx0000000C; AOAC=FED8\_1E00h

Bits	Description
31:0	Reserved.

**AOACx00000010 (FCH::AOAC::PERFMON\_TRAF\_CNT\_1\_0)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; AOACx00000010; AOAC=FED8\_1E00h

Bits	Description
31:0	Reserved.

**AOACx00000014 (FCH::AOAC::PERFMON\_TRAF\_CNT\_3\_2)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; AOACx00000014; AOAC=FED8\_1E00h

Bits	Description
31:0	Reserved.

**AOACx00000018 (FCH::AOAC::PERFMON\_TRAF\_CNT\_5\_4)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; AOACx00000018; AOAC=FED8\_1E00h

Bits	Description
31:0	Reserved.

**AOACx0000001C (FCH::AOAC::PERFMON\_TRAF\_CNT\_7\_6)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; AOACx0000001C; AOAC=FED8\_1E00h

Bits	Description
31:0	Reserved.



**AOACx00000020 (FCH::AOAC::PERFMON\_TRAF\_CNT\_ALL)**

Read-only. Reset: 0000\_0000h.

TrafficCount\_All[26:0] = Internal-Weighted-Count00 [23:0] + + Internal-Weighted-Count07 [23:0]

\_aliasHOSTLEGACY; AOACx00000020; AOAC=FED8\_1E00h

Bits	Description
31:27	Reserved.
26:0	<b>trafficcount_all_26_0</b> . Read-only. Reset: 000_0000h. Sum of weighted counts from each traffic_cntXX blocks.

**AOACx00000024 (FCH::AOAC::PERFMON\_INTR\_CNT)**

Read-only. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; AOACx00000024; AOAC=FED8\_1E00h

Bits	Description
31:24	<b>swbusy</b> . Read-only. Reset: 00h.
23:16	<b>swbusyen</b> . Read-only. Reset: 00h.
15:0	<b>intrcount_15_0</b> . Read-only. Reset: 0000h.

**AOACx00000030 (FCH::AOAC::ALTHPET\_TIMER\_L)**

Read-only.

Register 30h and 34hare read-only. It shows the current time with higher resolution than traditional RTC timer. AltMmTimer field shows the time with 64kHz resolution. It will wrap around at every second.

\_aliasHOSTLEGACY; AOACx00000030; AOAC=FED8\_1E00h

Bits	Description
31:24	<b>minute_7_0</b> . Read-only. Reset: XXXXXXXXXb. Minute field of the ALTHPET_TIMER
23:16	<b>second_7_0</b> . Read-only. Reset: XXXXXXXXXb. Second field of the ALTHPET_TIMER
15:0	<b>altmmtimer</b> . Read-only. Reset: XXXXXXXXXXXXXXXXXb. AltMmTimer field of the ALTHPET_TIMER

**AOACx00000034 (FCH::AOAC::ALTHPET\_TIMER\_H)**

Read-only.

\_aliasHOSTLEGACY; AOACx00000034; AOAC=FED8\_1E00h

Bits	Description
31:24	<b>year_7_0</b> . Read-only. Reset: XXXXXXXXXb. Year field of the ALTHPET_TIMER
23:16	<b>month_7_0</b> . Read-only. Reset: XXXXXXXXXb. Month field of the ALTHPET_TIMER
15:8	<b>day_7_0</b> . Read-only. Reset: XXXXXXXXXb. Day field of the ALTHPET_TIMER
7:0	<b>hour_7_0</b> . Read-only. Reset: XXXXXXXXXb. Hour field of the ALTHPET_TIMER

**AOACx00000038 (FCH::AOAC::ALTHPET\_ALARM\_L)**

Read-write. Reset: 0000\_0000h.

AltMmTimer can be programmed to trigger [SMI](#) (Event 43).

Whenever ALTHPET\_TIMER (L and H) matches the value defined in ALTHPET\_ALARM (L and H), we will generate a pulse on AltMmTimerSts (Event 43).

\_aliasHOSTLEGACY; AOACx00000038; AOAC=FED8\_1E00h

Bits	Description
31	Reserved.
30:24	<b>minute_alarm_6_0</b> . Read-write. Reset: 00h. Minute field of the ALTHPET_ALARM
23	Reserved.
22:16	<b>second_alarm_6_0</b> . Read-write. Reset: 00h. Second field of the ALTHPET_ALARM
15:0	<b>altmmtimer_alarm</b> . Read-write. Reset: 0000h. AltMmTimer field of the ALTHPET_ALARM

**AOACx0000003C (FCH::AOAC::ALTHPET\_ALARM\_H)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; AOACx0000003C; AOAC=FED8\_1E00h

Bits	Description
31:24	<b>year_alarm_7_0.</b> Read-write. Reset: 00h. Year field of the ALTHPET_ALARM
23:21	Reserved.
20:16	<b>month_alarm_4_0.</b> Read-write. Reset: 00h. Month field of the ALTHPET_ALARM
15:14	Reserved.
13:8	<b>day_alarm_5_0.</b> Read-write. Reset: 00h. Day field of the ALTHPET_ALARM
7:6	Reserved.
5:0	<b>hour_alarm_5_0.</b> Read-write. Reset: 00h. Hour field of the ALTHPET_ALARM

**AOACx00000040 (FCH::AOAC::DEVCTRL\_0)**

Read-write. Reset: 7Dh.

\_aliasHOSTLEGACY; AOACx00000040; AOAC=FED8\_1E00h

Bits	Description
7	<b>isswcontrol.</b> Read-write. Reset: 0. <b>Description:</b> 1: Sw controls control signals (PwrRstB, RefClkOk, RstB) to the device. 0: Hw controls control signals (PwrRstB, RefClkOk, RstB) to the device. To avoid glitch on the reset signals, SW must set IsSwControl bit first and then program SwPwrOnRstB, SwRefClkOk and SwRstB.
6	<b>swrstb.</b> Read-write. Reset: 1. <b>Description:</b> 0: RstB is asserted to the device if IsSwControl is set to 1. 1: RstB is de-asserted to the device if IsSwControl is set to 1.
5	<b>swrefclkok.</b> Read-write. Reset: 1. <b>Description:</b> 0: RefClkOk is de-asserted to the device if IsSwControl is set to 1. 1: RefClkOk is asserted to the device if IsSwControl is set to 1.
4	<b>swpwrnrstb.</b> Read-write. Reset: 1. <b>Description:</b> 0: PwrRstB is asserted to the device if IsSwControl is set to 1. 1: PwrRstB is de-asserted to the device if IsSwControl is set to 1.
3	<b>pwronddev.</b> Read-write. Reset: 1. <b>Description:</b> If SwControl is set to 0, SW can write this bit to trigger a HW controlled reset sequence to the device. 0: put device in reset state. 1: put device out of reset state.
2	<b>devicestate.</b> Read-write. Reset: 1. <b>Description:</b> SW records the device power state in this field. 0: device power is removed 1: device power is applied
1:0	<b>targeteddevicestate.</b> Read-write. Reset: 1h. <b>Description:</b> SW records D-State of the device in this field. 00: D0 UnInitialized 01: D0 Initialized 10: D1/D2/D3 Hot 11: D3 Cold

**AOACx00000041 (FCH::AOAC::DEVSTS\_0)**

Read-only. Reset: 27h.

\_aliasHOSTLEGACY; AOACx00000041; AOAC=FED8\_1E00h

Bits	Description
7	<b>stat1</b> . Read-only. Reset: 0. State of device.
6	<b>stat0</b> . Read-only. Reset: 0. State of device.
5	<b>clkok_state</b> . Read-only. Reset: 1. State of device's ClkOk signal.
4	<b>d3cold</b> . Read-only. Reset: 0. State of device's D3Cold signal.
3	<b>devoffgating_state</b> . Read-only. Reset: 0. State of device's DevOffGating signal.
2	<b>rstb_state</b> . Read-only. Reset: 1. State of device's RstB signal.
1	<b>refclkok_state</b> . Read-only. Reset: 1. State of device's RefClkOk signal.
0	<b>pwrrstb_state</b> . Read-only. Reset: 1. State of device's PwrRstB signal.

**AOACx00000042 (FCH::AOAC::DEVCTRL\_1)**

Read-write. Reset: 7Dh.

\_aliasHOSTLEGACY; AOACx00000042; AOAC=FED8\_1E00h

Bits	Description
7	<b>isswcontrol</b> . Read-write. Reset: 0. <b>Description:</b> 1: Sw controls control signals (PwrRstB, RefClkOk, RstB) to the device. 0: Hw controls control signals (PwrRstB, RefClkOk, RstB) to the device. To avoid glitch on the reset signals, SW must set IsSwControl bit first and then program SwPwrOnRstB, SwRefClkOk and SwRstB.
6	<b>swrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: RstB is asserted to the device if IsSwControl is set to 1. 1: RstB is de-asserted to the device if IsSwControl is set to 1.
5	<b>swrefclkok</b> . Read-write. Reset: 1. <b>Description:</b> 0: RefClkOk is de-asserted to the device if IsSwControl is set to 1. 1: RefClkOk is asserted to the device if IsSwControl is set to 1.
4	<b>swpwrnrrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: PwrRstB is asserted to the device if IsSwControl is set to 1. 1: PwrRstB is de-asserted to the device if IsSwControl is set to 1.
3	<b>pwronddev</b> . Read-write. Reset: 1. <b>Description:</b> If SwControl is set to 0, SW can write this bit to trigger a HW controlled reset sequence to the device. 0: put device in reset state. 1: put device out of reset state.
2	<b>devicestate</b> . Read-write. Reset: 1. <b>Description:</b> SW records the device power state in this field. 0: device power is removed 1: device power is applied
1:0	<b>targeteddevicestate</b> . Read-write. Reset: 1h. <b>Description:</b> SW records D-State of the device in this field. 00: D0 UnInitialized 01: D0 Initialized 10: D1/D2/D3 Hot 11: D3 Cold

**AOACx00000043 (FCH::AOAC::DEVSTS\_1)**

Read-only. Reset: 27h.

\_aliasHOSTLEGACY; AOACx00000043; AOAC=FED8\_1E00h

Bits	Description
7	<b>stat1</b> . Read-only. Reset: 0. State of device.
6	<b>stat0</b> . Read-only. Reset: 0. State of device.
5	<b>clkok_state</b> . Read-only. Reset: 1. State of device's ClkOk signal.
4	<b>d3cold</b> . Read-only. Reset: 0. State of device's D3Cold signal.
3	<b>devoffgating_state</b> . Read-only. Reset: 0. State of device's DevOffGating signal.
2	<b>rstb_state</b> . Read-only. Reset: 1. State of device's RstB signal.
1	<b>refclkok_state</b> . Read-only. Reset: 1. State of device's RefClkOk signal.
0	<b>pwr_rstb_state</b> . Read-only. Reset: 1. State of device's PwrRstB signal.

**AOACx00000044 (FCH::AOAC::DEVCTRL\_2)**

Read-write. Reset: 7Dh.

\_aliasHOSTLEGACY; AOACx00000044; AOAC=FED8\_1E00h

Bits	Description
7	<b>isswcontrol</b> . Read-write. Reset: 0. <b>Description:</b> 1: Sw controls control signals (PwrRstB, RefClkOk, RstB) to the device. 0: Hw controls control signals (PwrRstB, RefClkOk, RstB) to the device. To avoid glitch on the reset signals, SW must set IsSwControl bit first and then program SwPwrOnRstB, SwRefClkOk and SwRstB.
6	<b>swrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: RstB is asserted to the device if IsSwControl is set to 1. 1: RstB is de-asserted to the device if IsSwControl is set to 1.
5	<b>swrefclkok</b> . Read-write. Reset: 1. <b>Description:</b> 0: RefClkOk is de-asserted to the device if IsSwControl is set to 1. 1: RefClkOk is asserted to the device if IsSwControl is set to 1.
4	<b>swpwrn_rstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: PwrRstB is asserted to the device if IsSwControl is set to 1. 1: PwrRstB is de-asserted to the device if IsSwControl is set to 1.
3	<b>pwrndev</b> . Read-write. Reset: 1. <b>Description:</b> If SwControl is set to 0, SW can write this bit to trigger a HW controlled reset sequence to the device. 0: put device in reset state. 1: put device out of reset state.
2	<b>devicestate</b> . Read-write. Reset: 1. <b>Description:</b> SW records the device power state in this field. 0: device power is removed 1: device power is applied
1:0	<b>targeteddevicestate</b> . Read-write. Reset: 1h. <b>Description:</b> SW records D-State of the device in this field. 00: D0 UnInitialized 01: D0 Initialized 10: D1/D2/D3 Hot 11: D3 Cold

**AOACx00000045 (FCH::AOAC::DEVSTS\_2)**

Read-only. Reset: 27h.

\_aliasHOSTLEGACY; AOACx00000045; AOAC=FED8\_1E00h

Bits	Description
7	<b>stat1</b> . Read-only. Reset: 0. State of device.
6	<b>stat0</b> . Read-only. Reset: 0. State of device.
5	<b>clkok_state</b> . Read-only. Reset: 1. State of device's ClkOk signal.
4	<b>d3cold</b> . Read-only. Reset: 0. State of device's D3Cold signal.
3	<b>devoffgating_state</b> . Read-only. Reset: 0. State of device's DevOffGating signal.
2	<b>rstb_state</b> . Read-only. Reset: 1. State of device's RstB signal.
1	<b>refclkok_state</b> . Read-only. Reset: 1. State of device's RefClkOk signal.
0	<b>pwrrstb_state</b> . Read-only. Reset: 1. State of device's PwrRstB signal.

**AOACx00000046 (FCH::AOAC::DEVCTRL\_3)**

Read-write. Reset: 7Dh.

\_aliasHOSTLEGACY; AOACx00000046; AOAC=FED8\_1E00h

Bits	Description
7	<b>isswcontrol</b> . Read-write. Reset: 0. <b>Description:</b> 1: Sw controls control signals (PwrRstB, RefClkOk, RstB) to the device. 0: Hw controls control signals (PwrRstB, RefClkOk, RstB) to the device. To avoid glitch on the reset signals, SW must set IsSwControl bit first and then program SwPwrOnRstB, SwRefClkOk and SwRstB.
6	<b>swrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: RstB is asserted to the device if IsSwControl is set to 1. 1: RstB is de-asserted to the device if IsSwControl is set to 1.
5	<b>swrefclkok</b> . Read-write. Reset: 1. <b>Description:</b> 0: RefClkOk is de-asserted to the device if IsSwControl is set to 1. 1: RefClkOk is asserted to the device if IsSwControl is set to 1.
4	<b>swpwrnrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: PwrRstB is asserted to the device if IsSwControl is set to 1. 1: PwrRstB is de-asserted to the device if IsSwControl is set to 1.
3	<b>pwronddev</b> . Read-write. Reset: 1. <b>Description:</b> If SwControl is set to 0, SW can write this bit to trigger a HW controlled reset sequence to the device. 0: put device in reset state. 1: put device out of reset state.
2	<b>devicestate</b> . Read-write. Reset: 1. <b>Description:</b> SW records the device power state in this field. 0: device power is removed 1: device power is applied
1:0	<b>targeteddevicestate</b> . Read-write. Reset: 1h. <b>Description:</b> SW records D-State of the device in this field. 00: D0 UnInitialized 01: D0 Initialized 10: D1/D2/D3 Hot 11: D3 Cold

**AOACx00000047 (FCH::AOAC::DEVSTS\_3)**

Read-only. Reset: 27h.

\_aliasHOSTLEGACY; AOACx00000047; AOAC=FED8\_1E00h

Bits	Description
7	<b>stat1</b> . Read-only. Reset: 0. State of device.
6	<b>stat0</b> . Read-only. Reset: 0. State of device.
5	<b>clkok_state</b> . Read-only. Reset: 1. State of device's ClkOk signal.
4	<b>d3cold</b> . Read-only. Reset: 0. State of device's D3Cold signal.
3	<b>devoffgating_state</b> . Read-only. Reset: 0. State of device's DevOffGating signal.
2	<b>rstb_state</b> . Read-only. Reset: 1. State of device's RstB signal.
1	<b>refclkok_state</b> . Read-only. Reset: 1. State of device's RefClkOk signal.
0	<b>pwrrstb_state</b> . Read-only. Reset: 1. State of device's PwrRstB signal.

**AOACx00000048 (FCH::AOAC::DEVCTRL\_4)**

Read-write. Reset: 7Dh.

\_aliasHOSTLEGACY; AOACx00000048; AOAC=FED8\_1E00h

Bits	Description
7	<b>isswcontrol</b> . Read-write. Reset: 0. <b>Description:</b> 1: Sw controls control signals (PwrRstB, RefClkOk, RstB) to the device. 0: Hw controls control signals (PwrRstB, RefClkOk, RstB) to the device. To avoid glitch on the reset signals, SW must set IsSwControl bit first and then program SwPwrOnRstB, SwRefClkOk and SwRstB.
6	<b>swrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: RstB is asserted to the device if IsSwControl is set to 1. 1: RstB is de-asserted to the device if IsSwControl is set to 1.
5	<b>swrefclkok</b> . Read-write. Reset: 1. <b>Description:</b> 0: RefClkOk is de-asserted to the device if IsSwControl is set to 1. 1: RefClkOk is asserted to the device if IsSwControl is set to 1.
4	<b>swpwrnrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: PwrRstB is asserted to the device if IsSwControl is set to 1. 1: PwrRstB is de-asserted to the device if IsSwControl is set to 1.
3	<b>pwrondev</b> . Read-write. Reset: 1. <b>Description:</b> If SwControl is set to 0, SW can write this bit to trigger a HW controlled reset sequence to the device. 0: put device in reset state. 1: put device out of reset state.
2	<b>devicestate</b> . Read-write. Reset: 1. <b>Description:</b> SW records the device power state in this field. 0: device power is removed 1: device power is applied
1:0	<b>targeteddevicestate</b> . Read-write. Reset: 1h. <b>Description:</b> SW records D-State of the device in this field. 00: D0 UnInitialized 01: D0 Initialized 10: D1/D2/D3 Hot 11: D3 Cold

**AOACx00000049 (FCH::AOAC::DEVSTS\_4)**

Read-only. Reset: 27h.

\_aliasHOSTLEGACY; AOACx00000049; AOAC=FED8\_1E00h

Bits	Description
7	<b>stat1</b> . Read-only. Reset: 0. State of device.
6	<b>stat0</b> . Read-only. Reset: 0. State of device.
5	<b>clkok_state</b> . Read-only. Reset: 1. State of device's ClkOk signal.
4	<b>d3cold</b> . Read-only. Reset: 0. State of device's D3Cold signal.
3	<b>devoffgating_state</b> . Read-only. Reset: 0. State of device's DevOffGating signal.
2	<b>rstb_state</b> . Read-only. Reset: 1. State of device's RstB signal.
1	<b>refclkok_state</b> . Read-only. Reset: 1. State of device's RefClkOk signal.
0	<b>pwr rstb_state</b> . Read-only. Reset: 1. State of device's PwrRstB signal.

**AOACx0000004A (FCH::AOAC::DEVCTRL\_5)**

Read-write. Reset: 7Dh.

\_aliasHOSTLEGACY; AOACx0000004A; AOAC=FED8\_1E00h

Bits	Description
7	<b>isswcontrol</b> . Read-write. Reset: 0. <b>Description:</b> 1: Sw controls control signals (PwrRstB, RefClkOk, RstB) to the device. 0: Hw controls control signals (PwrRstB, RefClkOk, RstB) to the device. To avoid glitch on the reset signals, SW must set IsSwControl bit first and then program SwPwrOnRstB, SwRefClkOk and SwRstB.
6	<b>swrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: RstB is asserted to the device if IsSwControl is set to 1. 1: RstB is de-asserted to the device if IsSwControl is set to 1.
5	<b>swrefclkok</b> . Read-write. Reset: 1. <b>Description:</b> 0: RefClkOk is de-asserted to the device if IsSwControl is set to 1. 1: RefClkOk is asserted to the device if IsSwControl is set to 1.
4	<b>swpwr onrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: PwrRstB is asserted to the device if IsSwControl is set to 1. 1: PwrRstB is de-asserted to the device if IsSwControl is set to 1.
3	<b>pwr ondev</b> . Read-write. Reset: 1. <b>Description:</b> If SwControl is set to 0, SW can write this bit to trigger a HW controlled reset sequence to the device. 0: put device in reset state. 1: put device out of reset state.
2	<b>devicestate</b> . Read-write. Reset: 1. <b>Description:</b> SW records the device power state in this field. 0: device power is removed 1: device power is applied
1:0	<b>targeteddevicestate</b> . Read-write. Reset: 1h. <b>Description:</b> SW records D-State of the device in this field. 00: D0 UnInitialized 01: D0 Initialized 10: D1/D2/D3 Hot 11: D3 Cold

**AOACx0000004B (FCH::AOAC::DEVSTS\_5)**

Read-only. Reset: 27h.

\_aliasHOSTLEGACY; AOACx0000004B; AOAC=FED8\_1E00h

Bits	Description
7	<b>stat1</b> . Read-only. Reset: 0. State of device.
6	<b>stat0</b> . Read-only. Reset: 0. State of device.
5	<b>clkok_state</b> . Read-only. Reset: 1. State of device's ClkOk signal.
4	<b>d3cold</b> . Read-only. Reset: 0. State of device's D3Cold signal.
3	<b>devoffgating_state</b> . Read-only. Reset: 0. State of device's DevOffGating signal.
2	<b>rstb_state</b> . Read-only. Reset: 1. State of device's RstB signal.
1	<b>refclkok_state</b> . Read-only. Reset: 1. State of device's RefClkOk signal.
0	<b>pwr rstb_state</b> . Read-only. Reset: 1. State of device's PwrRstB signal.

**AOACx0000004C (FCH::AOAC::DEVCTRL\_6)**

Read-write. Reset: 7Dh.

\_aliasHOSTLEGACY; AOACx0000004C; AOAC=FED8\_1E00h

Bits	Description
7	<b>isswcontrol</b> . Read-write. Reset: 0. <b>Description:</b> 1: Sw controls control signals (PwrRstB, RefClkOk, RstB) to the device. 0: Hw controls control signals (PwrRstB, RefClkOk, RstB) to the device. To avoid glitch on the reset signals, SW must set IsSwControl bit first and then program SwPwrOnRstB, SwRefClkOk and SwRstB.
6	<b>swrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: RstB is asserted to the device if IsSwControl is set to 1. 1: RstB is de-asserted to the device if IsSwControl is set to 1.
5	<b>swrefclkok</b> . Read-write. Reset: 1. <b>Description:</b> 0: RefClkOk is de-asserted to the device if IsSwControl is set to 1. 1: RefClkOk is asserted to the device if IsSwControl is set to 1.
4	<b>swpwr onrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: PwrRstB is asserted to the device if IsSwControl is set to 1. 1: PwrRstB is de-asserted to the device if IsSwControl is set to 1.
3	<b>pwr ondev</b> . Read-write. Reset: 1. <b>Description:</b> If SwControl is set to 0, SW can write this bit to trigger a HW controlled reset sequence to the device. 0: put device in reset state. 1: put device out of reset state.
2	<b>devicestate</b> . Read-write. Reset: 1. <b>Description:</b> SW records the device power state in this field. 0: device power is removed 1: device power is applied
1:0	<b>targeteddevicestate</b> . Read-write. Reset: 1h. <b>Description:</b> SW records D-State of the device in this field. 00: D0 UnInitialized 01: D0 Initialized 10: D1/D2/D3 Hot 11: D3 Cold



**AOACx0000004D (FCH::AOAC::DEVSTS\_6)**

Read-only. Reset: 27h.

\_aliasHOSTLEGACY; AOACx0000004D; AOAC=FED8\_1E00h

Bits	Description
7	<b>stat1</b> . Read-only. Reset: 0. State of device.
6	<b>stat0</b> . Read-only. Reset: 0. State of device.
5	<b>clkok_state</b> . Read-only. Reset: 1. State of device's ClkOk signal.
4	<b>d3cold</b> . Read-only. Reset: 0. State of device's D3Cold signal.
3	<b>devoffgating_state</b> . Read-only. Reset: 0. State of device's DevOffGating signal.
2	<b>rstb_state</b> . Read-only. Reset: 1. State of device's RstB signal.
1	<b>refclkok_state</b> . Read-only. Reset: 1. State of device's RefClkOk signal.
0	<b>pwrrstb_state</b> . Read-only. Reset: 1. State of device's PwrRstB signal.

**AOACx0000004E (FCH::AOAC::DEVCTRL\_7)**

Read-write. Reset: 7Dh.

\_aliasHOSTLEGACY; AOACx0000004E; AOAC=FED8\_1E00h

Bits	Description
7	<b>isswcontrol</b> . Read-write. Reset: 0. <b>Description:</b> 1: Sw controls control signals (PwrRstB, RefClkOk, RstB) to the device. 0: Hw controls control signals (PwrRstB, RefClkOk, RstB) to the device. To avoid glitch on the reset signals, SW must set IsSwControl bit first and then program SwPwrOnRstB, SwRefClkOk and SwRstB.
6	<b>swrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: RstB is asserted to the device if IsSwControl is set to 1. 1: RstB is de-asserted to the device if IsSwControl is set to 1.
5	<b>swrefclkok</b> . Read-write. Reset: 1. <b>Description:</b> 0: RefClkOk is de-asserted to the device if IsSwControl is set to 1. 1: RefClkOk is asserted to the device if IsSwControl is set to 1.
4	<b>swpwrnrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: PwrRstB is asserted to the device if IsSwControl is set to 1. 1: PwrRstB is de-asserted to the device if IsSwControl is set to 1.
3	<b>pwronddev</b> . Read-write. Reset: 1. <b>Description:</b> If SwControl is set to 0, SW can write this bit to trigger a HW controlled reset sequence to the device. 0: put device in reset state. 1: put device out of reset state.
2	<b>devicestate</b> . Read-write. Reset: 1. <b>Description:</b> SW records the device power state in this field. 0: device power is removed 1: device power is applied
1:0	<b>targeteddevicestate</b> . Read-write. Reset: 1h. <b>Description:</b> SW records D-State of the device in this field. 00: D0 UnInitialized 01: D0 Initialized 10: D1/D2/D3 Hot 11: D3 Cold

**AOACx0000004F (FCH::AOAC::DEVSTS\_7)**

Read-only. Reset: 27h.

\_aliasHOSTLEGACY; AOACx0000004F; AOAC=FED8\_1E00h

Bits	Description
7	<b>stat1</b> . Read-only. Reset: 0. State of device.
6	<b>stat0</b> . Read-only. Reset: 0. State of device.
5	<b>clkok_state</b> . Read-only. Reset: 1. State of device's ClkOk signal.
4	<b>d3cold</b> . Read-only. Reset: 0. State of device's D3Cold signal.
3	<b>devoffgating_state</b> . Read-only. Reset: 0. State of device's DevOffGating signal.
2	<b>rstb_state</b> . Read-only. Reset: 1. State of device's RstB signal.
1	<b>refclkok_state</b> . Read-only. Reset: 1. State of device's RefClkOk signal.
0	<b>pwrrstb_state</b> . Read-only. Reset: 1. State of device's PwrRstB signal.

**AOACx00000050 (FCH::AOAC::DEVCTRL\_8)**

Read-write. Reset: 7Dh.

\_aliasHOSTLEGACY; AOACx00000050; AOAC=FED8\_1E00h

Bits	Description
7	<b>isswcontrol</b> . Read-write. Reset: 0. <b>Description:</b> 1: Sw controls control signals (PwrRstB, RefClkOk, RstB) to the device. 0: Hw controls control signals (PwrRstB, RefClkOk, RstB) to the device. To avoid glitch on the reset signals, SW must set IsSwControl bit first and then program SwPwrOnRstB, SwRefClkOk and SwRstB.
6	<b>swrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: RstB is asserted to the device if IsSwControl is set to 1. 1: RstB is de-asserted to the device if IsSwControl is set to 1.
5	<b>swrefclkok</b> . Read-write. Reset: 1. <b>Description:</b> 0: RefClkOk is de-asserted to the device if IsSwControl is set to 1. 1: RefClkOk is asserted to the device if IsSwControl is set to 1.
4	<b>swpwrnrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: PwrRstB is asserted to the device if IsSwControl is set to 1. 1: PwrRstB is de-asserted to the device if IsSwControl is set to 1.
3	<b>pwronddev</b> . Read-write. Reset: 1. <b>Description:</b> If SwControl is set to 0, SW can write this bit to trigger a HW controlled reset sequence to the device. 0: put device in reset state. 1: put device out of reset state.
2	<b>devicestate</b> . Read-write. Reset: 1. <b>Description:</b> SW records the device power state in this field. 0: device power is removed 1: device power is applied
1:0	<b>targeteddevicestate</b> . Read-write. Reset: 1h. <b>Description:</b> SW records D-State of the device in this field. 00: D0 UnInitialized 01: D0 Initialized 10: D1/D2/D3 Hot 11: D3 Cold

**AOACx00000051 (FCH::AOAC::DEVSTS\_8)**

Read-only. Reset: 27h.

\_aliasHOSTLEGACY; AOACx00000051; AOAC=FED8\_1E00h

Bits	Description
7	<b>stat1</b> . Read-only. Reset: 0. State of device.
6	<b>stat0</b> . Read-only. Reset: 0. State of device.
5	<b>clkok_state</b> . Read-only. Reset: 1. State of device's ClkOk signal.
4	<b>d3cold</b> . Read-only. Reset: 0. State of device's D3Cold signal.
3	<b>devoffgating_state</b> . Read-only. Reset: 0. State of device's DevOffGating signal.
2	<b>rstb_state</b> . Read-only. Reset: 1. State of device's RstB signal.
1	<b>refclkok_state</b> . Read-only. Reset: 1. State of device's RefClkOk signal.
0	<b>pwr_rstb_state</b> . Read-only. Reset: 1. State of device's PwrRstB signal.

**AOACx00000052 (FCH::AOAC::DEVCTRL\_9)**

Read-write. Reset: 7Dh.

\_aliasHOSTLEGACY; AOACx00000052; AOAC=FED8\_1E00h

Bits	Description
7	<b>isswcontrol</b> . Read-write. Reset: 0. <b>Description:</b> 1: Sw controls control signals (PwrRstB, RefClkOk, RstB) to the device. 0: Hw controls control signals (PwrRstB, RefClkOk, RstB) to the device. To avoid glitch on the reset signals, SW must set IsSwControl bit first and then program SwPwrOnRstB, SwRefClkOk and SwRstB.
6	<b>swrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: RstB is asserted to the device if IsSwControl is set to 1. 1: RstB is de-asserted to the device if IsSwControl is set to 1.
5	<b>swrefclkok</b> . Read-write. Reset: 1. <b>Description:</b> 0: RefClkOk is de-asserted to the device if IsSwControl is set to 1. 1: RefClkOk is asserted to the device if IsSwControl is set to 1.
4	<b>swpwr_rstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: PwrRstB is asserted to the device if IsSwControl is set to 1. 1: PwrRstB is de-asserted to the device if IsSwControl is set to 1.
3	<b>pwr_rstb_dev</b> . Read-write. Reset: 1. <b>Description:</b> If SwControl is set to 0, SW can write this bit to trigger a HW controlled reset sequence to the device. 0: put device in reset state. 1: put device out of reset state.
2	<b>devicestate</b> . Read-write. Reset: 1. <b>Description:</b> SW records the device power state in this field. 0: device power is removed 1: device power is applied
1:0	<b>targeteddevicestate</b> . Read-write. Reset: 1h. <b>Description:</b> SW records D-State of the device in this field. 00: D0 UnInitialized 01: D0 Initialized 10: D1/D2/D3 Hot 11: D3 Cold

**AOACx00000053 (FCH::AOAC::DEVSTS\_9)**

Read-only. Reset: 27h.

\_aliasHOSTLEGACY; AOACx00000053; AOAC=FED8\_1E00h

Bits	Description
7	<b>stat1</b> . Read-only. Reset: 0. State of device.
6	<b>stat0</b> . Read-only. Reset: 0. State of device.
5	<b>clkok_state</b> . Read-only. Reset: 1. State of device's ClkOk signal.
4	<b>d3cold</b> . Read-only. Reset: 0. State of device's D3Cold signal.
3	<b>devoffgating_state</b> . Read-only. Reset: 0. State of device's DevOffGating signal.
2	<b>rstb_state</b> . Read-only. Reset: 1. State of device's RstB signal.
1	<b>refclkok_state</b> . Read-only. Reset: 1. State of device's RefClkOk signal.
0	<b>pwrrstb_state</b> . Read-only. Reset: 1. State of device's PwrRstB signal.

**AOACx00000054 (FCH::AOAC::DEVCTRL\_10)**

Read-write. Reset: 7Dh.

\_aliasHOSTLEGACY; AOACx00000054; AOAC=FED8\_1E00h

Bits	Description
7	<b>isswcontrol</b> . Read-write. Reset: 0. <b>Description:</b> 1: Sw controls control signals (PwrRstB, RefClkOk, RstB) to the device. 0: Hw controls control signals (PwrRstB, RefClkOk, RstB) to the device. To avoid glitch on the reset signals, SW must set IsSwControl bit first and then program SwPwrOnRstB, SwRefClkOk and SwRstB.
6	<b>swrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: RstB is asserted to the device if IsSwControl is set to 1. 1: RstB is de-asserted to the device if IsSwControl is set to 1.
5	<b>swrefclkok</b> . Read-write. Reset: 1. <b>Description:</b> 0: RefClkOk is de-asserted to the device if IsSwControl is set to 1. 1: RefClkOk is asserted to the device if IsSwControl is set to 1.
4	<b>swpwrnrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: PwrRstB is asserted to the device if IsSwControl is set to 1. 1: PwrRstB is de-asserted to the device if IsSwControl is set to 1.
3	<b>pwronddev</b> . Read-write. Reset: 1. <b>Description:</b> If SwControl is set to 0, SW can write this bit to trigger a HW controlled reset sequence to the device. 0: put device in reset state. 1: put device out of reset state.
2	<b>devicestate</b> . Read-write. Reset: 1. <b>Description:</b> SW records the device power state in this field. 0: device power is removed 1: device power is applied
1:0	<b>targeteddevicestate</b> . Read-write. Reset: 1h. <b>Description:</b> SW records D-State of the device in this field. 00: D0 UnInitialized 01: D0 Initialized 10: D1/D2/D3 Hot 11: D3 Cold

**AOACx00000055 (FCH::AOAC::DEVSTS\_10)**

Read-only. Reset: 27h.

\_aliasHOSTLEGACY; AOACx00000055; AOAC=FED8\_1E00h

Bits	Description
7	<b>stat1</b> . Read-only. Reset: 0. State of device.
6	<b>stat0</b> . Read-only. Reset: 0. State of device.
5	<b>clkok_state</b> . Read-only. Reset: 1. State of device's ClkOk signal.
4	<b>d3cold</b> . Read-only. Reset: 0. State of device's D3Cold signal.
3	<b>devoffgating_state</b> . Read-only. Reset: 0. State of device's DevOffGating signal.
2	<b>rstb_state</b> . Read-only. Reset: 1. State of device's RstB signal.
1	<b>refclkok_state</b> . Read-only. Reset: 1. State of device's RefClkOk signal.
0	<b>pwr_rstb_state</b> . Read-only. Reset: 1. State of device's PwrRstB signal.

**AOACx00000056 (FCH::AOAC::DEVCTRL\_11)**

Read-write. Reset: 7Dh.

\_aliasHOSTLEGACY; AOACx00000056; AOAC=FED8\_1E00h

Bits	Description
7	<b>isswcontrol</b> . Read-write. Reset: 0. <b>Description:</b> 1: Sw controls control signals (PwrRstB, RefClkOk, RstB) to the device. 0: Hw controls control signals (PwrRstB, RefClkOk, RstB) to the device. To avoid glitch on the reset signals, SW must set IsSwControl bit first and then program SwPwrOnRstB, SwRefClkOk and SwRstB.
6	<b>swrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: RstB is asserted to the device if IsSwControl is set to 1. 1: RstB is de-asserted to the device if IsSwControl is set to 1.
5	<b>swrefclkok</b> . Read-write. Reset: 1. <b>Description:</b> 0: RefClkOk is de-asserted to the device if IsSwControl is set to 1. 1: RefClkOk is asserted to the device if IsSwControl is set to 1.
4	<b>swpwrnrrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: PwrRstB is asserted to the device if IsSwControl is set to 1. 1: PwrRstB is de-asserted to the device if IsSwControl is set to 1.
3	<b>pwronddev</b> . Read-write. Reset: 1. <b>Description:</b> If SwControl is set to 0, SW can write this bit to trigger a HW controlled reset sequence to the device. 0: put device in reset state. 1: put device out of reset state.
2	<b>devicestate</b> . Read-write. Reset: 1. <b>Description:</b> SW records the device power state in this field. 0: device power is removed 1: device power is applied
1:0	<b>targeteddevicestate</b> . Read-write. Reset: 1h. <b>Description:</b> SW records D-State of the device in this field. 00: D0 UnInitialized 01: D0 Initialized 10: D1/D2/D3 Hot 11: D3 Cold

**AOACx00000057 (FCH::AOAC::DEVSTS\_11)**

Read-only. Reset: 27h.

\_aliasHOSTLEGACY; AOACx00000057; AOAC=FED8\_1E00h

Bits	Description
7	<b>stat1</b> . Read-only. Reset: 0. State of device.
6	<b>stat0</b> . Read-only. Reset: 0. State of device.
5	<b>clkok_state</b> . Read-only. Reset: 1. State of device's ClkOk signal.
4	<b>d3cold</b> . Read-only. Reset: 0. State of device's D3Cold signal.
3	<b>devoffgating_state</b> . Read-only. Reset: 0. State of device's DevOffGating signal.
2	<b>rstb_state</b> . Read-only. Reset: 1. State of device's RstB signal.
1	<b>refclkok_state</b> . Read-only. Reset: 1. State of device's RefClkOk signal.
0	<b>pwrrstb_state</b> . Read-only. Reset: 1. State of device's PwrRstB signal.

**AOACx00000058 (FCH::AOAC::DEVCTRL\_12)**

Read-write. Reset: 7Dh.

\_aliasHOSTLEGACY; AOACx00000058; AOAC=FED8\_1E00h

Bits	Description
7	<b>isswcontrol</b> . Read-write. Reset: 0. <b>Description:</b> 1: Sw controls control signals (PwrRstB, RefClkOk, RstB) to the device. 0: Hw controls control signals (PwrRstB, RefClkOk, RstB) to the device. To avoid glitch on the reset signals, SW must set IsSwControl bit first and then program SwPwrOnRstB, SwRefClkOk and SwRstB.
6	<b>swrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: RstB is asserted to the device if IsSwControl is set to 1. 1: RstB is de-asserted to the device if IsSwControl is set to 1.
5	<b>swrefclkok</b> . Read-write. Reset: 1. <b>Description:</b> 0: RefClkOk is de-asserted to the device if IsSwControl is set to 1. 1: RefClkOk is asserted to the device if IsSwControl is set to 1.
4	<b>swpwrnrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: PwrRstB is asserted to the device if IsSwControl is set to 1. 1: PwrRstB is de-asserted to the device if IsSwControl is set to 1.
3	<b>pwronddev</b> . Read-write. Reset: 1. <b>Description:</b> If SwControl is set to 0, SW can write this bit to trigger a HW controlled reset sequence to the device. 0: put device in reset state. 1: put device out of reset state.
2	<b>devicestate</b> . Read-write. Reset: 1. <b>Description:</b> SW records the device power state in this field. 0: device power is removed 1: device power is applied
1:0	<b>targeteddevicestate</b> . Read-write. Reset: 1h. <b>Description:</b> SW records D-State of the device in this field. 00: D0 UnInitialized 01: D0 Initialized 10: D1/D2/D3 Hot 11: D3 Cold

**AOACx00000059 (FCH::AOAC::DEVSTS\_12)**

Read-only. Reset: 27h.

\_aliasHOSTLEGACY; AOACx00000059; AOAC=FED8\_1E00h

Bits	Description
7	<b>stat1</b> . Read-only. Reset: 0. State of device.
6	<b>stat0</b> . Read-only. Reset: 0. State of device.
5	<b>clkok_state</b> . Read-only. Reset: 1. State of device's ClkOk signal.
4	<b>d3cold</b> . Read-only. Reset: 0. State of device's D3Cold signal.
3	<b>devoffgating_state</b> . Read-only. Reset: 0. State of device's DevOffGating signal.
2	<b>rstb_state</b> . Read-only. Reset: 1. State of device's RstB signal.
1	<b>refclkok_state</b> . Read-only. Reset: 1. State of device's RefClkOk signal.
0	<b>pwrrstb_state</b> . Read-only. Reset: 1. State of device's PwrRstB signal.

**AOACx0000005A (FCH::AOAC::DEVCTRL\_13)**

Read-write. Reset: 74h.

\_aliasHOSTLEGACY; AOACx0000005A; AOAC=FED8\_1E00h

Bits	Description
7	<b>isswcontrol</b> . Read-write. Reset: 0. <b>Description:</b> 1: Sw controls control signals (PwrRstB, RefClkOk, RstB) to the device. 0: Hw controls control signals (PwrRstB, RefClkOk, RstB) to the device. To avoid glitch on the reset signals, SW must set IsSwControl bit first and then program SwPwrOnRstB, SwRefClkOk and SwRstB.
6	<b>swrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: RstB is asserted to the device if IsSwControl is set to 1. 1: RstB is de-asserted to the device if IsSwControl is set to 1.
5	<b>swrefclkok</b> . Read-write. Reset: 1. <b>Description:</b> 0: RefClkOk is de-asserted to the device if IsSwControl is set to 1. 1: RefClkOk is asserted to the device if IsSwControl is set to 1.
4	<b>swpwrnrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: PwrRstB is asserted to the device if IsSwControl is set to 1. 1: PwrRstB is de-asserted to the device if IsSwControl is set to 1.
3	<b>pwrondev</b> . Read-write. Reset: 0. <b>Description:</b> If SwControl is set to 0, SW can write this bit to trigger a HW controlled reset sequence to the device. 0: put device in reset state. 1: put device out of reset state.
2	<b>devicestate</b> . Read-write. Reset: 1. <b>Description:</b> SW records the device power state in this field. 0: device power is removed 1: device power is applied
1:0	<b>targeteddevicestate</b> . Read-write. Reset: 0h. <b>Description:</b> SW records D-State of the device in this field. 00: D0 UnInitialized 01: D0 Initialized 10: D1/D2/D3 Hot 11: D3 Cold

**AOACx0000005B (FCH::AOAC::DEVSTS\_13)**

Read-only. Reset: 27h.

\_aliasHOSTLEGACY; AOACx0000005B; AOAC=FED8\_1E00h

Bits	Description
7	<b>stat1</b> . Read-only. Reset: 0. State of device.
6	<b>stat0</b> . Read-only. Reset: 0. State of device.
5	<b>clkok_state</b> . Read-only. Reset: 1. State of device's ClkOk signal.
4	<b>d3cold</b> . Read-only. Reset: 0. State of device's D3Cold signal.
3	<b>devoffgating_state</b> . Read-only. Reset: 0. State of device's DevOffGating signal.
2	<b>rstb_state</b> . Read-only. Reset: 1. State of device's RstB signal.
1	<b>refclkok_state</b> . Read-only. Reset: 1. State of device's RefClkOk signal.
0	<b>pwrrstb_state</b> . Read-only. Reset: 1. State of device's PwrRstB signal.

**AOACx0000005C (FCH::AOAC::DEVCTRL\_14)**

Read-write. Reset: 74h.

\_aliasHOSTLEGACY; AOACx0000005C; AOAC=FED8\_1E00h

Bits	Description
7	<b>isswcontrol</b> . Read-write. Reset: 0. <b>Description:</b> 1: Sw controls control signals (PwrRstB, RefClkOk, RstB) to the device. 0: Hw controls control signals (PwrRstB, RefClkOk, RstB) to the device. To avoid glitch on the reset signals, SW must set IsSwControl bit first and then program SwPwrOnRstB, SwRefClkOk and SwRstB.
6	<b>swrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: RstB is asserted to the device if IsSwControl is set to 1. 1: RstB is de-asserted to the device if IsSwControl is set to 1.
5	<b>swrefclkok</b> . Read-write. Reset: 1. <b>Description:</b> 0: RefClkOk is de-asserted to the device if IsSwControl is set to 1. 1: RefClkOk is asserted to the device if IsSwControl is set to 1.
4	<b>swpwrnrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: PwrRstB is asserted to the device if IsSwControl is set to 1. 1: PwrRstB is de-asserted to the device if IsSwControl is set to 1.
3	<b>pwronddev</b> . Read-write. Reset: 0. <b>Description:</b> If SwControl is set to 0, SW can write this bit to trigger a HW controlled reset sequence to the device. 0: put device in reset state. 1: put device out of reset state.
2	<b>devicestate</b> . Read-write. Reset: 1. <b>Description:</b> SW records the device power state in this field. 0: device power is removed 1: device power is applied
1:0	<b>targeteddevicestate</b> . Read-write. Reset: 0h. <b>Description:</b> SW records D-State of the device in this field. 00: D0 UnInitialized 01: D0 Initialized 10: D1/D2/D3 Hot 11: D3 Cold



**AOACx0000005D (FCH::AOAC::DEVSTS\_14)**

Read-only. Reset: 27h.

\_aliasHOSTLEGACY; AOACx0000005D; AOAC=FED8\_1E00h

Bits	Description
7	<b>stat1</b> . Read-only. Reset: 0. State of device.
6	<b>stat0</b> . Read-only. Reset: 0. State of device.
5	<b>clkok_state</b> . Read-only. Reset: 1. State of device's ClkOk signal.
4	<b>d3cold</b> . Read-only. Reset: 0. State of device's D3Cold signal.
3	<b>devoffgating_state</b> . Read-only. Reset: 0. State of device's DevOffGating signal.
2	<b>rstb_state</b> . Read-only. Reset: 1. State of device's RstB signal.
1	<b>refclkok_state</b> . Read-only. Reset: 1. State of device's RefClkOk signal.
0	<b>pwrrstb_state</b> . Read-only. Reset: 1. State of device's PwrRstB signal.

**AOACx0000005E (FCH::AOAC::DEVCTRL\_15)**

Read-write. Reset: 74h.

\_aliasHOSTLEGACY; AOACx0000005E; AOAC=FED8\_1E00h

Bits	Description
7	<b>isswcontrol</b> . Read-write. Reset: 0. <b>Description:</b> 1: Sw controls control signals (PwrRstB, RefClkOk, RstB) to the device. 0: Hw controls control signals (PwrRstB, RefClkOk, RstB) to the device. To avoid glitch on the reset signals, SW must set IsSwControl bit first and then program SwPwrOnRstB, SwRefClkOk and SwRstB.
6	<b>swrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: RstB is asserted to the device if IsSwControl is set to 1. 1: RstB is de-asserted to the device if IsSwControl is set to 1.
5	<b>swrefclkok</b> . Read-write. Reset: 1. <b>Description:</b> 0: RefClkOk is de-asserted to the device if IsSwControl is set to 1. 1: RefClkOk is asserted to the device if IsSwControl is set to 1.
4	<b>swpwrnrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: PwrRstB is asserted to the device if IsSwControl is set to 1. 1: PwrRstB is de-asserted to the device if IsSwControl is set to 1.
3	<b>pwronddev</b> . Read-write. Reset: 0. <b>Description:</b> If SwControl is set to 0, SW can write this bit to trigger a HW controlled reset sequence to the device. 0: put device in reset state. 1: put device out of reset state.
2	<b>devicestate</b> . Read-write. Reset: 1. <b>Description:</b> SW records the device power state in this field. 0: device power is removed 1: device power is applied
1:0	<b>targeteddevicestate</b> . Read-write. Reset: 0h. <b>Description:</b> SW records D-State of the device in this field. 00: D0 UnInitialized 01: D0 Initialized 10: D1/D2/D3 Hot 11: D3 Cold

**AOACx0000005F (FCH::AOAC::DEVSTS\_15)**

Read-only. Reset: 27h.

\_aliasHOSTLEGACY; AOACx0000005F; AOAC=FED8\_1E00h

Bits	Description
7	<b>stat1</b> . Read-only. Reset: 0. State of device.
6	<b>stat0</b> . Read-only. Reset: 0. State of device.
5	<b>clkok_state</b> . Read-only. Reset: 1. State of device's ClkOk signal.
4	<b>d3cold</b> . Read-only. Reset: 0. State of device's D3Cold signal.
3	<b>devoffgating_state</b> . Read-only. Reset: 0. State of device's DevOffGating signal.
2	<b>rstb_state</b> . Read-only. Reset: 1. State of device's RstB signal.
1	<b>refclkok_state</b> . Read-only. Reset: 1. State of device's RefClkOk signal.
0	<b>pwrrstb_state</b> . Read-only. Reset: 1. State of device's PwrRstB signal.

**AOACx00000060 (FCH::AOAC::DEVCTRL\_16)**

Read-write. Reset: 7Dh.

\_aliasHOSTLEGACY; AOACx00000060; AOAC=FED8\_1E00h

Bits	Description
7	<b>isswcontrol</b> . Read-write. Reset: 0. <b>Description:</b> 1: Sw controls control signals (PwrRstB, RefClkOk, RstB) to the device. 0: Hw controls control signals (PwrRstB, RefClkOk, RstB) to the device. To avoid glitch on the reset signals, SW must set IsSwControl bit first and then program SwPwrOnRstB, SwRefClkOk and SwRstB.
6	<b>swrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: RstB is asserted to the device if IsSwControl is set to 1. 1: RstB is de-asserted to the device if IsSwControl is set to 1.
5	<b>swrefclkok</b> . Read-write. Reset: 1. <b>Description:</b> 0: RefClkOk is de-asserted to the device if IsSwControl is set to 1. 1: RefClkOk is asserted to the device if IsSwControl is set to 1.
4	<b>swpwrnrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: PwrRstB is asserted to the device if IsSwControl is set to 1. 1: PwrRstB is de-asserted to the device if IsSwControl is set to 1.
3	<b>pwronddev</b> . Read-write. Reset: 1. <b>Description:</b> If SwControl is set to 0, SW can write this bit to trigger a HW controlled reset sequence to the device. 0: put device in reset state. 1: put device out of reset state.
2	<b>devicestate</b> . Read-write. Reset: 1. <b>Description:</b> SW records the device power state in this field. 0: device power is removed 1: device power is applied
1:0	<b>targeteddevicestate</b> . Read-write. Reset: 1h. <b>Description:</b> SW records D-State of the device in this field. 00: D0 UnInitialized 01: D0 Initialized 10: D1/D2/D3 Hot 11: D3 Cold

**AOACx00000061 (FCH::AOAC::DEVSTS\_16)**

Read-only. Reset: 27h.

\_aliasHOSTLEGACY; AOACx00000061; AOAC=FED8\_1E00h

Bits	Description
7	<b>stat1</b> . Read-only. Reset: 0. State of device.
6	<b>stat0</b> . Read-only. Reset: 0. State of device.
5	<b>clkok_state</b> . Read-only. Reset: 1. State of device's ClkOk signal.
4	<b>d3cold</b> . Read-only. Reset: 0. State of device's D3Cold signal.
3	<b>devoffgating_state</b> . Read-only. Reset: 0. State of device's DevOffGating signal.
2	<b>rstb_state</b> . Read-only. Reset: 1. State of device's RstB signal.
1	<b>refclkok_state</b> . Read-only. Reset: 1. State of device's RefClkOk signal.
0	<b>pwrrstb_state</b> . Read-only. Reset: 1. State of device's PwrRstB signal.

**AOACx00000062 (FCH::AOAC::DEVCTRL\_17)**

Read-write. Reset: 7Dh.

\_aliasHOSTLEGACY; AOACx00000062; AOAC=FED8\_1E00h

Bits	Description
7	<b>isswcontrol</b> . Read-write. Reset: 0. <b>Description:</b> 1: Sw controls control signals (PwrRstB, RefClkOk, RstB) to the device. 0: Hw controls control signals (PwrRstB, RefClkOk, RstB) to the device. To avoid glitch on the reset signals, SW must set IsSwControl bit first and then program SwPwrOnRstB, SwRefClkOk and SwRstB.
6	<b>swrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: RstB is asserted to the device if IsSwControl is set to 1. 1: RstB is de-asserted to the device if IsSwControl is set to 1.
5	<b>swrefclkok</b> . Read-write. Reset: 1. <b>Description:</b> 0: RefClkOk is de-asserted to the device if IsSwControl is set to 1. 1: RefClkOk is asserted to the device if IsSwControl is set to 1.
4	<b>swpwrnrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: PwrRstB is asserted to the device if IsSwControl is set to 1. 1: PwrRstB is de-asserted to the device if IsSwControl is set to 1.
3	<b>pwronddev</b> . Read-write. Reset: 1. <b>Description:</b> If SwControl is set to 0, SW can write this bit to trigger a HW controlled reset sequence to the device. 0: put device in reset state. 1: put device out of reset state.
2	<b>devicestate</b> . Read-write. Reset: 1. <b>Description:</b> SW records the device power state in this field. 0: device power is removed 1: device power is applied
1:0	<b>targeteddevicestate</b> . Read-write. Reset: 1h. <b>Description:</b> SW records D-State of the device in this field. 00: D0 UnInitialized 01: D0 Initialized 10: D1/D2/D3 Hot 11: D3 Cold

**AOACx00000063 (FCH::AOAC::DEVSTS\_17)**

Read-only. Reset: 27h.

\_aliasHOSTLEGACY; AOACx00000063; AOAC=FED8\_1E00h

Bits	Description
7	<b>stat1</b> . Read-only. Reset: 0. State of device.
6	<b>stat0</b> . Read-only. Reset: 0. State of device.
5	<b>clkok_state</b> . Read-only. Reset: 1. State of device's ClkOk signal.
4	<b>d3cold</b> . Read-only. Reset: 0. State of device's D3Cold signal.
3	<b>devoffgating_state</b> . Read-only. Reset: 0. State of device's DevOffGating signal.
2	<b>rstb_state</b> . Read-only. Reset: 1. State of device's RstB signal.
1	<b>refclkok_state</b> . Read-only. Reset: 1. State of device's RefClkOk signal.
0	<b>pwrrstb_state</b> . Read-only. Reset: 1. State of device's PwrRstB signal.

**AOACx00000064 (FCH::AOAC::DEVCTRL\_18)**

Read-write. Reset: 74h.

\_aliasHOSTLEGACY; AOACx00000064; AOAC=FED8\_1E00h

Bits	Description
7	<b>isswcontrol</b> . Read-write. Reset: 0. <b>Description:</b> 1: Sw controls control signals (PwrRstB, RefClkOk, RstB) to the device. 0: Hw controls control signals (PwrRstB, RefClkOk, RstB) to the device. To avoid glitch on the reset signals, SW must set IsSwControl bit first and then program SwPwrOnRstB, SwRefClkOk and SwRstB.
6	<b>swrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: RstB is asserted to the device if IsSwControl is set to 1. 1: RstB is de-asserted to the device if IsSwControl is set to 1.
5	<b>swrefclkok</b> . Read-write. Reset: 1. <b>Description:</b> 0: RefClkOk is de-asserted to the device if IsSwControl is set to 1. 1: RefClkOk is asserted to the device if IsSwControl is set to 1.
4	<b>swpwrnrrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: PwrRstB is asserted to the device if IsSwControl is set to 1. 1: PwrRstB is de-asserted to the device if IsSwControl is set to 1.
3	<b>pwrndev</b> . Read-write. Reset: 0. <b>Description:</b> If SwControl is set to 0, SW can write this bit to trigger a HW controlled reset sequence to the device. 0: put device in reset state. 1: put device out of reset state.
2	<b>devicestate</b> . Read-write. Reset: 1. <b>Description:</b> SW records the device power state in this field. 0: device power is removed 1: device power is applied
1:0	<b>targeteddevicestate</b> . Read-write. Reset: 0h. <b>Description:</b> SW records D-State of the device in this field. 00: D0 UnInitialized 01: D0 Initialized 10: D1/D2/D3 Hot 11: D3 Cold

**AOACx00000065 (FCH::AOAC::DEVSTS\_18)**

Read-only. Reset: 27h.

\_aliasHOSTLEGACY; AOACx00000065; AOAC=FED8\_1E00h

Bits	Description
7	<b>stat1</b> . Read-only. Reset: 0. State of device.
6	<b>stat0</b> . Read-only. Reset: 0. State of device.
5	<b>clkok_state</b> . Read-only. Reset: 1. State of device's ClkOk signal.
4	<b>d3cold</b> . Read-only. Reset: 0. State of device's D3Cold signal.
3	<b>devoffgating_state</b> . Read-only. Reset: 0. State of device's DevOffGating signal.
2	<b>rstb_state</b> . Read-only. Reset: 1. State of device's RstB signal.
1	<b>refclkok_state</b> . Read-only. Reset: 1. State of device's RefClkOk signal.
0	<b>pwrrstb_state</b> . Read-only. Reset: 1. State of device's PwrRstB signal.

**AOACx00000066 (FCH::AOAC::DEVCTRL\_19)**

Read-write. Reset: 74h.

\_aliasHOSTLEGACY; AOACx00000066; AOAC=FED8\_1E00h

Bits	Description
7	<b>isswcontrol</b> . Read-write. Reset: 0. <b>Description:</b> 1: Sw controls control signals (PwrRstB, RefClkOk, RstB) to the device. 0: Hw controls control signals (PwrRstB, RefClkOk, RstB) to the device. To avoid glitch on the reset signals, SW must set IsSwControl bit first and then program SwPwrOnRstB, SwRefClkOk and SwRstB.
6	<b>swrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: RstB is asserted to the device if IsSwControl is set to 1. 1: RstB is de-asserted to the device if IsSwControl is set to 1.
5	<b>swrefclkok</b> . Read-write. Reset: 1. <b>Description:</b> 0: RefClkOk is de-asserted to the device if IsSwControl is set to 1. 1: RefClkOk is asserted to the device if IsSwControl is set to 1.
4	<b>swpwrnrrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: PwrRstB is asserted to the device if IsSwControl is set to 1. 1: PwrRstB is de-asserted to the device if IsSwControl is set to 1.
3	<b>pwronddev</b> . Read-write. Reset: 0. <b>Description:</b> If SwControl is set to 0, SW can write this bit to trigger a HW controlled reset sequence to the device. 0: put device in reset state. 1: put device out of reset state.
2	<b>devicestate</b> . Read-write. Reset: 1. <b>Description:</b> SW records the device power state in this field. 0: device power is removed 1: device power is applied
1:0	<b>targeteddevicestate</b> . Read-write. Reset: 0h. <b>Description:</b> SW records D-State of the device in this field. 00: D0 UnInitialized 01: D0 Initialized 10: D1/D2/D3 Hot 11: D3 Cold

**AOACx00000067 (FCH::AOAC::DEVSTS\_19)**

Read-only. Reset: 27h.

\_aliasHOSTLEGACY; AOACx00000067; AOAC=FED8\_1E00h

Bits	Description
7	<b>stat1</b> . Read-only. Reset: 0. State of device.
6	<b>stat0</b> . Read-only. Reset: 0. State of device.
5	<b>clkok_state</b> . Read-only. Reset: 1. State of device's ClkOk signal.
4	<b>d3cold</b> . Read-only. Reset: 0. State of device's D3Cold signal.
3	<b>devoffgating_state</b> . Read-only. Reset: 0. State of device's DevOffGating signal.
2	<b>rstb_state</b> . Read-only. Reset: 1. State of device's RstB signal.
1	<b>refclkok_state</b> . Read-only. Reset: 1. State of device's RefClkOk signal.
0	<b>pwrrstb_state</b> . Read-only. Reset: 1. State of device's PwrRstB signal.

**AOACx00000068 (FCH::AOAC::DEVCTRL\_20)**

Read-write. Reset: 74h.

\_aliasHOSTLEGACY; AOACx00000068; AOAC=FED8\_1E00h

Bits	Description
7	<b>isswcontrol</b> . Read-write. Reset: 0. <b>Description:</b> 1: Sw controls control signals (PwrRstB, RefClkOk, RstB) to the device. 0: Hw controls control signals (PwrRstB, RefClkOk, RstB) to the device. To avoid glitch on the reset signals, SW must set IsSwControl bit first and then program SwPwrOnRstB, SwRefClkOk and SwRstB.
6	<b>swrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: RstB is asserted to the device if IsSwControl is set to 1. 1: RstB is de-asserted to the device if IsSwControl is set to 1.
5	<b>swrefclkok</b> . Read-write. Reset: 1. <b>Description:</b> 0: RefClkOk is de-asserted to the device if IsSwControl is set to 1. 1: RefClkOk is asserted to the device if IsSwControl is set to 1.
4	<b>swpwrnrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: PwrRstB is asserted to the device if IsSwControl is set to 1. 1: PwrRstB is de-asserted to the device if IsSwControl is set to 1.
3	<b>pwronddev</b> . Read-write. Reset: 0. <b>Description:</b> If SwControl is set to 0, SW can write this bit to trigger a HW controlled reset sequence to the device. 0: put device in reset state. 1: put device out of reset state.
2	<b>devicestate</b> . Read-write. Reset: 1. <b>Description:</b> SW records the device power state in this field. 0: device power is removed 1: device power is applied
1:0	<b>targeteddevicestate</b> . Read-write. Reset: 0h. <b>Description:</b> SW records D-State of the device in this field. 00: D0 UnInitialized 01: D0 Initialized 10: D1/D2/D3 Hot 11: D3 Cold

**AOACx00000069 (FCH::AOAC::DEVSTS\_20)**

Read-only. Reset: 27h.

\_aliasHOSTLEGACY; AOACx00000069; AOAC=FED8\_1E00h

Bits	Description
7	<b>stat1</b> . Read-only. Reset: 0. State of device.
6	<b>stat0</b> . Read-only. Reset: 0. State of device.
5	<b>clkok_state</b> . Read-only. Reset: 1. State of device's ClkOk signal.
4	<b>d3cold</b> . Read-only. Reset: 0. State of device's D3Cold signal.
3	<b>devoffgating_state</b> . Read-only. Reset: 0. State of device's DevOffGating signal.
2	<b>rstb_state</b> . Read-only. Reset: 1. State of device's RstB signal.
1	<b>refclkok_state</b> . Read-only. Reset: 1. State of device's RefClkOk signal.
0	<b>pwrrstb_state</b> . Read-only. Reset: 1. State of device's PwrRstB signal.

**AOACx0000006A (FCH::AOAC::DEVCTRL\_21)**

Read-write. Reset: 74h.

\_aliasHOSTLEGACY; AOACx0000006A; AOAC=FED8\_1E00h

Bits	Description
7	<b>isswcontrol</b> . Read-write. Reset: 0. <b>Description:</b> 1: Sw controls control signals (PwrRstB, RefClkOk, RstB) to the device. 0: Hw controls control signals (PwrRstB, RefClkOk, RstB) to the device. To avoid glitch on the reset signals, SW must set IsSwControl bit first and then program SwPwrOnRstB, SwRefClkOk and SwRstB.
6	<b>swrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: RstB is asserted to the device if IsSwControl is set to 1. 1: RstB is de-asserted to the device if IsSwControl is set to 1.
5	<b>swrefclkok</b> . Read-write. Reset: 1. <b>Description:</b> 0: RefClkOk is de-asserted to the device if IsSwControl is set to 1. 1: RefClkOk is asserted to the device if IsSwControl is set to 1.
4	<b>swpwrnrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: PwrRstB is asserted to the device if IsSwControl is set to 1. 1: PwrRstB is de-asserted to the device if IsSwControl is set to 1.
3	<b>pwronddev</b> . Read-write. Reset: 0. <b>Description:</b> If SwControl is set to 0, SW can write this bit to trigger a HW controlled reset sequence to the device. 0: put device in reset state. 1: put device out of reset state.
2	<b>devicestate</b> . Read-write. Reset: 1. <b>Description:</b> SW records the device power state in this field. 0: device power is removed 1: device power is applied
1:0	<b>targeteddevicestate</b> . Read-write. Reset: 0h. <b>Description:</b> SW records D-State of the device in this field. 00: D0 UnInitialized 01: D0 Initialized 10: D1/D2/D3 Hot 11: D3 Cold

**AOACx0000006B (FCH::AOAC::DEVSTS\_21)**

Read-only. Reset: 27h.

\_aliasHOSTLEGACY; AOACx0000006B; AOAC=FED8\_1E00h

Bits	Description
7	<b>stat1</b> . Read-only. Reset: 0. State of device.
6	<b>stat0</b> . Read-only. Reset: 0. State of device.
5	<b>clkok_state</b> . Read-only. Reset: 1. State of device's ClkOk signal.
4	<b>d3cold</b> . Read-only. Reset: 0. State of device's D3Cold signal.
3	<b>devoffgating_state</b> . Read-only. Reset: 0. State of device's DevOffGating signal.
2	<b>rstb_state</b> . Read-only. Reset: 1. State of device's RstB signal.
1	<b>refclkok_state</b> . Read-only. Reset: 1. State of device's RefClkOk signal.
0	<b>pwr rstb_state</b> . Read-only. Reset: 1. State of device's PwrRstB signal.

**AOACx0000006C (FCH::AOAC::DEVCTRL\_22)**

Read-write. Reset: 74h.

\_aliasHOSTLEGACY; AOACx0000006C; AOAC=FED8\_1E00h

Bits	Description
7	<b>isswcontrol</b> . Read-write. Reset: 0. <b>Description:</b> 1: Sw controls control signals (PwrRstB, RefClkOk, RstB) to the device. 0: Hw controls control signals (PwrRstB, RefClkOk, RstB) to the device. To avoid glitch on the reset signals, SW must set IsSwControl bit first and then program SwPwrOnRstB, SwRefClkOk and SwRstB.
6	<b>swrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: RstB is asserted to the device if IsSwControl is set to 1. 1: RstB is de-asserted to the device if IsSwControl is set to 1.
5	<b>swrefclkok</b> . Read-write. Reset: 1. <b>Description:</b> 0: RefClkOk is de-asserted to the device if IsSwControl is set to 1. 1: RefClkOk is asserted to the device if IsSwControl is set to 1.
4	<b>swpwr onrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: PwrRstB is asserted to the device if IsSwControl is set to 1. 1: PwrRstB is de-asserted to the device if IsSwControl is set to 1.
3	<b>pwr ondev</b> . Read-write. Reset: 0. <b>Description:</b> If SwControl is set to 0, SW can write this bit to trigger a HW controlled reset sequence to the device. 0: put device in reset state. 1: put device out of reset state.
2	<b>devicestate</b> . Read-write. Reset: 1. <b>Description:</b> SW records the device power state in this field. 0: device power is removed 1: device power is applied
1:0	<b>targeteddevicestate</b> . Read-write. Reset: 0h. <b>Description:</b> SW records D-State of the device in this field. 00: D0 UnInitialized 01: D0 Initialized 10: D1/D2/D3 Hot 11: D3 Cold



**AOACx0000006D (FCH::AOAC::DEVSTS\_22)**

Read-only. Reset: 27h.

\_aliasHOSTLEGACY; AOACx0000006D; AOAC=FED8\_1E00h

Bits	Description
7	<b>stat1</b> . Read-only. Reset: 0. State of device.
6	<b>stat0</b> . Read-only. Reset: 0. State of device.
5	<b>clkok_state</b> . Read-only. Reset: 1. State of device's ClkOk signal.
4	<b>d3cold</b> . Read-only. Reset: 0. State of device's D3Cold signal.
3	<b>devoffgating_state</b> . Read-only. Reset: 0. State of device's DevOffGating signal.
2	<b>rstb_state</b> . Read-only. Reset: 1. State of device's RstB signal.
1	<b>refclkok_state</b> . Read-only. Reset: 1. State of device's RefClkOk signal.
0	<b>pwrrstb_state</b> . Read-only. Reset: 1. State of device's PwrRstB signal.

**AOACx0000006E (FCH::AOAC::DEVCTRL\_23)**

Read-write. Reset: 74h.

\_aliasHOSTLEGACY; AOACx0000006E; AOAC=FED8\_1E00h

Bits	Description
7	<b>isswcontrol</b> . Read-write. Reset: 0. <b>Description:</b> 1: Sw controls control signals (PwrRstB, RefClkOk, RstB) to the device. 0: Hw controls control signals (PwrRstB, RefClkOk, RstB) to the device. To avoid glitch on the reset signals, SW must set IsSwControl bit first and then program SwPwrOnRstB, SwRefClkOk and SwRstB.
6	<b>swrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: RstB is asserted to the device if IsSwControl is set to 1. 1: RstB is de-asserted to the device if IsSwControl is set to 1.
5	<b>swrefclkok</b> . Read-write. Reset: 1. <b>Description:</b> 0: RefClkOk is de-asserted to the device if IsSwControl is set to 1. 1: RefClkOk is asserted to the device if IsSwControl is set to 1.
4	<b>swpwrnrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: PwrRstB is asserted to the device if IsSwControl is set to 1. 1: PwrRstB is de-asserted to the device if IsSwControl is set to 1.
3	<b>pwrondev</b> . Read-write. Reset: 0. <b>Description:</b> If SwControl is set to 0, SW can write this bit to trigger a HW controlled reset sequence to the device. 0: put device in reset state. 1: put device out of reset state.
2	<b>devicestate</b> . Read-write. Reset: 1. <b>Description:</b> SW records the device power state in this field. 0: device power is removed 1: device power is applied
1:0	<b>targeteddevicestate</b> . Read-write. Reset: 0h. <b>Description:</b> SW records D-State of the device in this field. 00: D0 UnInitialized 01: D0 Initialized 10: D1/D2/D3 Hot 11: D3 Cold

**AOACx0000006F (FCH::AOAC::DEVSTS\_23)**

Read-only. Reset: 27h.

\_aliasHOSTLEGACY; AOACx0000006F; AOAC=FED8\_1E00h

Bits	Description
7	<b>stat1</b> . Read-only. Reset: 0. State of device.
6	<b>stat0</b> . Read-only. Reset: 0. State of device.
5	<b>clkok_state</b> . Read-only. Reset: 1. State of device's ClkOk signal.
4	<b>d3cold</b> . Read-only. Reset: 0. State of device's D3Cold signal.
3	<b>devoffgating_state</b> . Read-only. Reset: 0. State of device's DevOffGating signal.
2	<b>rstb_state</b> . Read-only. Reset: 1. State of device's RstB signal.
1	<b>refclkok_state</b> . Read-only. Reset: 1. State of device's RefClkOk signal.
0	<b>pwr_rstb_state</b> . Read-only. Reset: 1. State of device's PwrRstB signal.

**AOACx00000070 (FCH::AOAC::DEVCTRL\_24)**

Read-write. Reset: 74h.

\_aliasHOSTLEGACY; AOACx00000070; AOAC=FED8\_1E00h

Bits	Description
7	<b>isswcontrol</b> . Read-write. Reset: 0. <b>Description:</b> 1: Sw controls control signals (PwrRstB, RefClkOk, RstB) to the device. 0: Hw controls control signals (PwrRstB, RefClkOk, RstB) to the device. To avoid glitch on the reset signals, SW must set IsSwControl bit first and then program SwPwrOnRstB, SwRefClkOk and SwRstB.
6	<b>swrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: RstB is asserted to the device if IsSwControl is set to 1. 1: RstB is de-asserted to the device if IsSwControl is set to 1.
5	<b>swrefclkok</b> . Read-write. Reset: 1. <b>Description:</b> 0: RefClkOk is de-asserted to the device if IsSwControl is set to 1. 1: RefClkOk is asserted to the device if IsSwControl is set to 1.
4	<b>swpwrn_rstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: PwrRstB is asserted to the device if IsSwControl is set to 1. 1: PwrRstB is de-asserted to the device if IsSwControl is set to 1.
3	<b>pwrndev</b> . Read-write. Reset: 0. <b>Description:</b> If SwControl is set to 0, SW can write this bit to trigger a HW controlled reset sequence to the device. 0: put device in reset state. 1: put device out of reset state.
2	<b>devicestate</b> . Read-write. Reset: 1. <b>Description:</b> SW records the device power state in this field. 0: device power is removed 1: device power is applied
1:0	<b>targeteddevicestate</b> . Read-write. Reset: 0h. <b>Description:</b> SW records D-State of the device in this field. 00: D0 UnInitialized 01: D0 Initialized 10: D1/D2/D3 Hot 11: D3 Cold

**AOACx00000071 (FCH::AOAC::DEVSTS\_24)**

Read-only. Reset: 27h.

\_aliasHOSTLEGACY; AOACx00000071; AOAC=FED8\_1E00h

Bits	Description
7	<b>stat1</b> . Read-only. Reset: 0. State of device.
6	<b>stat0</b> . Read-only. Reset: 0. State of device.
5	<b>clkok_state</b> . Read-only. Reset: 1. State of device's ClkOk signal.
4	<b>d3cold</b> . Read-only. Reset: 0. State of device's D3Cold signal.
3	<b>devoffgating_state</b> . Read-only. Reset: 0. State of device's DevOffGating signal.
2	<b>rstb_state</b> . Read-only. Reset: 1. State of device's RstB signal.
1	<b>refclkok_state</b> . Read-only. Reset: 1. State of device's RefClkOk signal.
0	<b>pwrrstb_state</b> . Read-only. Reset: 1. State of device's PwrRstB signal.

**AOACx00000072 (FCH::AOAC::DEVCTRL\_25)**

Read-write. Reset: 7Dh.

\_aliasHOSTLEGACY; AOACx00000072; AOAC=FED8\_1E00h

Bits	Description
7	<b>isswcontrol</b> . Read-write. Reset: 0. <b>Description:</b> 1: Sw controls control signals (PwrRstB, RefClkOk, RstB) to the device. 0: Hw controls control signals (PwrRstB, RefClkOk, RstB) to the device. To avoid glitch on the reset signals, SW must set IsSwControl bit first and then program SwPwrOnRstB, SwRefClkOk and SwRstB.
6	<b>swrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: RstB is asserted to the device if IsSwControl is set to 1. 1: RstB is de-asserted to the device if IsSwControl is set to 1.
5	<b>swrefclkok</b> . Read-write. Reset: 1. <b>Description:</b> 0: RefClkOk is de-asserted to the device if IsSwControl is set to 1. 1: RefClkOk is asserted to the device if IsSwControl is set to 1.
4	<b>swpwrnrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: PwrRstB is asserted to the device if IsSwControl is set to 1. 1: PwrRstB is de-asserted to the device if IsSwControl is set to 1.
3	<b>pwronddev</b> . Read-write. Reset: 1. <b>Description:</b> If SwControl is set to 0, SW can write this bit to trigger a HW controlled reset sequence to the device. 0: put device in reset state. 1: put device out of reset state.
2	<b>devicestate</b> . Read-write. Reset: 1. <b>Description:</b> SW records the device power state in this field. 0: device power is removed 1: device power is applied
1:0	<b>targeteddevicestate</b> . Read-write. Reset: 1h. <b>Description:</b> SW records D-State of the device in this field. 00: D0 UnInitialized 01: D0 Initialized 10: D1/D2/D3 Hot 11: D3 Cold

**AOACx00000073 (FCH::AOAC::DEVSTS\_25)**

Read-only. Reset: 27h.

\_aliasHOSTLEGACY; AOACx00000073; AOAC=FED8\_1E00h

Bits	Description
7	<b>stat1</b> . Read-only. Reset: 0. State of device.
6	<b>stat0</b> . Read-only. Reset: 0. State of device.
5	<b>clkok_state</b> . Read-only. Reset: 1. State of device's ClkOk signal.
4	<b>d3cold</b> . Read-only. Reset: 0. State of device's D3Cold signal.
3	<b>devoffgating_state</b> . Read-only. Reset: 0. State of device's DevOffGating signal.
2	<b>rstb_state</b> . Read-only. Reset: 1. State of device's RstB signal.
1	<b>refclkok_state</b> . Read-only. Reset: 1. State of device's RefClkOk signal.
0	<b>pwrrstb_state</b> . Read-only. Reset: 1. State of device's PwrRstB signal.

**AOACx00000074 (FCH::AOAC::DEVCTRL\_26)**

Read-write. Reset: 7Dh.

\_aliasHOSTLEGACY; AOACx00000074; AOAC=FED8\_1E00h

Bits	Description
7	<b>isswcontrol</b> . Read-write. Reset: 0. <b>Description:</b> 1: Sw controls control signals (PwrRstB, RefClkOk, RstB) to the device. 0: Hw controls control signals (PwrRstB, RefClkOk, RstB) to the device. To avoid glitch on the reset signals, SW must set IsSwControl bit first and then program SwPwrOnRstB, SwRefClkOk and SwRstB.
6	<b>swrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: RstB is asserted to the device if IsSwControl is set to 1. 1: RstB is de-asserted to the device if IsSwControl is set to 1.
5	<b>swrefclkok</b> . Read-write. Reset: 1. <b>Description:</b> 0: RefClkOk is de-asserted to the device if IsSwControl is set to 1. 1: RefClkOk is asserted to the device if IsSwControl is set to 1.
4	<b>swpwrnrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: PwrRstB is asserted to the device if IsSwControl is set to 1. 1: PwrRstB is de-asserted to the device if IsSwControl is set to 1.
3	<b>pwronddev</b> . Read-write. Reset: 1. <b>Description:</b> If SwControl is set to 0, SW can write this bit to trigger a HW controlled reset sequence to the device. 0: put device in reset state. 1: put device out of reset state.
2	<b>devicestate</b> . Read-write. Reset: 1. <b>Description:</b> SW records the device power state in this field. 0: device power is removed 1: device power is applied
1:0	<b>targeteddevicestate</b> . Read-write. Reset: 1h. <b>Description:</b> SW records D-State of the device in this field. 00: D0 UnInitialized 01: D0 Initialized 10: D1/D2/D3 Hot 11: D3 Cold

**AOACx00000075 (FCH::AOAC::DEVSTS\_26)**

Read-only. Reset: 27h.

\_aliasHOSTLEGACY; AOACx00000075; AOAC=FED8\_1E00h

Bits	Description
7	<b>stat1</b> . Read-only. Reset: 0. State of device.
6	<b>stat0</b> . Read-only. Reset: 0. State of device.
5	<b>clkok_state</b> . Read-only. Reset: 1. State of device's ClkOk signal.
4	<b>d3cold</b> . Read-only. Reset: 0. State of device's D3Cold signal.
3	<b>devoffgating_state</b> . Read-only. Reset: 0. State of device's DevOffGating signal.
2	<b>rstb_state</b> . Read-only. Reset: 1. State of device's RstB signal.
1	<b>refclkok_state</b> . Read-only. Reset: 1. State of device's RefClkOk signal.
0	<b>pwr_rstb_state</b> . Read-only. Reset: 1. State of device's PwrRstB signal.

**AOACx00000076 (FCH::AOAC::DEVCTRL\_27)**

Read-write. Reset: 7Dh.

\_aliasHOSTLEGACY; AOACx00000076; AOAC=FED8\_1E00h

Bits	Description
7	<b>isswcontrol</b> . Read-write. Reset: 0. <b>Description:</b> 1: Sw controls control signals (PwrRstB, RefClkOk, RstB) to the device. 0: Hw controls control signals (PwrRstB, RefClkOk, RstB) to the device. To avoid glitch on the reset signals, SW must set IsSwControl bit first and then program SwPwrOnRstB, SwRefClkOk and SwRstB.
6	<b>swrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: RstB is asserted to the device if IsSwControl is set to 1. 1: RstB is de-asserted to the device if IsSwControl is set to 1.
5	<b>swrefclkok</b> . Read-write. Reset: 1. <b>Description:</b> 0: RefClkOk is de-asserted to the device if IsSwControl is set to 1. 1: RefClkOk is asserted to the device if IsSwControl is set to 1.
4	<b>swpwr_rstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: PwrRstB is asserted to the device if IsSwControl is set to 1. 1: PwrRstB is de-asserted to the device if IsSwControl is set to 1.
3	<b>pwr_rstb_dev</b> . Read-write. Reset: 1. <b>Description:</b> If SwControl is set to 0, SW can write this bit to trigger a HW controlled reset sequence to the device. 0: put device in reset state. 1: put device out of reset state.
2	<b>devicestate</b> . Read-write. Reset: 1. <b>Description:</b> SW records the device power state in this field. 0: device power is removed 1: device power is applied
1:0	<b>targeteddevicestate</b> . Read-write. Reset: 1h. <b>Description:</b> SW records D-State of the device in this field. 00: D0 UnInitialized 01: D0 Initialized 10: D1/D2/D3 Hot 11: D3 Cold

**AOACx00000077 (FCH::AOAC::DEVSTS\_27)**

Read-only. Reset: 27h.

\_aliasHOSTLEGACY; AOACx00000077; AOAC=FED8\_1E00h

Bits	Description
7	<b>stat1</b> . Read-only. Reset: 0. State of device.
6	<b>stat0</b> . Read-only. Reset: 0. State of device.
5	<b>clkok_state</b> . Read-only. Reset: 1. State of device's ClkOk signal.
4	<b>d3cold</b> . Read-only. Reset: 0. State of device's D3Cold signal.
3	<b>devoffgating_state</b> . Read-only. Reset: 0. State of device's DevOffGating signal.
2	<b>rstb_state</b> . Read-only. Reset: 1. State of device's RstB signal.
1	<b>refclkok_state</b> . Read-only. Reset: 1. State of device's RefClkOk signal.
0	<b>pwrrstb_state</b> . Read-only. Reset: 1. State of device's PwrRstB signal.

**AOACx00000078 (FCH::AOAC::DEVCTRL\_28)**

Read-write. Reset: 7Dh.

\_aliasHOSTLEGACY; AOACx00000078; AOAC=FED8\_1E00h

Bits	Description
7	<b>isswcontrol</b> . Read-write. Reset: 0. <b>Description:</b> 1: Sw controls control signals (PwrRstB, RefClkOk, RstB) to the device. 0: Hw controls control signals (PwrRstB, RefClkOk, RstB) to the device. To avoid glitch on the reset signals, SW must set IsSwControl bit first and then program SwPwrOnRstB, SwRefClkOk and SwRstB.
6	<b>swrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: RstB is asserted to the device if IsSwControl is set to 1. 1: RstB is de-asserted to the device if IsSwControl is set to 1.
5	<b>swrefclkok</b> . Read-write. Reset: 1. <b>Description:</b> 0: RefClkOk is de-asserted to the device if IsSwControl is set to 1. 1: RefClkOk is asserted to the device if IsSwControl is set to 1.
4	<b>swpwrnrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: PwrRstB is asserted to the device if IsSwControl is set to 1. 1: PwrRstB is de-asserted to the device if IsSwControl is set to 1.
3	<b>pwronddev</b> . Read-write. Reset: 1. <b>Description:</b> If SwControl is set to 0, SW can write this bit to trigger a HW controlled reset sequence to the device. 0: put device in reset state. 1: put device out of reset state.
2	<b>devicestate</b> . Read-write. Reset: 1. <b>Description:</b> SW records the device power state in this field. 0: device power is removed 1: device power is applied
1:0	<b>targeteddevicestate</b> . Read-write. Reset: 1h. <b>Description:</b> SW records D-State of the device in this field. 00: D0 UnInitialized 01: D0 Initialized 10: D1/D2/D3 Hot 11: D3 Cold

**AOACx00000079 (FCH::AOAC::DEVSTS\_28)**

Read-only. Reset: 27h.

\_aliasHOSTLEGACY; AOACx00000079; AOAC=FED8\_1E00h

Bits	Description
7	<b>stat1</b> . Read-only. Reset: 0. State of device.
6	<b>stat0</b> . Read-only. Reset: 0. State of device.
5	<b>clkok_state</b> . Read-only. Reset: 1. State of device's ClkOk signal.
4	<b>d3cold</b> . Read-only. Reset: 0. State of device's D3Cold signal.
3	<b>devoffgating_state</b> . Read-only. Reset: 0. State of device's DevOffGating signal.
2	<b>rstb_state</b> . Read-only. Reset: 1. State of device's RstB signal.
1	<b>refclkok_state</b> . Read-only. Reset: 1. State of device's RefClkOk signal.
0	<b>pwr_rstb_state</b> . Read-only. Reset: 1. State of device's PwrRstB signal.

**AOACx0000007A (FCH::AOAC::DEVCTRL\_29)**

Read-write. Reset: 74h.

\_aliasHOSTLEGACY; AOACx0000007A; AOAC=FED8\_1E00h

Bits	Description
7	<b>isswcontrol</b> . Read-write. Reset: 0. <b>Description:</b> 1: Sw controls control signals (PwrRstB, RefClkOk, RstB) to the device. 0: Hw controls control signals (PwrRstB, RefClkOk, RstB) to the device. To avoid glitch on the reset signals, SW must set IsSwControl bit first and then program SwPwrOnRstB, SwRefClkOk and SwRstB.
6	<b>swrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: RstB is asserted to the device if IsSwControl is set to 1. 1: RstB is de-asserted to the device if IsSwControl is set to 1.
5	<b>swrefclkok</b> . Read-write. Reset: 1. <b>Description:</b> 0: RefClkOk is de-asserted to the device if IsSwControl is set to 1. 1: RefClkOk is asserted to the device if IsSwControl is set to 1.
4	<b>swpwr_rstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: PwrRstB is asserted to the device if IsSwControl is set to 1. 1: PwrRstB is de-asserted to the device if IsSwControl is set to 1.
3	<b>pwr_rstb_dev</b> . Read-write. Reset: 0. <b>Description:</b> If SwControl is set to 0, SW can write this bit to trigger a HW controlled reset sequence to the device. 0: put device in reset state. 1: put device out of reset state.
2	<b>devicestate</b> . Read-write. Reset: 1. <b>Description:</b> SW records the device power state in this field. 0: device power is removed 1: device power is applied
1:0	<b>targeteddevicestate</b> . Read-write. Reset: 0h. <b>Description:</b> SW records D-State of the device in this field. 00: D0 UnInitialized 01: D0 Initialized 10: D1/D2/D3 Hot 11: D3 Cold

**AOACx0000007B (FCH::AOAC::DEVSTS\_29)**

Read-only. Reset: 27h.

\_aliasHOSTLEGACY; AOACx0000007B; AOAC=FED8\_1E00h

Bits	Description
7	<b>stat1</b> . Read-only. Reset: 0. State of device.
6	<b>stat0</b> . Read-only. Reset: 0. State of device.
5	<b>clkok_state</b> . Read-only. Reset: 1. State of device's ClkOk signal.
4	<b>d3cold</b> . Read-only. Reset: 0. State of device's D3Cold signal.
3	<b>devoffgating_state</b> . Read-only. Reset: 0. State of device's DevOffGating signal.
2	<b>rstb_state</b> . Read-only. Reset: 1. State of device's RstB signal.
1	<b>refclkok_state</b> . Read-only. Reset: 1. State of device's RefClkOk signal.
0	<b>pwrrstb_state</b> . Read-only. Reset: 1. State of device's PwrRstB signal.

**AOACx0000007C (FCH::AOAC::DEVCTRL\_30)**

Read-write. Reset: 7Dh.

\_aliasHOSTLEGACY; AOACx0000007C; AOAC=FED8\_1E00h

Bits	Description
7	<b>isswcontrol</b> . Read-write. Reset: 0. <b>Description:</b> 1: Sw controls control signals (PwrRstB, RefClkOk, RstB) to the device. 0: Hw controls control signals (PwrRstB, RefClkOk, RstB) to the device. To avoid glitch on the reset signals, SW must set IsSwControl bit first and then program SwPwrOnRstB, SwRefClkOk and SwRstB.
6	<b>swrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: RstB is asserted to the device if IsSwControl is set to 1. 1: RstB is de-asserted to the device if IsSwControl is set to 1.
5	<b>swrefclkok</b> . Read-write. Reset: 1. <b>Description:</b> 0: RefClkOk is de-asserted to the device if IsSwControl is set to 1. 1: RefClkOk is asserted to the device if IsSwControl is set to 1.
4	<b>swpwrnrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: PwrRstB is asserted to the device if IsSwControl is set to 1. 1: PwrRstB is de-asserted to the device if IsSwControl is set to 1.
3	<b>pwronddev</b> . Read-write. Reset: 1. <b>Description:</b> If SwControl is set to 0, SW can write this bit to trigger a HW controlled reset sequence to the device. 0: put device in reset state. 1: put device out of reset state.
2	<b>devicestate</b> . Read-write. Reset: 1. <b>Description:</b> SW records the device power state in this field. 0: device power is removed 1: device power is applied
1:0	<b>targeteddevicestate</b> . Read-write. Reset: 1h. <b>Description:</b> SW records D-State of the device in this field. 00: D0 UnInitialized 01: D0 Initialized 10: D1/D2/D3 Hot 11: D3 Cold



**AOACx0000007D (FCH::AOAC::DEVSTS\_30)**

Read-only. Reset: 27h.

\_aliasHOSTLEGACY; AOACx0000007D; AOAC=FED8\_1E00h

Bits	Description
7	<b>stat1</b> . Read-only. Reset: 0. State of device.
6	<b>stat0</b> . Read-only. Reset: 0. State of device.
5	<b>clkok_state</b> . Read-only. Reset: 1. State of device's ClkOk signal.
4	<b>d3cold</b> . Read-only. Reset: 0. State of device's D3Cold signal.
3	<b>devoffgating_state</b> . Read-only. Reset: 0. State of device's DevOffGating signal.
2	<b>rstb_state</b> . Read-only. Reset: 1. State of device's RstB signal.
1	<b>refclkok_state</b> . Read-only. Reset: 1. State of device's RefClkOk signal.
0	<b>pwrrstb_state</b> . Read-only. Reset: 1. State of device's PwrRstB signal.

**AOACx0000007E (FCH::AOAC::DEVCTRL\_31)**

Read-write. Reset: 7Dh.

\_aliasHOSTLEGACY; AOACx0000007E; AOAC=FED8\_1E00h

Bits	Description
7	<b>isswcontrol</b> . Read-write. Reset: 0. <b>Description:</b> 1: Sw controls control signals (PwrRstB, RefClkOk, RstB) to the device. 0: Hw controls control signals (PwrRstB, RefClkOk, RstB) to the device. To avoid glitch on the reset signals, SW must set IsSwControl bit first and then program SwPwrOnRstB, SwRefClkOk and SwRstB.
6	<b>swrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: RstB is asserted to the device if IsSwControl is set to 1. 1: RstB is de-asserted to the device if IsSwControl is set to 1.
5	<b>swrefclkok</b> . Read-write. Reset: 1. <b>Description:</b> 0: RefClkOk is de-asserted to the device if IsSwControl is set to 1. 1: RefClkOk is asserted to the device if IsSwControl is set to 1.
4	<b>swpwrnrstb</b> . Read-write. Reset: 1. <b>Description:</b> 0: PwrRstB is asserted to the device if IsSwControl is set to 1. 1: PwrRstB is de-asserted to the device if IsSwControl is set to 1.
3	<b>pwrondev</b> . Read-write. Reset: 1. <b>Description:</b> If SwControl is set to 0, SW can write this bit to trigger a HW controlled reset sequence to the device. 0: put device in reset state. 1: put device out of reset state.
2	<b>devicestate</b> . Read-write. Reset: 1. <b>Description:</b> SW records the device power state in this field. 0: device power is removed 1: device power is applied
1:0	<b>targeteddevicestate</b> . Read-write. Reset: 1h. <b>Description:</b> SW records D-State of the device in this field. 00: D0 UnInitialized 01: D0 Initialized 10: D1/D2/D3 Hot 11: D3 Cold

**AOACx0000007F (FCH::AOAC::DEVSTS\_31)**

Read-only. Reset: 27h.

\_aliasHOSTLEGACY; AOACx0000007F; AOAC=FED8\_1E00h

Bits	Description
7	<b>stat1</b> . Read-only. Reset: 0. State of device.
6	<b>stat0</b> . Read-only. Reset: 0. State of device.
5	<b>clkok_state</b> . Read-only. Reset: 1. State of device's ClkOk signal.
4	<b>d3cold</b> . Read-only. Reset: 0. State of device's D3Cold signal.
3	<b>devoffgating_state</b> . Read-only. Reset: 0. State of device's DevOffGating signal.
2	<b>rstb_state</b> . Read-only. Reset: 1. State of device's RstB signal.
1	<b>refclkok_state</b> . Read-only. Reset: 1. State of device's RefClkOk signal.
0	<b>pwrrestb_state</b> . Read-only. Reset: 1. State of device's PwrRstB signal.

**AOACx00000080 (FCH::AOAC::SHADOW\_REG\_REQUEST)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; AOACx00000080; AOAC=FED8\_1E00h

Bits	Description
31	<b>shadow_rst</b> . Read-write. Reset: 0. <b>Description:</b> SW can write this bit to reset shadow register control logics. (Write 1 to reset, and then write 0 to release the reset) Note: SHADOW_hang means somehow the current request is not completed. SW should do a SHADOW_rst and request again. The Shadow Reg Status bit should remain previous state from last successful save/restore of the corresponding IP. So we don't want to reset Shadow Reg Status bit by SHADOW_rst.
30	<b>request_sel</b> . Read-write. Reset: 0. <b>Description:</b> SW write this bit to select Request bank. 0: Select StoreRequest 1: Select RestoreRequest
29:0	<b>request</b> . Read-write. Reset: 0000_0000h. <b>Description:</b> Request[29:0] are actually shared by two register banks: StoreRequest[29:0] and RestoreRequest[29:0]. SW write Request_Sel bit to choose which bank to access. SW write 1 to these bits to request store or restore. The request type depends on which bank the bit is located (StoreRequest or RestoreRequest). Each bit is corresponding to a device being stored/restored. Write 0 has no effect to these registers. Once store/restore is done for a device, the corresponding bit will be cleared to 0 by HW. Only HW will be able to clear these bits.

**AOACx00000084 (FCH::AOAC::SHADOW\_REG\_STATUS)**

Read-write. Reset: 3FFF\_FFFFh.

\_aliasHOSTLEGACY; AOACx00000084; AOAC=FED8\_1E00h

Bits	Description
31:30	Reserved.
29:0	<b>status</b> . Read-write. Reset: 3FFF_FFFFh. <b>Description:</b> Reading these bits returns the status of the store/restore action. Each bit represents the status of a device. 0 means shadow register logic has finished store action for a device. 1 means shadow register has finished restoring action for a device. SW can also write this register to 1 or 0. This provide SW a way to override the status.

**AOACx00000088 (FCH::AOAC::SHADOW\_REG\_SRAM\_ADDR)**

Read-write. Reset: 0000\_0000h.

SW has indirect access to the SRAM in shadow register block via ShadowSRAM\_Addr and ShadowSRAM\_Data. SW can write ShadowSRAM\_Addr to an address it wants to access, and then read or write ShadowSRAM\_Data.

\_aliasHOSTLEGACY; AOACx00000088; AOAC=FED8\_1E00h

Bits	Description
31:16	Reserved.
15:0	<b>shadowsram_addr</b> . Read-write. Reset: 0000h. Shadow SRAM address (see NOTE)

**AOACx0000008C (FCH::AOAC::SHADOW\_REG\_SRAM\_DATA)**

Read-write. Reset: 0000\_0000h.

SW has indirect access to the SRAM in shadow register block via ShadowSRAM\_Addr and ShadowSRAM\_Data. SW can write ShadowSRAM\_Addr to an address it wants to access, and then read or write ShadowSRAM\_Data.

\_aliasHOSTLEGACY; AOACx0000008C; AOAC=FED8\_1E00h

Bits	Description
31:0	<b>shadowsram_data</b> . Read-write. Reset: 0000_0000h. Shadow SRAM data (see NOTE)

**AOACx00000090 (FCH::AOAC::SHADOW\_REG\_HW\_INIT\_EN)**

Read-write.

\_aliasHOSTLEGACY; AOACx00000090; AOAC=FED8\_1E00h

Bits	Description
31	<b>shadowsram_inds</b> . Read-write. Reset: X. <b>Description:</b> Deep Sleep status of Shadow SRAM. Read-only. 0: Shadow SRAM is in normal function mode 1: Shadow SRAM is in Deep Sleep mode
30	<b>forcemasterack</b> . Read-write. Reset: 0. <b>Description:</b> 0: Shadow Master dynamically turn on/off its internal clock base on the requests. 1: Shadow Master internal clock always enabled.
29:0	<b>hwinit_en</b> . Read-write. Reset: 0800_0016h. These bits configure the capability of "hardware initiated store/restore" for each device. When a device's HwInit_En bit is enabled, hardware will automatically initiate a store for that device before going into Power saving mode state, and a restore when waking up from Power saving mode state.

**AOACx00000094 (FCH::AOAC::POWER\_SAVING\_MODE\_CTRL)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; AOACx00000094; AOAC=FED8\_1E00h

Bits	Description
31:19	Reserved.
18	<b>clockslowdown_req.</b> Read-write. Reset: 0. <b>Description:</b> Write-only. Read always returns 0. <a href="#">MP1</a> can write 1 to this bit to request <a href="#">FCH</a> to Clock slow down state when PM_regx50[0] =1
17	<b>apuplloffreq.</b> Read-write. Reset: 0. <b>Description:</b> Write-only. Read always returns 0. <a href="#">MP1</a> can write 1 to this bit to request <a href="#">FCH</a> to shutdown CGPLL (CLOCK STOP) when PM_regx50[0] =1
16	<b>intrblocked.</b> Read-write. Reset: 0. <b>Description:</b> Read-only. If <a href="#">FCH</a> is sending an interrupt message when SW or <a href="#">MP1</a> write 1 to InterruptDis, the interrupt will be blocked "gracefully". We will wait until the interrupt is sent and then block the interrupt. This bit indicates the interrupt blocking status. 0: FCH interrupts are not blocked 1: FCH interrupts are blocked
15	<b>interruptdis.</b> Read-write. Reset: 0. <b>Description:</b> SW is able to set and clear this bit. HW can only set this bit. 1: interrupt from <a href="#">FCH</a> is disabled. 0: interrupt from FCH is enabled.
14	<b>arbiterdis.</b> Read-write. Reset: 0. <b>Description:</b> SW is able to set and clear this bit. HW can only set this bit. 1: <a href="#">FCH</a> upstream arbiter is disabled. 0: FCH upstream arbiter is enabled.
13	<b>maskioapic.</b> Read-write. Reset: 0. <b>Description:</b> 0: IOAPIC mask bits function normally 1: Mask all IOAPIC interrupts This bit is OR'd with all IOAPIC interrupt mask bits.
12	Reserved.
11	<b>anyupwakepowersavingmodeen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Power saving mode state can be wake up by GPIO controller and Shadow Timer. 1: Power saving mode state can be wake up by GPIO controller, Shadow Timer and any pending upstream message in ACPI.
10	<b>shadowtimerwakests.</b> Read-write. Reset: 0. <b>Description:</b> Read-only. HW will clear this bit during Power saving mode entry. 1: Shadow Timer fired and caused wake-up from Power saving mode state. 0: Shadow Timer did not fire.
9	<b>powersavingmoderesume.</b> Read-write. Reset: 0. Set to 1 by Power saving mode exit to indicate the system has resumed from Power saving mode state. The bit is cleared by Power saving mode entry or write-1-cleared by Sw.
8	<b>powersavingmodeenter.</b> Read-write. Reset: 0. <b>Description:</b> Read-only 1: indicate the system is in Power saving mode state. 0: indicate the system is in S0 state.
7:5	Reserved.
4	<b>powersavingmodetrigger.</b> Read-write. Reset: 0. <b>Description:</b> Write-only, read always return 0. Setting the bit to 1 to trigger Power saving mode power down sequence.
3	Reserved.
2	<b>powersavingmodeready2.</b> Read-write. Reset: 0.

	<b>Description:</b> Programmed by Driver. 0: Power saving mode can't be entered 1: Power saving mode can be entered
1	<b>powersavingmodeonslps3b.</b> Read-write. Reset: 0. <b>Description:</b> 0: SLP_S3# doesn't assert in Power saving mode state 1: SLP_S3# will assert in Power saving mode state
0	<b>powersavingmodeready.</b> Read-write. Reset: 0. <b>Description:</b> Programmed by BIOS. 0: Power saving mode can't be entered 1: Power saving mode can be entered

**AOACx00000098 (FCH::AOAC::POWER\_SAVING\_MODE\_DEBUG)**

Read-write.	
_aliasHOSTLEGACY; AOACx00000098; AOAC=FED8_1E00h	
Bits	Description
31:14	Reserved.
13	<b>powersavingmodedontwaitstpgnt.</b> Read-write. Reset: 1. <b>Description:</b> 0: Power saving mode state machine will wait for STPGNT after it sens STPCLK 1: Don't wait
12	<b>powersavingmodedontwaitssdb.</b> Read-write. Reset: 1. <b>Description:</b> 0: Wait for SDB (in PG1) to re-initialize before restore during Power saving mode wake-up 1: Don't wait
11	<b>powersavingmodedontblockpmiorst.</b> Read-write. Reset: 0. <b>Description:</b> 0: Block PciRstB to PMIO register block during Power saving mode 1: Do not block PciRstB to PMIO register block during Power saving mode
10	<b>powersavingmodeforce_clk.</b> Read-write. Reset: 0. <b>Description:</b> 0: Power saving mode state machine dynamically gate its local clock 1: Power saving mode state machine local clock always on
9	<b>powersavingmodebypassshdwreg.</b> Read-write. Reset: 0. <b>Description:</b> 0: During Power saving mode entry and exit, use ShadowReg to store and restore context of PG1 devices. 1: Bypass ShadowReg
8	<b>powersavingmodebypassshdwtnr.</b> Read-write. Reset: 0. <b>Description:</b> 0: During Power saving mode entry and exit, use ShadowTimer to store and restore HPET and AcpiTimer. 1: Bypass ShadowTimer
7:0	<b>powersavingmodextal_settle_time.</b> Read-write. Reset: XXXXXXXXb. <b>Description:</b> Debug purpose. SW should leave it at default value.

**AOACx0000009C (FCH::AOAC::SHADOW\_TIMER\_CTRL)**

Read-write.

\_aliasHOSTLEGACY; AOACx0000009C; AOAC=FED8\_1E00h

Bits	Description
31:24	<b>restoredoffset64.</b> Read-write. Reset: 00h. A programmable offset to be added to restored HPET 64bit timer this is to accounted for restore time uncertainty.
23:16	<b>restoredoffset.</b> Read-write. Reset: 00h. A programmable offset to be added to restored HPET 32bit timer and ACPI timer this is to accounted for restore time uncertainty.
15:8	<b>earlycount.</b> Read-write. Reset: XXXXXXXXb. A programmable offset to be subtracted from the alarm value
7:3	Reserved.
2	<b>earlycountunit.</b> Read-write. Reset: 0. <b>Description:</b> 0: The unit of EarlyCount is 1 RTC clock period. 1: The unit of EarlyCount is 16 RTC clock period
1	<b>shadowacpitimeren.</b> Read-write. Reset: 0. Enable control to perform store/restore operation for ACPI timer
0	<b>shadowhpeten.</b> Read-write. Reset: 0. Enable control to perform store/restore operation from HPET timer

**AOACx000000A0 (FCH::AOAC::PWRGOOD\_CTRL)**

Read-write. Reset: EE00\_E03Bh.

NOTE1:

NOTE2:

\_aliasHOSTLEGACY; AOACx000000A0; AOAC=FED8\_1E00h

Bits	Description
31	<b>swxhc0s5rstb.</b> Read-write. Reset: 1. <b>Description:</b> 0: XHC0 PHY is powered down. 1: XHC0 PHY is powered.
30	<b>swu2phys5rstb.</b> Read-write. Reset: 1. <b>Description:</b> 0: USB2 PHY is powered down. 1: USB2 PHY is powered. (See NOTE2 for the relationship between USB2 PHY and XHC controller)
29	Reserved.
28	<b>swsatalockphyif.</b> Read-write. Reset: 0. <b>Description:</b> 0: SATA PHY interface is not locked 1: SATA PHY interface is locked
27	<b>swusbpllrstb.</b> Read-write. Reset: 1. <b>Description:</b> SW can program this bit to toggle these USB related reset signals: oUsbPllRstB oUsb3PllRstB oUsbPllLockB oUsbDllRstB oGoodClkForUsb If SwUsbPllRstB is cleared to 0, the above signals will be driven to 0. After SW set SwUsbPllRstB to 1, HW will generate a de-assertion sequence for the above signals.
26	<b>swu3phys5rstb.</b> Read-write. Reset: 1. <b>Description:</b> 0: USB3 PHY is powered down. 1: USB3 PHY is powered. (See NOTE2 for the relationship between USB2 PHY and XHC controller)
25	Reserved.
24	<b>spi_pad_disable.</b> Read-write. Reset: 0. SW set this bit to 1 to disable the OE and PU of the SPI pads.
23	Reserved.
22:16	<b>swblockusbrst.</b> Read-write. Reset: 00h. <b>Description:</b> SW can set these bits to 1 to individually block the reset signals to USB2 and USB3. Combined with SwUsbPllRstB bit, SW can control the way it assert reset for USB. Bit 0: Block oUsbPllRstB Bit 1: Block oUsb3PllRstB Bit 2: Block oUsbPllLockB Bit 3: Block oUsbDllRstB Bit 4: Block oGoodClkForUsb Bit 5: Block oSoftKB_2PciRst Bit 6: Block oS3PciRstB
15	<b>powerallpwrland.</b> Read-write. Reset: 1. <b>Description:</b> If PowerAllPwrIsland is 1, we will sequentially power up all the power groups to avoid current surge. If the platform support AOAC, SW has to set this bit to 0 during boot-up. Otherwise, SW can leave it at 1. (See diagram in the NOTE1 below)
14	Reserved.
13	<b>swxhc1s5rstb.</b> Read-write. Reset: 1. <b>Description:</b> 0: XHC1 PHY is powered down. 1: XHC1 PHY is powered.

12	<b>swotgs5rstb.</b> Read-write. Reset: 0. <b>Description:</b> 0: Change OtgS5RstB signal to 0 1: Change OtgS5RstB signal to 1
11:9	Reserved.
8	<b>swsatablockoob_aoac.</b> Read-write. Reset: 0. <b>Description:</b> 0: SATA <a href="#">OOB</a> is not blocked 1: SATA OOB is blocked
7:6	Reserved.
5	<b>gbepwren.</b> Read-write. Reset: 1. <b>Description:</b> Control the power of GBE power island 0: Gbe is powered down 1: Gbe is powered up
4	<b>otgpwren.</b> Read-write. Reset: 1. <b>Description:</b> Control the power of OTG power island 0: Otg is powered down 1: Otg is powered up
3	<b>xhcpwren.</b> Read-write. Reset: 1. <b>Description:</b> Control the power of SSIC power island 0: Ssic is powered down 1: Ssic is powered up
2	<b>imcpwren.</b> Read-write. Reset: 0. <b>Description:</b> Control the power of IMC 0: IMC is powered down 1: IMC is powered up
1	<b>pg2pwren.</b> Read-write. Reset: 1. <b>Description:</b> Control the power of PG2 power island 0: PG2 is powered down 1: PG2 is powered up
0	<b>pg1apwren.</b> Read-write. Reset: 1. <b>Description:</b> Control the power of PG1a power island 0: PG1a is powered down 1: PG1a is powered up



**AOACx000000F0 (FCH::AOAC::SHDWREG\_DEBUG)**

Read-write.

\_aliasHOSTLEGACY; AOACx000000F0; AOAC=FED8\_1E00h

Bits	Description
31	Reserved.
30	<b>shadow_hang.</b> Read-write. Reset: 0. <b>Description:</b> Read-only. We have a timer to keep track of the save/restore process. When save/restore is on-going, the timer will be counting. When there is no save/restore, the timer is reset to 0. SHADOW_hang bit goes high when the timer timeout and save/restore is not done yet. SW can toggle SHADOW_rst bit to reset the shadow register control logic if the hang condition is detected. 0: Save/restore has been on-going for less than 8~12 ms 1: Save/restore has been on-going for at least 8~12 ms Note: SHADOW_hang means somehow the current request is not completed. SW should do a SHADOW_rst and request again. The Shadow Reg Status bit should remain previous state from last successful save/restore of the corresponding IP. So we don't want to reset Shadow Reg Status bit by SHADOW_rst.
29:0	<b>shadow_err.</b> Read-write. Reset: XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXb. <b>Description:</b> Write-1-clear. Write 0 has no effect. This register report errors encountered during each device's save/restore. The following error conditions will be recorded: AHB bus response error PCI bus master abort PCI bus slave abort Bit29: Error condition encountered during device 29 save/restore Bit28: Error condition encountered during device 28 save/restore Bit27: Error condition encountered during device 27 save/restore Bit26: Error condition encountered during device 26 save/restore Bit25: Error condition encountered during device 25 save/restore Bit24: Error condition encountered during device 24 save/restore Bit23: Error condition encountered during device 23 save/restore Bit22: Error condition encountered during device 22 save/restore Bit21: Error condition encountered during device 21 save/restore Bit20: Error condition encountered during device 20 save/restore Bit19: Error condition encountered during device 19 save/restore Bit18: Error condition encountered during device 18 save/restore Bit17: Error condition encountered during device 17 save/restore Bit16: Error condition encountered during device 16 save/restore Bit15: Error condition encountered during device 15 save/restore Bit14: Error condition encountered during device 14 save/restore Bit13: Error condition encountered during device 13 save/restore Bit12: Error condition encountered during device 12 save/restore Bit11: Error condition encountered during device 11 save/restore Bit10: Error condition encountered during device 10 save/restore Bit9 : Error condition encountered during device 9 save/restore Bit8 : Error condition encountered during device 8 save/restore Bit7 : Error condition encountered during device 7 save/restore Bit6 : Error condition encountered during device 6 save/restore Bit5 : Error condition encountered during device 5 save/restore Bit4 : Error condition encountered during device 4 save/restore Bit3 : Error condition encountered during device 3 save/restore Bit2 : Error condition encountered during device 2 save/restore Bit1 : Error condition encountered during device 1 save/restore Bit0 : Error condition encountered during device 0 save/restore

**AOACx000000F4 (FCH::AOAC::PWRRST\_DEBUG)**

Read-write.

NOTE1: When SW read 1 at oPG1a\_PwrGood, oPG2\_PwrGood, oGbe\_PwrGood, oOtg\_PwrGood or oSsic\_PwrGood, that means power-on sequence has completed for power group PG1a, PG2, GBE, OTG or SSIC, respectively.

NOTE2: When SW read 1 at PG1a\_CtrlSts, PG2\_CtrlSts, Gbe\_CtrlSts, Otg\_CtrlSts or Ssic\_CtrlSts, that means power-down sequence has completed for power group PG1a, PG2, GBE, OTG or SSIC, respectively.

\_aliasHOSTLEGACY; AOACx000000F4; AOAC=FED8\_1E00h

Bits	Description
31:0	<p><b>pwrrstdebugbus.</b> Read-write. Reset: XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXb.</p> <p><b>Description:</b> Read-only. Debug signals from PwrRst block:</p> <p>Bit31: Gbe_CtrlSts (see NOTE2)</p> <p>Bit30: PG1a_CtrlSts (see NOTE2)</p> <p>Bit29: PG2_CtrlSts (see NOTE2)</p> <p>Bit28: Ssic_CtrlSts (see NOTE2)</p> <p>Bit27: Otg_CtrlSts (see NOTE2)</p> <p>Bit26: oDebouncedRsmRstB</p> <p>Bit25: oPciRstB</p> <p>Bit24: oCpuPwrGood</p> <p>Bit23: oCpuRstB</p> <p>Bit22: oU2PHY5RstB</p> <p>Bit21: oUsb3S5RstB</p> <p>Bit20: oPllRstB</p> <p>Bit19: oPllLock</p> <p>Bit18: oGbe_PwrGood (see NOTE1)</p> <p>Bit17: oPG1a_PwrGood (see NOTE1)</p> <p>Bit16: oPG2_PwrGood (see NOTE1)</p> <p>Bit15: oSsic_PwrGood (see NOTE1)</p> <p>Bit14: oOtg_PwrGood (see NOTE1)</p> <p>Bit13: oPG1_ToAllEn</p> <p>Bit12: oPG1a_ToAllEn</p> <p>Bit11: oPG2_ToAllEn</p> <p>Bit10: oSsic_ToAllEn</p> <p>Bit9 : oSlpRstAsrtDone</p> <p>Bit8 : PowerSavingModeRstDsrtDone</p> <p>Bit7 : S0ResetB_Osc</p> <p>Bit6 : S5ResetB_Osc</p> <p>Bit5 : oDebouncedUsrRstB</p> <p>Bit4 : DevPwrRstB[iDebugSelDev][4]</p> <p>Bit3 : DevPwrRstB[iDebugSelDev][3]</p> <p>Bit2 : DevPwrRstB[iDebugSelDev][2]</p> <p>Bit1 : DevPwrRstB[iDebugSelDev][1]</p> <p>Bit0 : DevPwrRstB[iDebugSelDev][0]</p>

**AOACx000000F8 (FCH::AOAC::SW\_SEMOPHORE)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; AOACx000000F8; AOAC=FED8\_1E00h

Bits	Description
31	<b>drvrownaoacreg.</b> Read-write. Reset: 0. <b>Description:</b> Read only. Driver write Set_DrvrOwnAoacReg and Clr_DrvrOwnAoacReg bits to set or clear DrvrOwnAoacReg. When DrvrOwnAoacReg is 1, BiosOwnAoacReg will stay at 0 and cannot be written. Driver should always make sure DrvrOwnAoacReg is 1 before it writes AOAC Registers, and clear DrvrOwnAoacReg after it finishes the programming.
30	Reserved.
29	<b>clr_drvrownaoacreg.</b> Read-write. Reset: 0. Write only. Driver write 1 to this bit to clear DrvrOwnAoacReg.
28	<b>set_drvrownaoacreg.</b> Read-write. Reset: 0. Write only. Driver write 1 to this bit to set DrvrOwnAoacReg.
27	<b>biosownaoacreg.</b> Read-write. Reset: 0. <b>Description:</b> Read only. BIOS write Set_BiosOwnAoacReg and Clr_BiosOwnAoacReg bits to set or clear BiosOwnAoacReg. When BiosOwnAoacReg is 1, DrvrOwnAoacReg will stay at 0 and cannot be written. BIOS should always make sure BiosOwnAoacReg is 1 before it writes AOAC Registers, and clear BiosOwnAoacReg after it finishes the programming.
26	Reserved.
25	<b>clr_biosownaoacreg.</b> Read-write. Reset: 0. Write only. BIOS write 1 to this bit to clear BiosOwnAoacReg.
24	<b>set_biosownaoacreg.</b> Read-write. Reset: 0. Write only. BIOS write 1 to this bit to set BiosOwnAoacReg.
23:0	Reserved.

**AOACx000000FC (FCH::AOAC::AOAC\_DEBUG)**

Read-write. Reset: 0080\_0000h.

\_aliasHOSTLEGACY; AOACx000000FC; AOAC=FED8\_1E00h

Bits	Description
31:26	Reserved.
25	<b>shdwm_aclk_enable.</b> Read-write. Reset: 0. Read only
24	<b>shdwm_any_request.</b> Read-write. Reset: 0. Read only
23	<b>shdwm_sram_awake.</b> Read-write. Reset: 1. Read only
22	<b>shdwm_shadowclkon_s.</b> Read-write. Reset: 0. Read only
21	<b>shdwm_shadowinprogress_s.</b> Read-write. Reset: 0. Read only
20	<b>shdwm_ahbm32_aclk_enbf.</b> Read-write. Reset: 0. Read only
19	<b>shdwm_ahbm32_aclk_done.</b> Read-write. Reset: 0. Read only
18	<b>shdwm_ahbm32_aclk_req.</b> Read-write. Reset: 0. Read only
17:13	<b>shdwm_ctrlrid_4_0.</b> Read-write. Reset: 00h. Read only
12:8	<b>shdwm_state_4_0.</b> Read-write. Reset: 00h. Read only
7	<b>power_saving_mode_xtalpciclk_en.</b> Read-write. Reset: 0. Read only
6:4	<b>power_saving_mode_pd_st_2_0.</b> Read-write. Reset: 0h. Read only
3:0	<b>power_saving_mode_state_3_0.</b> Read-write. Reset: 0h. Read only

**11.3.8 ISA Bridge****11.3.8.1 SPI Registers**[FCH](#) SPI design is mode 0 only.

Register FCH::LPCHOSTSPIREG::SPI\_CNTRL0\_REGISTER, field SpiReadMode[2:0] specifies the SPI read mode:

*Table 191: SpiReadMode[2:0] Definitions*

Bits	Definition
000b	Normal read (up to 33M)
001b	Reserved
010b	Dual IO (1-1-2)
011b	Quad IO (1-1-4)
100b	Dual IO (1-2-2)
101b	Quad IO (1-4-4)
110b	Normal read (up to 66M)
111b	Fast Read

The SPI configuration registers are accessed through SPI base address. Software can communicate with the SPI ROM through the default memory or an alternate programming (a.k.a "Indexed mode") method:

- Memory access to the BIOS ROM address space is automatically handled by the hardware. The SPI ROM controller translates the memory address onto the SPI bus and accesses the SPI ROM data. Any other commands besides memory read or memory write to the SPI ROM need to go through the alternate programming (a.k.a "Indexed mode") method. SPI ROM access through the memory address is limited to a 24-bit address (16MB addressable space).
- With the alternate programming (a.k.a "Indexed mode") method, software needs to program the SPI\_OPCODE, SpiAddress, TXBYTE\_COUNT, RXBYTE\_COUNT, put the data into the transmit FIFO, and then execute the command. The hardware communicates with the SPI ROM using these parameters. This alternate programming (a.k.a "Indexed mode") method basically allows software to issue any flash vendor specific commands such as ERASE and STATUS. The alternate programming method can generate up to 32-bit addresses, but transfers are limited to "normal" (1-bit) mode.

#### 11.3.8.1.1 Programming for ROM Protection register

##### 11.3.8.1.1.1 SPI ROM Physical Address

Using a 64MB SPI ROM as an example, since only address[25:0] are needed for 64MB, SPI ROM will simply ignore value of address[31:26]. To access SPI ROM, the 64MB SPI ROM are addressed using following physical address:

- 16MB bank-0: 0xFC00\_0000 – 0xFCFF\_FFFF
- 16MB bank-1: 0xFD00\_0000 – 0xFDFF\_FFFF
- 16MB bank-2: 0xFE00\_0000 – 0xFEFF\_FFFF
- 16MB bank-3: 0xFF00\_0000 – 0xFFFF\_FFFF

##### 11.3.8.1.1.2 Program ROM Protection Register

Once physical address of protection region is determined, the ROM protection register can be programmed accordingly. Bits[11:0] are straight forward, bits[31:12]: RomBase need to match start physical address of protection region.

##### 11.3.8.1.1.2.1 Case-1, 0xFFFF0\_0000 – 0xFFFF0\_7FFF

If 32K SPI ROM space at physical address 0xFFFF0\_0000 – 0xFFFF0\_7FFF need to have both Write and Read protection, ROM protection register can be programmed to 0xFFFF0\_0607.

[7:0]: Range = 0x7, with bit[8] = 0 (unit = 4K), range = 32K

[9] = 1, Read protect

[10] = 1, Write protect

[31:12] = 0xFFFF0\_0, starting address is 0xFFFF0\_0000, with range = 32K, the protection region is 0xFFFF0\_0000 – 0xFFFF0\_7FFF

#### 11.3.8.1.1.2.2 Case-2, 0xFD46\_0000 - 0xFD4D\_FFFF

If 512K SPI ROM space at physical address 0xFD46\_0000 – 0xFD4D\_FFFF needs to have Write protection only, the ROM protection register can be programmed to 0xFD46\_0507.

[7:0]: Range = 0x7, with bit[8] = 1 (unit = 64K), range = 512K

[9] = 0, no Read protect

[10] = 1, Write protect

[31:12] = 0xFD46\_0, starting address is 0xFD46\_0000, with range = 512K, the protection region is 0xFD46\_0000 – 0xFD4D\_FFFF

#### 11.3.8.1.1.3 Index Mode (Indirect) Access

Opcode used in Index Mode determines if it is using 24-bit address mode or 32-bit address mode. For example:

- OpCode = 0x03, 24-bit address Read command
- OpCode = 0x13, 32-bit address Read command
- OpCode = 0x02, 24-bit address byte program command
- OpCode = 0x12, 32-bit address byte program command

##### 11.3.8.1.1.3.1 24-bit Address Index Mode

For Index mode, only address[25:0] are used for ROM protection address comparison. The address mapping of 24-bit address Index mode is:

Address[31:24]: 0x00, address[25:24] = 00b, point to bank-0 of 64 MB ROM (0xFC00\_0000 – 0xFCFF\_FFFF)

Address[23:16]: SPI\_regx80

Address[15:8]: SPI\_regx81

Address[7:0]: SPI\_regx82

##### 11.3.8.1.1.3.2 32-bit Address Index Mode

For Index mode, only address[25:0] are used for ROM protection address comparison. The address mapping of 32-bit address Index mode is:

Address[31:24]: SPI\_regx80, only address[25:24] used.

Address[23:16]: SPI\_regx81

Address[15:8]: SPI\_regx82

Address[7:0]: SPI\_regx83

#### 11.3.8.1.1.4 Exception

Register 'ROM Address Override' has been added to change [Logical address](#) to Physical address mapping, since Protection checking is using Address before 'ROM Address Override' mapping, caution need be paid when 'ROM Address Override[4:0]' not equal to 0x0.

Function of "ROM Address Override"

1. Bit[3:0] only apply to ROM2 (16MB) space, it is used to change ROM2 logical address to physical address mapping, it has no effect on ROM1 and ROM3
  1. Bit[3:0] = 0x0 or 0xF, ROM2 (0xFF00\_0000 – 0xFFFF\_FFFF) map to bank-3 (0xFF00\_0000 – 0xFFFF\_FFFF)
  2. Bit[3:0] = 0xC, ROM2 (0xFF00\_0000 – 0xFFFF\_FFFF) map to bank-0 (0xFC00\_0000 – 0xFCFF\_FFFF)

3. Bit[3:0] = 0xD, ROM2 (0xFF00\_0000 – 0xFFFF\_FFFF) map to bank-1 (0xFD00\_0000 – 0xFDFF\_FFFF)
4. Bit[3:0] = 0xE, ROM2 (0xFF00\_0000 – 0xFFFF\_FFFF) map to bank-2 (0xFE00\_0000 – 0xFEFF\_FFFF)
2. Bit[4] apply to all ROM1/ROM2/ROM3 space. However, since ROM1 and ROM2 are map to 0xFFxx\_xxxx by default, setting bit[4] = 1 will not affect ROM1/ROM2, only ROM3 (64MB) will be map to 0xFFxx\_xxxx (16MB).
  1. Bit[4] = 1, ROM3 (0xfd\_0000\_0000 – 0xfd\_00FF\_FFFF) map to bank-3 (0xFF00\_0000 – 0xFFFF\_FFFF)
    1. ROM3 (0xfd\_0100\_0000 – 0xfd\_01FF\_FFFF) map to bank-3 (0xFF00\_0000 – 0xFFFF\_FFFF)
    2. ROM3 (0xfd\_0200\_0000 – 0xfd\_02FF\_FFFF) map to bank-3 (0xFF00\_0000 – 0xFFFF\_FFFF)
    3. ROM3 (0xfd\_0300\_0000 – 0xfd\_03FF\_FFFF) map to bank-3 (0xFF00\_0000 – 0xFFFF\_FFFF)

#### 11.3.8.1.1.4.1 Case-1 (0xFFF0\_0000 – 0xFFF0\_7FFF)

When "ROM Address Override" register bit[4:0] != 0x00, there will be following side effects:

1. ROM1: no side effect.
2. ROM2:
  1. Bit[3:0] = 0x0 or 0xF, no side effect.
  2. Bit[3:0] = 0xC, host address 0xFFF0\_0000 – 0xFFF0\_7FFF is blocked.
    1. Side effect: SPI ROM 0xFCF0 – 0xFCF0\_7FFF is protected.
  3. Bit[3:0] = 0xD, host address 0xFFF0\_0000 – 0xFFF0\_7FFF is blocked.
    1. Side effect: SPI ROM 0xFDF0 – 0xFDF0\_7FFF is protected.
  4. Bit[3:0] = 0xE, host address 0xFFF0\_0000 – 0xFFF0\_7FFF is blocked.
    1. Side effect: SPI ROM 0xFE00 – 0xFE00\_7FFF is protected.
3. ROM3:
  1. Bit[4] = 0, no side effect.
  2. Bit[4] = 1, since all accesses through ROM3 are mapped to 0xFF00\_0000 – 0xFFFF\_FFFF. If accessed through 0xFD\_0000\_0000 – 0xFD\_02FF\_FFFF, it will access the ROM at 0xFF00\_0000 – 0xFFFF\_FFFF, which should be protected, but ROM protection comparison will not block it as address before "ROM Address Override" is used.
    1. Side effect: Need 3 more protection registers to block "0xFCF0\_0000 – 0xFCF0\_7FFF" and "0xFDF0\_0000 – 0xFDF0\_7FFF" and "0xFE00\_0000 – 0xFE00\_7FFF".

#### 11.3.8.1.1.4.2 Case-2 (0xFD46\_0000 – 0xFD4D\_FFFF)

When "ROM Address Override" register bit[4:0] != 0x00, there will be following side effects:

1. ROM1: no side effect.
2. ROM2:
  1. Bit[3:0] = 0x0 or 0xF, no side effect.
  2. Bit[3:0] = 0xC, no side effect, as ROM2 is mapped to 0xFC00\_0000 – 0xFCFF\_FFFF.
  3. Bit[3:0] = 0xD, since ROM2 is mapped to 0xFD00\_0000 – 0xFDFF\_FFFF, access to ROM2 address 0xFF46\_0000 – 0xFF4D\_FFFF needs to be blocked, which needs to program another ROM protection register with 0xFF46\_0407.
    1. Side effect: This will make SPI ROM 0xFF46\_0000 – 0xFF4D\_FFFF be protected when accessed through ROM1/ROM3.
  4. Bit[3:0] = 0xE, no side effect as ROM2 is mapped to 0xFE00\_0000 – 0xFEFF\_FFF.
3. ROM3:
  1. Bit[4]=0, no side effect
  2. Bit[4]=1, for ROM3 (0xfd\_0100\_0000 – 0xfd\_01FF\_FFFF) map to bank-3 (0xFF00\_0000 – 0xFFFF\_FFFF) case, ROM3 range 0xfd\_0146\_0000 – 0xfd\_014D\_FFFF will be blocked,
    1. Side effect: If bit[4]=1, all ROM access (ROM1/ROM2/ROM3) are map to 0xFF00\_0000 – 0xFFFF\_FFFF, which set protection for 0xFD46\_0000 – 0xFD4D\_FFFF should not exist.

**11.3.8.1.2 Serial Peripheral Interface (SPI) Registers**

**SPIx00000000 (FCH::LPCHOSTSPIREG::SPI\_CNTRL0\_REGISTER)**

Reset: 0FC0\_0000h.

\_aliasHOSTLEGACY; SPIx00000000; SPI=FEC1\_0000h

Bits	Description
31	<b>spibusy.</b> Read-write. Reset: 0. <b>Description:</b> Read-only. 0: SPI bus is idle 1: SPI bus is busy Note: When SpiBusy=1, ROM access is going on, SpiReadMode[2:0] should not be changed and ExecuteOpCode should not be set to 1 to start new operation.
30:29	<b>spireadmode_2_1.</b> Read-write. Reset: 0h. <b>Description:</b> These two bits and bit 18 in the same register Specify the Spi read mode: 000: Normal read (up to 33M) 001: Reserved 010: Dual-io (1-1-2) 011: Quad-io (1-1-4) 100: Dual-io (1-2-2) 101: Quad-io (1-4-4) 110: Normal read (up to 66M) 111: Fast read Note: before change SpiReadMode[2:0], software should read bit[31]: SpiBusy=0 to make sure no SPI operation is going on.
28	<b>spiclkgate.</b> Read-write. Reset: 0. Set to 1 to skip the 8th spiclk at the end data when doing read.
27:24	Reserved.
23	<b>spihostaccessromen.</b> Read-write. Reset: 1. <b>Description:</b> This is a clear-once protection bit once it is cleared to 0 it cannot be set back to 1. Once cleared to 0, some SPI registers cannot be written. Note: bit[23] and bit[22] were used for other function also, but those function were removed, so they are used for write-protection for certain registers only. Following registers are write-protect when bit[23:22] != 2'b11, 0x04[31:0] 0x08[31:0] 0x0C[31:24] 0x14[31:0] 0x18[31:0] 0x1C[1:0] 0x1D[1:0] 0x30[4:0] 0x40[31:0] 0x50[31:8] 0x54[31:8] 0x5C[7:0] 0x60[31:26] 0x64[31:0]
22	<b>spiaccessmacromen.</b> Read-write. Reset: 1. This is a clear-once protection bit once it is cleared to 0 it cannot be set back to 1. Once cleared to 0, some SPI registers cannot be written.
21	<b>illegalaccess.</b> Read-only. Reset: 0. <b>Description:</b> Read Only. 0. Legal Index mode Access 1. Illegal Index mode Access
20:19	Reserved.



18	<b>spireadmode_0.</b> Read-write. Reset: 0. <b>Description:</b> It is bit 0 of SpiReadMode to specify the spi read mode. Please see the definition of SpiReadMode in bit [30:29] below. Note: before change SpiReadMode[2:0], software should read bit[31]: SpiBusy=0 to make sure no SPI operation is going on.
17:12	Reserved.
11:10	<b>prot_compare_range.</b> Read-write. Reset: 0h. <b>Description:</b> Specify what address range used for ROM protection range comparison. This bit will be write protected when x00[23:22] not equal 11b. 00: address [25:12] are used 01: address [24:12] are used 10: address [23:12] are used 11: reserved
9	<b>index_cacheline_stop.</b> Read-write. Reset: 0. <b>Description:</b> 0: Index transfer stop at TxByteCnt or RxByteCnt 1: Index transfer stop at smaller value of Cacheline-boundary-ByteCnt or TxByteCnt/RxByteCnt. Cacheline-boundary-ByteCnt = 0x40 Address[5:0] Only when OpCode (x45[7:0]) match following command will Index_cacheline_stop =1 work, 24-bit address command: ByteCmd (x0C[31:24], default = 0x02) PAGEWR (0x18[23:16], default = 0x0A) DPWCmd (0x14[7:0], default = 0xB2) QPWCmd (0x14[15:8], default = 0xE2) ReadCmd (0x18[7:0], default = 0x03) FReadCmd (0x18[15:8], default = 0x0B) DPRCmd (0x40[23:16], default = 0xBB) QPRCmd (0x40[31:24], default = 0xEB) 32-bit address command: ByteCmd32 (0x50[15:8], default = 0x12) ReadCmd32(0x50[23:16],default= 0x13) FReadCmd32(0x50[31:24],default= 0x0C) DPRCmd32(0x54[23:16],default= 0xBC) QPRCmd32(0x54[31:24],default= 0xEC) This bit will be write protected when x00[23:22] not equal 11b.
8	<b>dis_index_retry.</b> Read-write. Reset: 0. <b>Description:</b> 0: PCI cycle write to x47[7]=1 to start Index mode transfer will be kept retried till Index mode transfer complete. This is backward compatible to previous design. 1: Once Index mode transfer is going on after write x47[7]=1, all register write PCI cycles to the same register block will be completed normally but write will be blocked thus register content is not changed (quietly dropped) till Index mode transfer complete thus software should not do any register write to the same register block when Index mode transfer is going on, all register read cycles to the same register block will be completed normally with read data returned, write/read to other register block will not be affected. For example, if SPIx47[7] is written =1 to start Index mode transfer, all register write to SPI register block will be quietly dropped while all register read to SPI register block will be completed normally, write/read to other register block will not be affected. This bit will be write protected when x00[23:22] not equal 11b.
7:0	Reserved.

**SPIx00000004 (FCH::LPCHOSTSPIREG::SPI\_RESTRICTEDCMD\_REGISTER)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; SPIx00000004; SPI=FEC1\_0000h

Bits	Description
31:24	<b>restrictedcmd3</b> . Read-write. Reset: 00h. Same as RestrictedCmd0
23:16	<b>restrictedcmd2</b> . Read-write. Reset: 00h. Same as RestrictedCmd0
15:8	<b>restrictedcmd1</b> . Read-write. Reset: 00h. Same as RestrictedCmd0
7:0	<b>restrictedcmd0</b> . Read-write. Reset: 00h. <b>Description:</b> This defines a restricted command code. If SPI_Opcode matches this register and SpiAccessRomEn and/or SpiHostAccessRomEn bit are cleared , 'Execute' bit of Index mode cannot be written, and the Index mode transfer will not occur. Note when either SpiAccessRomEn and/or SpiHostAccessRomEn bit are cleared, these registers become read-only and cannot be changed any more.

**SPIx00000008 (FCH::LPCHOSTSPIREG::SPI\_RESTRICTEDCMD2\_REGISTER)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; SPIx00000008; SPI=FEC1\_0000h

Bits	Description
31:24	<b>restrictedcmd7</b> . Read-write. Reset: 00h. Same as RestrictedCmd0
23:16	<b>restrictedcmd6</b> . Read-write. Reset: 00h. Same as RestrictedCmd0
15:8	<b>restrictedcmd5</b> . Read-write. Reset: 00h. Same as RestrictedCmd0
7:0	<b>restrictedcmd4</b> . Read-write. Reset: 00h. Same as RestrictedCmd0

**SPIx0000000C (FCH::LPCHOSTSPIREG::SPI\_CNTRL1\_REGISTER)**

Read-write. Reset: 0200\_0000h.

When either bit[22] and/or bit[23] of offset 00h are cleared, bit[31:24] of Host\_Mem\_Reg:0Ch become read-only and cannot be changed any more.

\_aliasHOSTLEGACY; SPIx0000000C; SPI=FEC1\_0000h

Bits	Description
31:24	<b>bytecommand</b> . Read-write. Reset: 02h. Specify the Byte Programmand Op Code.
23:0	Reserved.

**SPIx00000010 (FCH::LPCHOSTSPIREG::ESPI\_CNTRL\_REGISTER)**

Read-write. Reset: 0000h.

\_aliasHOSTLEGACY; SPIx00000010; SPI=FEC1\_0000h

Bits	Description
15	<b>lock_all_use_spi1.</b> Read-write. Reset: 0. when this bit set to =1, bit [15] and bit[13:8] are locked and cannot be written, it can only be written again when PSPx2E[1]: override_iSMMWrite =1, or LPC_RstB could reset it back to 0.
14	Reserved.
13	<b>romcp_use_spi1.</b> Read-write. Reset: 0. <b>Description:</b> 0: default, Host RomCopy mux on SPI0 Data/Clk, 1: Host RomCopy mux on SPI1 Data/Clk
12	<b>hfp_index_use_spi1.</b> Read-write. Reset: 0. <b>Description:</b> 0: default, HFP Index mux on SPI0 Data/Clk, 1: HFP Index mux on SPI1 Data/Clk
11	<b>psp_index_use_spi1.</b> Read-write. Reset: 0. <b>Description:</b> 0: default, <a href="#">ASP</a> Index mux on SPI0 Data/Clk, 1: ASP Index mux on SPI1 Data/Clk
10	<b>host_index_use_spi1.</b> Read-write. Reset: 0. <b>Description:</b> 0: default, Host Index mode mux on SPI0 Data/Clk, 1: Host Index mode mux on SPI1 Data/Clk
9	<b>tpm_psp_use_spi1.</b> Read-write. Reset: 0. <b>Description:</b> 0: default, TPM and <a href="#">ASP</a> mux on SPI0 Data/Clk, 1: TPM and ASP mux on SPI1 Data/Clk
8	<b>espi0_use_spi1.</b> Read-write. Reset: 0. <b>Description:</b> 0: default, eSPI0 mux on SPI0 Data/Clk, 1: eSPI0 mux on SPI1 Data/Clk.
7:2	Reserved.
1	<b>rom_addr_wr_prot.</b> Read-write. Reset: 0. <b>Description:</b> 0: ROM1/ROM2/ROM3 address registers can be written 1: ROM1/ROM2/ROM3 address registers cannot be written This bit will be write-protected once it is written 1, it can be enable for write again in <a href="#">SMI</a> , or <a href="#">ASP</a> can set PSPx2E[1]=1 to write to this register.
0	Reserved.

**SPIx00000014 (FCH::LPCHOSTSPIREG::SPI\_CMDVALUE1\_REGISTER)**

Read-write. Reset: 0000\_E2B2h.

When either bit[22] and/or bit[23] of offset 00h are cleared, bit[15:0] of Host\_Mem\_Reg:14h become read-only and cannot be changed any more.

\_aliasHOSTLEGACY; SPIx00000014; SPI=FEC1\_0000h

Bits	Description
31:16	Reserved.
15:8	<b>qpw_cmd.</b> Read-write. Reset: E2h. Command code of QPW (1-4-4 write), used to compare against the opcode sent out by the Index mode.
7:0	<b>dpw_cmd.</b> Read-write. Reset: B2h. Command code of DPW (1-2-2 write), used to compare against the opcode sent out by the Index mode.

**SPIx00000018 (FCH::LPCHOSTSPIREG::SPI\_CMDVALUE2\_REGISTER)**

Read-write. Reset: 020A\_0B03h.

When either bit[22] and/or bit[23] of offset 00h are cleared, bit[31:0] of Host\_Mem\_Reg:18h become read-only and cannot be changed any more.

\_aliasHOSTLEGACY; SPIx00000018; SPI=FEC1\_0000h

Bits	Description
31:24	<b>bytewr.</b> Read-write. Reset: 02h. This is used to compare against the opcode sent out by the Index mode. This is a predefined value to decode for the BYTEWR (byte write) command.
23:16	<b>pagewr.</b> Read-write. Reset: 0Ah. This is used to compare against the opcode sent out by the Index mode. This is a predefined value to decode for the PAGEWR (page write) command.
15:8	<b>fread.</b> Read-write. Reset: 0Bh. This is used to compare against the opcode sent out by the Index mode. This is a predefined value to decode for the Fread (fast read) command.
7:0	<b>read_cmd.</b> Read-write. Reset: 03h. This is used to compare against the opcode sent out by the Index mode. This is a predefined value to decode for the Read (Read byte) command.

**SPIx0000001C (FCH::LPCHOSTSPIREG::ROMCP\_CS\_REGISTER)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx0000001C; SPI=FEC1\_0000h

Bits	Description
7:3	Reserved.
2	<b>lock_romcp_cs.</b> Read-write. Reset: 0. When this bit is set to 1, SPIx1C[1:0] will be write protected. Once this bit is set to 1, this bit is write protected, only when PSPx2E[1] =1b can this bit be written again, or LPC_RstB could reset it back to 0.
1:0	<b>romcps.</b> Read-write. Reset: 0h. <b>Description:</b> These two bits select the alternate SPI_CS# for Romcp, these 2 bits will be write protected when SPIx00[23:22] != 11b or SPIx1C[2] =1b 00b Romcp select SPI_CS1_L 01b Romcp select SPI_CS2_L 10b Romcp select SPI_CS3_L 11b -- reserved

**SPIx0000001D (FCH::LPCHOSTSPIREG::ALT\_SPI\_CS\_REGISTER)**

Read-write. Reset: 08h.

When either bit[22] and/or bit[23] of offset 00h are cleared, bit[1:0] of Host\_Mem\_Reg:1Dh become read-only and cannot be changed any more

\_aliasHOSTLEGACY; SPIx0000001D; SPI=FEC1\_0000h

Bits	Description
7	Reserved.
6	<b>lock_spi_cs.</b> Read-write. Reset: 0. When this bit is set to 1, SPIx1D[1:0] will be write protected. Once this bit is set to 1, this bit is write protected, only when PSPx2E[1] =1b can this bit be written again, or LPC_RstB could reset it back to 0.
5	<b>spiprotectlock.</b> Read-write. Reset: 0. Once set, bits 3, 4, and 5 are no longer writeable.
4	Reserved.
3	<b>spiprotecten0.</b> Read-write. Reset: 1. Enable SPI read/write protection base on PCI reg 0x50, 0x54, 0x58, 0x5C.
2	Reserved.
1:0	<b>altspicsen.</b> Read-write. Reset: 0h. <b>Description:</b> These two bits select the alternate SPI_CS# for BIOS_ROM, these 2 bits will be write protected when SPIx00[23:22] != 11b or SPIx1D[6] =1b 00b BIOS ROM select SPI_CS1_L 01b BIOS ROM select SPI_CS2_L 10b BIOS ROM select SPI_CS3_L 11b -- reserved

**SPIx00000020 (FCH::LPCHOSTSPIREG::SPI100ENABLE\_REGISTER)**

Read-write. Reset: 3133\_0700h.

\_aliasHOSTLEGACY; SPIx00000020; SPI=FEC1\_0000h

Bits	Description
31:28	<b>normspeed.</b> Read-write. Reset: 3h. <b>Description:</b> Configure the SPI bus normal speed in new SPI100 engine. If the command is not using TpmSpeed and FastSpeed, it will use NormSpeed. The speed definition: 000: 66.66MHz 001: 33.33MHz 010: 22.22MHz 011: 16.66MHz 100: 100MHz 101: 800kHz 110: spi_spd6, defined in SPIx6C[5:0], default = 50MHz 111: spi_spd7, defined in SPIx6C[13:8], default = 4MHz
27:24	<b>fastspeednew.</b> Read-write. Reset: 1h. <b>Description:</b> Configure the SPI bus speed for the following command in new SPI100 engine: FAST READ DDR READ (1-1-2) QDR READ (1-1-4) DPR READ (1-2-2) QPR READ (1-4-4) The speed definition: 000: 66.66MHz 001: 33.33MHz 010: 22.22MHz 011: 16.66MHz 100: 100MHz 101: 800kHz 110: spi_spd6, defined in SPIx6C[5:0], default = 50MHz 111: spi_spd7, defined in SPIx6C[13:8], default = 4MHz
23:20	<b>altspeednew.</b> Read-write. Reset: 3h. <b>Description:</b> Configure the SPI bus speed for the AltOpCode mode in new SPI100 engine The speed definition: 000: 66.66MHz 001: 33.33MHz 010: 22.22MHz 011: 16.66MHz 100: 100MHz 101: 800kHz 110: spi_spd6, defined in SPIx6C[5:0], default = 50MHz 111: spi_spd7, defined in SPIx6C[13:8], default = 4MHz
19:16	<b>tpmspeed.</b> Read-write. Reset: 3h.

	<b>Description:</b> Configure the SPI bus speed for TPM read and write in new SPI100 engine. The speed definition: 000: 66.66MHz 001: 33.33MHz 010: 22.22MHz 011: 16.66MHz 100: 100MHz 101: 800kHz 110: spi_spd6, defined in SPIx6C[5:0], default = 50MHz 111: spi_spd7, defined in SPIx6C[13:8], default = 4MHz
15:12	Reserved.
11:8	<b>spicsdlysel.</b> Read-write. Reset: 7h. <b>Description:</b> 0000: 0 SPI clock cycles of SpiCs# de-assertion time. 0001: 1 SPI clock cycles of SpiCs# de-assertion time. 0010: 2 SPI clock cycles of SpiCs# de-assertion time. 0011: 3 SPI clock cycles of SpiCs# de-assertion time. 0100: 4 SPI clock cycles of SpiCs# de-assertion time. 0101: 5 SPI clock cycles of SpiCs# de-assertion time. 0110: 6 SPI clock cycles of SpiCs# de-assertion time. 0111: 7 SPI clock cycles of SpiCs# de-assertion time. 1000: 8 SPI clock cycles of SpiCs# de-assertion time. 1001: 9 SPI clock cycles of SpiCs# de-assertion time. 1010: 10 SPI clock cycles of SpiCs# de-assertion time. 1011: 11 SPI clock cycles of SpiCs# de-assertion time. 1100: 12 SPI clock cycles of SpiCs# de-assertion time. 1101: 13 SPI clock cycles of SpiCs# de-assertion time. 1110: 14 SPI clock cycles of SpiCs# de-assertion time. 1111: 15 SPI clock cycles of SpiCs# de-assertion time.
7:1	Reserved.
0	<b>usespi100.</b> Read-write. Reset: 0. <b>Description:</b> 0: Use old SPI100 engine (verified in SB900) 1: Use new SPI100 engine (new since ERIE, support 100MHz)

#### SPIx00000024 (FCH::LPCHOSTSPIREG::SPI100PRECYC0\_REGISTER)

Read-write. Reset: 0000_0000h.	
_aliasHOSTLEGACY; SPIx00000024; SPI=FEC1_0000h	
Bits	Description
31:0	Reserved.

#### SPIx00000028 (FCH::LPCHOSTSPIREG::SPI100PRECYC1\_CONFIG\_REGISTER)

Read-write. Reset: 0000_0000h.	
_aliasHOSTLEGACY; SPIx00000028; SPI=FEC1_0000h	
Bits	Description
31:0	Reserved.

**SPIx0000002C (FCH::LPCHOSTSPIREG::SPI100\_HOST\_PREFETCH\_CONFIG\_REGISTER)**

Read-write. Reset: 8000h.

**Prefetch Mechanism:**

Whenever there is read from Host, we will start to prefetch ROM data into the Host Prefetch Buffer.

The prefetch will start from the first address requested by Host, and finish when any of the following happens:

We have reached the maximum prefetch size defined in HostPrefetchSize and HostPrefOn64ByteBoundary register.

When Host requests an address that is not already prefetched and not going to be prefetched shortly, we stop current prefetch action and re-start a new prefetch with the first address being the current address requested by Host.

When there is a ROM-Write or AltOpCode request from Host, the on-going prefetch will be terminated, and the prefetch buffer will be flushed.

When there is a TPM-Write, TPM-Read, USB-Read or [EC](#)-Read request, the on-going prefetch will be halted. The contents of prefetch buffer will be preserved so that Host can access them later.

**Prefetch Prediction:**

We have logics to predict how soon the data in the current requested address will be fetched into the buffer. There are two algorithms in place. And depends on the setting of HostWillHitEn and HostHitSoonEn, we use either one of them:

"Will Hit" algorithm

We say the current requested address will be fetched "shortly" if this equation is true:

Current Requested Address  $\leq$  (First Prefetched Address + HostPrefetchSize)

"Hit Soon" algorithm

We say the current requested address will be fetched "shortly" if this equation is true:

Current Requested Address  $\leq$  (Last Prefetched Address + HostHitRange)

Of course, the current requested address also has to be equal to or larger than the first prefetched address.

If current requested address meet the criteria, the on-going prefetch will continue and Host will wait until the prefetch buffer received the requested data.

With the register default values, the prefetch behavior are:

Start prefetch only when host request on 64 byte boundary. Otherwise, get 1~4 bytes from ROM depends on byte-enable.

When there is a ROM-write or a miss, flush the prefetch buffer immediately (including on-going prefetch action).

Once a 64 byte prefetch begins, we don't stop it until all 64 bytes are fetched, unless a ROM-write or a miss happens.

"Miss" means the requested address is not in the range of the 64 bytes being prefetched.

\_aliasHOSTLEGACY; SPIx0000002C; SPI=FEC1\_0000h

Bits	Description
15	<b>rd4dw_en_host.</b> Read-write. Reset: 1. Enable host burst to 4 Dword. This bit need be =1 for SPI DMA Copy to work properly.
14:0	Reserved.

**SPIx0000002E (FCH::LPCHOSTSPIREG::TPM\_SPI\_DI\_TIMEOUT\_REGISTER)**

Read-write. Reset: 8000h.

\_aliasHOSTLEGACY; SPIx0000002E; SPI=FEC1\_0000h

Bits	Description
15:11	<b>tpm_di_to_cnt.</b> Read-write. Reset: 10h. SPI_DI_TO_counter is using 125ms Rtc8HzClk to increment, and these bits specify the timeout value. Due to synchronization, the actual delay is $N \times 125\text{ms}$ to $(N+1) \times 125\text{ms}$ . Default=16 for 2 seconds to 2.125 seconds. In spec, TIMEOUT_B is specified at 2 seconds.
10	<b>tpm_di_to_status.</b> Read-write. Reset: 0. When bit[9]=1 and TPM_DI_TO_counter reaches timeout, this bit is set to '1'. Software can write '1' to clear it., write '0' has no effect.
9	<b>tpm_di_to_enable.</b> Read-write. Reset: 0. When set to 1, if SPI_DI=0 during TPM access wait window, internal TPM_DI_TO_counter will start counting, once it reaches timeout value, internal SPI_DI will be forced to '1' to terminate TPM access, read cycle will return all '1' data, write cycle will be discarded.
8:0	Reserved.



**SPIx00000030 (FCH::LPCHOSTSPIREG::ROM2\_ADDR\_OVERRIDE\_REGISTER)**

Read-write. Reset: 14C0h.

NOTE1: When either bit[22] and/or bit[23] of offset 00h are cleared, bit[4:0] of Host\_Mem\_Reg:30h become read-only and cannot be changed any more.

NOTE2: 'ROM Address' used in this register description will be used as LPC ROM Address when LPC ROM is used, LPC ROM address does not use XOR. If SPI ROM is used, SPI ROM address [31:24] will be after XOR with offset x5C[7:0], SPIROM\_page[31:24]

\_aliasHOSTLEGACY; SPIx00000030; SPI=FEC1\_0000h

Bits	Description
15:4	Reserved.
3	<b>r2msk25.</b> Read-write. Reset: 0. When set to '1', R2VAL25 (bit[1]) will replace ROM Address[25] value when ROM2 range (defined by LPC PCIX6C[31:0]) is used to access ROM.
2	<b>r2msk24.</b> Read-write. Reset: 0. When set to '1', R2VAL24 (bit[0]) will replace ROM Address[24] value when ROM2 range (defined by LPC PCIX6C[31:0]) is used to access ROM.
1	<b>r2val25.</b> Read-write. Reset: 0. <b>Description:</b> When bit[3]=1, this bit will replace ROM Address[25] value when ROM2 range (defined by LPC PCIX6C[31:0]) is used to access ROM. When bit[3]=0, ROM Address[25] will be derived from Host Address.
0	<b>r2val24.</b> Read-write. Reset: 0. <b>Description:</b> When bit[2]=1, this bit will replace ROM Address[24] value when ROM2 range (defined by LPC PCIX6C[31:0]) is used to access ROM. When bit[2]=0, ROM Address[24] will be derived from Host Address.

**SPIx00000032 (FCH::LPCHOSTSPIREG::SPI100\_DUMMY\_CYCLE\_CONFIG\_REGISTER)**

Read-write. Reset: 4608h.

The cycle count for mode bits shall be included in the Dummy Cycle Config Register.

For example, if ROM vendor requires 4 cycles of dummy bits and 2 cycles of mode bits in QPR Read, we should put 6 in QPR\_DummyCyc[3:0] register. As a result, [FCH](#) will send 1 byte of mode bits and 2 bytes of dummy bits through Dout, Din, WP# and HOLD# pins.

NOTE:

For IndexMode, the dummy byte should be programmed into the IndexMode FIFO. The SPI100 Dummy Cycle Config Registers are not for IndexMode dummy bytes.

\_aliasHOSTLEGACY; SPIx00000032; SPI=FEC1\_0000h

Bits	Description
15:12	<b>dpr_dummycyc.</b> Read-write. Reset: 4h. Configure dummy cycle count for DPR READ (1-2-2) command. The cycle count shall include the cycle counts for both mode bits and dummy bits. (See NOTE)
11:8	<b>qpr_dummycyc.</b> Read-write. Reset: 6h. Configure dummy cycle count for QPR READ (1-4-4) command. The cycle count shall include the cycle counts for both mode bits and dummy bits. (See NOTE)
7:5	Reserved.
4:0	<b>fastread_dummycyc.</b> Read-write. Reset: 08h. Configure dummy cycle count for FAST READ command.

**SPIx00000034 (FCH::LPCHOSTSPIREG::SPI100\_RX\_TIMING\_CONFIG0\_REGISTER)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; SPIx00000034; SPI=FEC1\_0000h

Bits	Description
31:7	Reserved.
6	<b>dis_index_flush_rbuf.</b> Read-write. Reset: 0. <b>Description:</b> 0: Index access will flush prefetch buffer 1: Index access will not flush prefetch buffer
5	Reserved.
4	<b>flushhostprefetch.</b> Read-write. Reset: 0. If SW wants to flush the SPI100 Host prefetch buffer, SW can set this bit and then clear it.
3:0	Reserved.

**SPIx00000040 (FCH::LPCHOSTSPIREG::DDRCMDCODE)**

Read-write. Reset: 3Bh.

\_aliasHOSTLEGACY; SPIx00000040; SPI=FEC1\_0000h

Bits	Description
7:0	<b>ddr_cmd.</b> Read-write. Reset: 3Bh. Command code of DDR (1-1-2 read)

**SPIx00000041 (FCH::LPCHOSTSPIREG::QDRCMDCODE)**

Read-write. Reset: 6Bh.

\_aliasHOSTLEGACY; SPIx00000041; SPI=FEC1\_0000h

Bits	Description
7:0	<b>qdr_cmd.</b> Read-write. Reset: 6Bh. Command code of QDR (1-1-4 read)

**SPIx00000042 (FCH::LPCHOSTSPIREG::DPRCMDCODE)**

Read-write. Reset: BBh.

\_aliasHOSTLEGACY; SPIx00000042; SPI=FEC1\_0000h

Bits	Description
7:0	<b>dpr_cmd.</b> Read-write. Reset: BBh. Command code of DPR (1-2-2 read)

**SPIx00000043 (FCH::LPCHOSTSPIREG::QPRCMDCODE)**

Read-write. Reset: EBh.

When either bit[22] and/or bit[23] of offset 00h are cleared, bit[31:0] of Host\_Mem\_Reg:40h become read-only and cannot be changed any more.

\_aliasHOSTLEGACY; SPIx00000043; SPI=FEC1\_0000h

Bits	Description
7:0	<b>qpr_cmd.</b> Read-write. Reset: EBh. Command code of QPR (1-4-4 read)

**SPIx00000044 (FCH::LPCHOSTSPIREG::MODEBYTE)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx00000044; SPI=FEC1\_0000h

Bits	Description
7:0	<b>modebyte.</b> Read-write. Reset: 00h. Whenever DPR_CMD or QPR_CMD is used, ModeByte is also sent out onto the SPI stream

**SPIx00000045 (FCH::LPCHOSTSPIREG::CMDCODE)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx00000045; SPI=FEC1\_0000h

Bits	Description
7:0	<b>spi_opcode.</b> Read-write. Reset: 00h. When software uses the alternate program method to communicate with the SPI ROM, this register contains the OPCODE (command code).

**SPIx00000047 (FCH::LPCHOSTSPIREG::CMDTRIGGER)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx00000047; SPI=FEC1\_0000h

Bits	Description
7	<b>execute.</b> Read-write. Reset: 0. <b>Description:</b> Write 1 to execute the transaction in the alternate program registers. Writing 0 has no effect. When the transaction is complete, this bit will return 0. If the command is an illegal command, the bit cannot be set and thereby cannot execute. Note: before set Execute=1 software should read Host_Mem_Regx4C[31]: SpiBusy=0 to make sure no SPI operation is going on.
6:0	Reserved.

**SPIx00000048 (FCH::LPCHOSTSPIREG::TXBYTECOUNT)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx00000048; SPI=FEC1\_0000h

Bits	Description
7:0	<b>txbytecount.</b> Read-write. Reset: 00h. Number of bytes to be sent to SPI ROM in Index mode. This number does not include SPI_OpCode specified in offset 0x45

**SPIx0000004B (FCH::LPCHOSTSPIREG::RXBYTECOUNT)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx0000004B; SPI=FEC1\_0000h

Bits	Description
7:0	<b>rxbytecount.</b> Read-write. Reset: 00h. Number of bytes to be received from the SPI ROM in Index mode.

**SPIx0000004C (FCH::LPCHOSTSPIREG::SPISTATUS)**

Read-only. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; SPIx0000004C; SPI=FEC1\_0000h

Bits	Description
31	<b>spibusy.</b> Read-only. Reset: 0. <b>Description:</b> 1: Spi bus is busy 0: Spi busy is idle
30:8	Reserved.
7:0	<b>donebytecount.</b> Read-only. Reset: 00h. Indicate how many bytes has been received or sent in previous spi transaction

**SPIx00000050 (FCH::LPCHOSTSPIREG::ADDR32CTRL0)**

Read-write. Reset: 0C13\_1200h.

When either bit[22] and/or bit[23] of offset 00h are cleared, bit[31:1] of Host\_Mem\_Reg:50h become read-only and cannot be changed any more.

\_aliasHOSTLEGACY; SPIx00000050; SPI=FEC1\_0000h

Bits	Description
31:24	<b>freadcmd_addr_32.</b> Read-write. Reset: 0Ch. Fast Read Command Code of 32-bit address mode
23:16	<b>readcmd_addr_32.</b> Read-write. Reset: 13h. Read Command Code of 32-bit address mode
15:8	<b>bytewrcmd_addr_32.</b> Read-write. Reset: 12h. Byte Program Command Code of 32-bit address mode
7:1	Reserved.
0	<b>spi_rom_addr_32.</b> Read-write. Reset: 0. <b>Description:</b> 0: 24-bit address SPI ROM 1: 32-bit address SPI ROM This bit can only be changed when Host_Mem_Regx00[31]: SpiBusy =0, since this bit will affect Host Address to SPI ROM address mapping. This bit is write-protect when PSPxFC[14] =1

**SPIx00000054 (FCH::LPCHOSTSPIREG::ADDR32CTRL1)**

Read-write. Reset: ECBC\_6C3Ch.

When either bit[22] and/or bit[23] of offset 00h are cleared, bit[31:0] of Host\_Mem\_Reg:54h become read-only and cannot be changed any more.

\_aliasHOSTLEGACY; SPIx00000054; SPI=FEC1\_0000h

Bits	Description
31:24	<b>qpr_cmd_addr_32.</b> Read-write. Reset: ECh. QPR (1-4-4) Command Code of 32-bit address mode
23:16	<b>dpr_cmd_addr_32.</b> Read-write. Reset: BCh. DPR (1-2-2) Command Code of 32-bit address mode
15:8	<b>qdr_cmd_addr_32.</b> Read-write. Reset: 6Ch. QDR (1-1-4) Command Code of 32-bit address mode
7:0	<b>ddr_cmd_addr_32.</b> Read-write. Reset: 3Ch. DDR (1-1-2) Command Code of 32-bit address mode

**SPIx00000058 (FCH::LPCHOSTSPIREG::ADDR32CTRL2)**

Read-write. Reset: 0000\_4608h.

\_aliasHOSTLEGACY; SPIx00000058; SPI=FEC1\_0000h

Bits	Description
31:16	Reserved.
15:12	<b>dpr_dummycyc_addr_32.</b> Read-write. Reset: 4h. Configure dummy cycle count for DPR READ (1-2-2) command in 32-bit address mode (24-bit address mode at 0x32[15:12]).
11:8	<b>qpr_dummycyc_addr_32.</b> Read-write. Reset: 6h. Configure dummy cycle count for QPR READ (1-4-4) command in 32-bit address mode (24-bit address mode at 0x32[11:8]).
7:5	Reserved.
4:0	<b>fastread_dummycyc_addr_32.</b> Read-write. Reset: 08h. Configure dummy cycle count for FAST READ command in 32-bit address mode (24-bit address mode at 0x32[4:0])

**SPIx0000005C (FCH::LPCHOSTSPIREG::ADDR32CTRL3)**

Read-write. Reset: 0000\_0000h.

When either bit[22] and/or bit[23] of offset 00h are cleared, bit[7:0] of Host\_Mem\_Reg:5Ch become read-only and cannot be changed any more.

\_aliasHOSTLEGACY; SPIx0000005C; SPI=FEC1\_0000h

Bits	Description
31:8	Reserved.
7:0	<b>spirom_page_31_24.</b> Read-write. Reset: 00h. <b>Description:</b> Used for 32-bit address mode, produce SPIROMAddr[31:24] use XOR. SPIROMAddr[31:24] = SPI_ROM_page[31:24] ^ HostMemAddr[31:24] These bits can only be changed when Host_Mem_Regx00[31]: SpiBusy =0, since these bits will affect Host Address to SPI ROM address mapping.

**SPIx00000060 (FCH::LPCHOSTSPIREG::BAR\_64MB\_ROM3\_LOW)**

Read-write. Reset: 0000\_0000h.

When either bit[22] and/or bit[23] of offset 00h are cleared, bit[31:26] of Host\_Mem\_Reg:60h become read-only and cannot be changed any more.

\_aliasHOSTLEGACY; SPIx00000060; SPI=FEC1\_0000h

Bits	Description
31:26	<b>bar_64mb_31_26.</b> Read-write. Reset: 00h. Specify Base address [31:26] of 64MB BIOS ROM space.
25:0	Reserved.

**SPIx00000064 (FCH::LPCHOSTSPIREG::BAR\_64MB\_ROM3\_HIGH)**

Read-write. Reset: 0000\_00FDh.

When either bit[22] and/or bit[23] of offset 00h are cleared, bit[31:0] of Host\_Mem\_Reg:64h become read-only and cannot be changed any more.

\_aliasHOSTLEGACY; SPIx00000064; SPI=FEC1\_0000h

Bits	Description
31:0	<b>bar_64mb_63_32.</b> Read-write. Reset: 0000_00FDh. Specify Base address [63:32] of 64MB BIOS ROM space.

**SPIx00000068 (FCH::LPCHOSTSPIREG::SPI\_RESTRICTEDCMD3\_REGISTER)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; SPIx00000068; SPI=FEC1\_0000h

Bits	Description
31:24	<b>restrictedcmd11.</b> Read-write. Reset: 00h. Same as RestrictedCmd0
23:16	<b>restrictedcmd10.</b> Read-write. Reset: 00h. Same as RestrictedCmd0
15:8	<b>restrictedcmd9.</b> Read-write. Reset: 00h. Same as RestrictedCmd0
7:0	<b>restrictedcmd8.</b> Read-write. Reset: 00h. Same as RestrictedCmd0

**SPIx0000006C (FCH::LPCHOSTSPIREG::SPISPEED)**

Read-write. Reset: 3204h.

\_aliasHOSTLEGACY; SPIx0000006C; SPI=FEC1\_0000h

Bits	Description
15:14	Reserved.
13:8	<b>spi_spd7.</b> Read-write. Reset: 32h. <b>Description:</b> This register define SPI clock frequency when speed = 0x7 is specified in NormSpeed(offset 0x20[31:28]), FastSpeedNew(offset 0x20[27:24]), AltSpeedNew(offset 0x20[23:20]), TpmSpeed(offset 0x20[19:16]). For register value definition, please refer to bit[5:0] of this register
7:6	Reserved.
5:0	<b>spi_spd6.</b> Read-write. Reset: 04h. <b>Description:</b> This register define SPI clock frequency when speed = 0x6 is specified in NormSpeed(offset 0x20[31:28]), FastSpeedNew(offset 0x20[27:24]), AltSpeedNew(offset 0x20[23:20]), TpmSpeed(offset 0x20[19:16]). With value = N in this register, SPI clock = 200MHz/N Value 0 3 are not allowed to write to this register, hardware will write 0x4 if software is writing 0 3 to this register 0x4: 50MHz, 200MHz/4 0x32: 4MHz, 200MHz/50 0x3f: 3.17MHz, 200MHz/63

**SPIx00000070 (FCH::LPCHOSTSPIREG::HOST\_INT)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; SPIx00000070; SPI=FEC1\_0000h

Bits	Description
31:24	Reserved.
23:16	<b>host_int_enable.</b> Read-write. Reset: 00h. <b>Description:</b> 0: event occurrence will not set Host_Int_status 1: event occurrence will set Host_Int_status
15:8	<b>host_int_mask.</b> Read-write. Reset: 00h. <b>Description:</b> 0: associated Host_Int_status =1 will generate LPC_SPI_INT 1: mask interrupt when Host_Int_Status =1
7:0	<b>host_int_status.</b> Read-write. Reset: 00h. <b>Description:</b> Each bit will set to '1' when event occur and corresponding Host_Int_enable =1, software need write '1' to clear it. [0]: Host Index transfer done [1]: DMA Romcp done [7:2]: reserved

**SPIx00000074 (FCH::LPCHOSTSPIREG::LPC\_SPI\_INT)**

Read-only. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; SPIx00000074; SPI=FEC1\_0000h

Bits	Description
31:16	Reserved.
15:8	<b>hid_int_status.</b> Read-only. Reset: 00h. <b>Description:</b> HID interrupt normally route to MP2 (HIDx150[15] =0), and bit[15:8] will always read back 0x00. When HID interrupt route to Host (HIDx150[15] =1), bit[15:8] are HID Interrupt status, software can read these bits to find Interrupt source. To clear those HID interrupt status, software need write to HIDx154 [8]: HID Index transfer done [9]: HID DMA Copy done [10]: HID-basic-write done [11]: HID-basic-read done [12]: HID-acc-write done [13]: HID-acc-read done [14]: HID Int_do_DMA_acc_rd done [15]: HID device IRQ input
7:4	Reserved.
3	<b>psp_index_int.</b> Read-only. Reset: 0. If read '1', PSP_Index_Int is active, to clear it, write PSPx70[0] =1
2	<b>hpf_index_int.</b> Read-only. Reset: 0. If read '1', HFP_Index_Int is active, to clear it, write HFPx70[0] =1
1	<b>romcp_int.</b> Read-only. Reset: 0. If read '1', Romcp_Int is active, to clear it, write SPIx70[1] =1
0	<b>host_index_int.</b> Read-only. Reset: 0. If read '1', Host_Index_Int is active, to clear it, write SPIx70[0] =1

**SPIx00000078 (FCH::LPCHOSTSPIREG::FLASH\_IDLE\_CNT)**

Read-write. Reset: 0000\_0064h.

\_aliasHOSTLEGACY; SPIx00000078; SPI=FEC1\_0000h

Bits	Description
31:18	Reserved.
17	<b>flash_idle_cnt_to.</b> Read-write. Reset: 0. <b>Description:</b> Set to =1 when Flash Idle Counter TimeOut occur. Software write 1 to clear, write 0 have no function.
16	<b>flash_idle_cnt_enable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Flash Idle Counter is not enabled. 1: Flash Idle Counter is enabled. While this bit =1 and counter is counting, if software write this bit =0 before counter reaches TimeOut, counter will be stopped, and reset to 0.
15	Reserved.
14:8	<b>flash_idle_cnt_rd.</b> Read-write. Reset: 00h. Read Only, value of current Flash IDLE Counter
7	Reserved.
6:0	<b>flash_idle_cnt_to_val.</b> Read-write. Reset: 64h. <b>Description:</b> Time out value of Flash Idle Counter. Flash Idle Counter uses 1us clock to count. When counter is enabled (bit[16] =1) and time out occur, bit[17] will be set, and fch_secured_intr10 will assert, bit[16] will be cleared and counter will be reset to =0. If counter is enabled and counting, counter will be reset to =0 when there is SPI transaction to Flash, counter will resume counting from =0 when SPI transaction to Flash finished. default = 0x64 which is 100us. Max value is 0x7f which is 127us.

**SPIx00000080 (FCH::LPCHOSTSPIREG::FIFO0)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx00000080; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata.</b> Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx00000081 (FCH::LPCHOSTSPIREG::FIFO1)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx00000081; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata.</b> Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx00000082 (FCH::LPCHOSTSPIREG::FIFO2)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx00000082; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata.</b> Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx00000083 (FCH::LPCHOSTSPIREG::FIFO3)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx00000083; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata.</b> Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx00000084 (FCH::LPCHOSTSPIREG::FIFO4)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx00000084; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata</b> . Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx00000085 (FCH::LPCHOSTSPIREG::FIFO5)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx00000085; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata</b> . Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx00000086 (FCH::LPCHOSTSPIREG::FIFO6)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx00000086; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata</b> . Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx00000087 (FCH::LPCHOSTSPIREG::FIFO7)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx00000087; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata</b> . Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx00000088 (FCH::LPCHOSTSPIREG::FIFO8)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx00000088; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata</b> . Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx00000089 (FCH::LPCHOSTSPIREG::FIFO9)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx00000089; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata</b> . Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx0000008A (FCH::LPCHOSTSPIREG::FIFO10)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx0000008A; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata</b> . Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.



**SPIx0000008B (FCH::LPCHOSTSPIREG::FIFO11)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx0000008B; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata.</b> Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx0000008C (FCH::LPCHOSTSPIREG::FIFO12)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx0000008C; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata.</b> Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx0000008D (FCH::LPCHOSTSPIREG::FIFO13)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx0000008D; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata.</b> Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx0000008E (FCH::LPCHOSTSPIREG::FIFO14)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx0000008E; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata.</b> Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx0000008F (FCH::LPCHOSTSPIREG::FIFO15)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx0000008F; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata.</b> Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx00000090 (FCH::LPCHOSTSPIREG::FIFO16)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx00000090; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata.</b> Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx00000091 (FCH::LPCHOSTSPIREG::FIFO17)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx00000091; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata.</b> Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx00000092 (FCH::LPCHOSTSPIREG::FIFO18)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx00000092; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata.</b> Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx00000093 (FCH::LPCHOSTSPIREG::FIFO19)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx00000093; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata.</b> Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx00000094 (FCH::LPCHOSTSPIREG::FIFO20)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx00000094; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata.</b> Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx00000095 (FCH::LPCHOSTSPIREG::FIFO21)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx00000095; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata.</b> Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx00000096 (FCH::LPCHOSTSPIREG::FIFO22)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx00000096; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata.</b> Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx00000097 (FCH::LPCHOSTSPIREG::FIFO23)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx00000097; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata.</b> Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx00000098 (FCH::LPCHOSTSPIREG::FIFO24)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx00000098; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata.</b> Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx00000099 (FCH::LPCHOSTSPIREG::FIFO25)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx00000099; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata.</b> Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx0000009A (FCH::LPCHOSTSPIREG::FIFO26)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx0000009A; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata.</b> Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx0000009B (FCH::LPCHOSTSPIREG::FIFO27)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx0000009B; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata.</b> Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx0000009C (FCH::LPCHOSTSPIREG::FIFO28)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx0000009C; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata.</b> Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx0000009D (FCH::LPCHOSTSPIREG::FIFO29)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx0000009D; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata.</b> Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx0000009E (FCH::LPCHOSTSPIREG::FIFO30)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx0000009E; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata.</b> Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx0000009F (FCH::LPCHOSTSPIREG::FIFO31)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx0000009F; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata.</b> Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx000000A0 (FCH::LPCHOSTSPIREG::FIFO32)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx000000A0; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata</b> . Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx000000A1 (FCH::LPCHOSTSPIREG::FIFO33)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx000000A1; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata</b> . Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx000000A2 (FCH::LPCHOSTSPIREG::FIFO34)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx000000A2; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata</b> . Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx000000A3 (FCH::LPCHOSTSPIREG::FIFO35)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx000000A3; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata</b> . Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx000000A4 (FCH::LPCHOSTSPIREG::FIFO36)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx000000A4; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata</b> . Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx000000A5 (FCH::LPCHOSTSPIREG::FIFO37)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx000000A5; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata</b> . Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx000000A6 (FCH::LPCHOSTSPIREG::FIFO38)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx000000A6; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata</b> . Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx000000A7 (FCH::LPCHOSTSPIREG::FIFO39)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx000000A7; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata</b> . Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx000000A8 (FCH::LPCHOSTSPIREG::FIFO40)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx000000A8; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata</b> . Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx000000A9 (FCH::LPCHOSTSPIREG::FIFO41)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx000000A9; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata</b> . Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx000000AA (FCH::LPCHOSTSPIREG::FIFO42)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx000000AA; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata</b> . Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx000000AB (FCH::LPCHOSTSPIREG::FIFO43)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx000000AB; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata</b> . Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx000000AC (FCH::LPCHOSTSPIREG::FIFO44)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx000000AC; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata</b> . Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx000000AD (FCH::LPCHOSTSPIREG::FIFO45)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx000000AD; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata</b> . Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx000000AE (FCH::LPCHOSTSPIREG::FIFO46)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx000000AE; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata.</b> Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx000000AF (FCH::LPCHOSTSPIREG::FIFO47)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx000000AF; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata.</b> Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx000000B0 (FCH::LPCHOSTSPIREG::FIFO48)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx000000B0; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata.</b> Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx000000B1 (FCH::LPCHOSTSPIREG::FIFO49)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx000000B1; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata.</b> Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx000000B2 (FCH::LPCHOSTSPIREG::FIFO50)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx000000B2; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata.</b> Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx000000B3 (FCH::LPCHOSTSPIREG::FIFO51)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx000000B3; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata.</b> Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx000000B4 (FCH::LPCHOSTSPIREG::FIFO52)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx000000B4; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata.</b> Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx000000B5 (FCH::LPCHOSTSPIREG::FIFO53)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx000000B5; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata</b> . Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx000000B6 (FCH::LPCHOSTSPIREG::FIFO54)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx000000B6; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata</b> . Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx000000B7 (FCH::LPCHOSTSPIREG::FIFO55)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx000000B7; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata</b> . Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx000000B8 (FCH::LPCHOSTSPIREG::FIFO56)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx000000B8; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata</b> . Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx000000B9 (FCH::LPCHOSTSPIREG::FIFO57)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx000000B9; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata</b> . Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx000000BA (FCH::LPCHOSTSPIREG::FIFO58)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx000000BA; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata</b> . Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx000000BB (FCH::LPCHOSTSPIREG::FIFO59)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx000000BB; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata</b> . Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx000000BC (FCH::LPCHOSTSPIREG::FIFO60)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx000000BC; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata.</b> Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx000000BD (FCH::LPCHOSTSPIREG::FIFO61)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx000000BD; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata.</b> Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx000000BE (FCH::LPCHOSTSPIREG::FIFO62)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx000000BE; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata.</b> Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx000000BF (FCH::LPCHOSTSPIREG::FIFO63)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx000000BF; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata.</b> Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx000000C0 (FCH::LPCHOSTSPIREG::FIFO64)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx000000C0; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata.</b> Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx000000C1 (FCH::LPCHOSTSPIREG::FIFO65)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx000000C1; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata.</b> Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx000000C2 (FCH::LPCHOSTSPIREG::FIFO66)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx000000C2; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata.</b> Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.



**SPIx000000C3 (FCH::LPCHOSTSPIREG::FIFO67)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx000000C3; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata</b> . Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx000000C4 (FCH::LPCHOSTSPIREG::FIFO68)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx000000C4; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata</b> . Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx000000C5 (FCH::LPCHOSTSPIREG::FIFO69)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx000000C5; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata</b> . Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx000000C6 (FCH::LPCHOSTSPIREG::FIFO70)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx000000C6; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata</b> . Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx000000C7 (FCH::LPCHOSTSPIREG::FIFO71)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; SPIx000000C7; SPI=FEC1\_0000h

Bits	Description
7:0	<b>fifodata</b> . Read-write. Reset: 00h. Data FiFo byte N which used in command mode to send or receive data. These FIFO can be written/read in Double-word, Word, or Byte.

**SPIx000000FC (FCH::LPCHOSTSPIREG::SPI\_MISCCNTRL)**

Read-write. Reset: 0000h.

\_aliasHOSTLEGACY; SPIx000000FC; SPI=FEC1\_0000h

Bits	Description
15:11	Reserved.
10	<b>psp_own_spi</b> . Read-write. Reset: 0. Read Only. Value of PSPxFC[5]
9	<b>hfp_own_spi</b> . Read-write. Reset: 0. Read Only. Value of HFPxFC[5]
8	Reserved.
7	<b>en_map_spi_bx_to_cfg</b> . Read-write. Reset: 0. When set to 1, write/read to SPIxB0 xBF will be map to write/read LPC PCICFGxB0 xBF. This will allow processor to do SPI DMA Copy (controlled by LPC PCICFGxB0 xB9) through SPI Register space.
6	<b>romcp_new_scheme</b> . Read-write. Reset: 0. <b>Description:</b> Set to '1' to allow direct or Index mode memory read to SPI ROM to be 'inserted' between SPI DMA Copy cache line transfer If this bit is '0', software should not do any SPI Memory read during SPI DMA Copy operation
5	<b>hbios_spimutex</b> . Read-write. Reset: 0. <b>Description:</b> 0: Host-BIOS doesn't own SpiMutex 1: Host-BIOS owns SpiMutex Host-BIOS can't write the bit to 1 if the SpiMutex is owned by <a href="#">ASP</a> (PSPxFC[5]=1) or Host-FP (HFPxFC[5]=1)
4:0	Reserved.

**11.3.8.2 eSPI Registers**

The [MMIO](#) base address for accessing eSPI registers is defined in SPI BASE ADDR register .

**ESPI1SMNx00000000...ESPISMNx00000000 (FCH::ITF::ESPI::DN\_TXHDR\_0th)**

Reset: 0020\_0000h.

\_link1\_aliasSMN; ESPI1SMNx00000000; ESPI1SMN=02DCA000h

\_link0\_aliasSMN; ESPISMNx00000000; ESPISMN=02DC5000h

\_link1\_aliasHOSTLEGACY; ESPI1x00000000; ESPI1=FEC30000h

\_link0\_aliasHOSTLEGACY; ESPIx00000000; ESPI=FEC20000h

Bits	Description
31:24	<b>DNCMD_HDATA2.</b> Read-write. Reset: 00h. <b>Description:</b> The definition for this field is depended on SW_CMD_TYPE Independent channel command selected: Reserved, Always be 00h Peripheral selected : Length[7:0] VW selected: Reserved, Always be 00h OOB selected: Length[7:0] FLASH selected: Length[7:0]
23:16	<b>DNCMD_HDATA1.</b> Read-write. Reset: 20h. <b>Description:</b> The definition for this field is depended on SW_CMD_TYPE Independent channel command selected: Addres [7:0] of SET_CONFIGURATION/GET_CONFIGURATION Bit[1:0] needs to be 00. Note: In-Band command. These bits are ignored. Peripheral selected [23:20]: Tag [19:16]: Length[11:8] VW selected: Reserved, Always be 00h OOB selected: [23:20]: Tag [19:16]: Length[11:8] FLASH selected: [23:20]: Tag [19:16]: Length[11:8]
15:8	<b>DNCMD_HDATA0.</b> Read-write. Reset: 00h. <b>Description:</b> The definition for this field is depended on SW_CMD_TYPE. Independent command selected: Address [15:8] of SET_CONFIGURATION/GET_CONFIGURATION. [15:12]:0h [11:8]: address[11:8] Note: In-Band command. These bits are ignored. Peripheral selected: a) SW programs this byte to be Message cycle type(0001xxxy) to instruct the eSPI controller send down peripheral message with data(8 bytes+data byte N) or without data(total 8 bytes) b) SW programs this byte to be 'nsuccessful completion to instruct the eSPI controller send down unsuccessful completion VW selected: It indicates the Virtual Wire Count will be send down. Bit[5:0] represends how many Virtual Wire groups to be commnunicated in the same packets. NOTE: In the current design, it is limited to 16 groups(bit[5:4]=00) to save the registers needed. Only 8 indexes are defined In current eSPI spec v0.7. OOB selected: SW programs this byte to be 0x21 to instruct the eSPI controller send send down Tunneled SMBUS message to slave FLASH selected: For MAFS:SW prgrames this byte to be CycleType for Flash Completion, including Cpl/Unsuccessful Cpl/CplD. For SAFS:SW prgrames this byte to be CycleType for FLASH read/write/erase
7:5	Reserved.
4	<b>PUT_FLASH_NP_TRAN_ACTIVE.</b> Read-only. Reset: 0.

	<p><b>Description:</b> SW i/f programming PUT_FLASH_NP transmission active bit. This bit tells whether the PUT_FLASH_NP transmit is done or not. Generally it shall be set once bit [3] is set. When the PUT_FLASH_NP is deferred, bit[3] is cleared but this bit shall keep asserted until the deferred transaction is complete.</p> <p>0b: No PUT_FLASH_NP transmit on-going.</p> <p>1b: PUT_FLASH_NP_transmit on-going.</p>
3	<p><b>DNCMD_STATUS.</b> Read,<a href="#">Write-1-only</a>. Reset: 0.</p> <p><b>Description:</b> The bit needs to be set to 1 last by software after all eSPI specific registers are programmed to inform the protocol layer to send down command or packet, and hardware will automatically clear this bit to 0 after the packet is sent down.</p> <p>Note: If a SAFS downstream command is deferred, the hardware will automatically clear this bit. But bit[4] (PUT_FLASH_NP_TRAN_ACTIVE) will not be cleared by hardware until the SAFS downstream command is completed.</p>
2:0	<p><b>DNCMD_TYPE.</b> Read-write. Reset: 0h.</p> <p><b>Description:</b> TX Command Type:</p> <p>000: Set Configuration (Independent command)</p> <p>001: Get Configuration (Independent command)</p> <p>010: In-band RESET command (Independent command)</p> <p>011: reserved</p> <p>100: Peripheral Channel message down stream</p> <p>101: VW Channel down stream</p> <p>110: <a href="#">OOB</a> Channel down stream</p> <p>111: For MAFS:Flash Channel Cpl/CplD/Unsuccessful Cpl down stream. For SAFS:Flash Channel Request downstream</p>

**ESPI1SMNx00000004...ESPISMNx00000004 (FCH::ITF::ESPI::DN\_TXHDR\_1)**

Read-write. Reset: 0000\_0000h.

[\\_link1\\_aliasSMN](#); ESPI1SMNx00000004; ESPI1SMN=02DCA000h[\\_link0\\_aliasSMN](#); ESPISMNx00000004; ESPISMN=02DC5000h[\\_link1\\_aliasHOSTLEGACY](#); ESPI1x00000004; ESPI1=FEC30000h[\\_link0\\_aliasHOSTLEGACY](#); ESPIx00000004; ESPI=FEC20000h

Bits	Description
31:24	<b>DNCMD_HDATA6.</b> Read-write. Reset: 00h. <b>Description:</b> The definition for this field is depended on SW_CMD_TYPE Independent channel command selected: data[31:24] Peripheral selected : Message specific byte 2 VW selected: Reserved, Always be 00h <a href="#">OOB</a> selected: Reserved, Always be 00h FLASH selected: For MAFS: Reserved, Always be 00h For SAFS: If Cycle Type is FLASH_WRITE, FLASH_READ, FLAS_ERASE, this field is Address[31:24]. If Cycle Type is FLASH_RPMC_OP1 (R1R0 = 0x0) or FLASH_RPMC_RPMC_OP2, this field is reserved. If Cycle Type is FLASH_RPMC_OP1 (R1R0 = 0x1/2/3), this field is data byte 0.
23:16	<b>DNCMD_HDATA5.</b> Read-write. Reset: 00h. <b>Description:</b> The definition for this field is depended on SW_CMD_TYPE Independent channel command selected: data[23:16] Peripheral selected : Message specific byte 1 VW selected: Reserved, Always be 00h <a href="#">OOB</a> selected: <a href="#">SMBus</a> Byte Count. Need to program not greater than 128bytes FLASH selected: For MAFS: Reserved, Always be 00h For SAFS: If Cycle Type is FLASH_WRITE, FLASH_READ, FLAS_ERASE, this field is Address[23:16]. If Cycle Type is FLASH_RPMC_OP1 (R1R0 = 0x0) or FLASH_RPMC_RPMC_OP2, this field is reserved. If Cycle Type is FLASH_RPMC_OP1 (R1R0 = 0x1/2/3), this field is data byte 1.
15:8	<b>DNCMD_HDATA4.</b> Read-write. Reset: 00h. <b>Description:</b> The definition for this field is depended on SW_CMD_TYPE Independent channel command selected: data[15:8] Peripheral selected : Message specific byte 0 VW selected: Reserved, Always be 00h <a href="#">OOB</a> selected: <a href="#">SMBus</a> Command Op Code. FLASH selected: For MAFS: Reserved, Always be 00h For SAFS: If Cycle Type is FLASH_WRITE, FLASH_READ, FLAS_ERASE, this field is Address[15:8]. If Cycle Type is FLASH_RPMC_OP1 (R1R0 = 0x0) or FLASH_RPMC_RPMC_OP2, this field is reserved. If Cycle Type is FLASH_RPMC_OP1 (R1R0 = 0x1/2/3), this field is data byte 2.
7:0	<b>DNCMD_HDATA3.</b> Read-write. Reset: 00h.

	<p><b>Description:</b> The definition for this field is depended on SW_CMD_TYPE</p> <p>Independent channel command selected: data[7:0]</p> <p>Peripheral selected : Message code [7:0]</p> <p>VW selected: Reserved, Always be 00h</p> <p><a href="#">OOB</a> selected:</p> <p><a href="#">SMBus</a> Slave Address. Bit[0] needs to program to 1</p> <p>FLASH selected:</p> <p>For MAFS:</p> <p>Reserved, Always be 00h</p> <p>For SAFS:</p> <p>If Cycle Type is FLASH_WRITE, FLASH_READ, FLAS_ERASE, this field is Address[7:0].</p> <p>If Cycle Type is FLASH_RPMC_OP1 (R1R0 = 0x0) or FLASH_RPMC_RPMC_OP2, this field is reserved.</p> <p>If Cycle Type is FLASH_RPMC_OP1 (R1R0 = 0x1/2/3), this field is data byte 3.</p>
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#### ESPI1SMNx00000008...ESPISMNx00000008 (FCH::ITF::ESPI::DN\_TXHDR\_2)

Read-write. Reset: 0000\_0000h.

\_link1\_aliasSMN; ESPI1SMNx00000008; ESPI1SMN=02DCA000h

\_link0\_aliasSMN; ESPISMNx00000008; ESPISMN=02DC5000h

\_link1\_aliasHOSTLEGACY; ESPI1x00000008; ESPI1=FEC30000h

\_link0\_aliasHOSTLEGACY; ESPIx00000008; ESPI=FEC20000h

Bits	Description
31:8	Reserved.
7:0	<p><b>DNCMD_HDATA7.</b> Read-write. Reset: 00h.</p> <p><b>Description:</b> The definition for this field is depended on SW_CMD_TYPE</p> <p>Independent channel command selected: Reserved, Always be 00h</p> <p>Peripheral selected : Message specific byte 3</p> <p>VW selected: Reserved, Always be 00h</p> <p><a href="#">OOB</a> selected: Reserved, Always be 00h</p> <p>FLASH selected: Reserved, Always be 00h</p>

**ESPI1SMNx0000000C...ESPISMNx0000000C (FCH::ITF::ESPI::DN\_TXDATA\_PORT)**

Read-write. Reset: 0000\_0000h.

\_link1\_aliasSMN; ESPI1SMNx0000000C; ESPI1SMN=02DCA000h\_link0\_aliasSMN; ESPISMNx0000000C; ESPISMN=02DC5000h\_link1\_aliasHOSTLEGACY; ESPI1x0000000C; ESPI1=FEC30000h\_link0\_aliasHOSTLEGACY; ESPIx0000000C; ESPI=FEC20000h**Bits Description**31:24 **DN\_TXDATA\_B3**. Read-write. Reset: 00h.**Description:** The definition for this field is depended on SW\_CMD\_TYPE

Independent channel command selected: Reserved, Always be 00h

Peripheral selected : Message Data DWn[31:24]

VW selected: VW Index Group 2n+1 data

[OOB](#) selected: OOB Message DWn[31:24]

FLASH selected: For MAFS:Flash Cpl Data DWn[31:24] For SAFS:Flash write data [31:24]

23:16 **DN\_TXDATA\_B2**. Read-write. Reset: 00h.**Description:** The definition for this field is depended on SW\_CMD\_TYPE

Independent channel command selected: Reserved, Always be 00h

Peripheral selected : Message Data DWn[23:16]

VW selected: VW Index Group 2n+1

[OOB](#) selected: OOB Message DWn[23:16]

FLASH selected: For MAFS:Flash Cpl Data DWn[23:16] For SAFS:Flash write data [23:16]

15:8 **DN\_TXDATA\_B1**. Read-write. Reset: 00h.**Description:** The definition for this field is depended on SW\_CMD\_TYPE

Independent channel command selected: Reserved, Always be 00h

Peripheral selected : Message Data DWn[15:8]

VW selected: VW Index Group 2n Data

[OOB](#) selected: OOB Message DWn[15:8]

FLASH selected: For MAFS:Flash Cpl Data DWn[15:8] For SAFS:Flash write data [15:8]

7:0 **DN\_TXDATA\_B0**. Read-write. Reset: 00h.**Description:** The definition for this field is depended on SW\_CMD\_TYPE

Independent channel command selected: Reserved, Always be 00h

Peripheral selected : Message Data DWn[7:0]

VW selected: VW Index Group 2n

[OOB](#) selected: OOB Message DWn[7:0]

FLASH selected: For MAFS:Flash Cpl Data DWn[7:0] For SAFS:Flash write data [7:0]

**ESPI1SMNx00000010...ESPISMNx00000010 (FCH::ITF::ESPI::UP\_RXHDR\_0)**

Reset: 0000\_0000h.

\_link1\_aliasSMN; ESPI1SMNx00000010; ESPI1SMN=02DCA000h

\_link0\_aliasSMN; ESPISMNx00000010; ESPISMN=02DC5000h

\_link1\_aliasHOSTLEGACY; ESPI1x00000010; ESPI1=FEC30000h

\_link0\_aliasHOSTLEGACY; ESPIx00000010; ESPI=FEC20000h

Bits	Description
31:24	<b>UPCMD_HDATA2.</b> Read-only. Reset: 00h. <b>Description:</b> RX_LOW_LEN: This field store the Length[7:0] from GET_FLASH_NP(for MAFS)/GET_OOB/GET_FLASH_C(for SAFS) [31:24] Length[7:0]
23:16	<b>UPCMD_HDATA1.</b> Read-only. Reset: 00h. <b>Description:</b> RX_TAG_LEN: This field store the Tag and Length[11:8] which from eSPI packet received by GET_FLASH_NP(for MAFS)/GET_OOB/GET_FLASH_C(for SAFS) [23:20], Tag [19:16] Length[11:8]
15:8	<b>UPCMD_HDATA0.</b> Read-only. Reset: 00h. <b>Description:</b> Cycle Type This field store the cycle type from GET_FLASH_NP(for MAFS) and GET_OOB This field store the cycle type from GET_FLASH_C(for SAFS) and PUT_FLASH_NP with immediately response completion(for SAFS)
7:6	Reserved.
5:4	<b>SLAVE_SEL.</b> Read-only. Reset: 0h. <b>Description:</b> Slave N Received selected 00: The upstream packet is from Slave0 Others: Reserved
3	<b>UPCMD_STATUS.</b> Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> For <a href="#">OOB</a> channel, this bit will be set after received OOB message packet. For Flash channel, there are MAFS mode and SAFS mode: MAFS: this bit will be set after received Flash request packet. SAFS: this bit will be set after received Flash completion only after SW programming interface sending PUT_FLASH_NP. 1. When SW programming interface sending PUT_FLASH_NP cycle with immediately response completion or 2. Received completion by GET_FLASH_C for SW programming interface sending PUT_FLASH_NP. (For SAFS channel, GET_FLASH_C will not assert this bit) Note:eSPI will not send down another GET_OOB or GET_FLASH_NP(MAFS) or GET_FLASH_C(For SW programming interface sending PUT_FLASH_NP) before the Valid bit cleared by SW. This bit can be cleared by SW writing 1'b1 to this field.
2:0	<b>UPCMD_TYPE.</b> Read-only. Reset: 0h. <b>Description:</b> 000: For MAFS, Flash Channel Request (GET_FLASH_NP) 001: Upstream <a href="#">OOB</a> message (GET_OOB) 010: For SAFS, Flash Channel completion (GET_FLASH_C) 011: For SAFS, Current PUT_FLASH_NP Cycle response completion with header/data. Note: This value is only valid when PUT_FLASH_NP_HEADER_DATA_EN =1 or PUT_FLASH_NP_HEADER_EN =1 100: For SAFS, GET_STATUS with modifier. Others: Reserved.



**ESPI1SMNx00000014...ESPISMNx00000014 (FCH::ITF::ESPI::UP\_RXHDR\_1)**

Read-only. Reset: 0000\_0000h.

\_link1\_aliasSMN; ESPI1SMNx00000014; ESPI1SMN=02DCA000h

\_link0\_aliasSMN; ESPISMNx00000014; ESPISMN=02DC5000h

\_link1\_aliasHOSTLEGACY; ESPI1x00000014; ESPI1=FEC30000h

\_link0\_aliasHOSTLEGACY; ESPIx00000014; ESPI=FEC20000h

Bits	Description
31:24	<b>UPCMD_HDATA6.</b> Read-only. Reset: 00h. <b>Description:</b> The definition for this field is depended on RX_REQ_TYPE <a href="#">OOB</a> selected: Reserved FLASH selected(for MAFS only): Address[7:0]
23:16	<b>UPCMD_HDATA5.</b> Read-only. Reset: 00h. <b>Description:</b> The definition for this field is depended on RX_REQ_TYPE <a href="#">OOB</a> selected: <a href="#">SMBus</a> Byte Count FLASH selected(for MAFS only): Address[15:8]
15:8	<b>UPCMD_HDATA4.</b> Read-only. Reset: 00h. <b>Description:</b> The definition for this field is depended on RX_REQ_TYPE <a href="#">OOB</a> selected: <a href="#">SMBus</a> Command Opcode FLASH selected(for MAFS only): Address[23:16]
7:0	<b>UPCMD_HDATA3.</b> Read-only. Reset: 00h. <b>Description:</b> The definition for this field is depended on RX_REQ_TYPE <a href="#">OOB</a> selected <a href="#">SMBus</a> Slave Address FLASH selected(for MAFS only): Address[31:24]

**ESPI1SMNx00000018...ESPISMNx00000018 (FCH::ITF::ESPI::UP\_RXDATA\_PORT)**

Read-only. Reset: 0000\_0000h.

\_link1\_aliasSMN; ESPI1SMNx00000018; ESPI1SMN=02DCA000h

\_link0\_aliasSMN; ESPISMNx00000018; ESPISMN=02DC5000h

\_link1\_aliasHOSTLEGACY; ESPI1x00000018; ESPI1=FEC30000h

\_link0\_aliasHOSTLEGACY; ESPIx00000018; ESPI=FEC20000h

Bits	Description
31:0	<b>UP_RXDATA.</b> Read-only. Reset: 0000_0000h.

**ESPI1SMNx0000002C...ESPISMNx0000002C (FCH::ITF::ESPI::MASTER\_CAP)**

Read-only. Reset: Fixed,E849_EDAFh.	
_link1_aliasSMN; ESPI1SMNx0000002C; ESPI1SMN=02DCA000h	
_link0_aliasSMN; ESPISMNx0000002C; ESPISMN=02DC5000h	
_link1_aliasHOSTLEGACY; ESPI1x0000002C; ESPI1=FEC30000h	
_link0_aliasHOSTLEGACY; ESPIx0000002C; ESPI=FEC20000h	
Bits	Description
31	<b>CRC_CHECK_SUPPORT.</b> Read-only. Reset: Fixed,1.
30	<b>ALERT_MODE_SUPPORT.</b> Read-only. Reset: Fixed,1. A dedicated Alert# pin is used to signal the Alert event, or I/O[1] pin used for Alert.
29:28	<b>IO_MODE_SUPPORT.</b> Read-only. Reset: Fixed,2h. IO Mode support by Controller, Quad mode, Dual mode, single mode
27:25	<b>CLK_FREQ_SUPPORT.</b> Read-only. Reset: Fixed,4h. <b>Description:</b> Operating Support Frequency 000 20MHz 001 16.7MHz, 33MHz 011 16.7MHz, 33MHz, 66MHz 100 16.7MHz, 20MHz, 25MHz, 33MHz, 50MHz, 66MHz Note: This field has a default value of 000 to reflect tINIT-FREQ (Table21) of 20MHz max.
24:22	<b>SLAVE_NUM.</b> Read-only. Reset: Fixed,1h.
21:19	<b>PR_MAX_SIZE.</b> Read-only. Reset: Fixed,1h. 64 bytes address aligned max payload size.
18:13	<b>VW_MAX_SIZE.</b> Read-only. Reset: Fixed,0Fh. Operating Maximum Virtual Wire Count support
12:10	<b>OOB_MAX_SIZE.</b> Read-only. Reset: Fixed,3h. 256 bytes max payload size
9:7	<b>FLASH_MAX_SIZE.</b> Read-only. Reset: Fixed,3h. 256 bytes max payload size
6:4	<b>ESPI_VERSION.</b> Read-only. Reset: Fixed,2h. ESPI Version. 000b:Master support eSPI 0.7 version; 001b:Master support eSPI 0.75 version; 010b:Master support eSPI 1.0 version;
3	<b>PR_SUPPORT.</b> Read-only. Reset: Fixed,1.
2	<b>VW_SUPPORT.</b> Read-only. Reset: Fixed,1.
1	<b>OOB_SUPPORT.</b> Read-only. Reset: Fixed,1.
0	<b>FLASH_SUPPORT.</b> Read-only. Reset: Fixed,1.

**ESPI1SMNx00000030...ESPISMNx00000030 (FCH::ITF::ESPI::GLOBAL\_CONTROL\_0)**

Read-write. Reset: 0000_0008h.	
_link1_aliasSMN; ESPI1SMNx00000030; ESPI1SMN=02DCA000h	
_link0_aliasSMN; ESPISMNx00000030; ESPISMN=02DC5000h	
_link1_aliasHOSTLEGACY; ESPI1x00000030; ESPI1=FEC30000h	
_link0_aliasHOSTLEGACY; ESPIx00000030; ESPI=FEC20000h	
Bits	Description
31	<b>SAFS_Clk_Gate_EN.</b> Read-write. Reset: 0. When this bit is set, enable dynamic clock gating for boot from SAFS channel. And SAFS through register i/f is not impacted by this bit. Default is disable.
30	<b>PR_RST_EN_PLTRST.</b> Read-write. Reset: 0. This bit is used to control whether to reset ESPI peripheral channel when ACPI_PLTRSTB is received. Default value is 0 and not to reset
29:24	<b>WAIT_CNT.</b> Read-write. Reset: 00h. Specifies the timeout count for wait state. This value means the threshold of wait state timeout. For example, if program theses bits to 6'h11 (6'd17), it means timeout will be fired if device inserts 17 byte wait time, then host will disable eSPI_Clk output. By default, host will allow at most 16 byte wait time, and will time out if device inserts 17 bytes wait time, then eSPI_Clk will be disabled.
23:8	<b>WDG_CNT.</b> Read-write. Reset: 0000h. Specifies the timeout retry count for PCI downstream retries.
7	<b>RG_dbgclk_gating_en.</b> Read-write. Reset: 0.
6:4	<b>AL_IDLE_TIMER.</b> Read-write. Reset: 0h.  <b>Description:</b> Set the bits to select different Idle timer timeout value. Once the Idle timer reach the timeout value and Global Alink clock gating Enable set, eSPI will output ESPI_Stop_AlClk to do global Alink clock gating. Bits Selection 000 16 clocks 001 32 clocks 010 64 clocks 011 128 clocks 100 256 clocks 101 512 clocks 110 1024 clocks 111 2048 clocks
3	<b>AL_STOP_EN.</b> Read-write. Reset: 1. Set the bit to enable eSPI generating ESPI_Stop_AlClk to do global Alink clock gating once Global Alink Idle Timer reach the timeout value.
2	<b>PR_CLKGAT_EN.</b> Read-write. Reset: 0. Set the bit to enable Peripheral block do dynamic clock gating once the Slave Peripheral channel is disabled.
1	<b>WAIT_CHKEN.</b> Read-write. Reset: 0. Set the bit to enable the Wait State counter during eSPI bus turn around.
0	<b>WDG_EN.</b> Read-write. Reset: 0. Set the bit to enable the watchdog counter for all the PCI downstream transactions for eSPI.

**ESPI1SMNx00000034...ESPISMNx00000034 (FCH::ITF::ESPI::GLOBAL\_CONTROL\_1)**

Read-write.

\_link1\_aliasSMN; ESPI1SMNx00000034; ESPI1SMN=02DCA000h

\_link0\_aliasSMN; ESPISMNx00000034; ESPISMN=02DC5000h

\_link1\_aliasHOSTLEGACY; ESPI1x00000034; ESPI1=FEC30000h

\_link0\_aliasHOSTLEGACY; ESPIx00000034; ESPI=FEC20000h

**Bits Description**

31:22 Reserved.

21	<b>ESPI_REQ_NOTWITH_VW_REQ.</b> Read-write. When 0: It applies to the case where eSPI host controller only sits onto one data bus with device. Then if eSPI_VW_Req gets granted, no eSPI_Req shall need to be asserted to the same SPI controller further. When set to 1: It applies to the case where eSPI host controller might sit onto two data bus with device based on one SPI register setting. eSPI_Req and eSPI_VW_Req don't go to the same data bus. Then even if eSPI_VW_Req gets granted, eSPI_Req is still needed to be asserted to the related SPI controller further before issuing any transaction (like PUT_VM).
20	<b>ALERT_ENABLE.</b> Read-write. Reset: 0. When 0b: ALERT# to eSPI keep inactive(1). When set to 1b: Alert# value is monitored from Alert# or Din[1] depending on Alert_mode setting.
19	<b>FL_REQ_VALID_DIS.</b> Read-write. Reset: 0. When 0b: 1 bit[5:4] of VW index45 are treated as valid bits for FL_REQ/FL_REQ_ATOMIC. 2. bit[4] of VW index 43h, the valid bit will be 1 when sending down FL_GNT.
18	<b>ROM_SHARING_DIS.</b> Read-write. Reset: 0. <b>Description:</b> When this bit is 0b: 1. GET_VW will be sent down to eSPI bus as long as VW available status in GET_STATUS is set to 1 no matter VW channel is enabled or not. 2. If GET_VW without FL_Req bit set, this GET_VW should be discarded. 3. When receiving eSPI_VW_GNT indicating that SPI has granted this FL_Req and already tri-stated the bus, eSPI controller will unconditionally send down PUT_VW with the FL_ACK set without requesting SPI the bus usage (i.e., no eSPI_Req is asserted to SPI controller if bit [21] is 0b, otherwise, eSPI_Req is required to assert before issuing PUT_VW). When this bit is 1b, disable ROM access: 1. Get_VW/Put_VW will follow the normal eSPI protocol, i.e., the VW channel need be enabled first. 2. No eSPI_VW_Req/eSPI_VW_Atomic will be sent to eSPI host controller. 3. No response to eSPI_VW_GNT from eSPI controller.
17:13	<b>RGCMD_INT_MAP.</b> Read-write. Reset: 17h. <b>Description:</b> Register CMD interrupt mapping. When Register command (Downstream/Upstream peripheral message, Downstream/Upstream <a href="#">OOB</a> , Downstream VW, Channel Independent command) have finished, the interrupt eSPI controller generates will be mapped to interrupt pin according to this register setting. Bits Mapping 00000: IRQ0 00001: IRQ1 .... 10111: IRQ23 11111: <a href="#">SMI</a> #
12:8	<b>ERR_INT_MAP.</b> Read-write. Reset: 1Fh. <b>Description:</b> ERR interrupt mapping. When some errors happen to slave transactions and the related error interrupt enable has been set, the error interrupt will be mapped to interrupt pin according to following register setting. Bits Mapping 00000: IRQ0 00001: IRQ1 .... 10111: IRQ23 11111: <a href="#">SMI</a> #
7:3	Reserved.

2	<b>SUB_DECODE_EN.</b> Read-write. Reset: 0. Enable eSPI to do Subtractive Decode.
1	<b>BUS_MASTER_EN.</b> Read-write. Reset: 0. Enable eSPI Upstream Memory cycle posting.
0	<b>SW_RST.</b> Read-write. Reset: 0. Set the bit to do global controller resets for eSPI controller. All the state machines will return to idle, and all the request will be flushed. All the configuration registers will be reset to default value, and software needs to send In-Band Reset to each Slave device after controller reset so that both Master and Slave run in same configuration mode.

#### ESPI1SMNx00000038...ESPISMNx00000038 (FCH::ITF::ESPI::SEMAPHORE\_MISC\_CONTROL\_REG0)

Reset: 0000\_0000h.

\_link1\_aliasSMN; ESPI1SMNx00000038; ESPI1SMN=02DCA000h

\_link0\_aliasSMN; ESPISMNx00000038; ESPISMN=02DC5000h

\_link1\_aliasHOSTLEGACY; ESPI1x00000038; ESPI1=FEC30000h

\_link0\_aliasHOSTLEGACY; ESPIx00000038; ESPI=FEC20000h

Bits	Description
31	<b>espi_p1500_timeout_error_bit.</b> Read-only. Reset: 0. A 1b of this bit means the TDR access to eSPI registers times out. And this bit is real-time. When this bit is 1, it means the last JTAG W/R operation is timeout. This bit will be clear if this time JTAG W/R operation succeed.
30	<b>SW3_OWNER_CLR.</b> Read-write. Reset: 0. Clear SW3 ownership bit, Clear has higher priority than Set. Once eSPI is not needed, SW3 need write 1b to this bit to release the ownership. And this bit need be written back to 0b in the same cycle that bit [29] is set to 1, or at the end of SW0 releasing its ownership.
29	<b>SW3_OWNER_SET.</b> Read-write. Reset: 0. Set SW3 ownership bit. This bit is allowed to write only when all the status bit [15:8], [16], [20], [24], [28] are all 0b. Note: this bit should not be set simultaneously with <Set SW0/SW1/SW2 ownership bit> and SW4_USER_ID.
28	<b>SW3_OWNER_STATUS.</b> Read-only. Reset: 0. SW3 ownership status bit (recommend to use if SW0, SW1, SW2 are also occupied). Note: CLR has higher priority than SET
27	Reserved.
26	<b>SW2_OWNER_CLR.</b> Read-write. Reset: 0. Clear SW2 ownership bit, Clear has higher priority than Set. Once eSPI is not needed, SW2 need write 1b to this bit to release the ownership. And this bit need be written back to 0b in the same cycle that bit [25] is set to 1, or at the end of SW2 releasing its ownership.
25	<b>SW2_OWNER_SET.</b> Read-write. Reset: 0. Set SW2 ownership bit. This bit is allowed to write only when all the status bit [15:8], [16], [20], [24], [28] are all 0b. Note: this bit should not be set simultaneously with <Set SW0/SW1/SW3 ownership bit> and SW4_USER_ID.
24	<b>SW2_OWNER_STATUS.</b> Read-only. Reset: 0. SW2 (recommend X86 to use) ownership status bit. Note: CLR has higher priority than SET
23	Reserved.
22	<b>SW1_OWNER_CLR.</b> Read-write. Reset: 0. Clear SW1 ownership bit, Clear has higher priority than Set. Once eSPI is not needed, SW1 need write 1b to this bit to release the ownership. And this bit need be written back to 0b in the same cycle that bit [21] is set to 1, or at the end of SW1 releasing its ownership.
21	<b>SW1_OWNER_SET.</b> Read-write. Reset: 0. Set SW1 ownership bit. This bit is allowed to write only when all the status bit [15:8], [16], [20], [24], [28] are all 0b. Note: this bit should not be set simultaneously with <Set SW0/SW2/SW3 ownership bit> and SW4_USER_ID.
20	<b>SW1_OWNER_STATUS.</b> Read-only. Reset: 0. SW1 (recommend <a href="#">MP1</a> to use) ownership status bit. Note: CLR has higher priority than SET
19	Reserved.
18	<b>SW0_OWNER_CLR.</b> Read-write. Reset: 0. Clear SW0 ownership bit, Clear has higher priority than Set. Once eSPI is not needed, SW0 need write 1b to this bit to release the ownership. And this bit need be written back to 0b in the same cycle that bit [17] is set to 1, or at the end of SW0 releasing its ownership..
17	<b>SW0_OWNER_SET.</b> Read-write. Reset: 0. Set SW0 ownership bit. This bit is allowed to write only when all the status bit [15:8], [16], [20], [24], [28] are all 0b. Note: this bit should not be set simultaneously with <Set SW1/SW2/SW3 ownership bit> and SW4_USER_ID.
16	<b>SW0_OWNER_STATUS.</b> Read-only. Reset: 0. SW0 (recommend <a href="#">ASP</a> to use) ownership status bit. Note: CLR has higher priority than SET

15:8	<b>SW4_USER_ID</b> . Read-write. Reset: 00h. This is a second mechanism to support more players to operate eSPI in a system over 4 players are there. Anyone which need operate eSPI need poll this field to be 0h before writing its own ID to this field, and it can start to operate eSPI once this field is read to be its own ID. And once it doesn't need to operate eSPI, it need write this field back to 0b to release the usage of eSPI. In this mechanism, anyone which need operate eSPI is required to poll this field and all other status bits [16], [20], [24], [28] to be 0h before it is allowed to write its own ID to this field to claim the ownership, and once this field is read to be its own ID, it can start to operate eSPI. And once it doesn't need to operate eSPI, it can write this field back to 0b to release its ownership for eSPI. Users are not allowed to write 0h to this filed unless it owns eSPI, and users should use byte enable to avoid this field is wrongly overridden by 0b if they don't intend to use this filed. On the system level, each player should be assigned a unique non-zero ID. And writing ID to this field won't succeed if this filed is not zero.
7:0	Reserved.

**ESPI1SMNx00000044...ESPISMNx00000044 (FCH::ITF::ESPI::SLAVE0\_IO\_BASE\_REG0)**

Read-write. Reset: 0000\_0000h.

\_link1\_aliasSMN; ESPI1SMNx00000044; ESPI1SMN=02DCA000h

\_link0\_aliasSMN; ESPISMNx00000044; ESPISMN=02DC5000h

\_link1\_aliasHOSTLEGACY; ESPI1x00000044; ESPI1=FEC30000h

\_link0\_aliasHOSTLEGACY; ESPIx00000044; ESPI=FEC20000h

Bits	Description
31:16	<b>RANGE1</b> . Read-write. Reset: 0000h. IO decode base address for Range 1
15:0	<b>RANGE0</b> . Read-write. Reset: 0000h. IO decode base address for Range 0

**ESPI1SMNx00000048...ESPISMNx00000048 (FCH::ITF::ESPI::SLAVE0\_IO\_BASE\_REG1)**

Read-write. Reset: 0000\_0000h.

\_link1\_aliasSMN; ESPI1SMNx00000048; ESPI1SMN=02DCA000h

\_link0\_aliasSMN; ESPISMNx00000048; ESPISMN=02DC5000h

\_link1\_aliasHOSTLEGACY; ESPI1x00000048; ESPI1=FEC30000h

\_link0\_aliasHOSTLEGACY; ESPIx00000048; ESPI=FEC20000h

Bits	Description
31:16	<b>RANGE3</b> . Read-write. Reset: 0000h. IO decode base address for Range 3
15:0	<b>RANGE2</b> . Read-write. Reset: 0000h. IO decode base address for Range 2

**ESPI1SMNx0000004C...ESPISMNx0000004C (FCH::ITF::ESPI::SLAVE0\_IO\_SIZE)**

Read-write. Reset: 0000\_0000h.

\_link1\_aliasSMN; ESPI1SMNx0000004C; ESPI1SMN=02DCA000h

\_link0\_aliasSMN; ESPISMNx0000004C; ESPISMN=02DC5000h

\_link1\_aliasHOSTLEGACY; ESPI1x0000004C; ESPI1=FEC30000h

\_link0\_aliasHOSTLEGACY; ESPIx0000004C; ESPI=FEC20000h

Bits	Description
31:24	<b>RANGE3</b> . Read-write. Reset: 00h. Programmable IO Range3 size
23:16	<b>RANGE2</b> . Read-write. Reset: 00h. Programmable IO Range2 size
15:8	<b>RANGE1</b> . Read-write. Reset: 00h. Programmable IO Range1 size
7:0	<b>RANGE0</b> . Read-write. Reset: 00h. Programmable IO Range0 size

**ESPI1SMNx00000050...ESPISMNx00000050 (FCH::ITF::ESPI::SLAVE0\_MMIO\_BASE\_REG0)**

Read-write. Reset: 0000\_0000h.

\_link1\_aliasSMN; ESPI1SMNx00000050; ESPI1SMN=02DCA000h

\_link0\_aliasSMN; ESPISMNx00000050; ESPISMN=02DC5000h

\_link1\_aliasHOSTLEGACY; ESPI1x00000050; ESPI1=FEC30000h

\_link0\_aliasHOSTLEGACY; ESPIx00000050; ESPI=FEC20000h

Bits	Description
31:0	<b>RANGE0</b> . Read-write. Reset: 0000_0000h. <a href="#">MMIO</a> decode base address for Range 0

**ESPI1SMNx00000054...ESPISMNx00000054 (FCH::ITF::ESPI::SLAVE0\_MMIO\_BASE\_REG1)**

Read-write. Reset: 0000\_0000h.

[\\_link1\\_aliasSMN](#); ESPI1SMNx00000054; ESPI1SMN=02DCA000h[\\_link0\\_aliasSMN](#); ESPISMNx00000054; ESPISMN=02DC5000h[\\_link1\\_aliasHOSTLEGACY](#); ESPI1x00000054; ESPI1=FEC30000h[\\_link0\\_aliasHOSTLEGACY](#); ESPIx00000054; ESPI=FEC20000h**Bits Description**31:0 **RANGE1.** Read-write. Reset: 0000\_0000h. [MMIO](#) decode base address for Range 1**ESPI1SMNx00000058...ESPISMNx00000058 (FCH::ITF::ESPI::SLAVE0\_MMIO\_BASE\_REG2)**

Read-write. Reset: 0000\_0000h.

[\\_link1\\_aliasSMN](#); ESPI1SMNx00000058; ESPI1SMN=02DCA000h[\\_link0\\_aliasSMN](#); ESPISMNx00000058; ESPISMN=02DC5000h[\\_link1\\_aliasHOSTLEGACY](#); ESPI1x00000058; ESPI1=FEC30000h[\\_link0\\_aliasHOSTLEGACY](#); ESPIx00000058; ESPI=FEC20000h**Bits Description**31:0 **RANGE2.** Read-write. Reset: 0000\_0000h. [MMIO](#) decode base address for Range 2**ESPI1SMNx0000005C...ESPISMNx0000005C (FCH::ITF::ESPI::SLAVE0\_MMIO\_BASE\_REG3)**

Read-write. Reset: 0000\_0000h.

[\\_link1\\_aliasSMN](#); ESPI1SMNx0000005C; ESPI1SMN=02DCA000h[\\_link0\\_aliasSMN](#); ESPISMNx0000005C; ESPISMN=02DC5000h[\\_link1\\_aliasHOSTLEGACY](#); ESPI1x0000005C; ESPI1=FEC30000h[\\_link0\\_aliasHOSTLEGACY](#); ESPIx0000005C; ESPI=FEC20000h**Bits Description**31:0 **RANGE3.** Read-write. Reset: 0000\_0000h. [MMIO](#) decode base address for Range 3**ESPI1SMNx00000060...ESPISMNx00000060 (FCH::ITF::ESPI::SLAVE0\_MMIO\_SIZE\_REG0)**

Read-write. Reset: 0000\_0000h.

[\\_link1\\_aliasSMN](#); ESPI1SMNx00000060; ESPI1SMN=02DCA000h[\\_link0\\_aliasSMN](#); ESPISMNx00000060; ESPISMN=02DC5000h[\\_link1\\_aliasHOSTLEGACY](#); ESPI1x00000060; ESPI1=FEC30000h[\\_link0\\_aliasHOSTLEGACY](#); ESPIx00000060; ESPI=FEC20000h**Bits Description**31:16 **RANGE1.** Read-write. Reset: 0000h. Programmable [MMIO](#) Range1 size.15:0 **RANGE0.** Read-write. Reset: 0000h. Programmable [MMIO](#) Range0 size.**ESPI1SMNx00000064...ESPISMNx00000064 (FCH::ITF::ESPI::SLAVE0\_MMIO\_SIZE\_REG1)**

Read-write. Reset: 0000\_0000h.

[\\_link1\\_aliasSMN](#); ESPI1SMNx00000064; ESPI1SMN=02DCA000h[\\_link0\\_aliasSMN](#); ESPISMNx00000064; ESPISMN=02DC5000h[\\_link1\\_aliasHOSTLEGACY](#); ESPI1x00000064; ESPI1=FEC30000h[\\_link0\\_aliasHOSTLEGACY](#); ESPIx00000064; ESPI=FEC20000h**Bits Description**31:16 **RANGE3.** Read-write. Reset: 0000h. Programmable [MMIO](#) Range3 size.15:0 **RANGE2.** Read-write. Reset: 0000h. Programmable [MMIO](#) Range2 size.

**ESPI1SMNx00000068...ESPISMNx00000068 (FCH::ITF::ESPI::SLAVE0\_CONFIG)**

Read-write. Reset: 0000\_0728h.

\_link1\_aliasSMN; ESPI1SMNx00000068; ESPI1SMN=02DCA000h

\_link0\_aliasSMN; ESPISMNx00000068; ESPISMN=02DC5000h

\_link1\_aliasHOSTLEGACY; ESPI1x00000068; ESPI1=FEC30000h

\_link0\_aliasHOSTLEGACY; ESPIx00000068; ESPI=FEC20000h

Bits	Description
31	<b>CRC_CHECK_EN.</b> Read-write. Reset: 0. CRC Checking Enable: This bit is set to 1 by eSPI master to enable the CRC checking on the eSPI bus. 0b: CRC checking is disabled. 1b: CRC checking is enabled.
30	<b>ALERT_MODE_SEL.</b> Read-write. Reset: 0. <b>Description:</b> 0b: IO bit1 pin is used to signal the Alert event. 1b: A dedicated Alert# pin is used to signal the Alert event. Note: This bit can only be 0 in a single master-single slave topology. For single master-multiple slave topology, this bit must be programmed to 1.
29:28	<b>IO_MODE_SEL.</b> Read-write. Reset: 0h. I/O Mode Select. 00 Single I/O 01 Dual I/O 10 Quad I/O 11 Reserved.
27:25	<b>CLK_FREQ_SEL.</b> Read-write. Reset: 0h. <b>Description:</b> Operating Frequency: 000 20MHz; 001 25MHz; 010 33MHz; 011 50MHz; 100 66MHz; 110 16MHz; Others Reserved.
24:12	Reserved.
11	<b>FLASH_modifier_EN.</b> Read-write. Reset: 0. When this bit is set to 1, SAFS FLASH modifier is enable. And if UPCMD_STATUS(0x10[3]) is not cleared, GET_STATUS will not be sent to ESPI bus.
10	<b>SAFS_DEFER_VALID_EN.</b> Read-write. Reset: 1. When this bit is set, that means after PUT_FALSH_NP (flash read/write/erase) is sent to device, Slave response DEFER is a valid behavior and ESPI controller should accept it. When this bit is not set, that means after PUT_FALSH_NP (flash read/write/erase) is sent to device, Slave response DEFER is an invalid behavior and ESPI controller will report invalid response error. This bit default is 1b.
9	<b>PUT_FLASH_NP_HEADER_EN.</b> Read-write. Reset: 1. When this bit is set, that means after PUT_FALSH_NP (flash write/erase) is sent to device, Slave should respond with header (cycle type, tag, length) following Accept byte, which means this request is fulfilled. When this bit is not set, that means after PUT_FALSH_NP (flash read) is sent to device, Slave will respond without header following Accept byte, and controller need still issue additional GET_FALSH_C down to get the completion once it is ready. This bit default is 1b.
8	<b>PUT_FLASH_NP_HEADER_DATA_EN.</b> Read-write. Reset: 1. When this bit is set, that means after PUT_FALSH_NP (flash read) is sent to device, Slave should respond with header (cycle type, tag, length) and data (optional) following Accept byte, which means this request is fulfilled. When this bit is not set, that means after PUT_FALSH_NP (flash read) is sent to device, Slave will respond without header and data following Accept byte, and controller need still issue additional GET_FALSH_C down to get the completion once it is ready. This bit default is 1b.
7:5	<b>FLASH_MPS.</b> Read-write. Reset: 1h. <b>Description:</b> Flash Access Channel Maximum Payload Size Selected, 3 bits: default 001b 000b: Reserved. 001b: 64 bytes max payload size. 010b: 128 bytes max payload size. 011b: 256 bytes max payload size. 100b-111b: Reserved.
4	<b>FLASH_SHARING_MODE.</b> Read-write. Reset: 0. When Flash Access channel is enabled, this bit indicates the flash sharing scheme in operation. 0b: Master attached flash sharing. 1b: Slave attached flash sharing. Default will be 0b
3	<b>PR_EN.</b> Read-write. Reset: 1. Peripheral Channel Enable: This bit is set to 1 by eSPI master to enable the Peripheral channel.
2	<b>VW_EN.</b> Read-write. Reset: 0. Virtual Wire Channel Enable: This bit is set to 1 by eSPI master to enable the Virtual Wire channel.



1	<b>OOB_EN</b> . Read-write. Reset: 0. <a href="#">OOB</a> Message Channel Enable: This bit is set to 1 by eSPI master to enable the OOB Message channel.
0	<b>FLASH_EN</b> . Read-write. Reset: 0. Flash Access Channel Enable: This bit is set to 1 by eSPI master to enable the Flash Access channel.

**ESPI1SMNx0000006C...ESPISMNx0000006C (FCH::ITF::ESPI::SLAVE0\_INT\_EN)**

Read-write. Reset: 0000\_0000h.

\_link1\_aliasSMN; ESPI1SMNx0000006C; ESPI1SMN=02DCA000h

\_link0\_aliasSMN; ESPISMNx0000006C; ESPISMN=02DC5000h

\_link1\_aliasHOSTLEGACY; ESPI1x0000006C; ESPI1=FEC30000h

\_link0\_aliasHOSTLEGACY; ESPIx0000006C; ESPI=FEC20000h

Bits	Description
31	<b>FLASH_REQ_INT_EN.</b> Read-write. Reset: 0. Flash Request Received Enable for X86: Enable to generate a command interrupt to ACPI for X86 when Upstream Flash Request is received and valid to read
30	<b>RXOOB_INT_EN.</b> Read-write. Reset: 0. <b>OOB</b> Message Received Enable: Enable to generate a command interrupt when Upstream OOB Message is received and valid to read
29	<b>RXMSG_INT_EN.</b> Read-write. Reset: 0. Peripheral Message Received Enable: Enable to generate a command interrupt when Upstream Peripheral Msg is received and valid to read.
28	<b>DNCMD_INT_EN.</b> Read-write. Reset: 0. Downstream Register Command Complete Enable: Enable to generate a command interrupt when Downstream eSPI Registers programming Command has completed.
27	<b>RXVW_GRP3_INT_EN.</b> Read-write. Reset: 0. Virtual Wire Index Group 3 Received Enable: Enable to generate a command interrupt when Virtual Wire Index Group3 register specified Virtual Wire Packet is received
26	<b>RXVW_GRP2_INT_EN.</b> Read-write. Reset: 0. Virtual Wire Index Group 2 Received Enable: Enable to generate a command interrupt when Virtual Wire Index Group2 register specified Virtual Wire Packet is received
25	<b>RXVW_GRP1_INT_EN.</b> Read-write. Reset: 0. Virtual Wire Index Group 1 Received Enable: Enable to generate a command interrupt when Virtual Wire Index Group1 register specified Virtual Wire Packet is received
24	<b>RXVW_GRP0_INT_EN.</b> Read-write. Reset: 0. Virtual Wire Index Group 0 Received Enable: Enable to generate a command interrupt when Virtual Wire Index Group0 register specified Virtual Wire Packet is received
23	<b>FLASH_REQ_INT_2_RSMU_EN.</b> Read-write. Reset: 0. Enable to generate a command interrupt to RSMU when Upstream Flash Request (recorded in 0x70[31]), default is disable it.
22:20	Reserved.
19	<b>WDG_TIMEOUT_INT_EN.</b> Read-write. Reset: 0. Alink Bus Watch Dog Timer Timeout Enable: Enable generate an ERROR interrupt when Alink bus Watch dog timer timeout
18	<b>MST_ABORT_INT_EN.</b> Read-write. Reset: 0. Alink Bus Master Abort Enable: Enable generate an ERROR interrupt when eSPI Controller doing Master abort.
17	<b>UPFIFO_WDGTIM_INT_EN.</b> Read-write. Reset: 0. Enable to generate an interrupt when UPFIFO watchdog timer times out.
16	Reserved.
15	<b>PROTOCOL_ERR_INT_EN.</b> Read-write. Reset: 0. Protocol ERROR detected Enable: Enable to generate an ERROR interrupt when Protocol ERROR is detected
14	<b>RXFLASH_OVERFLOW_INT_EN.</b> Read-write. Reset: 0. FLASH Packet Data Length Over 256 bytes Enable: Enable to generate an ERROR interrupt when FLASH Packet data Over 256 bytes
13	<b>RXMSG_OVERFLOW_INT_EN.</b> Read-write. Reset: 0. Peripheral Message Data Length Over 32 bytes Enable: Enable to generate an ERROR interrupt when Peripheral Packet Message data Over 32 bytes
12	<b>RXOOB_OVERFLOW_INT_EN.</b> Read-write. Reset: 0. <b>OOB</b> Packet Data Length Over 256 bytes Enable: Enable to generate an ERROR interrupt when OOB Packet data Over 256 bytes
11	<b>ILLEGAL_LEN_INT_EN.</b> Read-write. Reset: 0. Illegal Response Length Received Enable: Enable generate an ERROR interrupt when Illegal length is received
10	<b>ILLEGAL_TAG_INT_EN.</b> Read-write. Reset: 0. Illegal Response Tag Received Enable: Enable to generate an ERROR interrupt when Illegal tag is received
9	<b>UNSUCSS_CPL_INT_EN.</b> Read-write. Reset: 0. Unsuccessful CPL Received Enable: Enable to generate an ERROR interrupt when Unsuccessful completion without data is received
8	<b>INVALID_CT_INT_EN.</b> Read-write. Reset: 0. Invalid Cycle Type Received Enable: Enable to generate an ERROR interrupt when Unrecognized Cycle Type is received
7	<b>INVALID_RSP_INT_EN.</b> Read-write. Reset: 0. Invalid Response Code Received Enable: Enable to generate an ERROR interrupt when Unrecognized Response is received

6	<b>NON_FATAL_ERR_INT_EN.</b> Read-write. Reset: 0. NON_FATAL_ERROR Response Code Received Enable: Enable to generate an ERROR interrupt when NON_FATAL_ERROR Response Code is received.
5	<b>FATAL_ERR_INT_EN.</b> Read-write. Reset: 0. FATAL_ERROR Response Code Received Enable: Enable to generate an ERROR interrupt when FATAL_ERROR Response Code is received.
4	<b>NO_RSP_INT_EN.</b> Read-write. Reset: 0. NO_RESPONSE Code received Enable: Enable to generate an ERROR interrupt when No_Response Response Code is received.
3	Reserved.
2	<b>CRC_ERR_INT_EN.</b> Read-write. Reset: 0. CRC Error detected Enable: Enable to generate an ERROR interrupt when CRC ERROR is detected on response phase.
1	<b>WAIT_TIMEOUT_INT_EN.</b> Read-write. Reset: 0. eSPI Bus Wait State Insertion Max Out Enable: Enable to generate an ERROR interrupt when eSPI Wait State timer timeout.
0	<b>BUS_ERR_INT_EN.</b> Read-write. Reset: 0. eSPI Bus Timing Error Enable: Enable generate an ERROR interrupt when eSPI Bus timing Error.

**ESPI1SMNx00000070...ESPISMNx00000070 (FCH::ITF::ESPI::SLAVE0\_INT\_STS)**

Read,Write-1-to-clear. Reset: 0000\_0000h.

\_link1\_aliasSMN; ESPI1SMNx00000070; ESPI1SMN=02DCA000h

\_link0\_aliasSMN; ESPISMNx00000070; ESPISMN=02DC5000h

\_link1\_aliasHOSTLEGACY; ESPI1x00000070; ESPI1=FEC30000h

\_link0\_aliasHOSTLEGACY; ESPIx00000070; ESPI=FEC20000h

Bits	Description
31	<b>FLASH_REQ_INT.</b> Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> For MAFS, Flash Request Received Status:Upstream Flash Request is received and valid to read. This bit set when Upstream Flash Request is received and valid to read. For SAFS, Flash Completion Received Status: This bit set when Flash completion with data (for flash read), or flash completion without data (for flash write or flash erase) or unsuccessful completion are received. Only for SW programming interface sending PUT_FLASH_NP. The condition is when GET_FLASH_C occurs, or PUT_FLASH_NP with immediately completion response. [PUT_FLASH_NP (write/erase) cycle with header response (PUT_FLASH_NP_HEADER_EN set to 1) or PUT_FLASH_NP (read) cycle with header/data response (PUT_FLASH_NP_HEADER_DATA_EN set to 1)].
30	<b>RXOOB_INT.</b> Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>OOB</b> Message Received Status:Upstream OOB Message is received and valid to read. This bit set when Upstream OOB Message is received and valid to read.
29	<b>RXMSG_INT.</b> Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Peripheral Message Received Status:Upstream Peripheral Msg is received and valid to read. This bit set when Upstream Peripheral Msg is received and valid to read.
28	<b>DNCMD_INT.</b> Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Downstream Register Command Complete Status:Downstream eSPI Registers Command has completed. This bit is set when downstream register programming has been completed. Software can program next command or get the data.
27	<b>RXVW_GRP3_INT.</b> Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Virtual Wire Index Group 3 Received Status:Virtual Wire Index Group3 register specified Virtual Wire Packet is received. This bit set when Virtual Wire Index Group3 register specified VW packet has been received.
26	<b>RXVW_GRP2_INT.</b> Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Virtual Wire Index Group 2 Received Status:Virtual Wire Index Group2 register specified Virtual Wire Packet is received. This bit set when Virtual Wire Index Group2 register specified VW packet has been received.
25	<b>RXVW_GRP1_INT.</b> Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Virtual Wire Index Group 1 Received Status:Virtual Wire Index Group1 register specified Virtual Wire Packet is received. This bit set when Virtual Wire Index Group1 register specified VW packet has been received.
24	<b>RXVW_GRP0_INT.</b> Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Virtual Wire Index Group 0 Received Status:Virtual Wire Index Group0 register specified Virtual Wire Packet is received. This bit set when Virtual Wire Index Group0 register specified VW packet has been received.
23:20	Reserved.
19	<b>WDG_TIMEOUT_INT.</b> Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Alink Bus Watch Dog Timer Timeout Status:Alink bus Watch dog timer timeout. This bit set when downstream command retry many times, and over the watch dog timeout value specified in eSPI Global Control and Status Register0
18	<b>MST_ABORT_INT.</b> Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Alink Bus Master Abort Status:eSPI Controller Master aborts. This bit set when eSPI controller doing Master Abort.
17	<b>UPFIFO_WDGTO.</b> Read, <a href="#">Write-1-to-clear</a> . Reset: 0. This bit is set when UPFIFO watchdog timer times out, and at the same time, eSPIx10[3], UPFIFO Valid Status bit will be cleared since this's a software error by not reading data out of UPFIFO in time, which might cause Get_Status not to be sent out for the incoming Alert event.
16	Reserved.
15	<b>PROTOCOL_ERR_INT.</b> Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Protocol ERROR detected Status:Protocol ERROR detected.
14	<b>RXFLASH_OVERFLOW_INT.</b> Read, <a href="#">Write-1-to-clear</a> . Reset: 0. FLASH Packet Data Length Over 256 bytes Status:FLASH Packet data Over 256 bytes. This bit set when FLASH packet data length is over 256 bytes.
13	<b>RXMSG_OVERFLOW_INT.</b> Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Peripheral Message Data Length Over 32 bytes Status:Peripheral Message Data Packet data Over 32 bytes. This bit set when Peripheral Message Data length is over 32 bytes.

12	<b>RXOOB_OVERFLOW_INT</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>OOB</b> Packet Data Length Over 256 bytes Status: OOB Packet data Over 256 bytes. This bit set when OOB packet data length is over 256 bytes.
11	<b>ILLEGAL_LEN_INT</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Illegal Response Length Received Status: Illegal Length Received. This bit set when slave returns a wrong length. Example 1. When peripheral downstream nonpost command with length = 3 receives slave's CPL/CPLD with length not equal to 3. 2. When slave sends the upstream request with length larger than max payload(64 bytes)
10	<b>ILLEGAL_TAG_INT</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Illegal Response Tag Received Status: Illegal Tag Received. This bit set when slave returns a wrong tag. For example, Peripheral send MEMR with Tag=0, but slave returns CPLD with Tag = 5.
9	<b>UNSUCSS_CPL_INT</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Unsuccessful CPL Received Status: Unsuccessful completion without data received. This bit will set when Unsuccessful Completion Packet is received.
8	<b>UNKNOWN_CT_INT</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Invalid Cycle Type Received Status: Unrecognized Cycle Type received. This bit will set when Unrecognized Cycle Type is received.
7	<b>UNKNOWN_RSP_INT</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Invalid Response Code Received Status: Unrecognized Response received. This bit will set when Unrecognized response code is received.
6	<b>NON_FATAL_ERR_INT</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. NON_FATAL_ERROR Response Code Received Status: NON_FATAL_ERROR Response Code received from slave. This bit will set when NON_FATAL_ERROR response code is received.
5	<b>FATAL_ERR_INT</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. FATAL_ERROR Response Code Received Status: FATAL_ERROR Response Code received from slave. This bit will set when FATAL_ERROR response code is received.
4	<b>NO_RSP_INT</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. NO_RESPONSE Code received Status: No_Response Response Code received from slave. This bit will set when No_Response response code is received.
3	Reserved.
2	<b>CRC_ERR_INT</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. CRC Error detected Status: CRC ERROR detected on response phase. This bit will set when CRC ERROR is detected on response phase.
1	<b>WAIT_TIMEOUT_INT</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. eSPI Bus Wait State Insertion Max Out Status: eSPI Wait State timer timeout. This bit will set when Slave insert more wait state than the counter specified in eSPI Global Control and Status Register0
0	<b>BUS_ERR_INT</b> . Read, <a href="#">Write-1-to-clear</a> . Reset: 0. eSPI Bus Timing Error Status: eSPI Bus timing Error is detected. This bit will set when eSPI link block detect Slave doesn't driver 1 after response CRC, and before CS# de-asserted.

#### ESPI1SMNx00000074...ESPISMNx00000074 (FCH::ITF::ESPI::SLAVE0\_RXMSG\_HDR0)

Read-only. Reset: 0000\_0000h.

\_link1\_aliasSMN; ESPI1SMNx00000074; ESPI1SMN=02DCA000h

\_link0\_aliasSMN; ESPISMNx00000074; ESPISMN=02DC5000h

\_link1\_aliasHOSTLEGACY; ESPI1x00000074; ESPI1=FEC30000h

\_link0\_aliasHOSTLEGACY; ESPIx00000074; ESPI=FEC20000h

Bits	Description
31:24	<b>BYTE3</b> . Read-only. Reset: 00h. Received Peripheral Message code
23:16	<b>BYTE2</b> . Read-only. Reset: 00h. Received Peripheral Message Length[7:0]
15:8	<b>BYTE1</b> . Read-only. Reset: 00h. [15:12]: Tag [11:8]: Length[11:8]
7:0	<b>CYCLETYP</b> . Read-only. Reset: 00h. CycleType[7:0] for Peripheral Msg/MsgD

**ESPI1SMNx00000078...ESPISMNx00000078 (FCH::ITF::ESPI::SLAVE0\_RXMSG\_HDR1)**

Read-only. Reset: 0000\_0000h.

\_link1\_aliasSMN; ESPI1SMNx00000078; ESPI1SMN=02DCA000h

\_link0\_aliasSMN; ESPISMNx00000078; ESPISMN=02DC5000h

\_link1\_aliasHOSTLEGACY; ESPI1x00000078; ESPI1=FEC30000h

\_link0\_aliasHOSTLEGACY; ESPIx00000078; ESPI=FEC20000h

**Bits Description**31:24 **SPECIFIC\_BYTE3**. Read-only. Reset: 00h. Peripheral Message Specific Byte323:16 **SPECIFIC\_BYTE2**. Read-only. Reset: 00h. Peripheral Message Specific Byte215:8 **SPECIFIC\_BYTE1**. Read-only. Reset: 00h. Peripheral Message Specific Byte17:0 **SPECIFIC\_BYTE0**. Read-only. Reset: 00h. Peripheral Message Specific Byte0**ESPI1SMNx0000007C...ESPISMNx0000007C (FCH::ITF::ESPI::SLAVE0\_RXMSG\_DATA\_PORT)**

Read-only. Reset: 0000\_0000h.

\_link1\_aliasSMN; ESPI1SMNx0000007C; ESPI1SMN=02DCA000h

\_link0\_aliasSMN; ESPISMNx0000007C; ESPISMN=02DC5000h

\_link1\_aliasHOSTLEGACY; ESPI1x0000007C; ESPI1=FEC30000h

\_link0\_aliasHOSTLEGACY; ESPIx0000007C; ESPI=FEC20000h

**Bits Description**31:0 **RXMSG\_DATA**. Read-only. Reset: 0000\_0000h.**ESPI1SMNx00000080...ESPISMNx00000080 (FCH::ITF::ESPI::SLAVE0\_IO\_BASE\_REG2)**

Read-write. Reset: 0000\_0000h.

\_link1\_aliasSMN; ESPI1SMNx00000080; ESPI1SMN=02DCA000h

\_link0\_aliasSMN; ESPISMNx00000080; ESPISMN=02DC5000h

\_link1\_aliasHOSTLEGACY; ESPI1x00000080; ESPI1=FEC30000h

\_link0\_aliasHOSTLEGACY; ESPIx00000080; ESPI=FEC20000h

**Bits Description**31:16 **RANGE5**. Read-write. Reset: 0000h. IO decode base address for Range 515:0 **RANGE4**. Read-write. Reset: 0000h. IO decode base address for Range 4**ESPI1SMNx00000084...ESPISMNx00000084 (FCH::ITF::ESPI::SLAVE0\_IO\_BASE\_REG3)**

Read-write. Reset: 0000\_0000h.

\_link1\_aliasSMN; ESPI1SMNx00000084; ESPI1SMN=02DCA000h

\_link0\_aliasSMN; ESPISMNx00000084; ESPISMN=02DC5000h

\_link1\_aliasHOSTLEGACY; ESPI1x00000084; ESPI1=FEC30000h

\_link0\_aliasHOSTLEGACY; ESPIx00000084; ESPI=FEC20000h

**Bits Description**31:16 **RANGE7**. Read-write. Reset: 0000h. IO decode base address for Range 715:0 **RANGE6**. Read-write. Reset: 0000h. IO decode base address for Range 6**ESPI1SMNx00000088...ESPISMNx00000088 (FCH::ITF::ESPI::SLAVE0\_IO\_SIZE1)**

Read-write. Reset: 0000\_0000h.

\_link1\_aliasSMN; ESPI1SMNx00000088; ESPI1SMN=02DCA000h

\_link0\_aliasSMN; ESPISMNx00000088; ESPISMN=02DC5000h

\_link1\_aliasHOSTLEGACY; ESPI1x00000088; ESPI1=FEC30000h

\_link0\_aliasHOSTLEGACY; ESPIx00000088; ESPI=FEC20000h

**Bits Description**31:24 **RANGE7**. Read-write. Reset: 00h. Programmable IO Range7 size23:16 **RANGE6**. Read-write. Reset: 00h. Programmable IO Range6 size15:8 **RANGE5**. Read-write. Reset: 00h. Programmable IO Range5 size7:0 **RANGE4**. Read-write. Reset: 00h. Programmable IO Range4 size

**ESPI1SMNx0000008C...ESPISMNx0000008C (FCH::ITF::ESPI::SLAVE0\_IO\_BASE\_REG4)**

Read-write. Reset: 0000\_0000h.

\_link1\_aliasSMN; ESPI1SMNx0000008C; ESPI1SMN=02DCA000h

\_link0\_aliasSMN; ESPISMNx0000008C; ESPISMN=02DC5000h

\_link1\_aliasHOSTLEGACY; ESPI1x0000008C; ESPI1=FEC30000h

\_link0\_aliasHOSTLEGACY; ESPIx0000008C; ESPI=FEC20000h

**Bits Description**31:16 **RANGE9.** Read-write. Reset: 0000h. IO decode base address for Range 915:0 **RANGE8.** Read-write. Reset: 0000h. IO decode base address for Range 8**ESPI1SMNx00000090...ESPISMNx00000090 (FCH::ITF::ESPI::SLAVE0\_IO\_BASE\_REG5)**

Read-write. Reset: 0000\_0000h.

\_link1\_aliasSMN; ESPI1SMNx00000090; ESPI1SMN=02DCA000h

\_link0\_aliasSMN; ESPISMNx00000090; ESPISMN=02DC5000h

\_link1\_aliasHOSTLEGACY; ESPI1x00000090; ESPI1=FEC30000h

\_link0\_aliasHOSTLEGACY; ESPIx00000090; ESPI=FEC20000h

**Bits Description**31:16 **RANGE11.** Read-write. Reset: 0000h. IO decode base address for Range 1115:0 **RANGE10.** Read-write. Reset: 0000h. IO decode base address for Range 10**ESPI1SMNx00000094...ESPISMNx00000094 (FCH::ITF::ESPI::SLAVE0\_IO\_SIZE2)**

Read-write. Reset: 0000\_0000h.

\_link1\_aliasSMN; ESPI1SMNx00000094; ESPI1SMN=02DCA000h

\_link0\_aliasSMN; ESPISMNx00000094; ESPISMN=02DC5000h

\_link1\_aliasHOSTLEGACY; ESPI1x00000094; ESPI1=FEC30000h

\_link0\_aliasHOSTLEGACY; ESPIx00000094; ESPI=FEC20000h

**Bits Description**31:24 **RANGE11.** Read-write. Reset: 00h. Programmable IO Range11 size23:16 **RANGE10.** Read-write. Reset: 00h. Programmable IO Range10 size15:8 **RANGE9.** Read-write. Reset: 00h. Programmable IO Range9 size7:0 **RANGE8.** Read-write. Reset: 00h. Programmable IO Range8 size**ESPI1SMNx00000098...ESPISMNx00000098 (FCH::ITF::ESPI::RESERVED\_RXMSG\_REG6)**

Read-write. Reset: 0000\_0000h.

\_link1\_aliasSMN; ESPI1SMNx00000098; ESPI1SMN=02DCA000h

\_link0\_aliasSMN; ESPISMNx00000098; ESPISMN=02DC5000h

\_link1\_aliasHOSTLEGACY; ESPI1x00000098; ESPI1=FEC30000h

\_link0\_aliasHOSTLEGACY; ESPIx00000098; ESPI=FEC20000h

**Bits Description**

31:24 Reserved.

23:0 **VW\_IRQ\_Inactive\_Polarity.** Read-write. Reset: 00\_0000h. This field is used to change the polarity of default value of Rx VW IRQ status. The default value of Rx VW IRQ is 0h, and a transition of 0 to 1b with this field shall change the default value of Rx VW IRQ to 1b

**ESPI1SMNx0000009C...ESPISMNx0000009C (FCH::ITF::ESPI::SLAVE0\_RXVW)**

Reset: 0007\_0C00h.

\_link1\_aliasSMN; ESPI1SMNx0000009C; ESPI1SMN=02DCA000h

\_link0\_aliasSMN; ESPISMNx0000009C; ESPISMN=02DC5000h

\_link1\_aliasHOSTLEGACY; ESPI1x0000009C; ESPI1=FEC30000h

\_link0\_aliasHOSTLEGACY; ESPIx0000009C; ESPI=FEC20000h

Bits	Description
31	<b>CPUTEMP_REQ.</b> Read, <a href="#">Write-1-to-clear</a> . Reset: 0. CPU Temperature Request(CPUTEMP_REQ): sent by Slave to request to read CPU temperature(not from standard spec). Set when received the CPUTEMP_REQ VW
30	<b>RTCTIME_REQ.</b> Read, <a href="#">Write-1-to-clear</a> . Reset: 0. RTC TIME Request(RTCTIME_REQ): sent by Slave to request to read RTC time(not from standard spec). Set when received the RTCTIME_REQ VW
29:20	Reserved.
19	<b>HOST_RST_ACK.</b> Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Host Reset Acknowledge(HOST_RST_ACK): Sent by Slave to acknowledge received HOST_RST_WARN virtual wire.
18	<b>RCIN_B.</b> Read, <a href="#">Write-1-only</a> . Reset: 1. Reset CPU INIT(RCIN#): Send to request CPU reset on behalf of the Keyboard controller.
17	<b>SMI_B.</b> Read, <a href="#">Write-1-only</a> . Reset: 1. System Management Interrupt(SMI#): Sent as general Purpose alert resulting in SMI code being invoked by BIOS.
16	<b>SCI_B.</b> Read, <a href="#">Write-1-only</a> . Reset: 1. System Controller Interrupt(SCI#): Sent as general Purpose alert resulting in ACPI method being invoked by OS.
15	<b>SLAVE_BOOT_LOAD_STS.</b> Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Slave Boot Load Status: Sent by <a href="#">EC</a> or <a href="#">BMC</a> upon completion of Slave Boot Load from the master attached flash. 0: The boot image is corrupted, incomplete or otherwise unusable. 1: The boot code load was successful and that the integrity of the image is intact, or the boot code load from master attached flash is not required.
14	<b>ERROR_NONFATAL.</b> Read, <a href="#">Write-1-to-clear</a> . Reset: 0. NON FATAL ERROR(ERROR_NONFATAL): Sent when a non-fatal error is detected not due to eSPI transaction on the bus.Note: Non-atal Error due to transaction on eSPI bus will be signaled through RSP phase.
13	<b>ERROR_FATAL.</b> Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Fatal Error(ERROR_FATAL): Sent when a fatal error is detected not due to eSPI transaction on the bus.Note: Fatal Error due to transaction on eSPI bus will be signaled through RSP phase.
12	<b>SLAVE_BOOT_LOAD_DONE.</b> Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Slave Boot Load Done(SLAVE_BOOT_LOAD_DONE):Sent when <a href="#">EC</a> or <a href="#">BMC</a> has completed its boot process as indication to eSPI master to continue with the G3 to S0 exit.
11	<b>PME_B.</b> Read, <a href="#">Write-1-only</a> . Reset: 1. PCI Power Management Event(PME#):Shared by multiple eSPI
10	<b>WAKE_B.</b> Read, <a href="#">Write-1-only</a> . Reset: 1. To wavke the Host from Sx on any event(WAKE#)
9	Reserved.
8	<b>OOB_RST_ACK.</b> Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <a href="#">OOB</a> reset Acknowledge(OOB_RST_ACK):Sent by Slave to acknowledge received OOB_RST_ACK virtual wire from Host.
7:5	<b>IRQ_STS.</b> Read-only. Reset: 0h.
	<b>Description:</b> IRQ Satus: IRQ status which specified by IRQ selection: Bits Status 000 IRQ keep 0 unchanged 001 IRQ keep 1 unchanged 010 IRQ changed from 1 to 0 (Clear) 011 IRQ changed from 0 to 1 (Set) 100 IRQ changed from 0->1->0(High pulse) 101 IRQ changed from 1->0->1(Low pulse) 110 IRQ changed from 1->1->0 or 1->0->0 or 0->0->0 111 IRQ changed from 0->0->1 or 0->1->1 or 1->1->1
4:0	<b>IRQ_SEL.</b> Read-write. Reset: 00h.



	<b>Description:</b> This field determine Slave N Received Virtual Wires Register bit[7:5] output which IRQ status. Bits Selection 00000: IRQ0 00001 IRQ1 .... 10111:IRQ23 others:Reserved
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#### ESPI1SMNx000000A0...ESPISMNx000000A0 (FCH::ITF::ESPI::SLAVE0\_RXVW\_DATA)

Read-only. Reset: 0000_0000h.	
_link1_aliasSMN; ESPI1SMNx000000A0; ESPI1SMN=02DCA000h	
_link0_aliasSMN; ESPISMNx000000A0; ESPISMN=02DC5000h	
_link1_aliasHOSTLEGACY; ESPI1x000000A0; ESPI1=FEC30000h	
_link0_aliasHOSTLEGACY; ESPIx000000A0; ESPI=FEC20000h	
Bits	Description
31:24	<b>GRP3.</b> Read-only. Reset: 00h. <b>Description:</b> Group3 Virtual Wire Data Register: When VW MISC CONTRL register bit3 set, eSPI master will check each received VW Index, if the received Index matches with Group3 Virtual Wire Index Selection Register, eSPI Master will update this field with the new received value.
23:16	<b>GRP2.</b> Read-only. Reset: 00h. <b>Description:</b> Group2 Virtual Wire Data Register: When VW MISC CONTRL register bit2 set, eSPI master will check each received VW Index, if the received Index matches with Group2 Virtual Wire Index Selection Register, eSPI Master will update this field with the new received value.
15:8	<b>GRP1.</b> Read-only. Reset: 00h. <b>Description:</b> Group1 Virtual Wire Data Register: When VW MISC CONTRL register bit1 set, eSPI master will check each received VW Index, if the received Index matches with Group1 Virtual Wire Index Selection Register, eSPI Master will update this field with the new received value.
7:0	<b>GRP0.</b> Read-only. Reset: 00h. <b>Description:</b> Group0 Virtual Wire Data Register: When VW MISC CONTRL register bit0 set, eSPI master will check each received VW Index, if the received Index matches with Group0 Virtual Wire Index Selection Register, eSPI Master will update this field with the new received value.

#### ESPI1SMNx000000A4...ESPISMNx000000A4 (FCH::ITF::ESPI::SLAVE0\_RXVW\_INDEX)

Read-write. Reset: 0000_0000h.	
_link1_aliasSMN; ESPI1SMNx000000A4; ESPI1SMN=02DCA000h	
_link0_aliasSMN; ESPISMNx000000A4; ESPISMN=02DC5000h	
_link1_aliasHOSTLEGACY; ESPI1x000000A4; ESPI1=FEC30000h	
_link0_aliasHOSTLEGACY; ESPIx000000A4; ESPI=FEC20000h	
Bits	Description
31:24	<b>GRP3.</b> Read-write. Reset: 00h. Group3 Virtual Wire Index Selection Register
23:16	<b>GRP2.</b> Read-write. Reset: 00h. Group2 Virtual Wire Index Selection Register
15:8	<b>GRP1.</b> Read-write. Reset: 00h. Group1 Virtual Wire Index Selection Register
7:0	<b>GRP0.</b> Read-write. Reset: 00h. Group0 Virtual Wire Index Selection Register

**ESPI1SMNx000000A8...ESPISMNx000000A8 (FCH::ITF::ESPI::SLAVE0\_RXVW\_MISC\_CNTL)**

Read-write. Reset: 0000\_0000h.

\_link1\_aliasSMN; ESPI1SMNx000000A8; ESPI1SMN=02DCA000h

\_link0\_aliasSMN; ESPISMNx000000A8; ESPISMN=02DC5000h

\_link1\_aliasHOSTLEGACY; ESPI1x000000A8; ESPI1=FEC30000h

\_link0\_aliasHOSTLEGACY; ESPIx000000A8; ESPI=FEC20000h

Bits	Description
31	<b>IRQ23_MASK.</b> Read-write. Reset: 0.
30	<b>IRQ22_MASK.</b> Read-write. Reset: 0.
29	<b>IRQ21_MASK.</b> Read-write. Reset: 0.
28	<b>IRQ20_MASK.</b> Read-write. Reset: 0.
27	<b>IRQ19_MASK.</b> Read-write. Reset: 0.
26	<b>IRQ18_MASK.</b> Read-write. Reset: 0.
25	<b>IRQ17_MASK.</b> Read-write. Reset: 0.
24	<b>IRQ16_MASK.</b> Read-write. Reset: 0.
23	<b>IRQ15_MASK.</b> Read-write. Reset: 0.
22	<b>IRQ14_MASK.</b> Read-write. Reset: 0.
21	<b>IRQ13_MASK.</b> Read-write. Reset: 0.
20	<b>IRQ12_MASK.</b> Read-write. Reset: 0.
19	<b>IRQ11_MASK.</b> Read-write. Reset: 0.
18	<b>IRQ10_MASK.</b> Read-write. Reset: 0.
17	<b>IRQ9_MASK.</b> Read-write. Reset: 0.
16	<b>IRQ8_MASK.</b> Read-write. Reset: 0.
15	<b>IRQ7_MASK.</b> Read-write. Reset: 0.
14	<b>IRQ6_MASK.</b> Read-write. Reset: 0.
13	<b>IRQ5_MASK.</b> Read-write. Reset: 0.
12	<b>IRQ4_MASK.</b> Read-write. Reset: 0.
11	<b>IRQ3_MASK.</b> Read-write. Reset: 0.
10	<b>IRQ2_MASK.</b> Read-write. Reset: 0.
9	<b>IRQ1_MASK.</b> Read-write. Reset: 0.
8	<b>IRQ0_MASK.</b> Read-write. Reset: 0.
7	<b>CPUTEMP_RTCTIME_VW_INDEX_SEL.</b> Read-write. Reset: 0. CPU_TEMP/RTC TIME VW index selection. 0:index 53(decimal), 1: index 63(decimal)
6	<b>CPUTEMP_RTCTIME_VW_EN.</b> Read-write. Reset: 0. Enabled hardware to Receive VW packet of index 53(63) from Slave to indicate the slave to request CPU_TEMP/RTC Time info. 1: Enable, 0: Disable.
5	Reserved.
4	<b>SUS_STAT_VWEN.</b> Read-write. Reset: 0. Enabled hardware to send VW packet when SUS_STAT# changes. 1: Enable, 0: Disable.
3	<b>GRP3_EN.</b> Read-write. Reset: 0. GRP3 Enable : When Set, VW channel will check received Index, if Index is same as Group3 Index register setting; VW will store the Data into Group3 Data register.
2	<b>GRP2_EN.</b> Read-write. Reset: 0. GRP2 Enable : When Set, VW channel will check received Index, if Index is same as Group2 Index register setting; VW will store the Data into Group2 Data register.
1	<b>GRP1_EN.</b> Read-write. Reset: 0. GRP1 Enable : When Set, VW channel will check received Index, if Index is same as Group1 Index register setting; VW will store the Data into Group1 Data register.
0	<b>GRP0_EN.</b> Read-write. Reset: 0. GRP0 Enable : When Set, VW channel will check received Index, if Index is same as Group0 Index register setting; VW will store the Data into Group0 Data register.

**ESPI1SMNx000000AC...ESPISMNx000000AC (FCH::ITF::ESPI::SLAVE0\_RXVW\_POLARITY)**

Read-write. Reset: 0000\_0000h.

\_link1\_aliasSMN; ESPI1SMNx000000AC; ESPI1SMN=02DCA000h

\_link0\_aliasSMN; ESPISMNx000000AC; ESPISMN=02DC5000h

\_link1\_aliasHOSTLEGACY; ESPI1x000000AC; ESPI1=FEC30000h

\_link0\_aliasHOSTLEGACY; ESPIx000000AC; ESPI=FEC20000h

Bits	Description
31:29	Reserved.
28	<b>OOB_RST_WARN_EN.</b> Read-write. Reset: 0. OOB_RST_WARN Enable: Enable Hardware sending Virtual Wire packet when HOST_RST_WARN change. There is no physical oob_Rst_warn output, so if there is HOST_RST_WARN asserted OOB_RST_WARN VW will be send if this bit is set. 1:enable; 0:disable
27	<b>NMIOUT_EN.</b> Read-write. Reset: 0. NMIOUT Enable: Enable Hardware sending Virtual Wire packet when NMIOUT change. 1:enable; 0:disable
26	<b>SMIOUT_EN.</b> Read-write. Reset: 0. SMIOUT Enable: Enable Hardware sending Virtual Wire packet when SMIOUT change. 1:enable; 0:disable
25	<b>HOST_RST_WARN_DIS.</b> Read-write. Reset: 0. HOST_RST_WARN Disable: Default is Enable Hardware sending Virtual Wire packet when HOST_RST_WARN change. 0:enable; 1:disable.
24	<b>PLTRSTB_DIS.</b> Read-write. Reset: 0. PLTRST# Disable: Default 0 to Enable Hardware sending Virtual Wire packet when PLTRST# change. 0:enable; 1:disable.
23	<b>IRQ23_POLARITY.</b> Read-write. Reset: 0.
22	<b>IRQ22_POLARITY.</b> Read-write. Reset: 0.
21	<b>IRQ21_POLARITY.</b> Read-write. Reset: 0.
20	<b>IRQ20_POLARITY.</b> Read-write. Reset: 0.
19	<b>IRQ19_POLARITY.</b> Read-write. Reset: 0.
18	<b>IRQ18_POLARITY.</b> Read-write. Reset: 0.
17	<b>IRQ17_POLARITY.</b> Read-write. Reset: 0.
16	<b>IRQ16_POLARITY.</b> Read-write. Reset: 0.
15	<b>IRQ15_POLARITY.</b> Read-write. Reset: 0.
14	<b>IRQ14_POLARITY.</b> Read-write. Reset: 0.
13	<b>IRQ13_POLARITY.</b> Read-write. Reset: 0.
12	<b>IRQ12_POLARITY.</b> Read-write. Reset: 0.
11	<b>IRQ11_POLARITY.</b> Read-write. Reset: 0.
10	<b>IRQ10_POLARITY.</b> Read-write. Reset: 0.
9	<b>IRQ9_POLARITY.</b> Read-write. Reset: 0.
8	<b>IRQ8_POLARITY.</b> Read-write. Reset: 0.
7	<b>IRQ7_POLARITY.</b> Read-write. Reset: 0.
6	<b>IRQ6_POLARITY.</b> Read-write. Reset: 0.
5	<b>IRQ5_POLARITY.</b> Read-write. Reset: 0.
4	<b>IRQ4_POLARITY.</b> Read-write. Reset: 0.
3	<b>IRQ3_POLARITY.</b> Read-write. Reset: 0.
2	<b>IRQ2_POLARITY.</b> Read-write. Reset: 0.
1	<b>IRQ1_POLARITY.</b> Read-write. Reset: 0.
0	<b>IRQ0_POLARITY.</b> Read-write. Reset: 0.

**ESPI1SMNx000000B0...ESPISMNx000000B0 (FCH::ITF::ESPI::SLAVE0\_IO\_BASE\_REG6)**

Read-write. Reset: 0000\_0000h.

[\\_link1\\_aliasSMN](#); ESPI1SMNx000000B0; ESPI1SMN=02DCA000h[\\_link0\\_aliasSMN](#); ESPISMNx000000B0; ESPISMN=02DC5000h[\\_link1\\_aliasHOSTLEGACY](#); ESPI1x000000B0; ESPI1=FEC30000h[\\_link0\\_aliasHOSTLEGACY](#); ESPIx000000B0; ESPI=FEC20000h**Bits Description**31:16 **RANGE13.** Read-write. Reset: 0000h. IO decode base address for Range 1315:0 **RANGE12.** Read-write. Reset: 0000h. IO decode base address for Range 12**ESPI1SMNx000000B4...ESPISMNx000000B4 (FCH::ITF::ESPI::SLAVE0\_IO\_BASE\_REG7)**

Read-write. Reset: 0000\_0000h.

[\\_link1\\_aliasSMN](#); ESPI1SMNx000000B4; ESPI1SMN=02DCA000h[\\_link0\\_aliasSMN](#); ESPISMNx000000B4; ESPISMN=02DC5000h[\\_link1\\_aliasHOSTLEGACY](#); ESPI1x000000B4; ESPI1=FEC30000h[\\_link0\\_aliasHOSTLEGACY](#); ESPIx000000B4; ESPI=FEC20000h**Bits Description**31:16 **RANGE15.** Read-write. Reset: 0000h. IO decode base address for Range 1515:0 **RANGE14.** Read-write. Reset: 0000h. IO decode base address for Range 14**ESPI1SMNx000000B8...ESPISMNx000000B8 (FCH::ITF::ESPI::SLAVE0\_IO\_SIZE3)**

Read-write. Reset: 0000\_0000h.

[\\_link1\\_aliasSMN](#); ESPI1SMNx000000B8; ESPI1SMN=02DCA000h[\\_link0\\_aliasSMN](#); ESPISMNx000000B8; ESPISMN=02DC5000h[\\_link1\\_aliasHOSTLEGACY](#); ESPI1x000000B8; ESPI1=FEC30000h[\\_link0\\_aliasHOSTLEGACY](#); ESPIx000000B8; ESPI=FEC20000h**Bits Description**31:24 **RANGE15.** Read-write. Reset: 00h. Programmable IO Range15 size23:16 **RANGE14.** Read-write. Reset: 00h. Programmable IO Range14 size15:8 **RANGE13.** Read-write. Reset: 00h. Programmable IO Range13 size7:0 **RANGE12.** Read-write. Reset: 00h. Programmable IO Range12 size**ESPI1SMNx000000BC...ESPISMNx000000BC (FCH::ITF::ESPI::SLAVE0\_MMIO\_BASE\_REG4)**

Read-write. Reset: 0000\_0000h.

[\\_link1\\_aliasSMN](#); ESPI1SMNx000000BC; ESPI1SMN=02DCA000h[\\_link0\\_aliasSMN](#); ESPISMNx000000BC; ESPISMN=02DC5000h[\\_link1\\_aliasHOSTLEGACY](#); ESPI1x000000BC; ESPI1=FEC30000h[\\_link0\\_aliasHOSTLEGACY](#); ESPIx000000BC; ESPI=FEC20000h**Bits Description**31:0 **RANGE4.** Read-write. Reset: 0000\_0000h. [MMIO](#) decode base address for Range 4**ESPI1SMNx000000C0...ESPISMNx000000C0 (FCH::ITF::ESPI::SLAVE0\_MMIO\_SIZE\_REG2)**

Read-write. Reset: 0000\_0000h.

[\\_link1\\_aliasSMN](#); ESPI1SMNx000000C0; ESPI1SMN=02DCA000h[\\_link0\\_aliasSMN](#); ESPISMNx000000C0; ESPISMN=02DC5000h[\\_link1\\_aliasHOSTLEGACY](#); ESPI1x000000C0; ESPI1=FEC30000h[\\_link0\\_aliasHOSTLEGACY](#); ESPIx000000C0; ESPI=FEC20000h**Bits Description**

31:25 Reserved.

24:0 **RANGE4.** Read-write. Reset: 000\_0000h. Programmable [MMIO](#) Range4 size, 1M - vA.6, 32M - vA.7

**ESPI1SMNx000000C4...ESPISMNx000000C4 (FCH::ITF::ESPI::MMIO\_CPUTEMP)**

Read-write. Reset: 0000\_0000h.

\_link1\_aliasSMN; ESPI1SMNx000000C4; ESPI1SMN=02DCA000h

\_link0\_aliasSMN; ESPISMNx000000C4; ESPISMN=02DC5000h

\_link1\_aliasHOSTLEGACY; ESPI1x000000C4; ESPI1=FEC30000h

\_link0\_aliasHOSTLEGACY; ESPIx000000C4; ESPI=FEC20000h

**Bits Description**31:0 **MMIO\_CPUTEMP**. Read-write. Reset: 0000\_0000h. [MMIO](#) address to send down CPU temperture.**ESPI1SMNx000000C8...ESPISMNx000000C8 (FCH::ITF::ESPI::MMIO\_RTCTIME)**

Read-write. Reset: 0000\_0000h.

\_link1\_aliasSMN; ESPI1SMNx000000C8; ESPI1SMN=02DCA000h

\_link0\_aliasSMN; ESPISMNx000000C8; ESPISMN=02DC5000h

\_link1\_aliasHOSTLEGACY; ESPI1x000000C8; ESPI1=FEC30000h

\_link0\_aliasHOSTLEGACY; ESPIx000000C8; ESPI=FEC20000h

**Bits Description**31:0 **MMIO\_RTCTIME**. Read-write. Reset: 0000\_0000h. [MMIO](#) address to send down RTC TIME.**ESPI1SMNx000000CC...ESPISMNx000000CC (FCH::ITF::ESPI::ESPI\_MiscCtrl1)**

Read-write. Reset: 0000\_0000h.

\_link1\_aliasSMN; ESPI1SMNx000000CC; ESPI1SMN=02DCA000h

\_link0\_aliasSMN; ESPISMNx000000CC; ESPISMN=02DC5000h

\_link1\_aliasHOSTLEGACY; ESPI1x000000CC; ESPI1=FEC30000h

\_link0\_aliasHOSTLEGACY; ESPIx000000CC; ESPI=FEC20000h

**Bits Description**31:17 **ESPI\_MiscCtrl1\_RESERVED0**. Read-write. Reset: 0000h.16 **UPFIFO\_WDG\_TimerEn**. Read-write. Reset: 0. Set the bit to enable the UPFIFO watchdog timer.15:0 **UPFIFO\_WDG\_Timer**. Read-write. Reset: 0000h.

**Description:** UPFIFO Watch dog counter: This counter times the duration of eSPIx10[3] staying at high level in case software is too slow to clear eSPIx10[3]. This counter will cumulate itself by 1 every 16 cycles of Alink clock. The setting value for this field is recommended to be less than the Alink Watchdog Timer so that the below situation can be saved back.

In some circumstances, software might be very slow or fail to clear eSPIx10[3]. At that time, if a Put\_Flash\_NP from register interface is deferred when SAFS flash modifier is enabled, eSPIx10[3] staying at high will prevent controller from sending out Get\_Status when Alert event is received (Otherwise, device might respond with flash completion data together with Accept response for Get\_Status, which will override the UPFIFO).

When this counter times out, it will clear eSPIx10[3] and record this software error into eSPIx70[17].

**ESPI1SMNx000000D0...ESPISMNx000000D0 (FCH::ITF::ESPI::ESPI\_LOWSECURITY\_CONTROL\_REG\_RESERVED1)**

Read-write. Reset: 0000\_0000h.

\_link1\_aliasSMN; ESPI1SMNx000000D0; ESPI1SMN=02DCA000h

\_link0\_aliasSMN; ESPISMNx000000D0; ESPISMN=02DC5000h

\_link1\_aliasHOSTLEGACY; ESPI1x000000D0; ESPI1=FEC30000h

\_link0\_aliasHOSTLEGACY; ESPIx000000D0; ESPI=FEC20000h

**Bits Description**31:0 **ESPI\_LOWSECURITY\_CONTROL\_REG\_RESERVED1**. Read-write. Reset: 0000\_0000h.

**ESPI1SMNx000000D4...ESPISMNx000000D4**  
**(FCH::ITF::ESPI::ESPI\_LOWSECURITY\_CONTROL\_REG\_RESERVED2)**

Read-write. Reset: 0000\_0000h.

\_link1\_aliasSMN; ESPI1SMNx000000D4; ESPI1SMN=02DCA000h\_link0\_aliasSMN; ESPISMNx000000D4; ESPISMN=02DC5000h\_link1\_aliasHOSTLEGACY; ESPI1x000000D4; ESPI1=FEC30000h\_link0\_aliasHOSTLEGACY; ESPIx000000D4; ESPI=FEC20000h

Bits	Description
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31:0	ESPI_LOWSECURITY_CONTROL_REG_RESERVED2. Read-write. Reset: 0000_0000h.
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**ESPI1SMNx000000D8...ESPISMNx000000D8**  
**(FCH::ITF::ESPI::ESPI\_LOWSECURITY\_CONTROL\_REG\_RESERVED3)**

Read-write. Reset: 0000\_0000h.

\_link1\_aliasSMN; ESPI1SMNx000000D8; ESPI1SMN=02DCA000h\_link0\_aliasSMN; ESPISMNx000000D8; ESPISMN=02DC5000h\_link1\_aliasHOSTLEGACY; ESPI1x000000D8; ESPI1=FEC30000h\_link0\_aliasHOSTLEGACY; ESPIx000000D8; ESPI=FEC20000h

Bits	Description
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31:0	ESPI_LOWSECURITY_CONTROL_REG_RESERVED3. Read-write. Reset: 0000_0000h.
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**ESPI1SMNx000000DC...ESPISMNx000000DC**  
**(FCH::ITF::ESPI::ESPI\_LOWSECURITY\_CONTROL\_REG\_RESERVED4)**

Read-write. Reset: 0000\_0000h.

\_link1\_aliasSMN; ESPI1SMNx000000DC; ESPI1SMN=02DCA000h\_link0\_aliasSMN; ESPISMNx000000DC; ESPISMN=02DC5000h\_link1\_aliasHOSTLEGACY; ESPI1x000000DC; ESPI1=FEC30000h\_link0\_aliasHOSTLEGACY; ESPIx000000DC; ESPI=FEC20000h

Bits	Description
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31:0	ESPI_LOWSECURITY_CONTROL_REG_RESERVED4. Read-write. Reset: 0000_0000h.
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**ESPI1SMNx000000E0...ESPISMNx000000E0**  
**(FCH::ITF::ESPI::ESPI\_LOWSECURITY\_CONTROL\_REG\_RESERVED5)**

Read-write. Reset: 0000\_0000h.

\_link1\_aliasSMN; ESPI1SMNx000000E0; ESPI1SMN=02DCA000h\_link0\_aliasSMN; ESPISMNx000000E0; ESPISMN=02DC5000h\_link1\_aliasHOSTLEGACY; ESPI1x000000E0; ESPI1=FEC30000h\_link0\_aliasHOSTLEGACY; ESPIx000000E0; ESPI=FEC20000h

Bits	Description
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31:0	ESPI_LOWSECURITY_CONTROL_REG_RESERVED5. Read-write. Reset: 0000_0000h.
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**ESPI1SMNx000000E4...ESPISMNx000000E4**  
**(FCH::ITF::ESPI::ESPI\_LOWSECURITY\_CONTROL\_REG\_RESERVED6)**

Read-write. Reset: 0000\_0000h.

\_link1\_aliasSMN; ESPI1SMNx000000E4; ESPI1SMN=02DCA000h\_link0\_aliasSMN; ESPISMNx000000E4; ESPISMN=02DC5000h\_link1\_aliasHOSTLEGACY; ESPI1x000000E4; ESPI1=FEC30000h\_link0\_aliasHOSTLEGACY; ESPIx000000E4; ESPI=FEC20000h

Bits	Description
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31:0	ESPI_LOWSECURITY_CONTROL_REG_RESERVED6. Read-write. Reset: 0000_0000h.
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**ESPI1SMNx000000E8...ESPISMNx000000E8**  
**(FCH::ITF::ESPI::ESPI\_LOWSECURITY\_CONTROL\_REG\_RESERVED7)**

Read-write. Reset: 0000\_0000h.

\_link1\_aliasSMN; ESPI1SMNx000000E8; ESPI1SMN=02DCA000h\_link0\_aliasSMN; ESPISMNx000000E8; ESPISMN=02DC5000h\_link1\_aliasHOSTLEGACY; ESPI1x000000E8; ESPI1=FEC30000h\_link0\_aliasHOSTLEGACY; ESPIx000000E8; ESPI=FEC20000h

Bits	Description
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31:0	ESPI_LOWSECURITY_CONTROL_REG_RESERVED7. Read-write. Reset: 0000_0000h.
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**ESPI1SMNx000000EC...ESPISMNx000000EC**  
**(FCH::ITF::ESPI::ESPI\_LOWSECURITY\_CONTROL\_REG\_RESERVED8)**

Read-write. Reset: 0000\_0000h.

\_link1\_aliasSMN; ESPI1SMNx000000EC; ESPI1SMN=02DCA000h\_link0\_aliasSMN; ESPISMNx000000EC; ESPISMN=02DC5000h\_link1\_aliasHOSTLEGACY; ESPI1x000000EC; ESPI1=FEC30000h\_link0\_aliasHOSTLEGACY; ESPIx000000EC; ESPI=FEC20000h

Bits	Description
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31:0	ESPI_LOWSECURITY_CONTROL_REG_RESERVED8. Read-write. Reset: 0000_0000h.
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**ESPI1SMNx000000F0...ESPISMNx000000F0**  
**(FCH::ITF::ESPI::ESPI\_LOWSECURITY\_CONTROL\_REG\_RESERVED9)**

Read-write. Reset: 0000\_0000h.

\_link1\_aliasSMN; ESPI1SMNx000000F0; ESPI1SMN=02DCA000h\_link0\_aliasSMN; ESPISMNx000000F0; ESPISMN=02DC5000h\_link1\_aliasHOSTLEGACY; ESPI1x000000F0; ESPI1=FEC30000h\_link0\_aliasHOSTLEGACY; ESPIx000000F0; ESPI=FEC20000h

Bits	Description
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31:0	ESPI_LOWSECURITY_CONTROL_REG_RESERVED9. Read-write. Reset: 0000_0000h.
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**ESPI1SMNx000000F4...ESPISMNx000000F4**  
**(FCH::ITF::ESPI::ESPI\_LOWSECURITY\_CONTROL\_REG\_RESERVED10)**

Read-write. Reset: 0000\_0000h.

\_link1\_aliasSMN; ESPI1SMNx000000F4; ESPI1SMN=02DCA000h\_link0\_aliasSMN; ESPISMNx000000F4; ESPISMN=02DC5000h\_link1\_aliasHOSTLEGACY; ESPI1x000000F4; ESPI1=FEC30000h\_link0\_aliasHOSTLEGACY; ESPIx000000F4; ESPI=FEC20000h

Bits	Description
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31:0	ESPI_LOWSECURITY_CONTROL_REG_RESERVED10. Read-write. Reset: 0000_0000h.
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**ESPI1SMNx000000F8...ESPISMNx000000F8**  
**(FCH::ITF::ESPI::ESPI\_LOWSECURITY\_CONTROL\_REG\_RESERVED11)**

Read-write. Reset: 0000\_0000h.

\_link1\_aliasSMN; ESPI1SMNx000000F8; ESPI1SMN=02DCA000h\_link0\_aliasSMN; ESPISMNx000000F8; ESPISMN=02DC5000h\_link1\_aliasHOSTLEGACY; ESPI1x000000F8; ESPI1=FEC30000h\_link0\_aliasHOSTLEGACY; ESPIx000000F8; ESPI=FEC20000h

Bits	Description
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31:0	ESPI_LOWSECURITY_CONTROL_REG_RESERVED11. Read-write. Reset: 0000_0000h.
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### ESPI1SMNx000000FC...ESPISMNx000000FC (FCH::ITF::ESPI::ESPI\_LOWSECURITY\_CONTROL\_REG\_RESERVED12)

Read-write. Reset: 0000\_0000h.

\_link1\_aliasSMN; ESPI1SMNx000000FC; ESPI1SMN=02DCA000h

\_link0\_aliasSMN; ESPI1SMNx000000FC; ESPI1SMN=02DC5000h

\_link1\_aliasHOSTLEGACY; ESPI1x000000FC; ESPI1=FEC30000h

\_link0\_aliasHOSTLEGACY; ESPIx000000FC; ESPI=FEC20000h

Bits	Description
31:0	ESPI_LOWSECURITY_CONTROL_REG_RESERVED12. Read-write. Reset: 0000_0000h.

## 11.3.9 MISC Registers

### 11.3.9.1 Miscellaneous (MISC) Registers



**MISCx00000000 (FCH::MISC::GPPCLKCNTROL)**

Read-write. Reset: 0000\_CFFh.

\_aliasHOSTLEGACY; MISCx00000000; MISC=FED8\_0E00h

Bits	Description
31:12	Reserved.
11:10	<b>gpp_clk15_clock_request_mapping.</b> Read-write. Reset: 3h. <b>Description:</b> GPP15 PCIE clock pins (GPP_CLK15P/GPP_CLK15N) output control by CLKREQ15# (or CLKREQ1G#) pin GPP_CLK15P/GPP_CLK15N pins can be controlled (turn OFF, ON, CLKREQ15# controlled) by the following options. GPP15_CLKREQ_Mapping: 00 Off 01 CLKREQ15# 10 Off, reserved 11 On (default)
9:8	<b>gpp_clk13_clock_request_mapping.</b> Read-write. Reset: 3h. <b>Description:</b> GPP13 PCIE clock pins (GPP_CLK13P/GPP_CLK13N) output control by CLKREQ13# pin GPP_CLK13P/GPP_CLK13N pins can be controlled (turn OFF, ON, CLKREQ13# controlled) by the following options. GPP13_CLKREQ_Mapping: 00 Off 01 CLKREQ13# 10 Off, reserved 11 On (default) Note: MISCx00000004[24] is an override bit which is XOR with GPP13_CLKREQ_Mapping.
7:6	<b>gpp_clk12_clock_request_mapping.</b> Read-write. Reset: 3h. <b>Description:</b> GPP12 PCIE clock pins (GPP_CLK12P/GPP_CLK12N) output control by CLKREQ12# pin GPP_CLK12P/GPP_CLK12N pins can be controlled (turn OFF, ON, CLKREQ12# controlled) by the following options. GPP12_CLKREQ_Mapping: 00 Off 01 CLKREQ12# 10 Off, reserved 11 On (default) Note: MISCx00000004[12] is an override bit which is XOR with GPP12_CLKREQ_Mapping.
5:4	<b>gpp_clk14_clock_request_mapping.</b> Read-write. Reset: 3h. <b>Description:</b> GPP14 PCIE clock pins (GPP_CLK14P/GPP_CLK14N) output control by CLKREQ14# pin GPP_CLK14P/GPP_CLK14N pins can be controlled (turn OFF, ON, CLKREQ14# controlled) by the following options. GPP14_CLKREQ_Mapping: 00 Off 01 CLKREQ14# 10 Off, reserved 11 On (default) Note: MISCx00000004[29] is an override bit which is XOR with GPP14_CLKREQ_Mapping.
3:2	<b>gpp_clk11_clock_request_mapping.</b> Read-write. Reset: 3h.

	<p><b>Description:</b> GPP11 PCIE clock pins (GPP_CLK11P/GPP_CLK11N) output control by CLKREQ11# pin. GPP_CLK11P/GPP_CLK11N pins can be controlled (turn OFF, ON, CLKREQ11# controlled) by the following options.</p> <p>GPP11_CLKREQ_Mapping:</p> <p>00 Off</p> <p>01 CLKREQ11#</p> <p>10 Off, reserved</p> <p>11 On (default)</p> <p>Note: MISCx00000004[9] is an override bit which is XOR with GPP11_CLKREQ_Mapping.</p>
1:0	<p><b>gpp_clk10_clock_request_mapping.</b> Read-write. Reset: 3h.</p> <p><b>Description:</b> GPP10 PCIE clock pins (GPP_CLK10P/GPP_CLK10N) output control by CLKREQ10# pin. Socket0 GPP10 is default output 100MHz (CG1PLL 100MHz) for Socket1 CG1PLL as refclk thru Socket1 GPP10 input.</p> <p>Socket1 GPP10 is default with input mode.</p> <p>If the platform is one socket only, then socket0 GPP10 can be controlled (turn OFF, ON, CLKREQ10# controlled) by the following options.</p> <p>GPP10_CLKREQ_Mapping:</p> <p>00 Off</p> <p>01 CLKREQ10#</p> <p>10 Off, reserved</p> <p>11 On (default)</p> <p>Note: MISCx00000004[11] is an override bit which is XOR with GPP10_CLKREQ_Mapping.</p>

#### MISCx00000004 (FCH::MISC::CLKOUTPUTCNTRL)

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISCx00000004; MISC=FED8\_0E00h

Bits	Description
31:0	Reserved.

**MISCx00000008 (FCH::MISC::CGPLLCONFIG1)**

Read-write. Reset: 6000\_0000h.

\_aliasHOSTLEGACY; MISCx00000008; MISC=FED8\_0E00h

Bits	Description
31	<b>xtal_refclk2x_clkenb.</b> Read-write. Reset: 0. <b>Description:</b> REFCLK2X clock enable/disable 0: Turn on 1: Turn off
30	<b>xtal_clkgen_s5_clken.</b> Read-write. Reset: 1. <b>Description:</b> CLKGEN_S5 RefClk Enable/disable 0: Turn off 1: Turn on
29	<b>xtal_clkgen_s0_clken.</b> Read-write. Reset: 1. <b>Description:</b> CLKGEN_S0 RefClk Enable/disable 0: Turn off 1: Turn on
28:9	Reserved.
8	<b>cg1_refdivsrc_override.</b> Read-write. Reset: 0. <b>Description:</b> CG1PLL Refclk Source Select Override This bit is used to override CG1PLL refclk source select. By default, Master_die CG1PLL refclk source is from CG_XTAL 48MHz and Slave_die is 100MHz from external clock chip For Master_die: 0: CG1PLL refclk source is from CG_XTAL 48MHz 1: CG1PLL refclk source is 100MHz from external clock chip For Slave_die: 0: CG1PLL refclk source is 100MHz from external clock chip 1: CG1PLL refclk source is from CG_XTAL 48MHz Note: Need to apply a reset after set this bit
7:5	Reserved.
4	<b>refclk_source_switch_mode.</b> Read-write. Reset: 0. <b>Description:</b> Refclk Source Switch Mode For CGPLL refclk source, it can be from either CG_XTAL or external reference source. 0: Switch refclk source on-the-fly 1: Need to apply a Cold Reset for switching different refclk source
3:1	Reserved.
0	<b>cg1_spread_spectrum_enable.</b> Read-write. Reset: 0. <b>Description:</b> CG1_PLL Spread Spectrum Enable 0: Disable Spread Spectrum (default) 1: Enable Spread Spectrum

**MISCx0000000C (FCH::MISC::CGPLLCONFIG2)**

Read-write. Reset: 0001\_0000h.

\_aliasHOSTLEGACY; MISCx0000000C; MISC=FED8\_0E00h

Bits	Description
31:0	Reserved.

**MISCx00000010 (FCH::MISC::CGPLLCONFIG3)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISCx00000010; MISC=FED8\_0E00h

Bits	Description
31:30	Reserved.
29	<b>cg1pll_fracn_en_override</b> . Read-write. Reset: 0. Used with CG1PLL frac-N and <a href="#">SSC</a> clocking only.
28:13	Reserved.
12:4	<b>cg1pll_fcw0_int_override</b> . Read-write. Reset: 000h. CG1PLL Override: Integer portion of Frequency Control Word0 (a.k.a. feedback divisor0).
3:2	Reserved.
1:0	<b>cg1pll_refclk_div_override</b> . Read-write. Reset: 0h. <b>Description:</b> CG1PLL Override: Reference clock divisor. Settings: 2'b00=1 2'b01=2 2'b1x=4

**MISCx00000014 (FCH::MISC::CGPLLCONFIG4)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISCx00000014; MISC=FED8\_0E00h

Bits	Description
31:24	Reserved.
23:8	<b>cg1pll_fcw1_frac_override</b> . Read-write. Reset: 0000h. CG1PLL Override: Fractional portion of Frequency Control Word1 (a.k.a. feedback divisor1). Intended to be used with frequency ramping. Also used to step PLL frequency and phase for DFT.
7:0	Reserved.

**MISCx00000018 (FCH::MISC::CGPLLCONFIG5)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISCx00000018; MISC=FED8\_0E00h

Bits	Description
31:16	<b>cg1pll_fcw_slew_frac_override</b> . Read-write. Reset: 0000h. <b>Description:</b> CG1PLL Override: Sets <a href="#">SSC</a> freq ramp rate. Set fractional change in programmed frequency per refclk cycle. e.g. 0.5% downspread SSC at 33.3kHz and fbdiv=80. FCW_slewrte_frac = $216 * 0.00485 * 80 / (15\mu s / 10ns) = 17$ Need 31.5kHz and -0.375%
15:0	Reserved.

**MISCx0000001C (FCH::MISC::CGPLLCONFIG6)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISCx0000001C; MISC=FED8\_0E00h

Bits	Description
31:28	Reserved.
27:26	<b>cgpll_gi_coarse_mant_override</b> . Read-write. Reset: 0h. CG1PLL Coarse integral path fp mult mantissa
25:21	Reserved.
20:17	<b>cg1pll_gp_coarse_exp_override</b> . Read-write. Reset: 0h. CG1PLL Override: Coarse proportional path fp mult exponent
16:13	<b>cg1pll_gp_coarse_mant_override</b> . Read-write. Reset: 0h. CG1PLL Override: Coarse proportional path fp mult mantissa
12:9	<b>cg1pll_gi_coarse_exp_override</b> . Read-write. Reset: 0h. CG1PLL Override: Coarse integral path fp mult exponent
8:0	Reserved.

**MISCx00000020 (FCH::MISC::IMPCALIBRATION)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISCx00000020; MISC=FED8\_0E00h

Bits	Description
31:0	Reserved.

**MISCx00000024 (FCH::MISC::CLKDRVSTH1)**

Read-write. Reset: 0024\_0249h.

\_aliasHOSTLEGACY; MISCx000000024; MISC=FED8\_0E00h

Bits	Description
31:24	Reserved.
23:21	<b>gpp5_clock_buffer_driving_strength_control.</b> Read-write. Reset: 1h. <b>Description:</b> Drive Strength control for GPP5 differential Clock Buffers Drive strength addition/subtraction relative to IMP_CTRL[4:0]. 3'bx00 : ~ -10% 3'bx01 : no change from IMP_CTRL 3'bx10 : ~ +10% 3'bx11 : ~ + 20% Default: 3'b001
20:18	<b>gpp4_clock_buffer_driving_strength_control.</b> Read-write. Reset: 1h. <b>Description:</b> Drive Strength control for GPP4 differential Clock Buffers Drive strength addition/subtraction relative to IMP_CTRL[4:0]. 3'bx00 : ~ -10% 3'bx01 : no change from IMP_CTRL 3'bx10 : ~ +10% 3'bx11 : ~ + 20% Default: 3'b001
17:12	Reserved.
11:9	<b>gpp_clk13_clock_buffer_driving_strength_control.</b> Read-write. Reset: 1h. <b>Description:</b> Drive Strength control for GPP_CLK13 differential Clock Buffers Drive strength addition/subtraction relative to IMP_CTRL[4:0]. 3'bx00 : ~ -10% 3'bx01 : no change from IMP_CTRL 3'bx10 : ~ +10% 3'bx11 : ~ + 20% Default: 3'b001
8:6	<b>gpp_clk12_clock_buffer_driving_strength_control.</b> Read-write. Reset: 1h. <b>Description:</b> Drive Strength control for GPP_CLK12 differential Clock Buffers Drive strength addition/subtraction relative to IMP_CTRL[4:0]. 3'bx00 : ~ -10% 3'bx01 : no change from IMP_CTRL 3'bx10 : ~ +10% 3'bx11 : ~ + 20% Default: 3'b001
5:3	<b>gpp_clk11_clock_buffer_driving_strength_control.</b> Read-write. Reset: 1h. <b>Description:</b> Drive Strength control for GPP_CLK11 differential Clock Buffers Drive strength addition/subtraction relative to IMP_CTRL[4:0]. 3'bx00 : ~ -10% 3'bx01 : no change from IMP_CTRL 3'bx10 : ~ +10% 3'bx11 : ~ + 20% Default: 3'b001
2:0	<b>gpp_clk10_clock_buffer_driving_strength_control.</b> Read-write. Reset: 1h.

	<b>Description:</b> Drive Strength control for GPP_CLK10 differential Clock Buffers Drive strength addition/subtraction relative to IMP_CTRL[4:0]. 3'bx00 : ~ -10% 3'bx01 : no change from IMP_CTRL 3'bx10 : ~ +10% 3'bx11 : ~ + 20% Default: 3'b001
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#### MISCx00000028 (FCH::MISC::CLKDRVSTH2)

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISCx00000028; MISC=FED8\_0E00h

Bits	Description
31:22	Reserved.
21	<b>bp_x48m_output_override.</b> Read-write. Reset: 0. <b>Description:</b> BP_X48M clock output override, set this to "1" will override the default enable/disable of BP_X48M_1 clock output. For BP_X48M output clocks, default enabled, this bit is to override default value.
20	Reserved.
19:12	<b>debug_sig_sel_0.</b> Read-write. Reset: 00h. <b>Description:</b> Debug Signal Selection 0 These bits are used to select internal signal for debug observation thru uPAD_S5_X48MO pin with MISCx00000028[27]=1 Bit19 is used to select debug signal either from S0 or S5. 0: Select S5 Debug Signal Group0 1: Select S0 Debug Signal Group0
11:0	Reserved.

#### MISCx0000002C (FCH::MISC::CLKGATEDCNTL)

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISCx0000002C; MISC=FED8\_0E00h

Bits	Description
31:18	Reserved.
17	<b>blinkclk_gateoffen.</b> Read-write. Reset: 0. Check: 1. <b>Description:</b> B-Link Clock Gate-Off Enable Internal B-Link clock has two clock trees: one is a free running clock and the other is a gated clock. When all controllers agree to stop the gated B-Link clock and this bit got set, clkgating logic will gate off the clock tree from clock root. Note: Need to enable with PM04[16]=1(non-sticky) and rsmu_local_reg_1C[31]=1(non-sticky). 0: Disable B-Link Clock Gate-Off function. Default 1: Enable B-Link Clock Gate-Off function
16	<b>alinkclk_gateoffen.</b> Read-write. Reset: 0. Check: 1. <b>Description:</b> A-Link Clock Gate-Off Enable Internal A-Link clock has two clock trees: one is a free-running clock and the other is a gated clock. When all controllers agree to stop the gated A-Link clock and this bit got set, clkgating logic will gate off the clock tree from clock root. Note: Need to enable with PM04[16]=1(non-sticky). 0: Disable A-Link Clock Gate-Off function. Default 1: Enable A-Link Clock Gate-Off function
15:0	Reserved.

**MISCx00000030 (FCH::MISC::CGPLL\_CONFIGURATION0)**

Read-write.

\_aliasHOSTLEGACY; MISCx00000030; MISC=FED8\_0E00h

Bits	Description
31:17	Reserved.
16	<b>uart3_14_77mhz_sclk_enable.</b> Read-write. Reset: 0. <b>Description:</b> UART3 14.77MHz SCLK Enable 0: Turn off UART0 14.77MHz SCLK 1: Turn on UART0 14.77MHz SCLK
15	<b>uart2_14_77mhz_sclk_enable.</b> Read-write. Reset: 0. <b>Description:</b> UART2 14.77MHz SCLK Enable 0: Turn off UART0 14.77MHz SCLK 1: Turn on UART0 14.77MHz SCLK
14	<b>uart1_14_77mhz_sclk_enable.</b> Read-write. Reset: 0. <b>Description:</b> UART1 14.77MHz SCLK Enable 0: Turn off UART0 14.77MHz SCLK 1: Turn on UART0 14.77MHz SCLK
13	<b>uart0_14_77mhz_sclk_enable.</b> Read-write. Reset: 0. <b>Description:</b> UART0 14.77MHz SCLK Enable 0: Turn off UART0 14.77MHz SCLK 1: Turn on UART0 14.77MHz SCLK
12:4	Reserved.
3	<b>usb0_rtcclk_enb.</b> Read-write. Reset: 0. <b>Description:</b> USB0 RTCCLK (root_RTC_CLK_0) Enable/Disable Note: USB0 RTCCLK clock root is in remote <a href="#">FCH</a> . This bit is from remote FCH Misc register. 0: Turn on 1: Turn off
2	<b>usb1_rtcclk_enb.</b> Read-write. Reset: 0. <b>Description:</b> USB1 RTCCLK (root_RTC_CLK_1) Enable/Disable Note: USB1 RTCCLK clock root is in local <a href="#">FCH</a> . This bit is from local FCH Misc register. 0: Turn on 1: Turn off
1:0	<b>pcie_phy_refclk_selection_override.</b> Read-write. Reset: XXb. <b>Description:</b> PCIE PHY Refclk Selection Override (P-PHY) CLKB_PCIE_PHY_P/N (fch_tile/CLKGEN) 00 = 100MHz CG1_PLL generated (default) 01 = 100MHz CG2_PLL generated 10 = EXT_GPP0_SRC 11 = EXT_GPP2_RX Note: MISCx000000BC[12] to select EXT_GPP0_SRC either is from GPP0 external input or GPP0 external input with divided-by-2 or divided-by-4

**MISCx00000034 (FCH::MISC::CGPLL\_CONFIGURATION1)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISCx00000034; MISC=FED8\_0E00h

Bits	Description
31:23	<b>cg1pll_fcw1_int_override.</b> Read-write. Reset: 000h. CG1PLL Override: Integer portion of Frequency Control Word0 (a.k.a. feedback divisor1). Intended to be used with frequency ramping. Also used to step PLL frequency and phase for DFT.
22:0	Reserved.



**MISCx00000038 (FCH::MISC::CGPLL\_CONFIGURATION2)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISCx00000038; MISC=FED8\_0E00h

Bits	Description
31:23	Reserved.
22:21	<b>cg1pll_external_refclk_sel_override.</b> Read-write. Reset: 0h. <b>Description:</b> CG1PLL External Refclk Selection Override (local <a href="#">FCH</a> ) This is the refclk mux source inside CLKGEN_S0. 00 = local GPP0_RX (external 100M) 01 = GPP2_RX 10 = CG1_100M 11 = remote GPP0_RX The MISCx00000038[22:21] are override bits to this mux inside CLKGEN_S0. The local CLKGEN_S0 default is "00" in iCLK mode and "01" in eCLK mode. The remote CLKGEN_S0 default is "10" in iCLK mode and "01" in eCLK mode. For example: If we want to use external 100MHz as CG1PLL refclk source thru local GPP0_RX in eCLK mode, then program MISCx00000038[22:21]="01". (default "01" XOR program MISCx00000038[22:21]="01" = "00") If we want to use external 100MHz as CG2PLL refclk source thru remote GPP2_RX in iCLK mode, then program MISCx00000038[22:21]="11". (default "10" XOR program MISCx00000038[22:21]="11" = "01")
20	<b>usb1_phy_cmlclk_static_off.</b> Read-write. Reset: 0. <b>Description:</b> USB1 PHY CML Clock Static Turn Off 0: USB1 PHY CML Clock will not be static turn off 1: USB1 PHY CML Clock will be static turn off
19	<b>usb0_phy_cmlclk_static_off.</b> Read-write. Reset: 0. <b>Description:</b> USB0 PHY CML Clock Static Turn Off 0: USB0 PHY CML Clock will not be static turn off 1: USB0 PHY CML Clock will be static turn off
18	<b>usb1_dbgclk_enb.</b> Read-write. Reset: 0. <b>Description:</b> USB1 DBGCLK Enable/Disable 0: Enable 1: Disable
17	<b>usb0_dbgclk_enb.</b> Read-write. Reset: 0. <b>Description:</b> USB0 DBGCLK Enable/Disable 0: Enable 1: Disable
16	<b>usb1_host_clk_selection_fw.</b> Read-write. Reset: 0. <b>Description:</b> USB1 Host Clock Selection_FW USB1 Host Clock can be either 300M generated from CGPLL or 48M generated from XTAL_PAD when CGPLL 300M generated clock is not available. MISCx00000038[15] is used to select the switching mechanism. For MISCx00000038[16]: 1: 300MHz generated by CGPLL 0: 48MHz generated from XTAL_PAD
15	<b>usb1_host_clk_switch_mechanism.</b> Read-write. Reset: 0.

	<b>Description:</b> USB1 Host Clock Switch_ Mechanism USB1 Host Clock can be either 300M generated from CGPLL or 48M generated from XTAL_PAD, default is 300M. Please refer USB's requirement. (pair-up with USB's sequence) USB1 Host Clock can be either 300M generated from CGPLL or 48M generated from XTAL_PAD when CGPLL 300M generated clock is not available. MISCx00000038[15] is used to select the switching mechanism. MISCx00000038[15] =0, HW dynamic switching between 300M and 48M according whether CGPLL is available or not. MISCx00000038[15]=1, FW switch thru MISCx00000038[16]
14	<b>usb1_host_clk_staticoff.</b> Read-write. Reset: 0. <b>Description:</b> USB1 Host Clock Static Off If USB1 is not used in a given platform, USB1_Host_Clk can be turn off by set this bit to "1". 0: Static Off function is not enabled 1: Static Off function is enabled
13	<b>usb0_host_clk_selection_fw.</b> Read-write. Reset: 0. <b>Description:</b> USB0 Host Clock Selection_FW USB0 Host Clock can be either 300M generated from CGPLL or 48M generated from XTAL_PAD when CGPLL 300M generated clock is not available. MISCx00000038[12] is used to select the switching mechanism. For MISCx00000038[13]: 1: 300MHz generated by CGPLL 0: 48MHz generated from XTAL_PAD
12	<b>usb0_host_clk_switch_mechanism.</b> Read-write. Reset: 0. <b>Description:</b> USB0 Host Clock Switch_ Mechanism USB0 Host Clock can be either 300M generated from CGPLL or 48M generated from XTAL_PAD, default is 300M. Please refer USB's requirement. (pair-up with USB's sequence) USB0 Host Clock can be either 300M generated from CGPLL or 48M generated from XTAL_PAD when CGPLL 300M generated clock is not available. MISCx00000038[12] is used to select the switching mechanism. MISCx00000038[12] =0, HW dynamic switching between 300M and 48M according whether CGPLL is available or not. MISCx00000038[12]=1, FW switch thru MISCx00000038[13]
11	<b>usb0_host_clk_staticoff.</b> Read-write. Reset: 0. <b>Description:</b> USB0 Host Clock Static Off If USB0 is not used in a given platform, USB0_Host_Clk can be turn off by set this bit to "1". 0: Static Off function is not enabled 1: Static Off function is enabled
10:0	Reserved.

#### MISCx0000003C (FCH::MISC::CGPLL\_CONFIGURATION3)

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISCx0000003C; MISC=FED8\_0E00h

Bits	Description
31:0	Reserved.

**MISCx00000040 (FCH::MISC::MISCCLKCNTRL0)**

Read-write. Reset: 0000\_4040h.

\_aliasHOSTLEGACY; MISCx00000040; MISC=FED8\_0E00h

Bits	Description
31	Reserved.
30	<b>cg1_cfg_update_req.</b> Read-write. Reset: 0. <b>Description:</b> Set this bit will request CG1_PLL to load spread related value into CG1_PLL. The bit will be clear "0" by hardware after request send to CG1_PLL.
29:28	Reserved.
27	<b>blink266m_gate_enb.</b> Read-write. Reset: 0. <b>Description:</b> Blink 288MHz Clock Gate_EnB Program "0" to gated off this clock from free running
26	Reserved.
25	<b>cg1_fbdiv_loaden.</b> Read-write. Reset: 0. Set "1" to enable loading CG1_PLL FB_DIV value form register
24:18	Reserved.
17	<b>usb0_refclk_drvier_pwdn_s5.</b> Read-write. Reset: 0. <b>Description:</b> USB0 (USB controller 0) Refclk Driver (differential) Power-Down in S5 When set this bit to "1", USB0 Refclk Driver will be turn off in S5 state.
16:15	Reserved.
14	<b>osclkswitchen.</b> Read-write. Reset: 1. <b>Description:</b> When this bit is set, the <a href="#">FCH</a> will use CG_XTAL 48M to generate the average 14MHz clock as OSC. 0: OSC is 12MHz (CG_XTAL 48M divided by 4) 1: OSC is average 14.318MHz.
13:12	Reserved.
11	<b>az_48mclk_pwdn.</b> Read-write. Reset: 0. <b>Description:</b> AZ 48MHz Clock Output Driver PWDN <a href="#">FCH</a> provided 48MHz clock for AZ. 0: AZ 48MHz Clock Output Driver is enable 1: AZ 48MHz Clock Output Driver is disable
10	Reserved.
9	<b>xtal48m_s5_pwdn_en.</b> Read-write. Reset: 0. <b>Description:</b> CG 48MHz XTAL Pad Power Down Enable when in S5 state Set this bit allow to power down CG XTAL pad in S5 state.
8:7	Reserved.
6	<b>usb0_refclk_drvier_en_s3.</b> Read-write. Reset: 1. <b>Description:</b> USB0 (USB controller 0) Refclk Driver (differential) Enable in S3 When set this bit to "0", USB0 Refclk Driver will be turn off in S3 state.
5	<b>usb1_refclk_drvier_pwdn_s3.</b> Read-write. Reset: 0. <b>Description:</b> USB1 (USB controller 1) Refclk Driver (differential) Power-Down in S3 When set this bit to "1", USB1 Refclk Driver will be turn off in S3 state.
4	Reserved.
3	<b>usb1_refclk_drvier_pwdn_s5.</b> Read-write. Reset: 0. <b>Description:</b> USB1 (USB controller 1) Refclk Driver (differential) Power-Down in S5 When set this bit to "1", USB1 Refclk Driver will be turn off in S5 state.
2	Reserved.
1	<b>corespeedmode.</b> Read-write. Reset: 0. <b>Description:</b> Slow down Internal Core Clock (B-Link clock) for power saving. 0: Full speed B-Link clock 1: Slow speed B-Link clock

0	Reserved.
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**MISCx00000044 (FCH::MISC::MISCCLKCNTL1)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISCx00000044; MISC=FED8\_0E00h

Bits	Description
31:0	Reserved.

**MISCx00000048 (FCH::MISC::MISCCLKCNTL2)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISCx00000048; MISC=FED8\_0E00h

Bits	Description
31:12	Reserved.
11	<b>fch_core_400m_switch_maskoff.</b> Read-write. Reset: 0. <b>Description:</b> <a href="#">FCH</a> core clock mux provides the capability to switch between 400MHz and 48MHz clock sources. Setting fch_core_400m_switch_maskoff to "1" will prevent switching of the FCH core clock source during CGPLL update requests triggered when FCH::MISC::MISCCLKCNTRL0[cg1_cfg_update_req] is set to "1" (atomic updates, like <a href="#">SSC</a> profile and SSC enable). 0: Allow FCH core clock switching from 400MHz to 48MHz during CGPLL update request. 1: Mask off FCH core clock switching during CGPLL update request.
10:0	Reserved.

**MISCx0000004C (FCH::MISC::MISCCLKCNTL3)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISCx0000004C; MISC=FED8\_0E00h

Bits	Description
31	<b>low_power_display_400mclk_enb.</b> Read-write. Reset: 0. <b>Description:</b> Low Power Display 400MHz Clock Output Enable/Disable Non Sticky bit. 0: Enable 1: Disable
30	<b>low_power_display_300mclk_enb.</b> Read-write. Reset: 0. <b>Description:</b> Low Power Display 300MHz Clock Output Enable/Disable Non Sticky bit. 0: Enable 1: Disable
29	<b>low_power_display_600mclk_enb.</b> Read-write. Reset: 0. <b>Description:</b> Low Power Display 600MHz Clock Output Enable/Disable Non Sticky bit. 0: Enable 1: Disable
28:12	Reserved.
11	<b>usb1_host_clk_enb.</b> Read-write. Reset: 0. <b>Description:</b> USB1 Host Clock EnableB/Disable Non Sticky bit. When resume, it will be enable (default setting "0") regardless what has been programmed and BIOS needs to program it again if this bit has been programmed to "1". 0: Enable 1: Disable
10	<b>usb0_host_clk_enb.</b> Read-write. Reset: 0. <b>Description:</b> USB0 Host Clock EnableB/Disable Non Sticky bit. When resume, it will be enable (default setting "0") regardless what has been programmed and BIOS needs to program it again if this bit has been programmed to "1". 0: Enable 1: Disable
9	<b>sata_sgpio_2_3_clk_enb.</b> Read-write. Reset: 0. <b>Description:</b> SATA SGPIO Clock Enable/Disable (for host controller 2 & 3) Non Sticky bit. 0: Turn on (Enable) 1: Turn off (Disable)
8	<b>sata_sgpio_0_1_clk_enb.</b> Read-write. Reset: 0. <b>Description:</b> SATA SGPIO Clock Enable/Disable (for host controller 1 & 2) Non Sticky bit. 0: Turn on (Enable) 1: Turn off (Disable)
7	<b>sata_100m_core_3_clk_enb.</b> Read-write. Reset: 0. <b>Description:</b> SATA 100M Core Clock Enable/Disable (for host controller 3) Non Sticky bit. 0: Turn on (Enable) 1: Turn off (Disable)
6	<b>sata_100m_core_2_clk_enb.</b> Read-write. Reset: 0.

	<b>Description:</b> SATA 100M Core Clock Enable/Disable (for host controller 2) Non Sticky bit. 0: Turn on (Enable) 1: Turn off (Disable)
5	<b>sata_100m_core_1_clk_enb.</b> Read-write. Reset: 0. <b>Description:</b> SATA 100M Core Clock Enable/Disable (for host controller 1) Non Sticky bit. 0: Turn on (Enable) 1: Turn off (Disable)
4	<b>sata_100m_core_0_clk_enb.</b> Read-write. Reset: 0. <b>Description:</b> SATA 100M Core Clock Enable/Disable (for host controller 0) Non Sticky bit. 0: Turn on (Enable) 1: Turn off (Disable)
3:2	Reserved.
1	<b>pcie_phy_p_refclk_static_pwdn_cntl.</b> Read-write. Reset: 0. <b>Description:</b> PCIE_P_Set_PHY Refclk Driver Static PWDN Control 0: Enable on-chip driver (default) 1: Disable on-chip driver (if it is unused) When resume, it will be static shut-down with on-chip driver enable (default setting) regardless what has been programmed and BIOS needs to program it again.
0	Reserved.

**MISCx00000054 (FCH::MISC::BOOT\_PARTITION)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISCx00000054; MISC=FED8\_0E00h

Bits	Description
31:6	Reserved.
5	<b>unbootable_slot_d_mask.</b> Read-write. Reset: 0. <b>Description:</b> Unbootable Mask bit for primary partition in A/B recovery scheme Bit[5] = 0 Partition (Slot) D is bootable Bit[5] = 1 Partition (Slot) D is not bootable
4	<b>unbootable_slot_c_mask.</b> Read-write. Reset: 0. <b>Description:</b> Unbootable Mask bit for primary partition in A/B recovery scheme Bit[4] = 0 Partition (Slot) C is bootable Bit[4] = 1 Partition (Slot) C is not bootable
3	<b>unbootable_slot_b_mask.</b> Read-write. Reset: 0. <b>Description:</b> Unbootable Mask bit for primary partition in A/B recovery scheme Bit[3] = 0 Partition (Slot) B is bootable Bit[3] = 1 Partition (Slot) B is not bootable
2	<b>unbootable_slot_a_mask.</b> Read-write. Reset: 0. <b>Description:</b> Unbootable Mask bit for primary partition in A/B recovery scheme Bit[2] = 0 Partition (Slot) A is bootable Bit[2] = 1 Partition (Slot) A is not bootable
1	<b>vddcr_baco_persist_spare.</b> Read-write. Reset: 0. <b>Description:</b> Bit[1] = 0 Boot when BACO domain starts from reset Bit[1] = 1 Boot when BACO domain persists
0	<b>vddcr_s5_persist.</b> Read-write. Reset: 0. <b>Description:</b> Bit[0] = 0 Initial cold Boot when all domains start from reset Bit[0] = 1 Boot when S5 domain persists

**MISCx00000058 (FCH::MISC::CLKCNTRL58)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISCx00000058; MISC=FED8\_0E00h**Bits Description**

31:0 Reserved.

**MISCx0000005C (FCH::MISC::CLKCNTRL5C)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISCx0000005C; MISC=FED8\_0E00h**Bits Description**

31:0 Reserved.

**MISCx00000060 (FCH::MISC::IDLECNTRL)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISCx00000060; MISC=FED8\_0E00h**Bits Description**31:24 **idlecount**. Read-write. Reset: 00h. This returns the idle count from the latest monitored period.

23:0 Reserved.

**MISCx00000064 (FCH::MISC::DSMXTRIG\_ROUTING)**

Read-write. Reset: FFFFh.

\_aliasHOSTLEGACY; MISCx00000064; MISC=FED8\_0E00h

Bits	Description
15	<b>dsmxtrig3_to_ec.</b> Read-write. Reset: 1. <b>Description:</b> 1: Enable CNB2ACPI_AL_trigB[3] low-pulse will trigger a 8051 ( <a href="#">EC</a> ) action 0: Disabled
14	<b>dsmxtrig2_to_ec.</b> Read-write. Reset: 1. <b>Description:</b> 1: Enable CNB2ACPI_AL_trigB[2] low-pulse will trigger a 8051 ( <a href="#">EC</a> ) action 0: Disabled
13	<b>dsmxtrig1_to_ec.</b> Read-write. Reset: 1. <b>Description:</b> 1: Enable CNB2ACPI_AL_trigB[1] low-pulse will trigger a 8051 ( <a href="#">EC</a> ) action 0: Disabled
12	<b>dsmxtrig0_to_ec.</b> Read-write. Reset: 1. <b>Description:</b> 1: Enable CNB2ACPI_AL_trigB[0] low-pulse will trigger a 8051 ( <a href="#">EC</a> ) action 0: Disabled
11	<b>dsmxtrig3_to_autotransaction.</b> Read-write. Reset: 1. <b>Description:</b> 1: Enable the falling of CNB2ACPI_AL_trigB[3] to trigger a pre-programmed transaction. 0: Disabled
10	<b>dsmxtrig2_to_autotransaction.</b> Read-write. Reset: 1. <b>Description:</b> 1: Enable the falling of CNB2ACPI_AL_trigB[2] to trigger a pre-programmed transaction. 0: Disabled
9	<b>dsmxtrig1_to_autotransaction.</b> Read-write. Reset: 1. <b>Description:</b> 1: Enable the falling of CNB2ACPI_AL_trigB[1] to trigger a pre-programmed transaction. 0: Disabled
8	<b>dsmxtrig0_to_autotransaction.</b> Read-write. Reset: 1. <b>Description:</b> 1: Enable the falling of CNB2ACPI_AL_trigB[0] to trigger a pre-programmed transaction. 0: Disabled
7	<b>dsmxtrig3_to_irq.</b> Read-write. Reset: 1. <b>Description:</b> 1: Enable CNB2ACPI_AL_trigB[3] being low to trigger a specific IRQ (depend on the setting in IO C00/C01 registers) 0: Disabled
6	<b>dsmxtrig2_to_irq.</b> Read-write. Reset: 1. <b>Description:</b> 1: Enable CNB2ACPI_AL_trigB[2] being low to trigger a specific IRQ (depend on the setting in IO C00/C01 registers) 0: Disabled
5	<b>dsmxtrig1_to_irq.</b> Read-write. Reset: 1. <b>Description:</b> 1: Enable CNB2ACPI_AL_trigB[1] being low to trigger a specific IRQ (depend on the setting in IO C00/C01 registers) 0: Disabled
4	<b>dsmxtrig0_to_irq.</b> Read-write. Reset: 1. <b>Description:</b> 1: Enable CNB2ACPI_AL_trigB[0] being low to trigger a specific IRQ (depend on the setting in IO C00/C01 registers) 0: Disabled
3	<b>dsmxtrig3_to_smi.</b> Read-write. Reset: 1. <b>Description:</b> 1: Enable the falling of CNB2ACPI_AL_trigB[3] to trigger an <a href="#">SMI</a> 0: Disabled
2	<b>dsmxtrig2_to_smi.</b> Read-write. Reset: 1. <b>Description:</b> 1: Enable the falling of CNB2ACPI_AL_trigB[2] to trigger an <a href="#">SMI</a> 0: Disabled



1	<b>dsmxtrig1_to_smi.</b> Read-write. Reset: 1.
	<b>Description:</b> 1: Enable the falling of CNB2ACPI_AL_trigB[1] to trigger an <a href="#">SMI</a> 0: Disabled
0	<b>dsmxtrig0_to_smi.</b> Read-write. Reset: 1.
	<b>Description:</b> 1: Enable the falling of CNB2ACPI_AL_trigB[0] to trigger an <a href="#">SMI</a> 0: Disabled

**MISCx00000068 (FCH::MISC::MEMPWRSVCNTRL)**

Read-write.

\_aliasHOSTLEGACY; MISCx00000068; MISC=FED8\_0E00h

Bits	Description
31	<b>ec_bypass_mem_dsd.</b> Read-write. Reset: 1. <a href="#">EC</a> memory BypassMemdsd control.
30	<b>bios_ram_bypass_mem_dsd.</b> Read-write. Reset: 1. <b>Description:</b> BIOS RAM BypassMemdsd control. 0: Enable memory DS features. 1: Disable memory DS. Default is 1'b1, memory DS is disabled.
29	<b>shdw_ram_bypass_mem_dsd.</b> Read-write. Reset: 1. <b>Description:</b> Shadow RAM BypassMemdsd control. 0: Enable memory DS features. 1: Disable memory DS. Default is 1'b1, memory DS is disabled.
28	<b>hub_mem_slp_dis.</b> Read-write. Reset: 0. USB Hub BypassMemdsd control
27	<b>ehci_mem_slp_dis.</b> Read-write. Reset: 0. USB2 BypassMemdsd control
26:21	Reserved.
20	<b>gbe_bypass_mem_dsd.</b> Read-write. Reset: 1. <b>Description:</b> GBE Memory BypassMemdsd control 1: Disable Memory <a href="#">Shutdown</a> . 0: Enable Memory Shutdown. Default is 1'b1, memory Shutdown is disabled.
19	<b>ufs_bypass_mem_dsd.</b> Read-write. Reset: 1. <b>Description:</b> UFS Memory BypassMemdsd control 1: Disable Memory shutdown. 0: Enable Memory shutdown. Default is 1'b1, memory <a href="#">Shutdown</a> is disabled. Note: While PCI reset assert, memory will keep shutdown regardless this bit.
18	<b>sd_bypass_mem_dsd.</b> Read-write. Reset: 1. SD memory BypassMemdsd control.
17	<b>sata_bypass_mem_dsd.</b> Read-write. Reset: 0. SATAMemory BypassMemdsd control.
16	<b>cfga_xhc_ncpu_mem_slp_dis.</b> Read-write. Reset: 0. USB3 memory BypassMemdsd control.
15	<b>hid_bypass_mem_dsd.</b> Read-write. Reset: 1. <b>Description:</b> HID memory (2 of them, 1024x32 and 512x32) BypassMemdsd control. 0: Enable memory DS and SD features. 1: Disable memory DS and SD. Default is 1'b1, memory DS/SD is disabled.
14:6	Reserved.
5	<b>i3c_bypass_mem_dsd.</b> Read-write. Reset: 1. I3C memory BypassMemdsd control.
4	<b>ila_bypass_mem_dsd.</b> Read-write. Reset: 1. ILA memory BypassMemdsd control.
3	<b>amba_bypass_mem_dsd.</b> Read-write. Reset: 1. <b>Description:</b> AMBA memory BypassMemdsd control. 0: Enable memory DS and SD features. 1: Disable memory DS and SD. Default is 1'b1, memory DS/SD is disabled.
2	<b>ab_bypass_mem_dsd.</b> Read-write. Reset: 1. AB memory BypassMemdsd control.
1	<b>sbg_bypass_mem_dsd.</b> Read-write. Reset: 1.

	<b>Description:</b> SBG memory BypassMemdsd control. 0: Enable memory DS and SD features. 1: Disable memory DS and SD. Default is 1'b1, memory DS/SD is disabled.
0	Reserved.

**MISCx00000070 (FCH::MISC::OSCFREQCOUNTER)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISCx00000070; MISC=FED8\_0E00h

Bits	Description
31	<b>countenable.</b> Read-write. Reset: 0. When set, it enables the internal counter to count the number of OSC clocks. When SW is not using this function, it should always set it back to 0 to conserve power.
30	<b>countisvalid.</b> Read-write. Reset: 0. When OscCountPerSec is valid, this bit is set. This bit is read only. SW should always wait for this bit to be set before it should read OscCountPerSec
29:28	Reserved.
27:0	<b>osccountpersec.</b> Read-write. Reset: 000_0000h. Number of OSC clocks per 1 second. Whenever bit 31 (CountEnable) is set, an internal counter will start counting the number of OSC clocks per second and record the count value here.

**MISCx00000074 (FCH::MISC::HPETCLKPERIOD)**

Read-write. Reset: 0429\_B17Eh.

\_aliasHOSTLEGACY; MISCx00000074; MISC=FED8\_0E00h

Bits	Description
31:0	<b>hpetclkperiod.</b> Read-write. Reset: 0429_B17Eh. The register controls the value of clkperiod register in HPET <a href="#">MMIO</a> register space.

**MISCx00000078 (FCH::MISC::POSTCODE)**

Read-only. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISCx00000078; MISC=FED8\_0E00h

Bits	Description
31:0	<b>postcode_31_0.</b> Read-only. Reset: 0000_0000h. <b>Description:</b> IO-Wr 83h~80h can write an internal 32-bit PostCode Register (PostCode[31:0]). IO-Rd 80h will return PostCode[7:0]. Reading Misc_Reg:7Bh~78h with PostCodeWidthSel=1 will return {24'b0, PostCode[7:0]}. Reading Misc_Reg:7Bh~78h with PostCodeWidthSel=0 will return PostCode[31:0].

**MISCx0000007C (FCH::MISC::POSTCODESTACK)**

Read-only. Reset: FFFF\_FFFFh.

\_aliasHOSTLEGACY; MISCx0000007C; MISC=FED8\_0E00h

Bits	Description
31:0	<b>postcodestack_31_0.</b> Read-only. Reset: FFFF_FFFFh. <b>Description:</b> 8 deep post code STACK read out window. Each time read will get 32 bits post code. Unused byte will return all 0s. If write full, will lost the oldest data and fill in the new data. When SW read out the STACK, it will read from new data to old data, and don't flush them. Extra read will get duplicate data.

**MISCx00000080 (FCH::MISC::STRAPSTATUS)**

Read-only.

\_aliasHOSTLEGACY; MISCx00000080; MISC=FED8\_0E00h

Bits	Description
31:28	<b>socket_id.</b> Read-only. Reset: XXXXb. Socket ID of the current socket.
27:24	<b>dieid.</b> Read-only. Reset: XXXXb. Die ID of the current Die.
23:20	<b>package_id.</b> Read-only. Reset: XXXXb. Reserved.
19:18	Reserved.
17	<b>clkgenstrap.</b> Read-only. Reset: X. <b>Description:</b> Defines clock generator. 0: Use 100Mhz PCIE clock as reference clock and generate internal clocks only. Note a 48Mhz crystal is still required in this configuration. 1: Use 48Mhz crystal clock and generate both internal and external clocks. External pull-up/Pull-down is required on the pin (this strap does have a weak internal 50K ohm pull-down resistor).
16:6	Reserved.
5	<b>waf_train_disable.</b> Read-only. Reset: 0. <b>Description:</b> WAFL_TRAINING_DISABLE = 0 (default) means WAFL link will be trained. WAFL_TRAINING_DISABLE = 1 means WAFL link will not be trained.
4	Reserved.
3	<b>romtype_1.</b> Read-only. Reset: X. <b>Description:</b> 0: ROM strap is SPI (see romtype_0 for full setting) 1: ROM strap is eSPI (see romtype_0 for full setting).
2	Reserved.
1	<b>romtype_0.</b> Read-only. Reset: X. <b>Description:</b> Boot rom selection: if romtype_1 = 0 and romtype_0 = 0: Reserved if romtype_1 = 0 and romtype_0 = 1: ROM strap is SPI if romtype_1 = 1 and romtype_0 = 0: eSPI with SAFS support if romtype_1 = 1 and romtype_0 = 1: eSPI without SAFS support
0	<b>alternateimage.</b> Read-only. Reset: X. <b>Description:</b> 0: SPI ROM does not support Alternate Image, 24-bit address SPI mode can be used to access ROM = 16MB 1: SPI ROM support Alternate Image, Software need to enable 32-bit address SPI mode to access ROM > 16MB

**MISCx00000088 (FCH::MISC::POSTCODE\_CONTROL)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISCx00000088; MISC=FED8\_0E00h

Bits	Description
31:1	Reserved.
0	<b>post_rd_ptr_rst.</b> Read-write. Reset: 0. Software reset bit for read pointer. When new turn of read needed, set this bit and read pointer will go back for next turn's read.

**MISCx00000090 (FCH::MISC::AUTOTRANSACTION)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; MISCx00000090; MISC=FED8\_0E00h

Bits	Description
7:4	<b>transactiontype</b> . Read-write. Reset: 0h. PCI Command type used for this transaction. For example, if this is programmed with a value of 3h, the transaction issue will be an IO write.
3:2	<b>bytecount</b> . Read-write. Reset: 0h. <b>Description:</b> 00: 1 byte 01: 2 bytes 10: 4 bytes 11: 4 bytes
1	<b>dualaddr</b> . Read-write. Reset: 0. <b>Description:</b> 0: Use single address cycle 1: Use dual address cycle
0	<b>autoexecute</b> . Read-write. Reset: 0. Writing this bit will cause the HW to execute the transaction defined by the definition below. Once it is written, this bit stays as 1 until the transaction is completed, in which case it will return to 0

**MISCx00000091 (FCH::MISC::ALLOWEC)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; MISCx00000091; MISC=FED8\_0E00h

Bits	Description
7:3	Reserved.
2	<b>autotriggerfromcpuen</b> . Read-write. Reset: 0. If this bit is set, a falling edge on KSO15/XDB[1] /(&cnb_fch_dsm_xtrig[3:0]) will trigger this autotransaction logic
1	<b>disableauto</b> . Read-write. Reset: 0. If this bit is set, the entire AutoTransaction logic is disabled. Once this bit is set, it cannot be cleared except by system reset
0	<b>allowectoautotransacten</b> . Read-write. Reset: 0. When this bit is 0, <a href="#">EC</a> cannot write to any of registers relating to any of the registers in the Auto Transaction Generation logic. When this bit is 1, then EC can change any of these bits. Only BIOS can change this bit.

**MISCx00000094 (FCH::MISC::AUTOADDRLOW)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISCx00000094; MISC=FED8\_0E00h

Bits	Description
31:0	<b>autoaddrlow</b> . Read-write. Reset: 0000_0000h. Low address to be used by the AutoExecute operation

**MISCx00000098 (FCH::MISC::AUTOADDRHIGH)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISCx00000098; MISC=FED8\_0E00h

Bits	Description
31:0	<b>autoaddrhigh</b> . Read-write. Reset: 0000_0000h. High address to be used by the AutoExecute operation. This register is only applicable when DualAddr = 1.

**MISCx0000009C (FCH::MISC::AUTODATA)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISCx0000009C; MISC=FED8\_0E00h

Bits	Description
31:0	<b>autodata</b> . Read-write. Reset: 0000_0000h. If the operation is read, this register will return the read data. If the TransactionType is a write command, this register will contain the write data. Note byte is aligned accordingly.

**MISCx000000A0 (FCH::MISC::CGPLLCNTRL0)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISCx000000A0; MISC=FED8\_0E00h

**Bits Description**

31:0 Reserved.

**MISCx000000A4 (FCH::MISC::CGPLLCNTRL1)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISCx000000A4; MISC=FED8\_0E00h

**Bits Description**

31:0 Reserved.

**MISCx000000A8 (FCH::MISC::CGPLLCNTRL2)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISCx000000A8; MISC=FED8\_0E00h

**Bits Description**

31:0 Reserved.

**MISCx000000AC (FCH::MISC::CGPLLCNTRL3)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISCx000000AC; MISC=FED8\_0E00h

**Bits Description**

31:23 Reserved.

22 **cpu\_refclk\_driver\_static\_pwdn.** Read-write. Reset: 0.

**Description:** CPU Refclk (100MHz) Driver Static PWDN  
 Program this bit will static turn off or on CPU refclk.  
 0 = enable (turn on)  
 1 = disable (turn off)

21 **cpu\_100m\_refclk\_selection.** Read-write. Reset: 0.

**Description:** CPU\_100M Refclk Selection  
 0 = 100MHz CG1\_PLL generated (default)  
 1 = GPP1 external refclk  
 Note: MISCx000000BC[11] to select EXT\_GPP1\_SRC either is from GPP1 external input or GPP1 external input with divided-by-2 or divided-by-4

20 **smu\_100m\_refclk\_selection.** Read-write. Reset: 0.

**Description:** SMU\_100M Refclk Selection  
 0 = 100MHz CG1\_PLL generated (default)  
 1 = GPP0 external refclk

19:0 Reserved.

**MISCx000000B0 (FCH::MISC::CGPLLCNTRL4)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISCx000000B0; MISC=FED8\_0E00h

**Bits Description**

31:0 Reserved.

**MISCx000000B4 (FCH::MISC::CGPLLCNTRL5)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISCx000000B4; MISC=FED8\_0E00h

**Bits Description**

31:0 Reserved.

**MISCx000000B8 (FCH::MISC::CGPLLCNTRL6)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISCx000000B8; MISC=FED8\_0E00h**Bits** **Description**

31:0 Reserved.

**MISCx000000BC (FCH::MISC::CGPLLCNTRL7)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISCx000000BC; MISC=FED8\_0E00h

Bits	Description
31:28	Reserved.
27:26	<b>gpp5_refclk_selection_override.</b> Read-write. Reset: 0h. <b>Description:</b> GPP5 Refclk selection Override 00 = CG_PLL generated 100MHz 01 = CG2_PLL generated 100MHz (not a valid option) 10 = Reserved 11 = Ext_GPP0_SRC Note: MISCx000000BC[13] to select EXT_GPP0_SRC either is from GPP0 external input or GPP0 external input with divided-by-2/divided-by-4
25:24	<b>gpp4_refclk_selection_override.</b> Read-write. Reset: 0h. <b>Description:</b> GPP4 Refclk selection Override 00 = CG_PLL generated 100MHz 01 = CG2_PLL generated 100MHz (not a valid option) 10 = Reserved 11 = Ext_GPP0_SRC Note: MISCx000000BC[13] to select EXT_GPP0_SRC either is from GPP0 external input or GPP0 external input with divided-by-2/divided-by-4
23:22	<b>gpp3_refclk_selection_override.</b> Read-write. Reset: 0h. <b>Description:</b> GPP3 Refclk selection Override 00 = CG_PLL generated 100MHz 01 = CG2_PLL generated 100MHz (not a valid option) 10 = Reserved 11 = Reserved Note: MISCx000000BC[13] to select EXT_GPP0_SRC either is from GPP0 external input or GPP0 external input with divided-by-2/divided-by-4
21:20	<b>gpp2_refclk_selection_override.</b> Read-write. Reset: 0h. <b>Description:</b> GPP2 Refclk selection Override 00 = CG_PLL generated 100MHz 01 = CG2_PLL generated 100MHz (not a valid option) 10 = Reserved 11 = Reserved Note: MISCx000000BC[13] to select EXT_GPP0_SRC either is from GPP0 external input or GPP0 external input with divided-by-2/divided-by-4
19:18	<b>gpp1_refclk_selection_override.</b> Read-write. Reset: 0h. <b>Description:</b> GPP1 Refclk selection Override 00 = CG_PLL generated 100MHz 01 = CG2_PLL generated 100MHz (not a valid option) 10 = Reserved 11 = Reserved Note: MISCx000000BC[13] to select EXT_GPP0_SRC either is from GPP0 external input or GPP0 external input with divided-by-2/divided-by-4
17:16	<b>gpp0_refclk_selection_override.</b> Read-write. Reset: 0h.



	<b>Description:</b> GPP0 Refclk selection Override 00 = CG1_PLL generated 100MHz 01 = CG2_PLL generated 100MHz (not a valid option) 10 = GPP2_RX (GPP2_BOT) 11 = Reserved Note: MISCx000000BC[12] to select EXT_GPP2_SRC either is from GPP2 external input or GPP2 external input with divided-by-2/divided-by-4
15	<b>ext_bypassclk_en.</b> Read-write. Reset: 0. <b>Description:</b> EXT_BYPASSCLK_EN Enable/Disable REF_BYPASSCLK external input thru GPP3_RX 0 = disable 1 = enable
14	<b>clk_cgpll_ext_pwdn.</b> Read-write. Reset: 0. <b>Description:</b> CLK_CGPLL_EXT_PWDN Enable/Disable CGPLL external refclk source thru GPP0 input. 0 = enable 1 = disable
13	<b>ext_gpp0_refclk_sel.</b> Read-write. Reset: 0. <b>Description:</b> EXT_GPP0_REFCLK_SEL 0 = GPP0 external input 1 = GPP0 external input divided-by-2(div-2 or div-4 depend on MISCx0000003C[1])
12	Reserved.
11	<b>ext_gpp1_refclk_sel.</b> Read-write. Reset: 0. <b>Description:</b> EXT_GPP1_REFCLK_SEL 0 = GPP1 external input 1 = GPP1 external input divided-by-2(div-2 or div-4 depend on MISCx0000003C[3])
10	<b>smu_100m_refclk_driver_pwdn.</b> Read-write. Reset: 0. <b>Description:</b> SMU_100M Refclk Driver PWDN 0 = enable 1 = disable
9:0	Reserved.

**MISCx000000C0 (FCH::MISC::IOTRAPPING0)**

Read-write. Reset: 0000h.

\_aliasHOSTLEGACY; MISCx000000C0; MISC=FED8\_0E00h

Bits	Description
15:0	<b>iotrappingadr0.</b> Read-write. Reset: 0000h. Specify the I/O address 0 which causes <a href="#">SMI</a> event.

**MISCx000000C2 (FCH::MISC::IOTRAPPING1)**

Read-write. Reset: 0000h.

\_aliasHOSTLEGACY; MISCx000000C2; MISC=FED8\_0E00h

Bits	Description
15:0	<b>iotrappingadr1.</b> Read-write. Reset: 0000h. Specify the I/O address 1 which causes <a href="#">SMI</a> event.

**MISCx000000C4 (FCH::MISC::IOTRAPPING2)**

Read-write. Reset: 0000h.

\_aliasHOSTLEGACY; MISCx000000C4; MISC=FED8\_0E00h

Bits	Description
15:0	<b>iotrappingadr2.</b> Read-write. Reset: 0000h. Specify the I/O address 2 which causes <a href="#">SMI</a> event.

**MISCx000000C6 (FCH::MISC::IOTRAPPING3)**

Read-write. Reset: 0000h.

\_aliasHOSTLEGACY; MISCx000000C6; MISC=FED8\_0E00h

Bits	Description
15:0	<b>iotrappingadr3</b> . Read-write. Reset: 0000h. Specify the I/O address 3 which causes <a href="#">SMI</a> event.

**MISCx000000C8 (FCH::MISC::CFGTRAPPING0)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISCx000000C8; MISC=FED8\_0E00h

Bits	Description
31:2	<b>cfgtrappingadr0</b> . Read-write. Reset: 0000_0000h. Specify the CFG address 0 which causes <a href="#">SMI</a> event.
1:0	Reserved.

**MISCx000000CC (FCH::MISC::SMITRAPPINGRWRDOVR)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISCx000000CC; MISC=FED8\_0E00h

Bits	Description
31:25	Reserved.
24:17	<b>i3cpadsmodeppodselect.</b> Read-write. Reset: 00h. <b>Description:</b> 0x00: I3C pads work on Open-Drain mode. 0xFF: I3C pads work on Push-Pull mode. Others: Reserved. Note: This field should only be 0x00 or 0xFF, other values are not recommended. This field should be set to 0xFF if any of pads I2C0 ~ 3 is set to the GPIO function.
16	<b>cfgtrappingrw0.</b> Read-write. Reset: 0. <b>Description:</b> 0: Trap on CFG read access on the address specified in CfgTrappingAdr0 1: Trap on CFG write access on the address specified in CfgTrappingAdr0
15:13	Reserved.
12	<b>memtrappingrdovr0.</b> Read-write. Reset: 0. Set to 1 to force read data to be replaced by MemRdOvrData0.
11:9	Reserved.
8	<b>memtrappingrw0.</b> Read-write. Reset: 0. <b>Description:</b> 0: Trap on MEM read access on the address specified in MemTrappingAdr0 1: Trap on MEM write access on the address specified in MemTrappingAdr0
7:4	Reserved.
3	<b>iotrappingrw3.</b> Read-write. Reset: 0. <b>Description:</b> 0: Trap on I/O read access on the address specified in IoTrappingAdr3 1: Trap on I/O write access on the address specified in IoTrappingAdr3
2	<b>iotrappingrw2.</b> Read-write. Reset: 0. <b>Description:</b> 0: Trap on I/O read access on the address specified in IoTrappingAdr2 1: Trap on I/O write access on the address specified in IoTrappingAdr2
1	<b>iotrappingrw1.</b> Read-write. Reset: 0. <b>Description:</b> 0: Trap on I/O read access on the address specified in IoTrappingAdr1 1: Trap on I/O write access on the address specified in IoTrappingAdr1
0	<b>iotrappingrw0.</b> Read-write. Reset: 0. <b>Description:</b> 0: Trap on I/O read access on the address specified in IoTrappingAdr0 1: Trap on I/O write access on the address specified in IoTrappingAdr0

**MISCx000000D0 (FCH::MISC::MEMTRAPPING0)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISCx000000D0; MISC=FED8\_0E00h

Bits	Description
31:2	<b>memtrappingadr0</b> . Read-write. Reset: 0000_0000h. Specify the 30-bit MEM address 0 which causes <a href="#">SMI</a> even, lowest 2 bits are ignored.
1:0	Reserved.

**MISCx000000D4 (FCH::MISC::MEMRDOVRDATA0)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISCx000000D4; MISC=FED8\_0E00h

Bits	Description
31:0	<b>memtrappingrdata0</b> . Read-write. Reset: 0000_0000h. The 32 bit data is used as the return data when the memory read trapping is enabled in MemTrapping0. With MemTrappingRdOvr0 = 1

**MISCx000000D8 (FCH::MISC::I2C0\_PADCTRL)**

Read-write. Reset: 0000\_003Ch.

This 32-bit register is used to control I3C and I2C pad.

\_aliasHOSTLEGACY; MISCx000000D8; MISC=FED8\_0E00h

Bits	Description
31:30	<b>spikercsel_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> Select RC constant for I2C spike suppression. Bit 1 for PAD1 and Bit 0 for PAD0. 1 = 20ns spike suppression 0 = 50ns spike suppression
29:28	<b>mode_1p8_1p1_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> Voltage Select pin. Bit 1 for PAD1 and Bit 0 for PAD0. 1 = 1.8V operation 0 = 1.1V operation
27:26	<b>mode_i3c_i2c_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> I3C or I2C mode enable. Bit 1 for PAD1 and Bit 0 for PAD0. 1= I3C mode 0 = I2C mode
25:24	<b>slewp_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> Active Rise Slew Compensation. Bit 1 for PAD1 and Bit 0 for PAD0. 1= Faster rise slew 0= Disable
23:22	<b>resbiasen_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> When the bias circuit is enabled (BiasCrtEn=1), ResBiasEn determines the bias current type. Bit 1 for PAD1 and Bit 0 for PAD0. 1= Constant-gm resistive current 0= Temperature compensated resistive current
21:20	<b>compsel_1_0.</b> Read-write. Reset: 0h. Unused.
19:18	<b>spare_1_0.</b> Read-write. Reset: 0h. Spare pins. Bit 1 for PAD1 and Bit 0 for PAD0.
17:16	<b>biascrten_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> Bias circuit should be ON only in I2C mode. Bit 1 for PAD1 and Bit 0 for PAD0. 1= Enable for I2C Fast/Fast plus mode slew spec 0= Disable for I2C Standard mode
15	<b>rsel1p1.</b> Read-write. Reset: 0. When asserted decreases or increases resistance by 10% for all RC timers. Must be used in conjunction with pin Mode_I3c_I2c = 0 only.
14	<b>rsel0p9.</b> Read-write. Reset: 0. When asserted decreases or increases resistance by 10% for all RC timers. Must be used in conjunction with pin Mode_I3c_I2c = 0 only.
13	<b>csel1p1.</b> Read-write. Reset: 0. When asserted decreases or increases capacitance by 10% for all RC timers. Must be used in conjunction with pin Mode_I3c_I2c = 0 only.
12	<b>csel0p9.</b> Read-write. Reset: 0. When asserted decreases or increases capacitance by 10% for all RC timers. Must be used in conjunction with pin Mode_I3c_I2c = 0 only.
11:10	<b>spikercen_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> Enables spike suppression in I2C mode only. Bit 1 for PAD1 and Bit 0 for PAD0. 1= Filter enable (must be used in conjunction with pin Mode_I3c_I2c = 0 only for 1.8V and 1.1V system) 0= Disable
9:8	<b>fallslewsel_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> I2C Mode select bits. Bit 1 for PAD1 and Bit 0 for PAD0. Must be used when Mode_I3c_I2c=0 pin. 1= I2C Fast Mode (Tx Freq=400kHz), Fast Plus Mode (Tx Freq=1MHz) 0= I2C Standard Mode, Tx Freq=100kHz.
7:6	<b>slewn_1_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> Active Fall Slew Compensation. Bit 1 for PAD1 and Bit 0 for PAD0. 1= Faster fall slew 0= Disable
5:4	<b>rxsel_1_0.</b> Read-write. Reset: 3h. <b>Description:</b> Select RX of operation. Bit 1 for PAD1 and Bit 0 for PAD0. 1= 1.8V or 1.1V RX (must be used in conjunction with pin Mode_1p8_1p1 = 1/0 for 1.8V and 1.1V system) 0= RX OFF
3:0	<b>od_rp_sw_3_0.</b> Read-write. Reset: Ch. <b>Description:</b> Open-drain pull-up switch. Bit 3 and 1 for PAD1, and Bit 2 and 0 for PAD0. This field is only meaningful when the corresponding pad works in I3C mode to enable/disable 600-ohm integrated pull-up resistor for 1.8v, or 800-ohm for 1.1v. OD_Rp_Sw[3] = 0x0: Pull-up enabled is controlled by I3C controller. OD_Rp_Sw[3] = 0x1: Pull-up enabled is controlled by OD_Rp_Sw[1]. OD_Rp_Sw[2] = 0x0: Pull-up enabled is controlled by I3C controller. OD_Rp_Sw[2] = 0x1: Pull-up enabled is controlled by OD_Rp_Sw[0]. Note: When the pad works in I2C 1.1v mode, it has an 800-ohm integrated pull-up resistor regardless of this field's value. When the pad works in I2C 1.8v mode, the external pull-up resistor is needed.

**MISCx000000DC (FCH::MISC::I2C1\_PADCTRL)**

Read-write. Reset: 0000\_003Ch.

This 32-bit register is used to control I3C and I2C pad.

\_aliasHOSTLEGACY; MISCx000000DC; MISC=FED8\_0E00h

Bits	Description
31:30	<b>spikercsel_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> Select RC constant for I2C spike suppression. Bit 1 for PAD1 and Bit 0 for PAD0. 1 = 20ns spike suppression 0 = 50ns spike suppression
29:28	<b>mode_1p8_1p1_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> Voltage Select pin. Bit 1 for PAD1 and Bit 0 for PAD0. 1 = 1.8V operation 0 = 1.1V operation
27:26	<b>mode_i3c_i2c_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> I3C or I2C mode enable. Bit 1 for PAD1 and Bit 0 for PAD0. 1= I3C mode 0 = I2C mode
25:24	<b>slewp_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> Active Rise Slew Compensation. Bit 1 for PAD1 and Bit 0 for PAD0. 1= Faster rise slew 0= Disable
23:22	<b>resbiasen_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> When the bias circuit is enabled (BiasCrtEn=1), ResBiasEn determines the bias current type. Bit 1 for PAD1 and Bit 0 for PAD0. 1= Constant-gm resistive current 0= Temperature compensated resistive current
21:20	<b>compsel_1_0.</b> Read-write. Reset: 0h. Unused.
19:18	<b>spare_1_0.</b> Read-write. Reset: 0h. Spare pins. Bit 1 for PAD1 and Bit 0 for PAD0.
17:16	<b>biascrten_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> Bias circuit should be ON only in I2C mode. Bit 1 for PAD1 and Bit 0 for PAD0. 1= Enable for I2C Fast/Fast plus mode slew spec 0= Disable for I2C Standard mode
15	<b>rsel1p1.</b> Read-write. Reset: 0. When asserted decreases or increases resistance by 10% for all RC timers. Must be used in conjunction with pin Mode_I3c_I2c = 0 only.
14	<b>rsel0p9.</b> Read-write. Reset: 0. When asserted decreases or increases resistance by 10% for all RC timers. Must be used in conjunction with pin Mode_I3c_I2c = 0 only.
13	<b>csel1p1.</b> Read-write. Reset: 0. When asserted decreases or increases capacitance by 10% for all RC timers. Must be used in conjunction with pin Mode_I3c_I2c = 0 only.
12	<b>csel0p9.</b> Read-write. Reset: 0. When asserted decreases or increases capacitance by 10% for all RC timers. Must be used in conjunction with pin Mode_I3c_I2c = 0 only.
11:10	<b>spikercen_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> Enables spike suppression in I2C mode only. Bit 1 for PAD1 and Bit 0 for PAD0. 1= Filter enable (must be used in conjunction with pin Mode_I3c_I2c = 0 only for 1.8V and 1.1V system) 0= Disable
9:8	<b>fallslewsel_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> I2C Mode select bits. Bit 1 for PAD1 and Bit 0 for PAD0. Must be used when Mode_I3c_I2c=0 pin. 1= I2C Fast Mode (Tx Freq=400kHz), Fast Plus Mode (Tx Freq=1MHz) 0= I2C Standard Mode, Tx Freq=100kHz.
7:6	<b>slewn_1_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> Active Fall Slew Compensation. Bit 1 for PAD1 and Bit 0 for PAD0. 1= Faster fall slew 0= Disable
5:4	<b>rxsel_1_0.</b> Read-write. Reset: 3h. <b>Description:</b> Select RX of operation. Bit 1 for PAD1 and Bit 0 for PAD0. 1= 1.8V or 1.1V RX (must be used in conjunction with pin Mode_1p8_1p1 = 1/0 for 1.8V and 1.1V system) 0= RX OFF
3:0	<b>od_rp_sw_3_0.</b> Read-write. Reset: Ch. <b>Description:</b> Open-drain pull-up switch. Bit 3 and 1 for PAD1, and Bit 2 and 0 for PAD0. This field is only meaningful when the corresponding pad works in I3C mode to enable/disable 600-ohm integrated pull-up resistor for 1.8v, or 800-ohm for 1.1v. OD_Rp_Sw[3] = 0x0: Pull-up enabled is controlled by I3C controller. OD_Rp_Sw[3] = 0x1: Pull-up enabled is controlled by OD_Rp_Sw[1]. OD_Rp_Sw[2] = 0x0: Pull-up enabled is controlled by I3C controller. OD_Rp_Sw[2] = 0x1: Pull-up enabled is controlled by OD_Rp_Sw[0]. Note: When the pad works in I2C 1.1v mode, it has an 800-ohm integrated pull-up resistor regardless of this field's value. When the pad works in I2C 1.8v mode, the external pull-up resistor is needed.



**MISCx000000E0 (FCH::MISC::I2C2\_PADCTRL)**

Read-write. Reset: 0000\_003Ch.

This 32-bit register is used to control I3C and I2C pad.

\_aliasHOSTLEGACY; MISCx000000E0; MISC=FED8\_0E00h

Bits	Description
31:30	<b>spikercsel_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> Select RC constant for I2C spike suppression. Bit 1 for PAD1 and Bit 0 for PAD0. 1 = 20ns spike suppression 0 = 50ns spike suppression
29:28	<b>mode_1p8_1p1_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> Voltage Select pin. Bit 1 for PAD1 and Bit 0 for PAD0. 1 = 1.8V operation 0 = 1.1V operation
27:26	<b>mode_i3c_i2c_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> I3C or I2C mode enable. Bit 1 for PAD1 and Bit 0 for PAD0. 1= I3C mode 0 = I2C mode
25:24	<b>slewp_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> Active Rise Slew Compensation. Bit 1 for PAD1 and Bit 0 for PAD0. 1= Faster rise slew 0= Disable
23:22	<b>resbiasen_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> When the bias circuit is enabled (BiasCrtEn=1), ResBiasEn determines the bias current type. Bit 1 for PAD1 and Bit 0 for PAD0. 1= Constant-gm resistive current 0= Temperature compensated resistive current
21:20	<b>compsel_1_0.</b> Read-write. Reset: 0h. Unused.
19:18	<b>spare_1_0.</b> Read-write. Reset: 0h. Spare pins. Bit 1 for PAD1 and Bit 0 for PAD0.
17:16	<b>biascrten_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> Bias circuit should be ON only in I2C mode. Bit 1 for PAD1 and Bit 0 for PAD0. 1= Enable for I2C Fast/Fast plus mode slew spec 0= Disable for I2C Standard mode
15	<b>rsel1p1.</b> Read-write. Reset: 0. When asserted decreases or increases resistance by 10% for all RC timers. Must be used in conjunction with pin Mode_I3c_I2c = 0 only.
14	<b>rsel0p9.</b> Read-write. Reset: 0. When asserted decreases or increases resistance by 10% for all RC timers. Must be used in conjunction with pin Mode_I3c_I2c = 0 only.
13	<b>csel1p1.</b> Read-write. Reset: 0. When asserted decreases or increases capacitance by 10% for all RC timers. Must be used in conjunction with pin Mode_I3c_I2c = 0 only.
12	<b>csel0p9.</b> Read-write. Reset: 0. When asserted decreases or increases capacitance by 10% for all RC timers. Must be used in conjunction with pin Mode_I3c_I2c = 0 only.
11:10	<b>spikercen_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> Enables spike suppression in I2C mode only. Bit 1 for PAD1 and Bit 0 for PAD0. 1= Filter enable (must be used in conjunction with pin Mode_I3c_I2c = 0 only for 1.8V and 1.1V system) 0= Disable
9:8	<b>fallslewsel_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> I2C Mode select bits. Bit 1 for PAD1 and Bit 0 for PAD0. Must be used when Mode_I3c_I2c=0 pin. 1= I2C Fast Mode (Tx Freq=400kHz), Fast Plus Mode (Tx Freq=1MHz) 0= I2C Standard Mode, Tx Freq=100kHz.
7:6	<b>slewn_1_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> Active Fall Slew Compensation. Bit 1 for PAD1 and Bit 0 for PAD0. 1= Faster fall slew 0= Disable
5:4	<b>rxsel_1_0.</b> Read-write. Reset: 3h. <b>Description:</b> Select RX of operation. Bit 1 for PAD1 and Bit 0 for PAD0. 1= 1.8V or 1.1V RX (must be used in conjunction with pin Mode_1p8_1p1 = 1/0 for 1.8V and 1.1V system) 0= RX OFF
3:0	<b>od_rp_sw_3_0.</b> Read-write. Reset: Ch. <b>Description:</b> Open-drain pull-up switch. Bit 3 and 1 for PAD1, and Bit 2 and 0 for PAD0. This field is only meaningful when the corresponding pad works in I3C mode to enable/disable 600-ohm integrated pull-up resistor for 1.8v, or 800-ohm for 1.1v. OD_Rp_Sw[3] = 0x0: Pull-up enabled is controlled by I3C controller. OD_Rp_Sw[3] = 0x1: Pull-up enabled is controlled by OD_Rp_Sw[1]. OD_Rp_Sw[2] = 0x0: Pull-up enabled is controlled by I3C controller. OD_Rp_Sw[2] = 0x1: Pull-up enabled is controlled by OD_Rp_Sw[0]. Note: When the pad works in I2C 1.1v mode, it has an 800-ohm integrated pull-up resistor regardless of this field's value. When the pad works in I2C 1.8v mode, the external pull-up resistor is needed.

**MISCx000000E4 (FCH::MISC::I2C3\_PADCTRL)**

Read-write. Reset: 0000\_003Ch.

This 32-bit register is used to control I3C and I2C pad.

\_aliasHOSTLEGACY; MISCx000000E4; MISC=FED8\_0E00h

Bits	Description
31:30	<b>spikercsel_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> Select RC constant for I2C spike suppression. Bit 1 for PAD1 and Bit 0 for PAD0. 1 = 20ns spike suppression 0 = 50ns spike suppression
29:28	<b>mode_1p8_1p1_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> Voltage Select pin. Bit 1 for PAD1 and Bit 0 for PAD0. 1 = 1.8V operation 0 = 1.1V operation
27:26	<b>mode_i3c_i2c_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> I3C or I2C mode enable. Bit 1 for PAD1 and Bit 0 for PAD0. 1= I3C mode 0 = I2C mode
25:24	<b>slewp_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> Active Rise Slew Compensation. Bit 1 for PAD1 and Bit 0 for PAD0. 1= Faster rise slew 0= Disable
23:22	<b>resbiasen_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> When the bias circuit is enabled (BiasCrtEn=1), ResBiasEn determines the bias current type. Bit 1 for PAD1 and Bit 0 for PAD0. 1= Constant-gm resistive current 0= Temperature compensated resistive current
21:20	<b>compsel_1_0.</b> Read-write. Reset: 0h. Unused.
19:18	<b>spare_1_0.</b> Read-write. Reset: 0h. Spare pins. Bit 1 for PAD1 and Bit 0 for PAD0.
17:16	<b>biascrten_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> Bias circuit should be ON only in I2C mode. Bit 1 for PAD1 and Bit 0 for PAD0. 1= Enable for I2C Fast/Fast plus mode slew spec 0= Disable for I2C Standard mode
15	<b>rsel1p1.</b> Read-write. Reset: 0. When asserted decreases or increases resistance by 10% for all RC timers. Must be used in conjunction with pin Mode_I3c_I2c = 0 only.
14	<b>rsel0p9.</b> Read-write. Reset: 0. When asserted decreases or increases resistance by 10% for all RC timers. Must be used in conjunction with pin Mode_I3c_I2c = 0 only.
13	<b>csel1p1.</b> Read-write. Reset: 0. When asserted decreases or increases capacitance by 10% for all RC timers. Must be used in conjunction with pin Mode_I3c_I2c = 0 only.
12	<b>csel0p9.</b> Read-write. Reset: 0. When asserted decreases or increases capacitance by 10% for all RC timers. Must be used in conjunction with pin Mode_I3c_I2c = 0 only.
11:10	<b>spikercen_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> Enables spike suppression in I2C mode only. Bit 1 for PAD1 and Bit 0 for PAD0. 1= Filter enable (must be used in conjunction with pin Mode_I3c_I2c = 0 only for 1.8V and 1.1V system) 0= Disable
9:8	<b>fallslewsel_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> I2C Mode select bits. Bit 1 for PAD1 and Bit 0 for PAD0. Must be used when Mode_I3c_I2c=0 pin. 1= I2C Fast Mode (Tx Freq=400kHz), Fast Plus Mode (Tx Freq=1MHz) 0= I2C Standard Mode, Tx Freq=100kHz.
7:6	<b>slewn_1_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> Active Fall Slew Compensation. Bit 1 for PAD1 and Bit 0 for PAD0. 1= Faster fall slew 0= Disable
5:4	<b>rxsel_1_0.</b> Read-write. Reset: 3h. <b>Description:</b> Select RX of operation. Bit 1 for PAD1 and Bit 0 for PAD0. 1= 1.8V or 1.1V RX (must be used in conjunction with pin Mode_1p8_1p1 = 1/0 for 1.8V and 1.1V system) 0= RX OFF
3:0	<b>od_rp_sw_3_0.</b> Read-write. Reset: Ch. <b>Description:</b> Open-drain pull-up switch. Bit 3 and 1 for PAD1, and Bit 2 and 0 for PAD0. This field is only meaningful when the corresponding pad works in I3C mode to enable/disable 600-ohm integrated pull-up resistor for 1.8v, or 800-ohm for 1.1v. OD_Rp_Sw[3] = 0x0: Pull-up enabled is controlled by I3C controller. OD_Rp_Sw[3] = 0x1: Pull-up enabled is controlled by OD_Rp_Sw[1]. OD_Rp_Sw[2] = 0x0: Pull-up enabled is controlled by I3C controller. OD_Rp_Sw[2] = 0x1: Pull-up enabled is controlled by OD_Rp_Sw[0]. Note: When the pad works in I2C 1.1v mode, it has an 800-ohm integrated pull-up resistor regardless of this field's value. When the pad works in I2C 1.8v mode, the external pull-up resistor is needed.

**MISCx000000E8 (FCH::MISC::I2C4\_PADCTRL)**

Read-write. Reset: 0000\_003Ch.

This register is used to assist in controlling Pad BP\_I3C4\_SCL/BP\_I3C4\_SDA. Pad0 means BP\_I3C4\_SCL, Pad 1 means BP\_I3C4\_SDA.

\_aliasHOSTLEGACY; MISCx000000E8; MISC=FED8\_0E00h

Bits	Description
31:19	Reserved.
18:17	<b>spare.</b> Read-write. Reset: 0h. Spare Pin
16	<b>biascrten.</b> Read-write. Reset: 0. Pbias should be on in Fast/Fast+ Mode internally overridden to turn on by FallSlew setting, to save power can be turned off in I2C Standard Mode FallSlew=00
15	<b>rsel1p1.</b> Read-write. Reset: 0. When asserted increases resistance by 10% for all RC timers
14	<b>rsel0p9.</b> Read-write. Reset: 0. When asserted decreases resistance by 10% for all RC timers
13	<b>csel1p1.</b> Read-write. Reset: 0. When asserted increases capacitance by 10% for all RC timers
12	<b>csel0p9.</b> Read-write. Reset: 0. When asserted decreases capacitance by 10% for all RC timers
11	<b>spikercsel.</b> Read-write. Reset: 0. Select RC constant for I2C spike suppression, 0=50ns, 1=20ns
10	<b>spikercen.</b> Read-write. Reset: 0. Enable Rx spike suppression, default=0
9	<b>slewn.</b> Read-write. Reset: 0. Enable Changing Strength of pre-drive for fall time compensation by 25%. Slewn=1 Enabled, 0=disabled.
8:7	<b>fallslewsel.</b> Read-write. Reset: 0h. <b>Description:</b> 00= Standard Mode Tx Freq=100kHz) 01= low speed 12ns..120ns Frequency TX<1MHz (FM/FM+) 10= not used 11= not used
6	<b>pden.</b> Read-write. Reset: 0. Pull-down enable for 1=Enable 0=Disable
5:4	<b>i2crrsel.</b> Read-write. Reset: 3h. <b>Description:</b> i2cRxSel<1:0>=0b01 Schmitt trigger for 3.3V input i2cRxSel<1:0>=0b10 Schmitt trigger for 3.3V input i2cRxSel<1:0>=0b11 Schmitt trigger for 1.8V input i2cRxSel<1:0>=0b00 All receivers off.
3:0	<b>ng.</b> Read-write. Reset: Ch. N Strength Control

**MISCx000000EC (FCH::MISC::I2C5\_PADCTRL)**

Read-write. Reset: 0000\_003Ch.

This register is used to assist in controlling Pad BP\_I3C5\_SCL/BP\_I3C5\_SDA. Pad0 means BP\_I3C5\_SCL, Pad 1 means BP\_I3C5\_SDA.

\_aliasHOSTLEGACY; MISCx000000EC; MISC=FED8\_0E00h

Bits	Description
31:19	Reserved.
18:17	<b>spare.</b> Read-write. Reset: 0h. Spare Pin
16	<b>biascrten.</b> Read-write. Reset: 0. Pbias should be on in Fast/Fast+ Mode internally overridden to turn on by FallSlew setting, to save power can be turned off in I2C Standard Mode FallSlew=00
15	<b>rsel1p1.</b> Read-write. Reset: 0. When asserted increases resistance by 10% for all RC timers
14	<b>rsel0p9.</b> Read-write. Reset: 0. When asserted decreases resistance by 10% for all RC timers
13	<b>csel1p1.</b> Read-write. Reset: 0. When asserted increases capacitance by 10% for all RC timers
12	<b>csel0p9.</b> Read-write. Reset: 0. When asserted decreases capacitance by 10% for all RC timers
11	<b>spikercsel.</b> Read-write. Reset: 0. Select RC constant for I2C spike suppression, 0=50ns, 1=20ns
10	<b>spikercen.</b> Read-write. Reset: 0. Enable Rx spike suppression, default=0
9	<b>slewn.</b> Read-write. Reset: 0. Enable Changing Strength of pre-drive for fall time compensation by 25%. Slewn=1 Enabled, 0=disabled.
8:7	<b>fallslewsel.</b> Read-write. Reset: 0h. <b>Description:</b> 00= Standard Mode Tx Freq=100kHz) 01= low speed 12ns..120ns Frequency TX<1MHz (FM/FM+) 10= not used 11= not used
6	<b>pden.</b> Read-write. Reset: 0. Pull-down enable for 1=Enable 0=Disable
5:4	<b>i2crxsel.</b> Read-write. Reset: 3h. <b>Description:</b> i2cRxSel<1:0>=0b01 Schmitt trigger for 3.3V input i2cRxSel<1:0>=0b10 Schmitt trigger for 3.3V input i2cRxSel<1:0>=0b11 Schmitt trigger for 1.8V input i2cRxSel<1:0>=0b00 All receivers off.
3:0	<b>ng.</b> Read-write. Reset: Ch. N Strength Control

**MISCx000000F0 (FCH::MISC::CLKCNTRLF0)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISCx000000F0; MISC=FED8\_0E00h

Bits	Description
31:0	Reserved.

**MISCx000000F4 (FCH::MISC::CLKCNTRLF4)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISCx000000F4; MISC=FED8\_0E00h

Bits	Description
31:0	Reserved.

**MISCx000000F8 (FCH::MISC::TDR\_SECURITY\_STATUS)**

Read-only.

\_aliasHOSTLEGACY; MISCx000000F8; MISC=FED8\_0E00h

Bits	Description
31:22	Reserved.
21	<b>tdr_i3c_control_updated.</b> Read-only. Reset: X. Tdr_I3C_CONTROL_accessed
20	<b>tdr_ioconfig_updated.</b> Read-only. Reset: X. Tdr_S5IODIRCONFIG_accessed Tdr_S0IODIRCONFIG_accessed Tdr_S5IODIRAPPEND_accessed Tdr_S0IODIRAPPEND_accessed
19	<b>tdr_s5_clkconfig_updated.</b> Read-only. Reset: X. Tdr_S5_PLLDFTCONFIG_accessed Tdr_S5_PLLDFTSTS_accessed Tdr_S5_CLKDFTCONFIG_accessed
18	<b>tdr_sdio_control_updated.</b> Read-only. Reset: X. Tdr_SDIO_CONTROL_accessed
17	<b>tdr_i2c_control_updated.</b> Read-only. Reset: X. Tdr_I2C_CONTROL_accessed
16	<b>tdr_gpio_control_updated.</b> Read-only. Reset: X. Tdr_GPIO18_CONTROL_accessed Tdr_GPIO33_CONTROL_accessed
15	<b>tdr_iodftcfg_updated.</b> Read-only. Reset: X. Tdr_IODFTCFG_accessed
14	<b>tdr_spare_updated.</b> Read-only. Reset: X. Tdr_SPARE_accessed
13	<b>classb_tdr_updated.</b> Read-only. Reset: X. A TDR that is only enabled after Cpl_aeb_valid has been updated.
12	<b>s0stateobserve_tdr_updated.</b> Read-only. Reset: X. Tdr_S0STATEOBSERVE_accessed
11	<b>ila_tdr_updated.</b> Read-only. Reset: X. Tdr_ILA_accessed
10	<b>idcode_tdr_updated.</b> Read-only. Reset: X. Tdr_IDCODE_accessed   Tdr_PKGID_accessed
9	<b>scan_tdr_updated.</b> Read-only. Reset: X. Tdr_SYSSCAN_accessed   Tdr_SCANCONFIG_accessed
8	<b>sysdebug_tdr_updated.</b> Read-only. Reset: X. Tdr_SYSDEBUG_accessed
7	<b>sdb_tdr_updated.</b> Read-only. Reset: X. Tdr_SDB_CONFIG_accessed   Tdr_SDB_STATUS_accessed
6	<b>mbist_tdr_updated.</b> Read-only. Reset: X. Tdr_MBISTCONFIG_accessed   Tdr_MEMBISTSTS_accessed
5	<b>iotstcntrl_tdr_updated.</b> Read-only. Reset: X. Tdr_IOTSTCNTRL_accessed
4	<b>testclkdis_tdr_updated.</b> Read-only. Reset: X. Tdr_TESTCLKDIS_accessed
3	<b>ateconfig_tdr_updated.</b> Read-only. Reset: X. Tdr_ATECONFIG_accessed
2	<b>pll_clk_dft_tdr_updated.</b> Read-only. Reset: X. Tdr_PLLDFT_accessed   Tdr_CLKDFT_accessed
1	<b>acpi_tdr_updated.</b> Read-only. Reset: X. Tdr_ACPIJTAGCMD_accessed   Tdr_ACPIJTAGSTATUS_accessed
0	<b>any_tdr_updated.</b> Read-only. Reset: X. <b>Description:</b> Read-only. Set if any of the <a href="#">FCH</a> TDR are Updated (Dfx Security Feature) 0: No FCH TDR has been updated since RsmrstB was asserted 1: One or More FCH TDR registers have been updated

**MISCx000000FC (FCH::MISC::CLKGATING\_CNTRL)**

Read-write. Reset: FFFF\_FFFFh.

\_aliasHOSTLEGACY; MISCx000000FC; MISC=FED8\_0E00h

Bits	Description
31:27	Reserved.
26	<b>hpet64_tmr_clkgatingdis.</b> Read-write. Reset: 1. <b>Description:</b> 0: the clock of HPET64 Timer block can be stopped if not being Accessed 1: the clock of HPET64 Timer block can't be stopped.
25	<b>hpet32_tmr_clkgatingdis.</b> Read-write. Reset: 1. <b>Description:</b> 0: the clock of HPET32 Timer block can be stopped if not being Accessed 1: the clock of HPET32 Timer block can't be stopped.
24	<b>boot_tmr_clkgatingdis.</b> Read-write. Reset: 1. <b>Description:</b> 0: the clock of Boot Timer block can be stopped if not being Accessed 1: the clock of Boot Timer block can't be stopped.
23	<b>long_tmr_clkgatingdis.</b> Read-write. Reset: 1. <b>Description:</b> 0: the clock of Long Timer block can be stopped if not being Accessed 1: the clock of Long Timer block can't be stopped.
22	<b>shrt_tmr_clkgatingdis.</b> Read-write. Reset: 1. <b>Description:</b> 0: the clock of Short Timer block can be stopped if not being Accessed 1: the clock of Short Timer block can't be stopped.
21	<b>asf_clkgatingdis.</b> Read-write. Reset: 1. <b>Description:</b> 0: the clock of ASF block can be stopped if not being Accessed 1: the clock of ASF block can't be stopped.
20	<b>asf_clkgen_clkgatingdis.</b> Read-write. Reset: 1. <b>Description:</b> 0: the clock of ASF Clock Generator block can be stopped if not being Accessed 1: the clock of ASF Clock Generator block can't be stopped.
19	<b>shdw_syscnt_clkgatingdis.</b> Read-write. Reset: 1. <b>Description:</b> 0: the clock of Shadow System Counter block can be stopped if not being Accessed 1: the clock of Shadow System Counter block can't be stopped.
18	<b>acpi_msi_clkgatingdis.</b> Read-write. Reset: 1. <b>Description:</b> 0: the clock of ACPI MSI block can be stopped if not being Accessed. 1: the clock of ACPI MSI block can't be stopped.
17	<b>usb_legacy_clkgatingdis.</b> Read-write. Reset: 1. <b>Description:</b> 0: the clock of USB Legacy block can be stopped if not being Accessed. 1: the clock of USB Legacy block can't be stopped.
16	<b>isa_bridge_clkgatingdis.</b> Read-write. Reset: 1. <b>Description:</b> 0: the clock of ISA Bridge block can be stopped if not being Accessed. 1: the clock of ISA Bridge block can't be stopped.
15	<b>acpi_debug_clkgatingdis.</b> Read-write. Reset: 1. <b>Description:</b> 0: the clock of ACPI debug block can be stopped if not being Accessed. 1: the clock of ACPI debug block can't be stopped.
14	<b>tmr_8254_clkgatingdis.</b> Read-write. Reset: 1. <b>Description:</b> 0: the clock of 8254 timer block can be stopped if not being Accessed. 1: the clock of 8254 timer block can't be stopped.
13	<b>shdw_pcislave_clkgatingdis.</b> Read-write. Reset: 1. <b>Description:</b> 0: the clock of Shadow pcislave block can be stopped if not being Accessed. 1: the clock of Shadow pcislave block can't be stopped.
12	<b>watchdogtimerblk_clkgatingdis.</b> Read-write. Reset: 1. <b>Description:</b> 0: the clock of WatchDogTimer block can be stopped if not being Accessed. 1: the clock of WatchDogTimer block can't be stopped.

11	<b>acdctmrblk_clkgatingdis.</b> Read-write. Reset: 1. <b>Description:</b> 0: the clock of AcDcTmr block can be stopped if not being Accessed. 1: the clock of AcDcTmr block can't be stopped.
10	<b>biosramblk_clkgatingdis.</b> Read-write. Reset: 1. <b>Description:</b> 0: the clock of Bios Ram block can be stopped if not being Accessed. 1: the clock of Bios Ram block can't be stopped.
9:7	Reserved.
6	<b>obffblk_clkgatingdis.</b> Read-write. Reset: 1. <b>Description:</b> 0: the clock of OBFF block can be stopped if not being Accessed. 1: the clock of OBFF block can't be stopped.
5	<b>smbus0_clkgatingdis.</b> Read-write. Reset: 1. <b>Description:</b> 0: the clock of Smbus0 block can be stopped if not being Accessed. 1: the clock of Smbus0 block can't be stopped.
4	Reserved.
3	<b>aoacregblk_clkgatingdis.</b> Read-write. Reset: 1. <b>Description:</b> 0: the clock of Aoac register block can be stopped if not being Accessed. 1: the clock of Aoac register block can't be stopped.
2	<b>pmio2regblk_clkgatingdis.</b> Read-write. Reset: 1. <b>Description:</b> 0: the clock of Pmio2 register block can be stopped if not being Accessed. 1: the clock of Pmio2 register block can't be stopped.
1	<b>pmioregblk_clkgatingdis.</b> Read-write. Reset: 1. <b>Description:</b> 0: the clock of Pmio register block can be stopped if not being Accessed. 1: the clock of Pmio register block can't be stopped.
0	<b>miscregblk_clkgatingdis.</b> Read-write. Reset: 1. <b>Description:</b> 0: the clock of Misc register block can be stopped if not being Accessed. 1: the clock of Misc register block can't be stopped.



**11.3.9.2      Miscellaneous (MISC2) Registers**

**MISC2x00000000 (FCH::MISC2::RMT\_CLKCNTL\_0\_REG)**

Read-write. Reset: 1000\_CFFCh.

\_aliasHOSTLEGACY; MISC2x00000000; MISC2=FED8\_1300h

Bits	Description
31:12	Reserved.
11:10	<b>gpp_clk05_clock_request_mapping.</b> Read-write. Reset: 3h. <b>Description:</b> GPP05 PCIE clock pins (GPP_CLK05P/GPP_CLK05N) output control by CLKREQ05# (or CLKREQG#) pin GPP_CLK05P/GPP_CLK05N pins can be controlled (turn OFF, ON, CLKREQ05# controlled) by the following options. GPP05_CLKREQ_Mapping: 00 Off 01 CLKREQ05# 10 Off, reserved 11 On (default)
9:8	<b>gpp_clk03_clock_request_mapping.</b> Read-write. Reset: 3h. <b>Description:</b> GPP03 PCIE clock pins (GPP_CLK03P/GPP_CLK03N) output control by CLKREQ03# pin GPP_CLK03P/GPP_CLK03N pins can be controlled (turn OFF, ON, CLKREQ03# controlled) by the following options. GPP03_CLKREQ_Mapping: 00 Off 01 CLKREQ03# 10 Off, reserved 11 On (default) Note: MISC2x00000004[24] is an override bit which is XOR with GPP03_CLKREQ_Mapping.
7:6	<b>gpp_clk02_clock_request_mapping.</b> Read-write. Reset: 3h. <b>Description:</b> GPP02 PCIE clock pins (GPP_CLK02P/GPP_CLK02N) output control by CLKREQ02# pin eCLK Mode: Socket0/1 GPP02 is default with input mode. Cannot be controlled by these bits. But can be override by MISC2x00000004[12]. iCLK Mode: Socket0/1 GPP02 can be controlled (turn OFF, ON, CLKREQ02# controlled) by the following options. GPP02_CLKREQ_Mapping: 00 Off 01 CLKREQ02# 10 Off, reserved 11 On (default) Note: MISC2x00000004[12] is an override bit which is XOR with GPP02_CLKREQ_Mapping.
5:4	<b>gpp_clk04_clock_request_mapping.</b> Read-write. Reset: 3h. <b>Description:</b> GPP04 PCIE clock pins (GPP_CLK04P/GPP_CLK04N) output control by CLKREQ04# pin GPP_CLK04P/GPP_CLK04N pins can be controlled (turn OFF, ON, CLKREQ04# controlled) by the following options. GPP04_CLKREQ_Mapping: 00 Off 01 CLKREQ04# 10 Off, reserved 11 On (default) Note: MISC2x00000004[29] is an override bit which is XOR with GPP04_CLKREQ_Mapping.
3:2	<b>gpp_clk01_clock_request_mapping.</b> Read-write. Reset: 3h.

	<b>Description:</b> GPP01 PCIE clock pins (GPP_CLK01P/GPP_CLK01N) output control by CLKREQ01# pin GPP_CLK01P/GPP_CLK01N pins can be controlled (turn OFF, ON, CLKREQ01# controlled) by the following options. GPP01_CLKREQ_Mapping: 00 Off 01 CLKREQ01# 10 Off, reserved 11 On (default) Note: MISC2x00000004[9] is an override bit which is XOR with GPP01_CLKREQ_Mapping.
1:0	Reserved.

#### MISC2x00000004 (FCH::MISC2::RMT\_CLKCNTL\_1\_REG)

Read-write. Reset: 0000\_00F0h.

\_aliasHOSTLEGACY; MISC2x00000004; MISC2=FED8\_1300h

Bits	Description
31:0	Reserved.

#### MISC2x00000008 (FCH::MISC2::RMT\_CLKCNTL\_2\_REG)

Read-write. Reset: 1800\_1E00h.

\_aliasHOSTLEGACY; MISC2x00000008; MISC2=FED8\_1300h

Bits	Description
31:9	Reserved.
8	<b>cg2_refdivsrc_override.</b> Read-write. Reset: 0. <b>Description:</b> CG2PLL Refclk Source Select Override This bit is used to override CG2PLL refclk source select. By default, Master_die and Slave_die CG2PLL refclk source is from CG1PLL generated 100MHz. This bit shall be kept to default value. Note: Need to apply a reset after set this bit
7:5	Reserved.
4	<b>refclk_source_switch_mode.</b> Read-write. Reset: 0. <b>Description:</b> Refclk Source Switch Mode For CGPLL refclk source, it can be from either CG_XTAL or external reference source. Note: for CG2PLL, refclk source has no CG_XTAL connected. 0: Switch refclk source on-the-fly 1: Need to apply a Cold Reset for switching different refclk source
3:1	Reserved.
0	<b>cg2_spread_spectrum_enable.</b> Read-write. Reset: 0. <b>Description:</b> CG2_PLL Spread Spectrum Enable 0: Disable Spread Spectrum (default) 1: Enable Spread Spectrum

#### MISC2x0000000C (FCH::MISC2::RMT\_CLKCNTL\_3\_REG)

Read-write. Reset: 0000\_5555h.

\_aliasHOSTLEGACY; MISC2x0000000C; MISC2=FED8\_1300h

Bits	Description
31:0	Reserved.

**MISC2x00000010 (FCH::MISC2::RMT\_CLKCNTL\_4\_REG)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISC2x00000010; MISC2=FED8\_1300h

Bits	Description
31:30	Reserved.
29	<b>cg2pll_fracn_en_override.</b> Read-write. Reset: 0. Used with CG2PLL frac-N and <a href="#">SSC</a> clocking only.
28:13	Reserved.
12:4	<b>cg2pll_fcw0_int_override.</b> Read-write. Reset: 000h. CG2PLL Override: Integer portion of Frequency Control Word0 (a.k.a. feedback divisor0).
3:2	Reserved.
1:0	<b>cg2pll_refclk_div_override.</b> Read-write. Reset: 0h. <b>Description:</b> CG2PLL Override: Reference clock divisor. Settings: 2'b00=1 2'b01=2 2'b1x=4

**MISC2x00000014 (FCH::MISC2::RMT\_CLKCNTL\_5\_REG)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISC2x00000014; MISC2=FED8\_1300h

Bits	Description
31:24	Reserved.
23:8	<b>cg2pll_fcw1_frac_override.</b> Read-write. Reset: 0000h. CG2PLL Override: Fractional portion of Frequency Control Word1 (a.k.a. feedback divisor1). Intended to be used with frequency ramping. Also used to step PLL frequency and phase for DFT.
7:0	Reserved.

**MISC2x00000018 (FCH::MISC2::RMT\_CLKCNTL\_6\_REG)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISC2x00000018; MISC2=FED8\_1300h

Bits	Description
31:16	<b>cg2pll_fcw_slew_frac_override.</b> Read-write. Reset: 0000h. <b>Description:</b> CG2PLL Override: Sets <a href="#">SSC</a> freq ramp rate. Set fractional change in programmed frequency per refclk cycle. e.g. 0.5% downspread SSC at 33.3kHz and fbdiv=80. FCW_slewrates_frac = $216 * 0.00485 * 80 / (15\mu s / 10ns) = 17$ Need 31.5kHz and -0.375%
15:0	Reserved.

**MISC2x0000001C (FCH::MISC2::RMT\_CLKCNTL\_7\_REG)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISC2x0000001C; MISC2=FED8\_1300h

Bits	Description
31:28	Reserved.
27:26	<b>cgpll_gi_coarse_mant_override</b> . Read-write. Reset: 0h. CG2PLL Coarse integral path fp mult mantissa
25:21	Reserved.
20:17	<b>cg2pll_gp_coarse_exp_override</b> . Read-write. Reset: 0h. CG2PLL Override: Coarse proportional path fp mult exponent
16:13	<b>cg2pll_gp_coarse_mant_override</b> . Read-write. Reset: 0h. CG2PLL Override: Coarse proportional path fp mult mantissa
12:9	<b>cg2pll_gi_coarse_exp_override</b> . Read-write. Reset: 0h. CG2PLL Override: Coarse integral path fp mult exponent
8:0	Reserved.

**MISC2x00000020 (FCH::MISC2::RMT\_CLKDRVSTH\_0\_REG)**

Read-write.

\_aliasHOSTLEGACY; MISC2x00000020; MISC2=FED8\_1300h

Bits	Description
31:0	Reserved.

**MISC2x00000024 (FCH::MISC2::RMT\_CLKDRVSTH\_1\_REG)**

Read-write. Reset: 0024\_0249h.

\_aliasHOSTLEGACY; MISC2x00000024; MISC2=FED8\_1300h

Bits	Description
31:24	Reserved.
23:21	<b>gpp05_clock_buffer_driving_strength_control.</b> Read-write. Reset: 1h. <b>Description:</b> Drive Strength control for GPP05 differential Clock Buffers Drive strength addition/subtraction relative to IMP_CTRL[4:0]. 3'bx00 : ~ -10% 3'bx01 : no change from IMP_CTRL 3'bx10 : ~ +10% 3'bx11 : ~ + 20% Default: 3'b001
20:18	<b>gpp04_clock_buffer_driving_strength_control.</b> Read-write. Reset: 1h. <b>Description:</b> Drive Strength control for GPP04 differential Clock Buffers Drive strength addition/subtraction relative to IMP_CTRL[4:0]. 3'bx00 : ~ -10% 3'bx01 : no change from IMP_CTRL 3'bx10 : ~ +10% 3'bx11 : ~ + 20% Default: 3'b001
17:12	Reserved.
11:9	<b>gpp_clk03_clock_buffer_driving_strength_control.</b> Read-write. Reset: 1h. <b>Description:</b> Drive Strength control for GPP_CLK03 differential Clock Buffers Drive strength addition/subtraction relative to IMP_CTRL[4:0]. 3'bx00 : ~ -10% 3'bx01 : no change from IMP_CTRL 3'bx10 : ~ +10% 3'bx11 : ~ + 20% Default: 3'b001
8:6	<b>gpp_clk02_clock_buffer_driving_strength_control.</b> Read-write. Reset: 1h. <b>Description:</b> Drive Strength control for GPP_CLK02 differential Clock Buffers Drive strength addition/subtraction relative to IMP_CTRL[4:0]. 3'bx00 : ~ -10% 3'bx01 : no change from IMP_CTRL 3'bx10 : ~ +10% 3'bx11 : ~ + 20% Default: 3'b001
5:3	<b>gpp_clk01_clock_buffer_driving_strength_control.</b> Read-write. Reset: 1h. <b>Description:</b> Drive Strength control for GPP_CLK01 differential Clock Buffers Drive strength addition/subtraction relative to IMP_CTRL[4:0]. 3'bx00 : ~ -10% 3'bx01 : no change from IMP_CTRL 3'bx10 : ~ +10% 3'bx11 : ~ + 20% Default: 3'b001
2:0	<b>gpp_clk00_clock_buffer_driving_strength_control.</b> Read-write. Reset: 1h.

	<b>Description:</b> Drive Strength control for GPP_CLK00 differential Clock Buffers Drive strength addition/subtraction relative to IMP_CTRL[4:0]. 3'bx00 : ~ -10% 3'bx01 : no change from IMP_CTRL 3'bx10 : ~ +10% 3'bx11 : ~ + 20% Default: 3'b001
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#### MISC2x00000028 (FCH::MISC2::RMT\_CLKDRVSTH\_2\_REG)

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISC2x00000028; MISC2=FED8\_1300h

Bits	Description
31:0	Reserved.

#### MISC2x0000002C (FCH::MISC2::RMT\_CLKDRVSTH\_3\_REG)

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISC2x0000002C; MISC2=FED8\_1300h

Bits	Description
31:0	Reserved.

#### MISC2x00000030 (FCH::MISC2::RMT\_PLLCNTL\_0\_REG)

Read-write.

\_aliasHOSTLEGACY; MISC2x00000030; MISC2=FED8\_1300h

Bits	Description
31:4	Reserved.
3	<b>usb0_rtcclk_enb.</b> Read-write. Reset: 0. <b>Description:</b> USB0 RTCCLK (root_RTC_CLK_0) Enable/Disable 0: Turn on 1: Turn off
2	Reserved.
1:0	<b>pcie_phy_refclk_selection_override.</b> Read-write. Reset: XXb. <b>Description:</b> PCIE PHY Refclk Selection Override ( G-PHY) CLKB_PCIE_PHY_P/N 00 = 100MHz CG2_PLL generated (default) 01 = 100MHz CG2_PLL generated 10 = EXT_GPP0_SRC 11 = EXT_GPP2_RX Note: MISC2x000000BC[12] to select EXT_GPP0_SRC either is from GPP0 external input or GPP0 external input with divided-by-2 or divided-by-4

#### MISC2x00000034 (FCH::MISC2::RMT\_PLLCNTL\_1\_REG)

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISC2x00000034; MISC2=FED8\_1300h

Bits	Description
31:23	<b>cg2pll_fcw1_int_override.</b> Read-write. Reset: 000h. CG2PLL Override: Integer portion of Frequency Control Word0 (a.k.a. feedback divisor1). Intended to be used with frequency ramping. Also used to step PLL frequency and phase for DFT.
22:0	Reserved.

**MISC2x00000038 (FCH::MISC2::RMT\_PLLCNTL\_2\_REG)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISC2x00000038; MISC2=FED8\_1300h

Bits	Description
31:23	Reserved.
22:21	<b>cg2pll_external_refclk_sel_override.</b> Read-write. Reset: 0h. <b>Description:</b> CG2PLL External Refclk Selection Override This is the refclk mux source inside CLKGEN_S0. 00 = local GPP0_RX (external 100M) 01 = GPP2_RX 10 = CG2_100M 11 = remote GPP0_RX The MISC2x00000038[22:21] are override bits to this mux inside CLKGEN_S0. The local CLKGEN_S0 default is "00" in iCLK mode and "01" in eCLK mode. The remote CLKGEN_S0 default is "10" in iCLK mode and "01" in eCLK mode. For example: If we want to use external 100MHz as CG2PLL refclk source thru local GPP0_RX in eCLK mode, then program MISC2x00000038[22:21]="01". (default "01" XOR program MISC2x00000038[22:21]="01" = "00") If we want to use external 100MHz as CG2PLL refclk source thru remote GPP2_RX in iCLK mode, then program MISC2x00000038[22:21]="11". (default "10" XOR program MISC2x00000038[22:21]="11" = "01")
20:0	Reserved.

**MISC2x0000003C (FCH::MISC2::CGPLL\_CONFIGURATION)**

Read-write. Reset: 0000\_3310h.

\_aliasHOSTLEGACY; MISC2x0000003C; MISC2=FED8\_1300h

Bits	Description
31:0	Reserved.

**MISC2x00000040 (FCH::MISC2::RMT\_MISCCNTL\_0\_REG)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISC2x00000040; MISC2=FED8\_1300h

Bits	Description
31	Reserved.
30	<b>cg2_cfg_update_req.</b> Read-write. Reset: 0. <b>Description:</b> Set this bit will request CG2_PLL to load spread related value into CG2_PLL. The bit will be clear "0" by hardware after request send to CG2_PLL.
29:26	Reserved.
25	<b>cg2_fbdiv_loaden.</b> Read-write. Reset: 0. Set "1" to enable loading CG2_PLL FB_DIV value form register
24:0	Reserved.

**MISC2x00000044 (FCH::MISC2::RMT\_MISCCNTL\_1\_REG)**

Read-write. Reset: 0060\_0000h.

\_aliasHOSTLEGACY; MISC2x00000044; MISC2=FED8\_1300h

Bits	Description
31:0	Reserved.

**MISC2x00000048 (FCH::MISC2::RMT\_MISCCNTL\_2\_REG)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISC2x00000048; MISC2=FED8\_1300h

Bits	Description
31:0	Reserved.



**MISC2x0000004C (FCH::MISC2::RMT\_MISCCNTL\_3\_REG)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISC2x0000004C; MISC2=FED8\_1300h

Bits	Description
31:4	Reserved.
3	<b>pcie_phy_g_refclk_static_pwdn_cntl.</b> Read-write. Reset: 0. <b>Description:</b> PCIE_G_Set_PHY Refclk Driver Static PWDN Control 0: Enable on-chip driver (default) 1: Disable on-chip driver (if it is unused) When resume, it will be static shut-down with on-chip driver enable (default setting) regardless what has been programmed and BIOS needs to program it again.
2:0	Reserved.

**MISC2x00000058 (FCH::MISC2::RMT\_MISCCNTL58)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISC2x00000058; MISC2=FED8\_1300h

Bits	Description
31:0	Reserved.

**MISC2x0000005C (FCH::MISC2::RMT\_MISCCNTL5C)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISC2x0000005C; MISC2=FED8\_1300h

Bits	Description
31:0	Reserved.

**MISC2x00000060 (FCH::MISC2::IDLECNTRLCOPY)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISC2x00000060; MISC2=FED8\_1300h

Bits	Description
31:0	Reserved.

**MISC2x00000070 (FCH::MISC2::RMT\_CTRL0)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISC2x00000070; MISC2=FED8\_1300h

Bits	Description
31:2	Reserved.
1	<b>rst_usb_s5_rmt.</b> Read-write. Reset: 0. <b>Description:</b> Write '1' to make Cpl_VDDCR_S5_RESETh_rmt=0 to reset USB in remote tile. Need to write '0' to deassert Cpl_VDDCR_S5_RESETh=1. This bit is not for normal operation, it is to be used for recovery when something went wrong.
0	<b>mask_usb_s5_rst_rmt.</b> Read-write. Reset: 0. <b>Description:</b> Set to '1' to mask oDevAllRstB to gen Cpl_VDDCR_S5_RESETh_rmt =0 in remote tile to reset USB, default=0

**MISC2x000000A0 (FCH::MISC2::RMT\_CG1PLLCNTL\_0\_REG)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISC2x000000A0; MISC2=FED8\_1300h

Bits	Description
31:0	Reserved.

**MISC2x000000A4 (FCH::MISC2::RMT\_CG1PLLCNTL\_1\_REG)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISC2x000000A4; MISC2=FED8\_1300h**Bits Description**

31:0 Reserved.

**MISC2x000000A8 (FCH::MISC2::RMT\_CG1PLLCNTL\_2\_REG)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISC2x000000A8; MISC2=FED8\_1300h**Bits Description**

31:0 Reserved.

**MISC2x000000AC (FCH::MISC2::RMT\_CG1PLLCNTL\_3\_REG)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISC2x000000AC; MISC2=FED8\_1300h**Bits Description**

31:0 Reserved.

**MISC2x000000B0 (FCH::MISC2::RMT\_CG2PLLCNTL\_0\_REG)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISC2x000000B0; MISC2=FED8\_1300h**Bits Description**

31:0 Reserved.

**MISC2x000000B4 (FCH::MISC2::RMT\_CG2PLLCNTL\_1\_REG)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISC2x000000B4; MISC2=FED8\_1300h**Bits Description**

31:0 Reserved.

**MISC2x000000B8 (FCH::MISC2::RMT\_CG2PLLCNTL\_2\_REG)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISC2x000000B8; MISC2=FED8\_1300h**Bits Description**

31:0 Reserved.

**MISC2x000000BC (FCH::MISC2::RMT\_CG2PLLCNTL\_3\_REG)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISC2x000000BC; MISC2=FED8\_1300h

Bits	Description
31:28	Reserved.
27:26	<b>gpp5_refclk_selection_override.</b> Read-write. Reset: 0h. <b>Description:</b> GPP5 Refclk selection Override 00 = CG_PLL generated 100MHz 01 = CG2_PLL generated 100MHz (not a valid option) 10 = Reserved 11 = Ext_GPP0_SRC Note: MISC2x000000BC[13] to select EXT_GPP0_SRC either is from GPP0 external input or GPP0 external input with divided-by-2/divided-by-4
25:24	<b>gpp4_refclk_selection_override.</b> Read-write. Reset: 0h. <b>Description:</b> GPP4 Refclk selection Override 00 = CG_PLL generated 100MHz 01 = CG2_PLL generated 100MHz (not a valid option) 10 = Reserved 11 = Ext_GPP0_SRC Note: MISC2x000000BC[13] to select EXT_GPP0_SRC either is from GPP0 external input or GPP0 external input with divided-by-2/divided-by-4
23:22	<b>gpp3_refclk_selection_override.</b> Read-write. Reset: 0h. <b>Description:</b> GPP3 Refclk selection Override 00 = CG_PLL generated 100MHz 01 = CG2_PLL generated 100MHz (not a valid option) 10 = Reserved 11 = Reserved Note: MISC2x000000BC[13] to select EXT_GPP0_SRC either is from GPP0 external input or GPP0 external input with divided-by-2/divided-by-4
21:20	<b>gpp2_refclk_selection_override.</b> Read-write. Reset: 0h. <b>Description:</b> GPP2 Refclk selection Override 00 = CG_PLL generated 100MHz 01 = CG2_PLL generated 100MHz (not a valid option) 10 = Reserved 11 = Reserved Note: MISC2x000000BC[13] to select EXT_GPP0_SRC either is from GPP0 external input or GPP0 external input with divided-by-2/divided-by-4
19:18	<b>gpp1_refclk_selection_override.</b> Read-write. Reset: 0h. <b>Description:</b> GPP1 Refclk selection Override 00 = CG_PLL generated 100MHz 01 = CG2_PLL generated 100MHz (not a valid option) 10 = Reserved 11 = Reserved Note: MISC2x000000BC[13] to select EXT_GPP0_SRC either is from GPP0 external input or GPP0 external input with divided-by-2/divided-by-4
17:16	<b>gpp0_refclk_selection_override.</b> Read-write. Reset: 0h.

	<b>Description:</b> GPP0 Refclk selection Override 00 = CG2_PLL generated 100MHz 01 = CG2_PLL generated 100MHz (not a valid) 10 = GPP2_RX (GPP2_BOT) 11 = Reserved Note: MISC2x000000BC[12] to select EXT_GPP2_SRC either is from GPP2 external input or GPP2 external input with divided-by-2/divided-by-4
15	Reserved.
14	<b>clk_cgpll_ext_pwdn.</b> Read-write. Reset: 0. <b>Description:</b> CLK_CGPLL_EXT_PWDN Enable/Disable CGPLL external refclk source thru GPP0 input. 0 = enable 1 = disable
13	<b>ext_gpp0_refclk_sel.</b> Read-write. Reset: 0. <b>Description:</b> EXT_GPP0_REFCLK_SEL 0 = GPP0 external input 1 = GPP0 external input divided-by-2(div-2 or div-4 depend on MISC2x0000003C[1])
12	Reserved.
11	<b>ext_gpp1_refclk_sel.</b> Read-write. Reset: 0. <b>Description:</b> EXT_GPP1_REFCLK_SEL 0 = GPP1 external input 1 = GPP1 external input divided-by-2(div-2 or div-4 depend on MISC2x0000003C[3])
10	<b>smu_100m_refclk_driver_pwdn.</b> Read-write. Reset: 0. <b>Description:</b> SMU_100M Refclk Driver PWDN 0 = enable 1 = disable
9:0	Reserved.

#### MISC2x000000F0 (FCH::MISC2::RMT\_MISCCNTLF0)

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISC2x000000F0; MISC2=FED8\_1300h

Bits	Description
31:0	Reserved.

#### MISC2x000000F4 (FCH::MISC2::RMT\_MISCCNTLF4)

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; MISC2x000000F4; MISC2=FED8\_1300h

Bits	Description
31:0	Reserved.

### 11.3.9.3 Power Management (PM) Registers and Standard ACPI Registers

Table 192: ACPI MMIO Space Allocation

00FFh-0000h	<a href="#">SMBus</a> PCI configuration registers, see .
01FFh-0100h	Reserved.
02FFh-0200h	<a href="#">SMI</a> , see 11.3.3 [SMI Registers].
03FFh-0300h	PMIO and ACPI, see 11.3.9.3 [Power Management (PM) Registers and Standard ACPI Registers].
08FFh-0800h	
05FFh-0500h	BIOS RAM

06FFh-0600h	CMOS RAM
07FFh-0700h	CMOS
09FFh-0900h	ASF registers, see .
0AFFh-0A00h	SMBus registers, see .
0BFFh-0B00h	Watchdog registers, see 11.3.5 [Watchdog Timer (WDT) Registers].
0CFFh-0C00h	HPET, see 11.3.4 [High Precision Event Timer (HPET) Registers].
0DFFh-0D00h	IOMux, see 11.3.10.1 [IOMUX Registers].
0EFFh-0E00h	Miscellaneous registers, see 11.3.9.1 [Miscellaneous (MISC) Registers].
10FFh-1000h	Reserved.
11FFh-1100h	Reserved.
12FFh-1200h	Remote Tile GPIO+IOMUX, see 11.3.10.3 [REMOTE GPIO and IOMUX Registers].
13FFh-1300h	Remote CGPLL-MISC2, see 11.3.9.2 [Miscellaneous (MISC2) Registers].
14FFh-1400h	DP-VGA
19FFh-1500h	GPIO Registers, see 11.3.10.2 [GPIO Registers].
1BFFh-1B00h	Reserved.
1CFFh-1C00h	Reserved.
1DFFh-1D00h	Wake Device (AC DC timer), see 11.3.6 [Wake Alarm Device (AcDcTimer) Registers].
1EFFh-1E00h	Reserved.
1FFFh-1F00h	Reserved.

The way of accessing PM registers is through the direct mapping scheme. The direct mapping through Memory Mapped IO is 0xFED8\_03XX.

PMx00000000 (FCH::PM::DECODEEN)	
Read-write. Reset: E302_0B10h.	
_aliasHOSTLEGACY; PMx00000000; PM=FED8_0300h	
Bits	Description
31:30	<b>ioapicconfig.</b> Read-write. Reset: 3h. Set to 11 to improve IoApic latency
29	<b>hpet_msi_en.</b> Read-write. Reset: 1. Set to 1 to expose MSI cap in HPET Cap register..
28	<b>hpet_width_sel.</b> Read-write. Reset: 0. <b>Description:</b> 0: HPET is 32-bit 1: HPET is 64-bit
27:26	<b>watchdogoptions.</b> Read-write. Reset: 0h. Set to 00 for normal WatchDogTimer operation.
25:24	<b>watchdogfreq.</b> Read-write. Reset: 3h. <b>Description:</b> This registers define the clock frequency used by the WatchDogTimer 00: 32us 01: 10ms 10: 100ms 11: 1s
23:21	<b>asfclkssel.</b> Read-write. Reset: 0h. <b>Description:</b> The value controls the frequency of ASF master clock its definition is: 000: ~100kHz 001: ~200kHz 010: ~300kHz 011:~ 400kHz 100:~ 600kHz 101:~ 800kHz 110:~ 900kHz 111:~1MHz
20:19	<b>smbus0sel.</b> Read-write. Reset: 0h. <b>Description:</b> SmBus port selection. There is only one SMBUS engine controlling four SMBUS ports. This register routes the SMBUS engine to the desired port. 00: Port 0 (For SMBUS on the board) 01: Port 2 (Dedicated for <a href="#">TSI</a> polling)
18	<b>asfclkswitch.</b> Read-write. Reset: 0. Set to 1 to change ASF master clock from RTC(32k) to the clock defined in ASFClkSel of the same register.
17	<b>asfclkstretchen.</b> Read-write. Reset: 1. Set to 1 to enable clock stretching support.
16	<b>asfsmmasteren.</b> Read-write. Reset: 0. Set to 1 to enable ASF SMBUS master function.
15:8	<b>smbusasfiobase.</b> Read-write. Reset: 0Bh. <b>Description:</b> Smbus Io base = {Smbus0AsfIoBase[7:0], 0x00} ASF Io base = {Smbus0AsfIoBase[7:0], 0x20} By default Smbus Io base is 0xB00 and ASF Io base is 0xB20
7	<b>watchdogtmren.</b> Read-write. Reset: 0. Set to 1 to enable WatchDog Timer memory(FEB00000 ~ FEB00003) decoding, and enable WatchDog Timer operation.
6	<b>hpeten.</b> Read-write. Reset: 0. Set to 1 to enable HPET memory(FED00000 ~ FED001FF) decoding.
5	<b>ioapicen.</b> Read-write. Reset: 0. Set to 1 to enable IoApic memory(FEC00000 ~ FEC0007F) decoding.
4	<b>smbusasfioen.</b> Read-write. Reset: 1. Set to 1 to enable Smbus and Asf Io decoding. Smbus and Asf Io range are defined in Smbus0AsfIoBase.
3	<b>dmaport80.</b> Read-write. Reset: 0. Set to 1 to pass Io port 0x80, 0x81, 0x82, 0x83 to legacy Dma Io range.
2	<b>legacydmaioen.</b> Read-write. Reset: 0. Set to 1 to enable legacy Dma Io range.
1	<b>cf9ioen.</b> Read-write. Reset: 0. Set to 1 to enable CF9 Io port decoding
0	<b>legacyioen.</b> Read-write. Reset: 0.

<b>Description:</b> Set to 1 to enable the following Io decoding: 0x20, 0x21, 0xA0, 0xA1 (PIC) 0x40, 0x41, 0x42, 0x43, 0x61 (8254 timer) 0x70, 0x71, 0x72, 0x73 (Rtc) 0x92
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**PMx00000004 (FCH::PM::ISACONTROL)**

Read-write.

PrtcControl registers are reset by RsmRstB and UsrRstB. RsmRstB is asserted during G3 state. UsrRstB is asserted when the system reset button is pressed (in S0 state). dPassEnable will be 0 during G3 state so that when S5 power is down, the invalid values of PrtcControl Registers will be isolated to 0 for PRTC.

One important requirement is:

Rtc32kHz clock's availability should not have any dependency with the PrtcControl Registers. This is because we use Rtc32kHz clock for various reset de-bounce logics including the reset for PrtcControl Registers.

\_aliasHOSTLEGACY; PMx00000004; PM=FED8\_0300h

Bits	Description
31	<b>rtc_bg_adj5.</b> Read-write. Reset: 0. PRTC band-gap control bit
30	<b>rtc_bg_adj4.</b> Read-write. Reset: 0. PRTC band-gap control bit
29	<b>rtc_bg_adj3.</b> Read-write. Reset: 0. PRTC band-gap control bit
28	<b>rtc_bg_adj2.</b> Read-write. Reset: 0. PRTC band-gap control bit
27	<b>rtc_bg_adj1.</b> Read-write. Reset: 0. PRTC band-gap control bit
26	<b>rtc_bg_adj0.</b> Read-write. Reset: 0. PRTC band-gap control bit
25	<b>rtc_bg_set_en.</b> Read-write. Reset: 0. <b>Description:</b> This is the enable for the PRTC 32kHz band-gap control bits (rtc_bg_adj0~5). 0: PRTC band-gap uses its own hard-wired configuration. 1: PRTC band-gap uses the rtc_bg_adj* bits.
24	<b>rtc_high_res.</b> Read-write. Reset: 0. Debug purpose register requested by PRTC designer.
23:22	Reserved.
21	<b>rtc_osc_op1.</b> Read-write. Reset: 0. PRTC oscillator control bit
20	<b>rtc_osc_op0.</b> Read-write. Reset: 0. PRTC oscillator control bit
19	<b>rtc_osc_set1.</b> Read-write. Reset: 0. PRTC oscillator control bit
18	<b>rtc_osc_set0.</b> Read-write. Reset: 0. PRTC oscillator control bit
17	<b>rtc_osc_set_en.</b> Read-write. Reset: 0. This is the latch enable for the PRTC 32kHz oscillator control bits (rtc_osc_set0~1, rtc_osc_op0~1).
16	<b>abclkgateen.</b> Read-write. Reset: 0. <b>Description:</b> Master switch for Alink and Blink clock gating. 0: Disabled 1: Enabled
15	<b>pm_lock_iomux.</b> Read-write. Reset: 0. Set to 1 to lock all IOMUX registers from write, once set to =1, this bit cannot be written 0. This bit is reset by PCIReset.
14:12	Reserved.
11	<b>f.</b> Read-write. Reset: 0. Legacy BM_REQ# function enable bit it is now for debug purpose only.
10	Reserved.
9	<b>drqmasken.</b> Read-write. Reset: 0. Set to 1 to allow DMA DRQ input to block clock gating
8	<b>dmaenhanceen.</b> Read-write. Reset: 0. Set to 1 to enable enhancement of legacy Dma.
7:6	Reserved.
5	<b>read_shadow.</b> Read-write. Reset: 0. Set to 1 to allow to read Pic ICWX, OCWX register through Io port 21h/A1h.
4:2	Reserved.
1	<b>mmioen.</b> Read-write. Reset: 1. Set to 1 to enable Acpi Mmio range (FED8_0000 ~FED8_1FFF). The space is allocated as specified in Table shows the Address mapping of each ACPI block in front of register PM_regx00
0	<b>biosramen.</b> Read-write. Reset: 0. Set to 1 to enable bios Ram whose base is FED1_0000 (256 bytes)



**PMx00000008 (FCH::PM::PCICONTROL)**

Read-write.

SLP\_TYP is located in AcpiPm1CntBlk offset 00h, bits 10~12.

\_aliasHOSTLEGACY; PMx00000008; PM=FED8\_0300h

Bits	Description
31:26	Reserved.
25	<b>force_slpstate_retry.</b> Read-write. Reset: 0. Set to 1 to send out <a href="#">SMI</a> message before the completion response of IO write to SLP_TYP register. This is to be used in conjunction with SMI trapping on write to SLP_TYP register
24	<b>force_stpclk_retry.</b> Read-write. Reset: 1. <b>Description:</b> Set to 1 to send out STPCLK message before the completion response of the following 3 types of request: I/O write to Slp_typ register I/O write Ldt_stp command C1e cycle Normally it is required to send out STPCLK before completion of the cycles listed above, except for the case of <a href="#">SMI</a> trapping. In that case, this bit should be left as 0
23:21	Reserved.
20	<b>shutdownoption.</b> Read-write. Reset: 0. <b>Description:</b> 0: Issue Init message upstream when receiving shutdown message. 1 : Generate Pci reset when receiving shutdown message.
19	<b>masternowait.</b> Read-write. Reset: 1. <b>Description:</b> 1: ACPI PCI Master doesn't wait for Slave idle when it wants to request bus. 0: Old behavior. PCI Master will wait for Slave idle. Note: Software need keep this bit to 1. In rare case, if there is downstream cycle to ACPI register (from CPU/ <a href="#">SMN</a> /M2P) and there is upstream Interrupt message pending, state machine will lock up if this bit is not set to 1.
18	<b>echostfix.</b> Read-write. Reset: 1. Not used.
17	<b>changedma.</b> Read-write. Reset: 0. Not used.
16	<b>gatedma.</b> Read-write. Reset: 0. Not used.
15	<b>clock_slow_mask.</b> Read-write. Reset: 0. Not used.
14:12	<b>ext_intr_time.</b> Read-write. Reset: 0h. Specify the extended interrupt time in 2 microsecond intervals. This is used for preventing APU from re-entering C state right away when it just breaks out from a C state
11	<b>dly_en.</b> Read-write. Reset: 0. Not used.
10	<b>ignr_usb_smi_req.</b> Read-write. Reset: 1. Not used.
9	<b>block_acpi_s5_intr_st.</b> Read-write. Reset: 0. Set to 1, it will block the acpi_s5 interrupt status to send out.
8	<b>pic_apic_arbiter.</b> Read-write. Reset: 1. Set to 1 to arbitrate between PIC request and IOAPIC request
7	<b>force_smaf_match.</b> Read-write. Reset: 0. Set to 1 to enable STPGNT message matching to the expected SMAF.
6	<b>nmimsgsel.</b> Read-write. Reset: 0. <b>Description:</b> 0: Encode NMI request as legacy PIC NMI message type. 1: NMI request as NMI message type.
5	<b>picmsgsel.</b> Read-write. Reset: 0. <b>Description:</b> 0: Encode PIC interrupt request as Legacy PIC ExtInt message type 1: encode PIC interrupt request as ExtInt message type
4	<b>msg_intr_enable.</b> Read-write. Reset: 0. Set to 1 to deliver legacy PIC interrupt as message type.
3	Reserved.
2	<b>fake_dma_en.</b> Read-write. Reset: 0. Not used
1	<b>undo_wrtd_done.</b> Read-write. Reset: 0. Not used
0	<b>undo_dma_change.</b> Read-write. Reset: 0. Not used

**PMx0000000C (FCH::PM::STPCLKSMAF)**

Read-write. Reset: 5543\_2106h.

\_aliasHOSTLEGACY; PMx0000000C; PM=FED8\_0300h

Bits	Description
31	Reserved.
30:28	<b>ttsmmaf.</b> Read-write. Reset: 5h. System management action field for Thermal Throttling STPCLK message
27	Reserved.
26:24	<b>nssmaf.</b> Read-write. Reset: 5h. System management action field for Normal Throttling STPCLK message
23	Reserved.
22:20	<b>s3smmaf.</b> Read-write. Reset: 4h. System management action field for S3 STPCLK message
19	Reserved.
18:16	<b>s1smmaf.</b> Read-write. Reset: 3h. System management action field for S1 STPCLK message
15	Reserved.
14:12	<b>vfsmaf.</b> Read-write. Reset: 2h. System management action field for VFID STPCLK message
11	Reserved.
10:8	<b>c3smmaf.</b> Read-write. Reset: 1h. System management action field for C3 STPCLK message
7	Reserved.
6:4	<b>c2smmaf.</b> Read-write. Reset: 0h. System management action field for C2 STPCLK message
3	Reserved.
2:0	<b>s4s5smmaf.</b> Read-write. Reset: 6h. System management action field for S4/5 STPCLK message

**PMx00000010 (FCH::PM::PWRRSTCFG)**

Read-write.

\_aliasHOSTLEGACY; PMx00000010; PM=FED8\_0300h

Bits	Description
15:7	Reserved.
6	<b>fatalrsttos5rst.</b> Read-write. Reset: 1.
5	<b>rtclkchken_s5reg.</b> Read-write. Reset: 1. <b>Description:</b> 0: RtcClkChk function is disabled 1: RtcClkChk function depends on the strap pin. If the strapped value is 1, RtcClkChk function is enabled. The strap name is RtcClkChkEn_strap.
4	<b>slps3waitrstasrt.</b> Read-write. Reset: 1. Debug purpose
3:2	<b>rstblksel_1_0.</b> Read-write. Reset: 1h. <b>Description:</b> 00: Always use old logic for reset signals. 01: Use new logic for reset signals during Power saving mode entry/exit, otherwise, use old logic. 10: Always use new logic for reset signals. 11: Always use new logic for reset signals. Note: Old logic: fch_pwr_detect New logic: fch_PwrRst
1	<b>toggleallpwrgoodoncf9.</b> Read-write. Reset: 0. <b>Description:</b> 1: De-assert and then assert all PwrGood signals (for PG1, PG1a, PG2 and XHC) during CF9 reset. 0: During CF9 reset, PG1_PwrGood stay at high. PG1a_PwrGood, PG2_PwrGood and Xhc_PwrGood behavior depend on TogglePG1aPG2PGXHConCf9 register bit during CF9 reset.
0	<b>togglepg1apg2pgxhconcf9.</b> Read-write. Reset: 1. <b>Description:</b> 1: De-assert and then assert PG1a_PwrGood, PG2_PwrGood and Xhc_PwrGood during CF9 reset. 0: PG1a_PwrGood, PG2_PwrGood and Xhc_PwrGood stay at high during CF9 reset.

**PMx00000012 (FCH::PM::FCHPWRGOODTMR)**

Read-write.

\_aliasHOSTLEGACY; PMx00000012; PM=FED8\_0300h

Bits	Description
15:11	Reserved.
10:0	<b>fchpwrgoodtmr</b> . Read-write. Reset: 150h. T1, Debouncetimer value for FCHPwrGood, and the delay timer value for PwrRstB deassertion of devices in PG1. For 300X mode, default = 0x14

**PMx00000014 (FCH::PM::PGPWRGOODTOALLENTMR)**

Read-write.

\_aliasHOSTLEGACY; PMx00000014; PM=FED8\_0300h

Bits	Description
15:11	Reserved.
10:0	<b>pgpwrgoodtoallentmr</b> . Read-write. Reset: 016h. <b>Description:</b> T18, Timer for PwrGood to AllEn for all the tiles. For 300X mode, default = 0x08

**PMx00000016 (FCH::PM::PGPWRGOODASSERTIONTMR)**

Read-write.

\_aliasHOSTLEGACY; PMx00000016; PM=FED8\_0300h

Bits	Description
15:11	Reserved.
10:0	<b>pgpwrgoodassertiontmr</b> . Read-write. Reset: 020h. <b>Description:</b> T19, Timer for DebouncedPwrGood to PwrGood of all the tiles, For 300X mode, default = 0x10

**PMx00000018 (FCH::PM::PWRGATETMR)**

Read-write. Reset: A864\_8642h.

\_aliasHOSTLEGACY; PMx00000018; PM=FED8\_0300h

Bits	Description
31:28	<b>pwrilanddaughterassertiontmr</b> . Read-write. Reset: Ah. T24, Timer for PwrOn=0 to Daughter_SD=1 of PG1a
27:24	<b>pwrilandmotherassertiontmr</b> . Read-write. Reset: 8h. T23, Timer for PwrOn=0 to Mother_SD=1 of PG1a
23:20	<b>pwrilandmemdaughterassertiontmr</b> . Read-write. Reset: 6h. T22, Timer for PwrOn=0 to Mem_Daughter_SD=1 of PG1a
19:16	<b>pwrilandmemmotherassertiontmr</b> . Read-write. Reset: 4h. T21, Timer for PwrOn=0 to Mem_Mother_SD=1 of PG1a
15:12	<b>pwrilandmemmotherdeassertiontmr</b> . Read-write. Reset: 8h. T17, Timer for PwrOn=1 to Mem_Mother_SD=0 of PG1a
11:8	<b>pwrilandmemdaughterdeassertiontmr</b> . Read-write. Reset: 6h. T16, Timer for PwrOn=1 to Mem_Daughter_SD=0 of PG1a
7:4	<b>pwrilandmotherdeassertiontmr</b> . Read-write. Reset: 4h. T15, Timer for PwrOn=1 to Mother_SD =0 of PG1a
3:0	<b>pwrilanddaughterdeassertiontmr</b> . Read-write. Reset: 2h. T14, Timer for PwrOn=1 to Daughter_SD =0 of PG1a

**PMx0000001C (FCH::PM::PLLSTBTMR)**

Read-write.

\_aliasHOSTLEGACY; PMx0000001C; PM=FED8\_0300h

Bits	Description
15:11	Reserved.
10:0	<b>pllrstbtmr</b> . Read-write. Reset: 040h. Delay timer value for PllRstB deassertion. For 300X mode, default = 0x01

**PMx0000001E (FCH::PM::PLLLOCKTMR)**

Read-write.

\_aliasHOSTLEGACY; PMx0000001E; PM=FED8\_0300h

Bits	Description
15:11	Reserved.
10:0	<b>plllocktmr</b> . Read-write. Reset: 03Ch. Delay timer value for PllLock assertion. For 300X mode, default = 0x04

**PMx00000020 (FCH::PM::PCIRSTBTMR)**

Read-write.

\_aliasHOSTLEGACY; PMx00000020; PM=FED8\_0300h

Bits	Description
15:11	Reserved.
10:0	<b>pcirstbtmr</b> . Read-write. Reset: 120h. Delay timer value for PciRstB deassertion. For 300X mode, default = 0x28

**PMx00000022 (FCH::PM::CPURSTBTMR)**

Read-write.

\_aliasHOSTLEGACY; PMx00000022; PM=FED8\_0300h

Bits	Description
15:11	Reserved.
10:0	<b>cpurstbtmr</b> . Read-write. Reset: 19Ch. Delaytimer value for CpuRstB deassertion. For 300X mode, default = 0x3C

**PMx00000024 (FCH::PM::NBPWRGOODTMR)**

Read-write.

\_aliasHOSTLEGACY; PMx00000024; PM=FED8\_0300h

Bits	Description
15:11	Reserved.
10:0	<b>nbpwrgoodtmr</b> . Read-write. Reset: 0A0h. Delay timer value for NBPwrGood assertion

**PMx00000026 (FCH::PM::CPUPWRGOODTMR)**

Read-write.

\_aliasHOSTLEGACY; PMx00000026; PM=FED8\_0300h

Bits	Description
15:11	Reserved.
10:0	<b>cpupwrgoodtmr</b> . Read-write. Reset: 0E0h. <b>Description:</b> Delay timer value for CpuPwrGood assertion, For 300X mode, default = 0x08

**PMx00000028 (FCH::PM::S0TOS5ENTMR)**

Read-write.

\_aliasHOSTLEGACY; PMx00000028; PM=FED8\_0300h

Bits	Description
15:11	Reserved.
10:0	<b>s0tos5entmr</b> . Read-write. Reset: 055h. T12, timer for DebouncedPwrGood=1 to S5TilePwrMux=1, PwrGoodOsc=0 to xSLP_S3_/xSLP_S5_=0

**PMx0000002A (FCH::PM::S5TOS0ENTMR)**

Read-write.

\_aliasHOSTLEGACY; PMx0000002A; PM=FED8\_0300h

Bits	Description
15:11	Reserved.
10:0	<b>s5tos0entmr</b> . Read-write. Reset: 010h. T3, timer for DebouncedPwrGood=1 to S5_ToAllEn=1

**PMx0000002C (FCH::PM::SLPRSTTMR)**

Read-write.

\_aliasHOSTLEGACY; PMx0000002C; PM=FED8\_0300h

Bits	Description
15:11	Reserved.
10:0	<b>slprsttmr</b> . Read-write. Reset: 080h. T13, Timer for S3/S5 Sleep Reset pulse width

**PMx0000002E (FCH::PM::OVERRIDEDEVSTTMR)**

Read-write.

\_aliasHOSTLEGACY; PMx0000002E; PM=FED8\_0300h

Bits	Description
15:12	Reserved.
11:8	<b>overriderstbtmr</b> . Read-write. Reset: 0h. Override Default RstBTmr for device resets
7:4	<b>overrideefclkoktmr</b> . Read-write. Reset: 0h. Override Default RefClkOkTmr for device resets
3:0	<b>overridepwrstbtmr</b> . Read-write. Reset: 0h. Override Default PwrRstBTmr for device resets

**PMx00000030 (FCH::PM::OVERRIDEPWRRSTBASRTTMR)**

Read-write.

\_aliasHOSTLEGACY; PMx00000030; PM=FED8\_0300h

Bits	Description
15:11	Reserved.
10:0	<b>overridepwrstbasrttmr</b> . Read-write. Reset: 000h. Override Default PwrRstBASrtTmr for device resets

**PMx00000032 (FCH::PM::OVERRIDEREFCLKOKDSRTTMR)**

Read-write.

\_aliasHOSTLEGACY; PMx00000032; PM=FED8\_0300h

Bits	Description
15:11	Reserved.
10:0	<b>overrideefclkokdsrttmr</b> . Read-write. Reset: 000h. Override Default RefClkOkDsrTmr for device resets

**PMx00000034 (FCH::PM::OVERRIDEENABLE)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; PMx00000034; PM=FED8\_0300h

Bits	Description
31:0	<b>overrideenable</b> . Read-write. Reset: 0000_0000h. Enable DevRst block timing override. Each bit enables the override for a device's DevRst block. When the bit is 1, the corresponding device's DevRst block will use the timing defined in PM_Reg:2E~33h, instead of the original hardwired values.

**PMx00000038 (FCH::PM::DEVST\_RSTBONLY)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; PMx00000038; PM=FED8\_0300h

Bits	Description
31:0	<b>devrst_rstbonly</b> . Read-write. Reset: 0000_0000h. Each bit is corresponding to a device's DevRst block. This is for debug purpose. When a bit is set 1, the corresponding device's PwrRsB and RefClkOk will be identical with RstB. When the bit is 0, the device's resets have default behaviors. Please refer to FCH_AOAC_Design_Specification for detail reset sequence and timing.

**PMx0000003C (FCH::PM::S0RESETTMR)**

Read-write.

\_aliasHOSTLEGACY; PMx0000003C; PM=FED8\_0300h

Bits	Description
15:12	Reserved.
11:0	<b>s0resettmr.</b> Read-write. Reset: 800h. <b>Description:</b> Timer value for S0ResetB For 300X mode, default = 0x83

**PMx0000003E (FCH::PM::PWRRSTCNFG)**

Read-write. Reset: E601h.

\_aliasHOSTLEGACY; PMx0000003E; PM=FED8\_0300h

Bits	Description
15:8	<b>osc16usinterval.</b> Read-write. Reset: E6h. In decimal 230 (or 16us) by default. It is used to set the Osc16Us counter limit. It is the base timer tick to increment various reset counter. Whenever we should enter into Power saving mode, <a href="#">PMFW</a> can change Osc16UsInterval to a smaller value. Upon Power saving mode exit, it can change it back to the default value.
7	Reserved.
6	<b>keep_warmrst_bf_mp1_ack.</b> Read-write. Reset: 0. <b>Description:</b> 0: warm reset sequence does not wait for MP1_WarmResetAck when en_MP1_WarmResetAck (PMx70[0]) =1 1: warm reset sequence waits for MP1_WarmResetAck indefinitely when en_MP1_WarmResetAck (PMx70[0]) =1
5:4	Reserved.
3	<b>en_coldrst_mp1ack.</b> Read-write. Reset: 0. <b>Description:</b> Before set this bit =1, PMx70[0]: en_MP1_WarmResetAck need be set =1 first. This bit is reset by RsmRstB. 0: Cold Reset is not blocked by MP1_WarmResetAck protocol 1: Cold Reset is blocked by MP1_WarmResetAck protocol
2	<b>smerr_l_en.</b> Read-write. Reset: 0. <b>Description:</b> The output enable of SMERR_L. 1: SMERR_L pad is output mode, 0: SMERR_L pad is input mode.
1	<b>en_mp1_warmresetack2.</b> Read-write. Reset: 0. <b>Description:</b> Chiken bit to select the gated iOsc16Us. 1: select the gated iOsc16Us by warm_rst_block_noncpu_rst which synced to osc clock domain. 0: select the original iOsc16Us.
0	<b>encpuwaitdev.</b> Read-write. Reset: 1. <b>Description:</b> 0: PwrRst block doesn't wait for non-D3 devices RstB de-assertion before it de-asserts CpuRstB. 1: PwrRst block will wait until all non-D3 devices RstB are de-asserted, and then de-assert CpuRstB. Note: "non-D3 devices" refer to those devices that are not currently in D3.

**PMx00000040 (FCH::PM::ESPIINTRCTRL)**

Read-write. Reset: 00FF\_FFFFh.

\_aliasHOSTLEGACY; PMx00000040; PM=FED8\_0300h

Bits	Description
31:24	Reserved.
23:0	<b>espidvintrmask.</b> Read-write. Reset: FF_FFFFh. <b>Description:</b> SW can set these bits to mask of eSPI Device IRQ23~0. 1: Mask off the interrupt 0: No mask

**PMx00000044 (FCH::PM::BOOTTIMEREN)**

Reset: 1E00\_0000h.

\_aliasHOSTLEGACY; PMx00000044; PM=FED8\_0300h

Bits	Description
31	<b>boottmrdisable.</b> Read-write. Reset: 0. Set to 1 to stop boot timer. Once set it to 1, timer will reset back to 0. When this bit is set back to 0, timer starts counting from 0. This bit will clear itself on any reset (this bit is non-sticky).
30	<b>failbootrststs.</b> Read-write, Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: Boot timer has not been fired. 1: Boot timer has been fired. Write 1 to clear it to 0.
29	<b>expireboottmr.</b> Read-write. Reset: 0. Set to 1 to force boot timer to expire then, NB PwrGood can be asserted.
28	<b>boottmrstopongalink.</b> Read-write. Reset: 1. Set to 1 to stop boot timer when <a href="#">FCH</a> observes the good boot after PCI reset.
27	<b>boottmrfuncen.</b> Read-write. Reset: 1. <b>Description:</b> 0: Disable boot timer function. 1: Enable boot timer function. The boot timer will start to count down and toggle NBPwrGood after 1.26s ( $2^{24}/(66.6M/5)$ ) if SW has not set the bit 29 to 1 after PCI reset or resuming from S3/S4/S5. This bit is persistent through any reset or sleep (this bit is sticky).
26:25	<b>boottmrdivsel.</b> Read-write. Reset: 3h. <b>Description:</b> Select the Fail Boot Timer limit. 00b: 1.26 Second, using Divide_by_5, 01b: 2.26 Second, using Divide_by_9 10b: 3.26 Second, using Divide_by_13 11b: 4.26 Second, using Divide_by_17, default for server, which need longer delay
24:0	<b>failboottimer.</b> Read-write. Reset: 000_0000h. <b>Description:</b> Read Only. The counter of APU Boot timer (66.6MHz/5), which starts counting when all of the the following conditions are met: Bit31 of this register =0 Bit27 of this register =1 PCI reset is not asserted. Set bit31=1 will stop the timer and reset timer back to 0, it will count from 0 again if bit31 is set back to 0, bit31 is a non-sticky bit and will get clear to 0 on any reset. Set bit27=0 will disable timer permanently because bit27 is a sticky bit. Bit27 will reset back to 1 if there is a S5 power loss or it can be written back to 1 by software. The timer itself cannot be written directly. It will reset back to 0 whenever bit31=1 or bit27=0 or a reset has occurred.

**PMx00000048 (FCH::PM::PGPWRENDLY)**

Read-write. Reset: 5935\_2B21h.

\_aliasHOSTLEGACY; PMx00000048; PM=FED8\_0300h

Bits	Description
31:24	<b>pg1pwrdownldlytmr.</b> Read-write. Reset: 59h. PG1 Power Down delay timer
23:16	<b>xhcpwrendlytmr.</b> Read-write. Reset: 35h. XhcPwrEn delay timer
15:8	<b>pg2pwrendlytmr.</b> Read-write. Reset: 2Bh. PG2PwrEn delay timer
7:0	<b>pg1apwrendlytmr.</b> Read-write. Reset: 21h. PG1aPwrEn delay timer, For 300X mode, default = 0x18

**PMx0000004C (FCH::PM::I2CINPUTTHRESHOLD)**

Read-write. Reset: 493F\_0000h.

\_aliasHOSTLEGACY; PMx0000004C; PM=FED8\_0300h

Bits	Description
31:24	<b>gbepwrendlytmr.</b> Read-write. Reset: 49h. GbePwrEn delay timer
23:16	<b>otgpwrendlytmr.</b> Read-write. Reset: 3Fh. OtgPwrEn delay timer
15:6	Reserved.
5	<b>i2c5inputthresholdhi.</b> Read-write. Reset: 0. <b>Description:</b> Configure I2C5 input threshold 0: Low threshold 1: High threshold
4	<b>i2c4inputthresholdhi.</b> Read-write. Reset: 0. <b>Description:</b> Configure I2C4 input threshold 0: Low threshold 1: High threshold
3	<b>i2c3inputthresholdhi.</b> Read-write. Reset: 0. <b>Description:</b> Configure I2C3 input threshold 0: Low threshold 1: High threshold
2	<b>i2c2inputthresholdhi.</b> Read-write. Reset: 0. <b>Description:</b> Configure I2C2 input threshold 0: Low threshold 1: High threshold
1	<b>i2c1inputthresholdhi.</b> Read-write. Reset: 0. <b>Description:</b> Configure I2C1 input threshold 0: Low threshold 1: High threshold
0	<b>i2c0inputthresholdhi.</b> Read-write. Reset: 0. <b>Description:</b> Configure I2C0 input threshold 0: Low threshold 1: High threshold

**PMx00000050 (FCH::PM::APUPLLCTRL)**

Read-write. Reset: 3F3E\_0000h.

\_aliasHOSTLEGACY; PMx00000050; PM=FED8\_0300h

Bits	Description
31:24	<b>apupllrstbtmr.</b> Read-write. Reset: 3Fh. Configure the PllLock assertion time. Unit is 16usec.
23:16	<b>apupllpwrrstbtmr.</b> Read-write. Reset: 3Eh. Configure the PllRstB deassertion time. Unit is 16usec.
15:2	Reserved.
1	<b>vidchg_use_newscheme.</b> Read-write. Reset: 0. <b>Description:</b> 0: old scheme, 8xPcick wide VIDCHG_req generated when wakeup from Clock slow down or Clock stop 1: new scheme, while in Clock slow down or Clock stop, VIDCHG_req assert =1 when receiving wakeup signal, VIDCHG_req deassert =0 after receiving VIDCHG_ack =1, VIDCHG_ack will deassert =0 after seeing VIDCHG_req =0
0	<b>apupllctrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable 1: Enable APU to power down CGPLL (Clock stop) or slow down clock (Clock slow down) When this bit is 1, ApuPllOffReq or ClockSlowDown_req bit in AOAC_Reg0x94 can be written by APU (or to be more precise, <a href="#">MP1</a> ) to power down the CGPLL or slow down clock.



**PMx00000054 (FCH::PM::SERIALIRQCONFIG)**

Read-write. Reset: 0000h.

\_aliasHOSTLEGACY; PMx00000054; PM=FED8\_0300h

Bits	Description
15	Reserved.
14	<b>pmx54bit7_nonsticky</b> . Read-write. Reset: 0. <b>Description:</b> 1: bit[7] is non-Sticky 0: bit[7] is Sticky
13	<b>softwareirq12</b> . Read-write. Reset: 0. <b>Description:</b> 1: IRQ12 input is high 0: IRQ12 input is low
12	<b>softwareirq1</b> . Read-write. Reset: 0. <b>Description:</b> 1: IRQ1 input is high 0: IRQ1 input is low
11	Reserved.
10	<b>undo_ser_irq_change</b> . Read-write. Reset: 0. Not used.
9	<b>legacy_dis</b> . Read-write. Reset: 0. Not used.
8	<b>siirq_cntrl</b> . Read-write. Reset: 0. Not used.
7	<b>serialirqenable</b> . Read-write. Reset: 0. <b>Description:</b> Setting this bit to 1 enable the serial IRQ function. When bit[14]=0, this bit is stick, default. When bit[14]=1, this bit is non-sticky
6	<b>serirqmode</b> . Read-write. Reset: 0. <b>Description:</b> 0: Continuous mode 1: Active (quiet) mode
5:2	<b>numserirqbits</b> . Read-write. Reset: 0h. <b>Description:</b> Total number of serial IRQ's = 17 + NumSerIrqbts 0: 17 serial IRQ's (15 IRQ, <a href="#">SMI#</a> , + IOCHK#) 1: 18 serial IRQ's (15 IRQ, SMI#, IOCHK#, INTA#) ... 15: 32 serial IRQ's The serial IRQ can support 15 IRQ#, SMI#, IOCHK#, INTA#, INTB#, INTC#, and INTD#. When serial SMI# is used, BIOS will need to check SIO (or device that generates serial SMI#) for status.
1:0	<b>numstartbits</b> . Read-write. Reset: 0h. <b>Description:</b> This field defines the number of clocks in the start frame. Start Frame Width = 4 + 2 * NumStartBits

**PMx00000056 (FCH::PM::RTCCONTROL)**

Read-write.

\_aliasHOSTLEGACY; PMx00000056; PM=FED8\_0300h

Bits	Description
15	<b>rtcdecodedis.</b> Read-write. Reset: 0. <b>Description:</b> When it is 1, acpismbus stop to decode port 0x70/71/72/73. Note that, the reg nmi_en is in 0x70 bit7, this bit also block by RtcDecodeDis. Firmware have to config nmi_en before disable RTC decoding.
14	<b>extrartccmosen.</b> Read-write. Reset: 0. When it is 1, SW can access the extra 16 bytes of RTC CMOS RAM.
13	<b>altcmosmapen.</b> Read-write. Reset: 0. When enabled, bank 1 of CMOS RAM is changed. Index 00:0D will still return the time and alarm settings. Index 0E:7F will return the absolute offset 8E:FF.
12	<b>centuryen.</b> Read-write. Reset: 1. Enable RTC Century support.
11	<b>mask_rtc_clk_out.</b> Read-write. Reset: 0. Set to 1 to disable RtcClk output.
10	<b>rtcclkdrive.</b> Read-write. Reset: 1. <b>Description:</b> 0: HIGHDRIVE tied low for RtcClkOut pad 1: HIGHDRIVE tied high for RtcClkOut pad
9:7	Reserved.
6	<b>rtc_test_en.</b> Read-write. Reset: 0. <b>Description:</b> This bit is for simulation only. Please do not change its value in real silicon. 0: Normal speed for prescaler 1: We replace 8kHz by OSC clock in prescaler. As the result, the prescaler 8kHz clock and all the clock divided from it can be speed up.
5	Reserved.
4	<b>rtcprotectc0_cf.</b> Read-write. Reset: 0. When set, RTC RAM index C0:CFh will be locked from read/write. This bit can only be written once.
3	<b>rtcprotectd0_df.</b> Read-write. Reset: 0. When set, RTC RAM index D0:DFh will be locked from read/write. This bit can only be written once.
2	<b>rtcprotecte0_ef.</b> Read-write. Reset: 0. When set, RTC RAM index E0:EFh will be locked from read/write. This bit can only be written once.
1	<b>rtcprotectf0_ff.</b> Read-write. Reset: 0. When set, RTC RAM index F0:FFh will be locked from read/write. This bit can only be written once.
0	<b>rt_cprotect38_3f.</b> Read-write. Reset: 0. When set, RTC RAM index 38:3Fh will be locked from read/write. This bit can only be written once.

**PMx00000058 (FCH::PM::VRT\_T1)**

Read-write. Reset: 01h.

\_aliasHOSTLEGACY; PMx00000058; PM=FED8\_0300h

Bits	Description
7:0	<b>vrt_t1.</b> Read-write. Reset: 01h. To conserve power, the RTC battery is sampled periodically for checking its state of health. VRT_T1 and VRT_T2 make up the interval of the checking. When VRT_Enable is high, the battery is being sampled. When VRT_enable is low, the battery is not being sampled. This register defines the time of VRT enable being high for RTC battery monitor circuit, in milliseconds.

**PMx00000059 (FCH::PM::VRT\_T2)**

Read-write. Reset: FFh.

\_aliasHOSTLEGACY; PMx00000059; PM=FED8\_0300h

Bits	Description
7:0	<b>vrt_t2.</b> Read-write. Reset: FFh. This register defines the time of VRT enable being low for the RTC battery monitor circuit, in 4 ms increments.

**PMx0000005A (FCH::PM::INTRUDERCONTROL)**

Read-write. Reset: 11h.

\_aliasHOSTLEGACY; PMx0000005A; PM=FED8\_0300h

Bits	Description
7	Reserved.
6	<b>cmoserasests.</b> Read-write. Reset: 0. Indicate that a CMOS Erase has been occurred.
5	<b>cmoseraseclr.</b> Read-write. Reset: 0. Write to 1 to clear CMOS Erase status.
4	<b>cmoserasedis.</b> Read-write. Reset: 1. Set to 1 to disable CMOS Erase.
3	Reserved.
2	<b>intruderalertsts.</b> Read-write. Reset: 0. <b>Description:</b> Read Only. The status bit will be set to 1 if an Intruder alter event (pad-IntruderAlert#=0) has occurred . Software need to set bit[1] to clear this status bit. To Arm®: set bit[0]=1, bit[1]=0 After Trigger: read bit[2] for status To re-Arm: set bit[0]=1, bit[1]=1 wait a short time set bit[1]=0
1	<b>intruderalertclr.</b> Read-write. Reset: 0. <b>Description:</b> Write 1 to clear the IntruderAlert status bit (bit[2]: IntruderAlertSts). Software need to write this bit 0 to enable pad-IntruderAlert#=0 to set bit[2]: IntruderAlertSts
0	<b>intruderalertpuen.</b> Read-write. Reset: 1. <b>Description:</b> 1: enable internal pullup (>200K). Please noted that pullup is enabled when both bit[0]=1 and bit[2]=0, if pad-IntruderAlert# is '0' while bit[1]=0, bit[2] will be set, and internal pullup will be disabled to save power. 0: disable internal pullup, when bit[0]=0, internal pullup is disabled.

**PMx0000005B (FCH::PM::RTCShadow)**

Read-write.

RTC\_AIE is defined at RTC\_Reg:0Bh[bit5].

Note1: These four bits(bit[7:4]) don't have any default value. After power on, their values are undertermined. SW has to program PwrFailShadow to give them values.

\_aliasHOSTLEGACY; PMx0000005B; PM=FED8\_0300h

Bits	Description
7	<b>forcepwron.</b> Read-write. Reset: X. <b>Description:</b> 0: If RTC AIE = 1, will wakeup when RTC alarm fires after a power failure/resume. (See Note) 1: If RTC AIE =1, will force power on after power resumes regardless of Bit[5:4] setting. (See Note)
6	<b>powerstate.</b> Read-write. Reset: X. <b>Description:</b> Power state indicator. 0: Off 1: On
5:4	<b>pwrfailoption.</b> Read-write. Reset: XXb. <b>Description:</b> These two bits will determine how system should resume after a power failure. 00: Always offalways power off after power resumes 01: Always onalways power on after power resumes 10: Always offalways power off after power resumes 11: Use previousresume to same setting when power fails
3:0	<b>pwrfailshadow.</b> Read-write. Reset: 0h. Writing to these four bits will set the value onto bits [7:4]. Software should always set bit 2 = 1.

**PMx0000005C (FCH::PM::LLBCNTRL)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; PMx0000005C; PM=FED8\_0300h

Bits	Description
7:3	Reserved.
2	<b>allowwakes3en.</b> Read-write. Reset: 0. Set to 1 to allow LLB# as wake event in S3.
1	<b>useaswakeen.</b> Read-write. Reset: 0. Set to 1 to treat LLB# as wake event.
0	<b>blockwakeen.</b> Read-write. Reset: 0. Set 1 to block wake event if LLB# is asserted. But if UseAsWakeEn and AllowWakeS3En are all set to 1, LLB# and other wake events can wake the system up from S3.

**PMx0000005D (FCH::PM::RTCGPIO)**

Read-write.

\_aliasHOSTLEGACY; PMx0000005D; PM=FED8\_0300h

Bits	Description
7	<b>ortclkpub.</b> Read-write. Reset: 0. <b>Description:</b> Pull up control for RTCCLK pad 0: Enable pull up 1: Disable pull up
6:2	Reserved.
1	<b>rtcirqgpioenb.</b> Read-write. Reset: 1. RtcIrq Gpio Output Enable
0	<b>rtcirqgpioout.</b> Read-write. Reset: 0. RtcIrq Gpio Output

**PMx0000005E (FCH::PM::RTCEXTINDEX)**

Read-write.

\_aliasHOSTLEGACY; PMx0000005E; PM=FED8\_0300h

Bits	Description
7:0	<b>index.</b> Read-write. Reset: XXXXXXXXb. Specify the offset of RTC Extended Registers to be read/written from PM_REG:5Fh

**PMx0000005F (FCH::PM::RTCEXTDATA)**

Read-write.

\_aliasHOSTLEGACY; PMx0000005F; PM=FED8\_0300h

Bits	Description
7:0	<b>data.</b> Read-write. Reset: XXXXXXXXb. Read data or write data of RTC Extended Registers

**PMx00000060 (FCH::PM::ACPIPM1EVTBLK)**

Read-write. Reset: 0000h.

\_aliasHOSTLEGACY; PMx00000060; PM=FED8\_0300h

Bits	Description
15:2	<b>acpипm1evtblk.</b> Read-write. Reset: 0000h. These bits define the least significant byte of the 16 bit I/O range base address of the ACPI power management Event Block. Bit 2 corresponds to Addr[2] and bit 7 corresponds to Addr[7].
1:0	Reserved.

**PMx00000062 (FCH::PM::ACPIPM1CNTBLK)**

Read-write. Reset: 0400h.

\_aliasHOSTLEGACY; PMx00000062; PM=FED8\_0300h

Bits	Description
15:1	<b>acpипm1cntblk.</b> Read-write. Reset: 0200h. These bits define the least significant byte of the 16 bit I/O base address of the ACPI power management Control block. Bit 1 corresponds to Addr[1] and bit 7 corresponds to Addr[7].
0	Reserved.

**PMx00000064 (FCH::PM::ACPIPM1TMRBLK)**

Read-write. Reset: 0000h.

\_aliasHOSTLEGACY; PMx00000064; PM=FED8\_0300h

Bits	Description
15:1	<b>acpипmtmrblk.</b> Read-write. Reset: 0000h. These bits define the least significant byte of the 16 bit I/O base address of the ACPI power management Timer block. Bit 1 corresponds to Addr[1] and bit 7 corresponds to Addr[7].
0	Reserved.

**PMx00000066 (FCH::PM::P\_CNTBLK)**

Read-write. Reset: 0000h.

\_aliasHOSTLEGACY; PMx00000066; PM=FED8\_0300h

Bits	Description
15:0	Reserved.

**PMx00000068 (FCH::PM::ACPIGPE0BLK)**

Read-write. Reset: 0000h.

\_aliasHOSTLEGACY; PMx00000068; PM=FED8\_0300h

Bits	Description
15:2	<b>acpигpe0blk.</b> Read-write. Reset: 0000h. These bits define the least significant byte of the 16 bit I/O base address of the ACPI power management General Purpose Event block. Bit 2 corresponds to Addr[2] and bit 7 corresponds to Addr[7]. Addr[1:0] are ignored because this register block is 4 byte long.
1:0	Reserved.

**PMx0000006A (FCH::PM::ACPISMICMD)**

Read-write. Reset: 00B0h.

\_aliasHOSTLEGACY; PMx0000006A; PM=FED8\_0300h

Bits	Description
15:0	<b>acpismicmd.</b> Read-write. Reset: 00B0h. These bits define the least significant byte of the 16 bit I/O base address of the ACPI <a href="#">SMI</a> Command block. Bit 0 corresponds to Addr[0] and bit 7 corresponds to Addr[7]. The address is required to be WORD-aligned (Addr[0]=0)

**PMx0000006E (FCH::PM::ACPIPMACNTBLK)**

Read-write. Reset: 0000h.

\_aliasHOSTLEGACY; PMx0000006E; PM=FED8\_0300h

Bits	Description
15:0	<b>acpipmacntblk.</b> Read-write. Reset: 0000h. These bits define the most significant byte of the 16 bit I/O base address. Bit 0 corresponds to Addr[8] and bit 7 corresponds to Addr[15].

**PMx00000070 (FCH::PM::MP1\_WARMRESETACK\_WLAN\_CLK\_REQ)**

Read-write. Reset: 3F3E\_0170h.

\_aliasHOSTLEGACY; PMx00000070; PM=FED8\_0300h

Bits	Description
31:24	<b>wlanpllrbtmtmr.</b> Read-write. Reset: 3Fh. Configure the PllLock assertion (0->1) time after PllRstB deasserts (0->1). Unit is 16usec.
23:16	<b>wlanpllpwrrstbtmtmr.</b> Read-write. Reset: 3Eh. Configure the PllRstB deassertion (0->1) time. Unit is 16usec.
15	<b>bp_reset_l_in_2nd_fch_value.</b> Read-write. Reset: 0. <b>Description:</b> When bit 14 of this register is 1'b0, this bit is useless. When bit 14 of this register is 1'b1: When this bit is set to 1'b0, the Secondary <a href="#">FCH</a> starts a warm reset sequence when BP_RESET_L toggles When this bit is set to 1'b1, the Secondary FCH ignores the toggling on BP_RESET_L
14	<b>bp_reset_l_in_2nd_fch_override.</b> Read-write. Reset: 0. <b>Description:</b> For the primary <a href="#">FCH</a> , this bit is useless. For the secondary FCH: When this bit is set to 1'b0, the Secondary FCH will ignore the toggling on BP_RESET_L only when the Secondary FCH is used as a <a href="#">PCIe</a> endpoint. When this bit is set to 1'b1, the Secondary FCH behaviour about the toggling on BP_RESET_L will be decided by bit 15 in this register.
13:3	<b>wdt_warmresetack_tmr.</b> Read-write. Reset: 02Eh. <b>Description:</b> Time out value of MP1_Watchdog timer, this time is using 16.2us Osc clock to do increment. default=0x2E After append 2'b11, the Timer is 187. (16.2us*187=3.029ms), max=16.2us*8191=132.694ms
2	<b>en_slv_cpurst.</b> Read-write. Reset: 0. when set to 1, Master <a href="#">FCH</a> will do reset when Slave FCH asserts CpuRstB=0. Slave FCH will do Warm Reset for sync_flood.
1	<b>en_wdt_warmresetack.</b> Read-write. Reset: 0. when bit[0]=1, set to 1 to enable MP1_Watchdog Timer for WarmResetAck handshake, if MP1_WarmResetAck rising edge not detected before MP1_Watchdog Timer time out, <a href="#">Cold reset</a> will be generated.
0	<b>en_mp1_warmresetack.</b> Read-write. Reset: 0. set to 1 to enable MP1_WarmResetAck handshake, all <a href="#">FCH</a> controlled Devices Reset, except PLL and APU, will be blocked till MP1_WarmResetAck rising edge or MP1_Watchdog Timer time out.

**PMx00000074 (FCH::PM::ACPICONFIG)**

Read-write. Reset: 1000\_0140h.

\_aliasHOSTLEGACY; PMx00000074; PM=FED8\_0300h

Bits	Description
31	<b>delay_gpp_off_time.</b> Read-write. Reset: 0. <b>Description:</b> When BP_PWR_GOOD is used as RESET button, once pressed, PCI GPP clock will be stopped right away while PciRST# will be active (=0) some time later, this bit is used to meet customer's request to have PCI GPP clock running after PciRST# active. This bit is reset by RsmRstB only. 1: PCI BPP clock keep running for some time after PciRST#=0 0: PCI BPP clock stopped right away when BP_PWR_GOOD=0
30	Reserved.
29	<b>rtcwakealarm.</b> Read-write. Reset: 0. Set to 1 to only rtc alarm to wake up the system.
28	<b>pcieeventmap.</b> Read-write. Reset: 1. Set to 1 to route pme message from APU to gevent 24, Hotplug message from APU to gevent 7..
27	<b>wakepinasgevent.</b> Read-write. Reset: 0. Set to 1 to treat Wake# pin as Gevent input.
26	<b>pcie_wak_intr_dis.</b> Read-write. Reset: 0. Set to 1 to disable interrupt from Pcie_wak_sts
25	<b>pcie_wak_mask.</b> Read-write. Reset: 0. Set to 1 to disable PCIE_WAK_STS and PCIE_WAK_DIS function. This is used for supporting ACPI 3.0 specification. If ACPI 3.0 is not supported, this bit should be left as 1
24	<b>pcienative.</b> Read-write. Reset: 0. Setting to 1 will block <a href="#">PCIe</a> GPP PME message and HotPlug message from generating SCI. This is used for supporting ACPI 3.0 specification. If ACPI 3.0 is not supported, this bit should be left as 0
23	<b>rst_usb_s5.</b> Read-write. Reset: 0. Write '1' to make Cpl_VDDCR_S5_RESETEn=0 to reset USB,MP2, etc. Need to write '0' to deassert Cpl_VDDCR_S5_RESETEn=1. This bit is not for normal operation, it is to be used for recovery when something went wrong.
22	<b>usersmureset.</b> Read-write. Reset: 0. <b>Description:</b> 0: fch_rsmu_hard_resetsb is not used to reset fch_rsmu, SDP, AB. 1: fch_rsmu_hard_resetsb is used to reset fch_rsmu, SDP, AB.
21	<b>mask_usb_s5_rst.</b> Read-write. Reset: 0. Set to '1' to mask oDevAllRstB to gen Cpl_VDDCR_S5_RESETEn=0 to reset USB/MP2/..., default=0
20	<b>en_df_intrwake.</b> Read-write. Reset: 0. <b>Description:</b> 0: disable FCH_DF_IntrWake in s5_misc.vpp 1: enable FCH_DF_IntrWake in s5_misc.vpp
19	Reserved.
18	<b>en_sync_flood.</b> Read-write. Reset: 0. <b>Description:</b> 0: disable SYNC_FLOOD 1: enable SYNC_FLOOD
17	<b>en_shutdown_msg.</b> Read-write. Reset: 0. <b>Description:</b> 0: disable SHUTDOWN message 1: enable SHUTDOWN message
16	<b>sw_s5pwrmux.</b> Read-write. Reset: 0. <b>Description:</b> When PM_regx74[15]=0, this bit control oS5PwrMux to USB. This bit will be reset to 0 by PllLock=0, thus it will be reset to 0 on any S5/S3 entry. 0: USB is powered by S5-domain VDDCR_SOC_S5 (bypass to S5 rail mode) 1: USB is powered by CLDO Vout (regulation mode, to be used in S0)
15	<b>sw_s5pwrmux_override_n.</b> Read-write. Reset: 0. <b>Description:</b> 0: use PM_regx74[16] to control oS5PwrMux to USB. 1: use iPllock to control oS5PwrMux to USB. When iPllock is unlock (=0), USB is powered by S5-domain VDDCR_SOC_S5 (bypass to S5 rail mode) When iPllock is locked (=1), USB is powered by CLDO Vout (regulation mode, to be used in S0)
14	<b>sel_smu_thermtrip.</b> Read-write. Reset: 0.

	<b>Description:</b> 0: use synched SMU_ThermTrip to drive pad BP_THERMTRIP_L 1: use SMU_ThermTrip directly to drive pad BP_THERMTRIP_L
13	<b>sel_pwrgrd_pad.</b> Read-write. Reset: 0. <b>Description:</b> 0: SPI_FBCLK_mux will use debounced PwrGood PAD input (~10ms) as ResetB to avoid glitch. 1: SPI_FBCLK_mux will use PwrGood PAD input as ResetB
12:10	Reserved.
9	<b>acpireducedhwen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Acpi Fixed register interface is enabled 1: the decoding of Acpi Fixed registers and Sci are disabled. In addition wake function from pm1a is disabled as well.
8	<b>pwnbtnen.</b> Read-write. Reset: 1. Set to 1 to enable power button support in pm1a block
7	<b>bios_rls.</b> Read-write. Reset: 0. Set to 1 to generate SCI. Read always return 0
6	<b>maskarbdis.</b> Read-write. Reset: 1. Set to 1 to disable ArbDis function in the ACPI register. ArbDis is not really used, but it still needs to be accessible by OS.
5	Reserved.
4	<b>tmr_en_en.</b> Read-write. Reset: 0. Set to 1 enable TMR_EN function in the standard ACPI register.
3	<b>slpbtn_en_en.</b> Read-write. Reset: 0. Set to 1 to enable SLPBTN_EN function in the standard ACPI register.
2	<b>rtc_en_en.</b> Read-write. Reset: 0. Set to 1 to enable RTC_EN function in the standard ACPI register.
1	<b>gbl_en_en.</b> Read-write. Reset: 0. Set to 1 to enable GBL function in the standard ACPI PmControl register.
0	<b>decen_acpi.</b> Read-write. Reset: 0. Set to 1 to enable decoding of the standard ACPI registers

**PMx00000078 (FCH::PM::WAKEIOADDR)**

Read-write. Reset: 0000\_FFFFh.

\_aliasHOSTLEGACY; PMx00000078; PM=FED8\_0300h

Bits	Description
31:17	Reserved.
16	<b>mp1_wdt_cnt_clr.</b> Read-write. Reset: 0. <b>Description:</b> Write one clear. Write this bit to one, it will clear the MP1_WDT_cnt in PwrRst.
15:0	<b>wakeiobaseaddress.</b> Read-write. Reset: FFFFh. The register specifies the wake I/O address. Any I/O write to the I/O address can cause APU to wake from C state. This is an obsolete function that is not used anymore

**PMx0000007E (FCH::PM::CSTATEEN)**

Read-write. Reset: 0060h.

\_aliasHOSTLEGACY; PMx0000007E; PM=FED8\_0300h

Bits	Description
15:6	Reserved.
5	<b>k8c1etoc3en.</b> Read-write. Reset: 1. Set to 1 to put APU into C3 state in C1e state.
4	<b>k8c1etoc2en.</b> Read-write. Reset: 0. Set to 1 to put APU into C2 state in C1e state.
3:0	Reserved.



**PMx00000080 (FCH::PM::BREAKEVENT)**

Read-write. Reset: 0026\_0000h.

\_aliasHOSTLEGACY; PMx00000080; PM=FED8\_0300h

Bits	Description
31:24	Reserved.
23:16	<b>scratchbit16_23</b> . Read-write. Reset: 26h.
15:5	Reserved.
4	<b>scratchbit4</b> . Read-write. Reset: 0. Scratch bit used by Software
3	<b>scratchbit3</b> . Read-write. Reset: 0. Scratch bit used by Software
2	<b>scratchbit2</b> . Read-write. Reset: 0. Scratch bit used by Software
1	Reserved.
0	<b>scratchbit0</b> . Read-write. Reset: 0. Scratch bit used by Software

**PMx00000088 (FCH::PM::CSTATECONTROL)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; PMx00000088; PM=FED8\_0300h

Bits	Description
31:11	Reserved.
10	<b>sw_sync_flood</b> . Read-write. Reset: 0. When PMx8c[27]=1, write this bit =1 will generate SW_sync_flood. Since this register is non-sticky, this bit will be cleared by PciRstB, thus software no need to write 0 after write 1 should this SW_sync_flood is enabled to generate Reset (PMx74[18]=1).
9:6	Reserved.
5	<b>slp_en</b> . Read-write. Reset: 0. Enable LDTSTOP# as an output
4:3	Reserved.
2	<b>dlyslpen</b> . Read-write. Reset: 0. Set to 1 to delay recognition of STPGNT# until there is no pending read in AB
1:0	Reserved.

**PMx0000008C (FCH::PM::BTTNSCICONTROL)**

Read-write. Reset: 00FF\_FFFFh.

\_aliasHOSTLEGACY; PMx0000008C; PM=FED8\_0300h

Bits	Description
31	<b>btn_diswake_pressins0.</b> Read-write. Reset: 0. <b>Description:</b> 1: no wakeup when button pressed in S0, and software put system in S3 while button still pressed and then released in less than 4s 0: default, when button is pressed and released in less than 4s, if system is in S3/S5, system will always do wakeup.
30	<b>sci_btn_fall_edge.</b> Read-write. Reset: 0. <b>Description:</b> 1: set PWRBTN_STS_reg to gen SCI at button falling edge (after 16ms debounce) 0: default, no SCI at button falling edge
29	<b>wlan_fp6_iso_en.</b> Read-write. Reset: 0. <b>Description:</b> 0: WLAN ISO off, S5 WLAN PMA to S5 WLAN digital signals are disconnected. 1: WLAN ISO on, S5 WLAN PMA to S5 WLAN digital signals are connected.
28	<b>smireg_use_s5rst.</b> Read-write. Reset: 0. <b>Description:</b> This bit is reset by RsmRstB only. 0: some registers inside <a href="#">SMI</a> (acpi_event) module are reset by PciRstB 1: some registers inside SMI (acpi_event) module are reset by S5RstB
27	<b>sw_sync_flood_enable.</b> Read-write. Reset: 0. <b>Description:</b> 0: PMx88[10] cannot generate SW_sync_flood. 1: PMx88[10] can generate SW_sync_flood.
26	<b>dis_sci_wakeup_power_saving_mode.</b> Read-write. Reset: 0. <b>Description:</b> 0: sci_wakeup can wake Power saving mode 1: sci_wakeup cannot wake Power saving mode
25	<b>dis_pic_irq_8_power_saving_mode.</b> Read-write. Reset: 0. <b>Description:</b> 0: pic_irq_8 can wakeup Power saving mode 1: pic_irq_8 cannot wakeup Power saving mode
24	<b>acpialarm_nchk_tmren.</b> Read-write. Reset: 0. <b>Description:</b> 0: ACPIAlarm will check TMR_EN =1 1: ACPIAlarm will not check TMR_EN
23:0	<b>espi1devintrmask.</b> Read-write. Reset: FF_FFFFh. <b>Description:</b> SW can set these bits to mask of eSPI_1 Device IRQ23~0. 1: Mask off the interrupt 0: No mask

**PMx00000090 (FCH::PM::SPIPADPUPD)**

Read-write. Reset: 88A4\_0959h.

\_aliasHOSTLEGACY; PMx00000090; PM=FED8\_0300h

Bits	Description
31	<b>boot_timer_cold_rst.</b> Read-write. Reset: 1. When bit[31]=0, Boot Timer Reset is doing warm reset (toggle Cpu_ResetB only). By setting bit[31]=1, Boot Timer Reset will do cold reset (toggle both Cpu_ResetB and Cpu_PwrGood).
30	<b>dis_spi_pupd_sw.</b> Read-write. Reset: 0. <b>Description:</b> Set to 1 to disable all SPI PAD pullup/pulldown defined in this register. When we are in S3/S5, external S0VDD will be power-off, though SPI PADs are in S5, depends on board design, S0VDD may be connected to SPI PAD. To enable SPI ROM sharing with external <a href="#">EC</a> , all pullup/pulldown need be disabled so external EC can drive SPI signals to access SPI ROM. Software can set bit[30]=1 without change bit [11:0] value before getting into S3/S5, after exit S3/S5, software need to reset bit[30]=0.
29	<b>dis_spi_pupd_hw.</b> Read-write. Reset: 0. If set to 1, when system is in Power saving mode or S3 or S5, all SPI PAD pullup/pulldown defined in this register will be disabled.
28	<b>spi2_cs1_l_pulldown.</b> Read-write. Reset: 0. control pad SPI2_CS1 pulldown, 1: Enable 0: disable
27	<b>spi2_cs1_l_pullup.</b> Read-write. Reset: 1. control pad SPI2_CS1 pullup, 1: Enable 0: disable
26:24	<b>st_sx.</b> Read-write. Reset: 0h. <b>Description:</b> Read Only, indicate the current S-state value, for debug purpose only, as in Clock stop mode/Power saving mode/S3/S4/S5, Host cannot read register value, 0x0: S0 state 0x1: Clock slow down state 0x2: Clock stop state 0x3: S3 state 0x4: Power saving mode state 0x5: S4/S5 state 0x6, 0x7: reserved
23	<b>spi1_hold_l_pulldown.</b> Read-write. Reset: 1. control pad SPI1_HOLD_L pulldown, 1: Enable 0: disable
22	<b>spi1_hold_l_pullup.</b> Read-write. Reset: 0. control pad SPI1_HOLD_L pullup, 1: Enable 0: disable
21	<b>spi1_wp_l_pulldown.</b> Read-write. Reset: 1. control pad SPI1_WP_L pulldown, 1: Enable 0: disable
20	<b>spi1_wp_l_pullup.</b> Read-write. Reset: 0. control pad SPI1_WP_L pullup, 1: Enable 0: disable
19	<b>spi1_cs1_l_pulldown.</b> Read-write. Reset: 0. control pad SPI1_CS1 pulldown, 1: Enable 0: disable
18	<b>spi1_cs1_l_pullup.</b> Read-write. Reset: 1. control pad SPI1_CS1 pullup, 1: Enable 0: disable
17	<b>bt_gpio_1p8v_receive.</b> Read-write. Reset: 0. <b>Description:</b> 0: GPIO7/GPIO8 are 3.3V receiver 1: GPIO7/GPIO8 are 1.8V receiver, when they used as BT receiver
16:12	Reserved.
11	<b>spi_clk_pulldown.</b> Read-write. Reset: 1. control pad SPI_CLK pulldown, 1: Enable 0: disable
10	<b>spi_clk_pullup.</b> Read-write. Reset: 0. control pad SPI_CLK pullup, 1: Enable 0: disable
9	<b>spi_cs1_pulldown.</b> Read-write. Reset: 0. control pad SPI_CS1 pulldown, 1: Enable 0: disable
8	<b>spi_cs1_pullup.</b> Read-write. Reset: 1. control pad SPI_CS1 pullup, 1: Enable 0: disable
7	<b>spi_hold_l_pulldown.</b> Read-write. Reset: 0. control pad SPI_HOLD_L pulldown, 1: Enable 0: disable
6	<b>spi_hold_l_pullup.</b> Read-write. Reset: 1. control pad SPI_HOLD_L pullup, 1: Enable 0: disable
5	<b>spi_wp_l_pulldown.</b> Read-write. Reset: 0. control pad SPI_WP_L pulldown, 1: Enable 0: disable
4	<b>spi_wp_l_pullup.</b> Read-write. Reset: 1. control pad SPI_WP_L pullup, 1: Enable 0: disable
3	<b>spi_do_pulldown.</b> Read-write. Reset: 1. control pad SPI_DO pulldown, 1: Enable 0: disable
2	<b>spi_do_pullup.</b> Read-write. Reset: 0. control pad SPI_DO pullup, 1: Enable 0: disable
1	<b>spi_di_pulldown.</b> Read-write. Reset: 0. control pad SPI_DI pulldown, 1: Enable 0: disable
0	<b>spi_di_pullup.</b> Read-write. Reset: 1. control pad SPI_DI pullup, 1: Enable 0: disable

**PMx00000094 (FCH::PM::CSTATETIMING0)**

Read-write. Reset: 0010\_0089h.

\_aliasHOSTLEGACY; PMx00000094; PM=FED8\_0300h

**Bits Description**

31:0 Reserved.

**PMx000000A0 (FCH::PM::MESSAGECSTATE)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; PMx000000A0; PM=FED8\_0300h

**Bits Description**

31	<b>checkcoreiddis.</b> Read-write. Reset: 0. <b>Description:</b> 1: Ignore Core Id check when MultiCoreEnbit set 1. 0: Enable Core Id check when MultiCoreEnbit set 1.
30:21	<b>pmxa4reserved2.</b> Read-write. Reset: 000h.
20:16	<b>tmrseloverride.</b> Read-write. Reset: 00h. <b>Description:</b> This is to be used with bit TimerTickChgMsgEn. In case <a href="#">FCH</a> auto-timer detection logic is not functioning properly, one can use these bits to override the logic and force the logic to monitor the specific timer. Bit 0 When set, use HPET Bit 1 When set, use RTC Bit 2 if HPET is selected, setting bit 2 will force the logic to monitor HPET timer 0. Bit 3 if HPET is selected, setting bit 3 will force the logic to monitor HPET timer 1. Bit 4 if HPET is selected, setting bit 4 will force the logic to monitor HPET timer2.
15:11	Reserved.
10	<b>clkintrtagen.</b> Read-write. Reset: 0. When enabled, <a href="#">FCH</a> will mark the periodic timer interrupt.
9:2	Reserved.
1	<b>timertickchgmsgen.</b> Read-write. Reset: 0. When enabled, <a href="#">FCH</a> will send a message to CPU indicating the latest periodic timer interval. FCH will automatically determine which timer (PIT, RTC, or HPET) is being used.
0	<b>obattmodechgmsgen.</b> Read-write. Reset: 0. When enabled, <a href="#">FCH</a> will automatically send a message to CPU indicating the power mode (AC vs battery). In addition, every time it is changed, FCH will generate a message to indicate the update.

**PMx000000A4 (FCH::PM::MISCDEBUG)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; PMx000000A4; PM=FED8\_0300h

**Bits Description**

31:3	Reserved.
2	<b>blockgeventsmi.</b> Read-write. Reset: 0. <b>Description:</b> 1: Block GEVENT <a href="#">SMI</a> 0: Unblock GEVEN SMI
1	<b>blocksci.</b> Read-write. Reset: 0. <b>Description:</b> 1: Block SCI 0: Unblock SCI
0	Reserved.

**PMx000000A8 (FCH::PM::VIRTUALWIRE)**

Read-write. Reset: 0023\_0085h.

\_aliasHOSTLEGACY; PMx000000A8; PM=FED8\_0300h

Bits	Description
31:27	Reserved.
26:16	<b>otherpwrrsttmr.</b> Read-write. Reset: 023h. <b>Description:</b> Parametised the reset timing wait time for other devices. For 300X mode, default = 0x18
15:11	Reserved.
10:0	<b>pg1pwrrsttmr.</b> Read-write. Reset: 085h. <b>Description:</b> Parametised the reset timing wait time for devices in PG1. For 300X mode, default = 0x18

**PMx000000B0 (FCH::PM::DEFERTIMETICK\_OBFFENABLE)**

Read-write.

\_aliasHOSTLEGACY; PMx000000B0; PM=FED8\_0300h

Bits	Description
31	<b>sw_obff_override.</b> Read-write. Reset: 0. <b>Description:</b> 0: CpuActive/MemActive from Data Fabric are used for OBFF. 1: bit[30:29] are used for OBFF.
30	<b>sw_obff_cpuactive.</b> Read-write. Reset: 0. When bit[31]=Sw_obff_override=1, this bit will override CpuActive from Data Fabric to control OBFF operation when bit[11]=OBFFEn=1
29	<b>sw_obff_memactive.</b> Read-write. Reset: 0. When bit[31]=Sw_obff_override=1, this bit will override MemActive from Data Fabric to control OBFF operation when bit[11]=OBFFEn=1
28	<b>long10usdelay.</b> Read-write. Reset: 0. <b>Description:</b> Spec requires ACTIVE/OBFF -> IDLE to wait at least 10us, for other transition ACTIVE/IDLE -> OBFF or OBFF/IDLE -> ACTIVE, the delay is controlled by this bit. 0: use 3x400ns (400ns controlled by bit[6:2]) 1: use 10us (10us controlled by bit[21:12])
27	<b>cpuactive.</b> Read-write. Reset: X. <b>Description:</b> Read Only. State of Internal signal CpuActive that from Data Fabric
26	<b>memactive.</b> Read-write. Reset: X. <b>Description:</b> Read Only. State of Internal signal MemActive that from Data Fabric.
25:24	<b>obff_state.</b> Read-write. Reset: 0h. <b>Description:</b> Read Only. Internal OBFF state machine states. 00: IDLE (when bit[11]=OBFFEn=0, OBFF_state is IDLE) 01: OBFF 11: ACTIVE
23	<b>obff_transition_done.</b> Read-write. Reset: 1. <b>Description:</b> Read Only. 1: OBFF transition is done 0: OBFF transition is going on.
22	<b>en_obff_blk_wake.</b> Read-write. Reset: 0. <b>Description:</b> 0: input of pad_WAKE_L will not be blocked from generating event when OBFF state machine output pattern. 1: input of pad_WAKE_L will be blocked from generating event when OBFF state machine output pattern of "IDLE/ACTIVE -> OBFF" or "IDLE/OBFF -> ACTIVE", and will be enabled when OBFF state machine output pattern of "OBFF/ACTIVE -> IDLE)
21:12	<b>cnt10usper48m.</b> Read-write. Reset: 1E0h. <b>Description:</b> Number of 48MHz clock for 10us delay, used for spec requirement "when platform enter CPU Active or OBFF, platform should not return to Idle in less than 10us". Software can change this value to adjust the delay. Default=0x1e0=480*(1sec/48M)=10us
11	<b>obffen.</b> Read-write. Reset: 0. Set to 1 to enable OBFF function which toggling WAKE#
10:8	<b>defertimertickvalue.</b> Read-write. Reset: 0h.

	<b>Description:</b> 000: No skipping 001: Skip 1 timer tick 010: Skip 2 timer ticks 011: Skip 3 timer ticks 100: Skip 4 timer ticks 101: Skip 5 timer ticks 110: Skip 6 timer ticks 111: Skip 7 timer ticks
7	<b>force_obff_blk_wake.</b> Read-write. Reset: 0. When set to 1, input of pad_WAKE_L will always be blocked from generating event.
6:2	<b>cnt400nsper48m.</b> Read-write. Reset: 14h. <b>Description:</b> Number of 48MHz (20.83ns) clock for 400ns delay, used for pulse width (both high and low pulse) of WAKE# protocol, software can change this value to adjust the WAKE# pulse width. Default=0x14=20*20.83 =417ns.
1	<b>forcetmrticken.</b> Read-write. Reset: 0. If bit 0 is set along with this bit and <a href="#">FCH</a> has skipped a timer tick interrupt, FCH will immediately generate the timer tick interrupt upon C state exit
0	<b>defertimerticken.</b> Read-write. Reset: 0. When set, <a href="#">FCH</a> will skip a number of timer tick interrupts based on the defined value in DeterTimeTickValue when CPU is in C state. When CPU is not in C state, FCH will not skip any timer tick interrupts.

**PMx000000B4 (FCH::PM::ACPIMISCDEBUG)**

Read-write. Reset: 0080\_0000h.

\_aliasHOSTLEGACY; PMx000000B4; PM=FED8\_0300h

Bits	Description
31:24	Reserved.
23	<b>intrtoggleonldtstp</b> . Read-write. Reset: 1. <b>Description:</b> Configure the behavior of "DMA/Interrupt indicator": When LdtStpB behaves as interrupt indicator, this bit configure the way it indicates interrupt: 0: The interrupt is signaled as a level signal. 1: The interrupt is signaled as a clock signal with 2us or 4us period depends on LDTSTPBTrSel.
22	<b>ldtstpaboutputdis</b> . Read-write. Reset: 0. <b>Description:</b> Configure the behavior of "DMA/Interrupt indicator": Disable LdtStpB output: 0: LdtStpB output enabled 1: LdtStpB output disabled
21	<b>wakecstateinslp</b> . Read-write. Reset: 0. <b>Description:</b> Configure the behavior of "DMA/Interrupt indicator": 0: Do not wake C State before entering S State. 1: Wake C State before entering S State.
20	<b>mergeallowldtstpwithldtstp</b> . Read-write. Reset: 0. <b>Description:</b> Configure the behavior of "DMA/Interrupt indicator": Change the definition of pin DMAACTIVE_L (ALLOWLDTSTP). 0: Drive DMAACTIVE_L to low when there is pending upstream request. 1: Output 2us/4us toggling on DMAACTIVE_L (ALLOWLDTSTP) when there is pending interrupt request and not in C0 state to DMAACTIVE_L otherwise drive DMAACTIVE_L to low when there is pending upstream request
19	<b>intronldtstpben</b> . Read-write. Reset: 0. <b>Description:</b> Configure the behavior of "DMA/Interrupt indicator": Change the definition of LdtStpB pin to "interrupt indicator". 0: LdtStpB behaves as LdtStpB 1: LdtStpB behaves as interrupt indicator
18	<b>ldtstpbtmrsl</b> . Read-write. Reset: 0. <b>Description:</b> Configure the behavior of "DMA/Interrupt indicator": Select 2us or 4us toggling on DMAACTIVE_L (ALLOWLDTSTP) or LDTSTPB_L according to Merge_Interrupt_Dma_Reg value. 0: 2us 1: 4us
17	Reserved.
16	<b>oallowldtstpout</b> . Read-write. Reset: 0. <b>Description:</b> Control the input/output direction of pin AllowLdtStp. 0: (default) AllowLdtStp is input to <a href="#">FCH</a> driven by APU. 1: AllowLdtStp as output pin to APU to indicate FCH traffic activities.
15:1	Reserved.
0	<b>fid_protect_en</b> . Read-write. Reset: 0. Set to 1 to skip C-state transition when <a href="#">FID/VID</a> message is received concurrently.



**PMx000000B8 (FCH::PM::TPRESET2)**

Read-write. Reset: 88h.

\_aliasHOSTLEGACY; PMx000000B8; PM=FED8\_0300h

Bits	Description
7:6	<b>clkgatecntrl.</b> Read-write. Reset: 2h. <b>Description:</b> These two bits control whether SMBUS module will allow clock gating to the internal 66MHz core clock 00: Disable the clock gating function 01: Wait 16 clocks before allowing clock gating to the SMBUS module 10: Wait 64 clocks before allowing clock gating to the SMBUS module 11: Wait 256 clocks before allowing clock gating to the SMBUS module
5:0	<b>tpreset2.</b> Read-write. Reset: 08h. Timing parameter used for S* -> S0 state transitions. This register determines the LDTSTOP# deassertion delay in 8s increment with 8s uncertainty.

**PMx000000B9 (FCH::PM::MISCDEBUG2)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; PMx000000B9; PM=FED8\_0300h

Bits	Description
7	Reserved.
6	<b>test_pwr_btn.</b> Read-write. Reset: 0. <b>Description:</b> This bit is used to speed up simulation 1'b1: debounce 16ms counter is 0x12 1'b0: debounce 16ms counter is 0x1ff
5:4	Reserved.
3	<b>clkrundisable.</b> Read-write. Reset: 0. Legacy DMA and serial IRQ logic reside in this module and they are running on the 33MHz CLK. Setting this bit will disable this module's ability to support CLKRUN# function from PCIBridge. In other words, when this bit is set, this module will prevent PCIBridge from stopping the 33MHz clock
2	<b>test_pm_tmr.</b> Read-write. Reset: 0. <b>Description:</b> 0: normal PM timer function 1: PM timer function run in test mode
1	<b>test_1ms.</b> Read-write. Reset: 0. <b>Description:</b> 0: normal delay in S state timing 1: Speed up S state delay by 7 times
0	<b>t32_64.</b> Read-write. Reset: 0. <b>Description:</b> Delay timer for S2: 0: 32 pci clk 1: 64 pci clk

**PMx000000BA (FCH::PM::S\_STATECONTROL)**

Read-write. Reset: 0000h.

\_aliasHOSTLEGACY; PMx000000BA; PM=FED8\_0300h

Bits	Description
15	<b>maskpmsgsngen.</b> Read-write. Reset: 0. When set (along with PmeMsgEn=1), PmeAck message coming from <a href="#">PCIe</a> device will be ignored and ACPI S state logic will solely use the timeout mechanism to sequence through the S3 state. This bit is used as an option to guard against multiple PmeAck messages coming from CNB and internal <a href="#">FCH</a> PCIe bridge so FCH S state logic will not sequence into S3 state prematurely.
14	<b>wakepinenable.</b> Read-write. Reset: 0. Set to 1 to enable wakeup from WAKE# pin.
13	<b>agptimeadj.</b> Read-write. Reset: 0. If set to 1, S* -> S0 state transitions will use 1ms clock for timing sequence otherwise, 8s clock will be used.
12:6	Reserved.
5	<b>overrideshorttimemode.</b> Read-write. Reset: 0. <b>Description:</b> It is only available when ShortTimeMode is enabled. When this bit is set high, ShortTimeMode will be disabled for Osc16Us_new.
4	<b>pmsgsngtrig.</b> Read-write. Reset: 0. <b>Description:</b> SW write this bit to trigger a PmeTurnOff sequence to NB. Reading this bit returns the status of the PmeTurnOff sequence (1 means not done 0 means done)
3	<b>pmsgsngen.</b> Read-write. Reset: 0. Set to 1 to enable PmeTurnOff/PmeMsgAck handshake.
2	<b>stpcklen.</b> Read-write. Reset: 0. <b>Description:</b> 0: disable STPCLK/STPGNT handshake in S state transition 1: Enable STPCLK/STPGNT handshake in S state transition
1	<b>allowoffset.</b> Read-write. Reset: 0. Set to 1 to add extra delay for STPCLK. Only valid if AgpTimeAdj is set.
0	<b>longslps3.</b> Read-write. Reset: 0. Set to 1 to extend SLP_S3# assertion to 1s minimum.

**PMx000000BC (FCH::PM::THROTTLINGCONTROL)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; PMx000000BC; PM=FED8\_0300h

Bits	Description
7:0	Reserved.

**PMx000000BD (FCH::PM::RCINBRSTENABLE)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; PMx000000BD; PM=FED8\_0300h

Bits	Description
7	<b>rcinbrstenable.</b> Read-write. Reset: 0.
6	<b>hostrstwarndisable.</b> Read-write. Reset: 0. Disable early indicator of PLTRST_B for eSPI
5	<b>rcinbrstenable1.</b> Read-write. Reset: 0.
4	<b>hostrstwarnenable_1.</b> Read-write. Reset: 0. Enable early indicator of PLTRST_B for eSPI1
3:0	Reserved.

**PMx000000BE (FCH::PM::RESETCONTROL1)**

Read-write. Reset: 72h.

\_aliasHOSTLEGACY; PMx000000BE; PM=FED8\_0300h

Bits	Description
7	<b>rsttocpupwrgden.</b> Read-write. Reset: 0. If set to 1, <a href="#">FCH</a> toggles CPUPG on every reset.
6	<b>hwm_resetooption.</b> Read-write. Reset: 1. <b>Description:</b> 0: Hwm function(Pmio2 register block) is reset by RsmRst. 1: Hwm function(Pmio2 register block) is reset by PciRst.
5	<b>slp_typen_control.</b> Read-write. Reset: 1. <b>Description:</b> Set to 1 to enable the function of SLP_TYPEn bit in PmControl register [AcpiPm1CntBlk:00h]. The SLP_TYPEn bit in PmControl register has no effect if this bit is clear.
4	<b>kbrsten.</b> Read-write. Reset: 1. Set to 1 to enable KB_RST# pin to trigger KB Reset.
3	<b>kb_trig_type.</b> Read-write. Reset: 0. <b>Description:</b> If kb_trig_type == 0, we will use the level trigger as kb_reset_src. If kb_sel_edge == 1, we will use edge trigger as kb_reset_src. This will give customers the choice how to trigger a keyboard reset.
2	<b>kb_sel_edge.</b> Read-write. Reset: 0. <b>Description:</b> This bit is applicable when kb_trig_type is set high. If kb_sel_edge == 0, negedge will be used as the kb_reset_src. If kb_sel_edge == 1, posedge will be used as the kb_reset_src.
1	<b>kb_pcirst_en.</b> Read-write. Reset: 1. Set to 1 to make PCI reset during KB Reset, which can be triggered by KB_RST# pin or <a href="#">EC</a> .
0	<b>softreseten.</b> Read-write. Reset: 0. Set to 1 to block any reset request until the system is not C state.

**PMx000000BF (FCH::PM::RESETCONTROL2)**

Read-write. Reset: C0h.

\_aliasHOSTLEGACY; PMx000000BF; PM=FED8\_0300h

Bits	Description
7	<b>pwrgoodenb.</b> Read-write. Reset: 1. Output enable for PwrGood pin (active low)
6	<b>pwrgoodout.</b> Read-write. Reset: 1. Output data for PwrGood pin
5	<b>bypass_pwr_good.</b> Read-write. Reset: 0. If asserted, Southbridge will not wait for deassertion of PWRGOOD to monitor wakeup events.
4	<b>resetpcie2.</b> Read-write. Reset: 0. This bit is to be used with GEVENT4 mux select bits. If GEVENT4 IO mux select bits are set to 10b, GEVENT4# pin will become PCIE_RST2#
3	<b>shutdownpinen.</b> Read-write. Reset: 0. <a href="#">Shutdown</a> system if seeing a negative edge on pinSHUTDOWN#
2	<b>overridewarmrst.</b> Read-write. Reset: 0. Add a S5 sticky bit "OverrideWarmRst" to override DevAllRstB so S5 GPIO can be persistent and not being reset by warm reset.
1	<b>selnew16us.</b> Read-write. Reset: 0. <b>Description:</b> When this bit is set high, Osc16Us_new will be used in PwrRst except MP1_WDT_cnt. When this bit is low, Osc16Us will be used in PwrRst.
0	Reserved.

**PMx000000C0 (FCH::PM::S5\_RESET\_STATUS)**

Reset: 0000\_0800h.

This register shows the source of previous reset.

\_aliasHOSTLEGACY; PMx000000C0; PM=FED8\_0300h

Bits	Description
31	<b>sw_sync_flood_flag.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. PMxC0[31] will be set if sw_sync_flood (PMx88[10]) trigger reset. Write 1 to clear. Bit[31] and Bit[28:16] except bit[20] will be cleared by Last reset event except the associated bit will be set.
30	<b>sdp_parity_err.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> When there is 'parity error', Sync_Flood reset will occur and PMxC0[27] will be set if enabled, in order to distinguish 'parity error' and 'CPU sync flood', PMxC0[30] will be set when there is SDP parity Error, thus software can distinguish 'parity error' and 'CPU sync flood'. This bit will not be cleared by other reset event, software need write 1 to clear. SDP parity error will not clear any status bit in this register.
29	<b>mp1_wdtout.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. This bit will be set to 1 when MP1_Watchdog timer time out (this indicates there was a failed warm reset handshake between <a href="#">MP1</a> and <a href="#">FCH</a> ). This bit will not be cleared by other reset event, software need write 1 to clear. MP1_Watchdog timer time out will not clear any status bit in this register.
28	Reserved.
27	<b>sync_flood.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. system reset was caused by a SYNC_FLOOD event which was due to an UE error( when PMx74[18]=1). Write 1 to clear. Bit[31] and Bit[28:16] except bit[20] will be cleared by Last reset event except the associated bit will be set.
26	<b>remotereseetfromasf.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. system reset was caused by a remote RESET command from ASF. Write 1 to clear. Bit[31] and Bit[28:16] except bit[20] will be cleared by Last reset event except the associated bit will be set.
25	<b>watchdogissuereset.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. system reset was caused by WatchDog Timer. Write 1 to clear. Bit[31] and Bit[28:16] except bit[20] will be cleared by Last reset event except the associated bit will be set.
24	<b>failbootrst.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. system reset was caused by AMD Fail boot timer. Write 1 to clear. Bit[31] and Bit[28:16] except bit[20] will be cleared by Last reset event except the associated bit will be set.
23	<b>shutdown_msg.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. system reset was caused by a SHUTDOWN command from CPU (when PMx08[20]=1 and PMx74[17]=1). Write 1 to clear. Bit[31] and Bit[28:16] except bit[20] will be cleared by Last reset event except the associated bit will be set.
22	<b>kb_reset.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. system reset was caused by assertion of KB_RST_L.. Write 1 to clear. Bit[31] and Bit[28:16] except bit[20] will be cleared by Last reset event except the associated bit will be set.
21	<b>sleepreset.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Reset status from Sleep state (Power saving mode, S3, 4, or 5) transition. Write 1 to clear. Bit[31] and Bit[28:16] except bit[20] will be cleared by Last reset event except the associated bit will be set.
20	<b>do_k8_full_reset.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> system reset was caused by CF9 = 0x0E. Write 1 to clear. [Note] Write CF9=0xE will set this bit=1, but write CF9=0xE will generate SLpRst later which will set bit[21]=SleepReset. In order to keep this bit =1, this bit will not be cleared by hardware, software need to write 1 to clear this bit . Bit[31] and Bit[28:16] except bit[20] will be cleared by Last reset event except the associated bit will be set.
19	<b>do_k8_reset.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. system reset was caused by CF9 = 0x06. Write 1 to clear. Bit[31] and Bit[28:16] except bit[20] will be cleared by Last reset event except the associated bit will be set.
18	<b>do_k8_init.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. system reset was caused by CF9 = 0x04. Write 1 to clear. Bit[31] and Bit[28:16] except bit[20] will be cleared by Last reset event except the associated bit will be set.

17	<b>soft_pcirst.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. system reset was caused by writing to PMIO 0xC4[0] (PciReset). Write 1 to clear. Bit[31] and Bit[28:16] except bit[20] will be cleared by Last reset event except the associated bit will be set.
16	<b>usrrstb.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. Last reset was caused by BP_SYS_RST_L assertion. Write 1 to clear. Bit[31] and Bit[28:16] except bit[20] will be cleared by Last reset event except the associated bit will be set.
15:14	<b>pmturnofftime.</b> Read-write. Reset: 0h. <b>Description:</b> 00: 1ms 01: 2ms 10: 4ms 11: 8ms
13:10	Reserved.
9	<b>intthermaltrip.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. system was shut down due to an internal ThermalTrip event. Write 1 to clear
8:5	Reserved.
4	<b>remotepowerdownfromasf.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. SOC has received a remote Power Off command from ASF. Write 1 to clear.
3	Reserved.
2	<b>shutdown.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. system was shut down due to ShutDown event (SHUTDOWN# pin). Write 1 to clear.
1	<b>pwrbtn4second.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. system was shut down due to 4s PwrButton event. Write 1 to clear.
0	<b>thermaltrip.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. system was shut down due to BP_THERMTRIP_L assertion. Write 1 to clear.

**PMx000000C4 (FCH::PM::RESETCOMMAND)**

Read-write. Reset: 28h.	
_aliasHOSTLEGACY; PMx000000C4; PM=FED8_0300h	
Bits	Description
7	<b>reseten.</b> Read-write. Reset: 0. <b>Description:</b> 0: Not allow to write bit 0 1: Allow to write bit 0.
6	<b>resetallacpi.</b> Read-write. Reset: 0. Writing 1 to emulate a Reset Button event.
5	<b>resetbuttonen.</b> Read-write. Reset: 1. <b>Description:</b> 1: reset from reset button (SYS_RESET_L) will generate S5Reset. 0: Disable SYS_RESET_L to generate S5Reset, it can be used as Gevent19/GPIO1.
4	<b>resetpcie.</b> Read-write. Reset: 0. Set to 1 to reset Gpp port.
3	<b>usrrstb2pll.</b> Read-write. Reset: 1. Set to 1 to stop Pll when reset button is pressed.
2	<b>selectdebug.</b> Read-write. Reset: 0. <b>Description:</b> 0: Select the PM_Reg C0 to be S5/Reset Status register. 1: Select the PM_Reg C0 to be a debug status register.
1	<b>memrstdisable.</b> Read-write. Reset: 0. When set, the memory reset function at DDR_RST# pin will be disabled.
0	<b>pcireset.</b> Read-write. Reset: 0. Writing 1 to do a PCI reset

**PMx000000C5 (FCH::PM::CF9SHADOW)**

Read-write.

\_aliasHOSTLEGACY; PMx000000C5; PM=FED8\_0300h

Bits	Description
7:4	Reserved.
3	<b>fullrst.</b> Read-write. Reset: 0. <b>Description:</b> 0: Assert reset signals only 1: Place system in S5 state for 3 to 5 seconds
2	<b>rstcmd.</b> Read-write. Reset: 0. <b>Description:</b> Write with 1 to generate reset as specified by bit[3,1]. Write only. Always read as 0.
1	<b>sysrst.</b> Read-write. Reset: 0. <b>Description:</b> 0: Send INIT HT message 1: Reset as specified by bit3
0	Reserved.

**PMx000000C6 (FCH::PM::HTCONTROL)**

Read-write. Reset: 0000h.

\_aliasHOSTLEGACY; PMx000000C6; PM=FED8\_0300h

Bits	Description
15:0	Reserved.

**PMx000000C8 (FCH::PM::MISC\_PMIO)**

Read-write. Reset: 0028\_800Ch.

\_aliasHOSTLEGACY; PMx000000C8; PM=FED8\_0300h

Bits	Description
31:24	<b>clkintrvectorord.</b> Read-write. Reset: 00h. Clock interrupt value, when bit[22] (clkintrvectororden) is set to 1.
23	Reserved.
22	<b>clkintrvectororden.</b> Read-write. Reset: 0. <b>Description:</b> This bit is used to select the source of the clock interrupt value. When this bit is 0, clock interrupt value is the value of bit[7:0] (vector) of IOAPIC REDIRECTION_TABLE_ENTRY_<0~23>_LOW_32BIT registers. When this bit is 1, clock interrupt value is the value of bit[31:24] (clkintrvectorord).
21	<b>align_s3s5.</b> Read-write. Reset: 1. <b>Description:</b> 0: Old scheme, BP_SLP_S5_L and BP_SLP_S3_L may not be aligned, this is default. 1: new scheme, BP_SLP_S5_L and BP_SLP_S3_L are aligned.
20	Reserved.
19	<b>usecpurst.</b> Read-write. Reset: 1. If this bit is not set, system reset will cause INIT# instead of CPURST#.
18:16	Reserved.
15	<b>rsmu_cpl_gate_dis.</b> Read-write. Reset: 1. <b>Description:</b> Chicken bit to disable the gating for Cpl signals between RSMU and <a href="#">MP1</a> . If it is low, gating enabled. If it is high, gating disabled.
14	<b>ocpupwrgood_sel.</b> Read-write. Reset: 0. <b>Description:</b> Chicken bit to disable the gating for signals between RSMU and <a href="#">MP1</a> . If it is low, gating enabled. If it is high, gating disabled.
13	<b>id_change_en.</b> Read-write. Reset: 0. Setting this bit will allow the software to change the DeviceID and RevisionID.
12	<b>s5resetoverride.</b> Read-write. Reset: 0. Set to 1 to mask off internet PCI reset used in ACPI.
11	<b>writebackenable.</b> Read-write. Reset: 0. HD audio/modem write back enable. If set, the WakeOnRing status bit will be written back to HD Audio controller upon system power up.
10	<b>llb_en.</b> Read-write. Reset: 0. If set, LLB function is enabled, and system won't wakeup from ACPI S state until LLB# is de-asserted.
9:8	<b>temp_polarity.</b> Read-write. Reset: 0h. <b>Description:</b> Temperature polarity control for THRMTRIP and TALERT respectively. 0: Active low 1: Active high
7	Reserved.
6	<b>twarnen.</b> Read-write. Reset: 0. If set, it enables TALERT# pin
5	Reserved.
4	<b>en_slv_iso_therm_fast.</b> Read-write. Reset: 0. This bit is used by Slave Die only, for Master Die, this bit is dummy register bit.
3	<b>tdeaden.</b> Read-write. Reset: 1. When set, GEVENT2 takes up the THRMTRIP function. When THRMTRIP pin is low and TFATAL_EN(bit2 of the same register) is set, hardware will switch the system to S5 automatically.
2	<b>tfatal_en.</b> Read-write. Reset: 1. This bit enables both the soft PCIRST and the THRMTRIP function.
1	<b>instatntoffenable.</b> Read-write. Reset: 0. Enable fast shutdown upon THERMTRIP# event
0	<b>cpu_io_pulldowndrvstrength.</b> Read-write. Reset: 0. When set, the integrated pull-down drive strength of all CPU Ios are increased by 50%.

**PMx000000CC (FCH::PM::SOFTFASTRST)**

Read-write. Reset: 4FFF\_FFEh.

\_aliasHOSTLEGACY; PMx000000CC; PM=FED8\_0300h

Bits	Description
31	<b>softfastrst</b> . Read-write. Reset: 0. Write 1'b1 to this bit to trigger a Soft Fast Reset to the S0 components corresponding to SoftFastRst[21:0]. SoftFastRst[21:0] need to be configured properly before use this function.
30:28	Reserved.
27	<b>softfastrstdisable_for_pci</b> . Read-write. Reset: 1. <b>Description:</b> set this bit as 1'b1/1'b0 to disable/enable Soft Fast Reset for Pci Reset When this bit is asserted, SoftFastRstCounter(PMIOxD0) should be at least 0x12C to ensure the hardware works well.
26	Reserved.
25	<b>softfastrstdisable_for_nb</b> . Read-write. Reset: 1. set this bit as 1'b1/1'b0 to disable/enable Soft Fast Reset for NB
24	<b>softfastrstdisable_for_emmc</b> . Read-write. Reset: 1. set this bit as 1'b1/1'b0 to disable/enable Soft Fast Reset for eMMC
23	<b>softfastrstdisable_for_espi</b> . Read-write. Reset: 1. set this bit as 1'b1/1'b0 to disable/enable Soft Fast Reset for eSPI
22	<b>softfastrstdisable_for_uart3</b> . Read-write. Reset: 1. set this bit as 1'b1/1'b0 to disable/enable Soft Fast Reset for UART3
21	<b>softfastrstdisable_for_sd1</b> . Read-write. Reset: 1. set this bit as 1'b1/1'b0 to disable/enable Soft Fast Reset for SD1
20	<b>softfastrstdisable_for_espi1</b> . Read-write. Reset: 1. set this bit as 1'b1/1'b0 to disable/enable Soft Fast Reset for eSPI
19	<b>softfastrstdisable_for_i3c0</b> . Read-write. Reset: 1. set this bit as 1'b1/1'b0 to disable/enable Soft Fast Reset for I3C0
18	<b>softfastrstdisable_for_uart4</b> . Read-write. Reset: 1. set this bit as 1'b1/1'b0 to disable/enable Soft Fast Reset for UART4
17	<b>softfastrstdisable_for_amba</b> . Read-write. Reset: 1. set this bit as 1'b1/1'b0 to disable/enable Soft Fast Reset for AMBA
16	<b>softfastrstdisable_for_uart2</b> . Read-write. Reset: 1. set this bit as 1'b1/1'b0 to disable/enable Soft Fast Reset for UART2
15	<b>softfastrstdisable_for_i3c3</b> . Read-write. Reset: 1. set this bit as 1'b1/1'b0 to disable/enable Soft Fast Reset for I3C3
14	<b>softfastrstdisable_for_i3c2</b> . Read-write. Reset: 1. set this bit as 1'b1/1'b0 to disable/enable Soft Fast Reset for I3C2
13	<b>softfastrstdisable_for_i3c1</b> . Read-write. Reset: 1. set this bit as 1'b1/1'b0 to disable/enable Soft Fast Reset for I3C1
12	<b>softfastrstdisable_for_uart1</b> . Read-write. Reset: 1. set this bit as 1'b1/1'b0 to disable/enable Soft Fast Reset for UART1
11	<b>softfastrstdisable_for_uart0</b> . Read-write. Reset: 1. set this bit as 1'b1/1'b0 to disable/enable Soft Fast Reset for UART0
10	<b>softfastrstdisable_for_i2c5</b> . Read-write. Reset: 1. set this bit as 1'b1/1'b0 to disable/enable Soft Fast Reset for I2C5
9	<b>softfastrstdisable_for_i2c4</b> . Read-write. Reset: 1. set this bit as 1'b1/1'b0 to disable/enable Soft Fast Reset for I2C4
8	<b>softfastrstdisable_for_i2c3</b> . Read-write. Reset: 1. set this bit as 1'b1/1'b0 to disable/enable Soft Fast Reset for I2C3
7	<b>softfastrstdisable_for_i2c2</b> . Read-write. Reset: 1. set this bit as 1'b1/1'b0 to disable/enable Soft Fast Reset for I2C2



6	<b>softfastrstdisable_for_i2c1</b> . Read-write. Reset: 1. set this bit as 1'b1/1'b0 to disable/enable Soft Fast Reset for I2C1
5	<b>softfastrstdisable_for_i2c0</b> . Read-write. Reset: 1. set this bit as 1'b1/1'b0 to disable/enable Soft Fast Reset for I2C0
4	Reserved.
3	<b>softfastrstdisable_for_acpi_s5</b> . Read-write. Reset: 1. set this bit as 1'b1/1'b0 to disable/enable Soft Fast Reset for ACPI_S5
2	<b>softfastrstdisable_for_acpi_s0</b> . Read-write. Reset: 1. set this bit as 1'b1/1'b0 to disable/enable Soft Fast Reset for ACPI_S0
1	<b>softfastrstdisable_for_ab</b> . Read-write. Reset: 1. set this bit as 1'b1/1'b0 to disable/enable Soft Fast Reset for AB
0	Reserved.

**PMx000000D0 (FCH::PM::SOFTFASTRSTCOUNTER)**

Read-write. Reset: 0064h.

\_aliasHOSTLEGACY; PMx000000D0; PM=FED8\_0300h

Bits	Description
15:10	Reserved.
9:0	<b>softfastrstcounter</b> . Read-write. Reset: 064h. Duration of Soft Fast Reset, countered by PciClk

**PMx000000D2 (FCH::PM::PMIODEBUG)**

Read-write. Reset: 30h.

\_aliasHOSTLEGACY; PMx000000D2; PM=FED8\_0300h

Bits	Description
7	Reserved.
6	<b>cf9rstdisable</b> . Read-write. Reset: 0. When set, write to CF9 will not generate a reset. The purpose of this bit is to allow BIOS to trap CF9
5:0	Reserved.

**PMx000000D4 (FCH::PM::PWRRSTDEBSEL)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; PMx000000D4; PM=FED8\_0300h

Bits	Description
7:5	Reserved.
4:0	<b>debugseldev</b> . Read-write. Reset: 00h. Debug Bus Select for PwrRst signals

**PMx000000D5 (FCH::PM::ALTMMMIOEN)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; PMx000000D5; PM=FED8\_0300h

Bits	Description
7:3	Reserved.
2	<b>lock_wr</b> . Read-write. Reset: 0. <b>Description:</b> 0: PMxD4[31:8] can be written. 1: PMxD4[31:8] cannot be written All bits of PMxD5 ~ PMxD7 are reset by S5Reset, except this bit. This bit is default to be reset by PciReset when PMx50[5] ==0, when PMx50[5] ==1, this bit is reset by S5Reset.
1	<b>alt_addr_width_sel</b> . Read-write. Reset: 0. <b>Description:</b> 1h : alternate address is 64bit width, 0h : alternate address is 32bit width. Value will be locked when PMxD5[2] =1
0	<b>alt_addr_en</b> . Read-write. Reset: 0. <b>Description:</b> Alternate address enable bit. Value will be locked when PMxD5[2] =1

**PMx000000D6 (FCH::PM::ALTMIOBASE)**

Read-write. Reset: 0000h.

\_aliasHOSTLEGACY; PMx000000D6; PM=FED8\_0300h

Bits	Description
15:0	<b>lower_addr_alt.</b> Read-write. Reset: 0000h. <b>Description:</b> Lower bits of base address. Its value only take effect when alternate address is enabled. For example, when it is set as 0xABCD and alternate address width is 32bit, base address will be 0xABCD_0000. If it is 64 bit then the base address is 0xFFFF_FFFF_ABCD_0000. Value will be locked when PMxD5[2] =1

**PMx000000D8 (FCH::PM::EPROM\_EFUSEINDEX)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; PMx000000D8; PM=FED8\_0300h

Bits	Description
7:0	Reserved.

**PMx000000D9 (FCH::PM::EPROM\_EFUSEDATA)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; PMx000000D9; PM=FED8\_0300h

Bits	Description
7:0	Reserved.

**PMx000000DA (FCH::PM::SATACONFIG)**

Read-write. Reset: 0011h.

\_aliasHOSTLEGACY; PMx000000DA; PM=FED8\_0300h

Bits	Description
15:8	<b>pmio_xda_sataconfig.</b> Read-write. Reset: 00h. Not used.
7:6	<b>ref_div_sel.</b> Read-write. Reset: 0h. <b>Description:</b> This is CP_PLL_CLKR, the reference clock divider setting. 00: Divide by 1 (25MHz reference clock) 01: Divide by 2 10: Divide by 4 (100MHz reference clock) 11: Same as 10
5:4	<b>ref_clk_sel.</b> Read-write. Reset: 1h. <b>Description:</b> This is CP_PLL_REFCLK_SEL, the reference clock source selection for SATA PLL. 00/10: Reference clock from crystal oscillator via PAD_XTALI and PAD_XTALO 01: Reference clock from internal clock through CP_PLL_REFCLK_P and CP_PLL_REFCLK_N via RDL 11: same as 01
3	<b>hiddenide.</b> Read-write. Reset: 0. <b>Description:</b> 0: IDE controller is exposed and Combined Mode is enabled. SATA controller has control over Port0 through Port3, IDE controller has control over Port4 and Port5 1: IDE controller is hidden and Combined Mode is disabled, SATA controller has full control of all 6 Ports when operating in non-IDE mode
2	<b>setmaxgen2.</b> Read-write. Reset: 0. <b>Description:</b> 0: SATA controller operates in maximum Gen3 (3.0Gbps) speed 1: SATA controller operates in maximum Gen2 (3.0Gbps) speed and saves more power on PLL.
1	<b>channel_sel.</b> Read-write. Reset: 0. <b>Description:</b> 0: SATA Port4 and Port5 utilizing Primary IDE channel 1: SATA Port4 and Port5 utilizing Secondary IDE channel
0	<b>sataenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: SATA controller is disabled 1: SATA controller is enabled

**PMx000000DC (FCH::PM::PMIO\_XDC\_SATACONFIG)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; PMx000000DC; PM=FED8\_0300h

Bits	Description
31:0	<b>pmio_xdc_sataconfig.</b> Read-write. Reset: 0000_0000h. <b>Description:</b> Used by Sata DEVSLP. This register only reset by RsmRstB or UsrRstB, BIOS need to clear this register to 0x0 after WarmReset so that device can response with SATA controller's <a href="#">OOB</a> .

**PMx000000E0 (FCH::PM::ABREGBAR)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; PMx000000E0; PM=FED8\_0300h

Bits	Description
31:16	Reserved.
15:3	<b>abregbar.</b> Read-write. Reset: 0000h. The 13 bits are mapped into AB IO base[15:3]. AB IO Base [2:0] are tied to 0.
2:0	Reserved.

**PMx000000E4 (FCH::PM::ABDEBUG)**

Read-write. Reset: 0000h.

\_aliasHOSTLEGACY; PMx000000E4; PM=FED8\_0300h

Bits	Description
15	<b>ab_jtagmuxhost_en.</b> Read-write. Reset: 0. oAB_JtagMuxHost_en
14:7	Reserved.
6	<b>sdpdebugmode.</b> Read-write. Reset: 0. Select the SDP Debug mode.
5	<b>sdpdebugen.</b> Read-write. Reset: 0. Enable the SDP Debug mode.
4	<b>reqfilteron.</b> Read-write. Reset: 0. Not used.
3:2	<b>arbcontrol.</b> Read-write. Reset: 0h. Not used.
1:0	<b>blinkcontrol.</b> Read-write. Reset: 0h. <b>Description:</b> Control the behavior on Blink pad. // 00 off // 01 hz, // 10 hz, // 11 always on

**PMx000000E6 (FCH::PM::DACCNTL)**

Read-write. Reset: 0001h.

\_aliasHOSTLEGACY; PMx000000E6; PM=FED8\_0300h

Bits	Description
15:0	<b>daccntrl.</b> Read-write. Reset: 0001h. For VGA tile

**PMx000000EA (FCH::PM::UFSCNTRL)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; PMx000000EA; PM=FED8\_0300h

Bits	Description
7:4	Reserved.
3	<b>mphy_pwrokvddc</b> . Read-write. Reset: 0. <b>Description:</b> 0: No deassertion or don't force PwrOkVddc going to MPHY to low 1: Deassert or force PwrOkVddc going to MPHY to low
2	<b>mphy_cpbypassrefclk_en</b> . Read-write. Reset: 0. <b>Description:</b> 0: Pad is output or Enable 26MHz output or Disable BypRefClk input 1: Pad is input or Disable 26MHz output or Enable BypRefClk input
1	<b>byp_mphy_debugbus</b> . Read-write. Reset: 0. <b>Description:</b> 0: Don't Bypass MPHY DSM Debug Bus 1: Bypass MPHY DSM Debug Bus
0	<b>dis26mhzpadgt</b> . Read-write. Reset: 0. <b>Description:</b> 0: Enable 26MHz pad gating as per design logic 1: Disable 26MHz pad gating and always enable 26 MHz output

**PMx000000EB (FCH::PM::AZEN)**

Read-write. Reset: 01h.

\_aliasHOSTLEGACY; PMx000000EB; PM=FED8\_0300h

Bits	Description
7:2	Reserved.
1	<b>aznosnoopenable</b> . Read-write. Reset: 0. <b>Description:</b> When set, HD AUDIO data transfer will not cause the BM_STS bit to be set and to wake up the CPU from C3 state. Under current C1e implementation, there is no need to set this bit.
0	<b>azenable</b> . Read-write. Reset: 1. <b>Description:</b> 0: Disable HD audio controller 1: Enable HD audio controller

**PMx000000ED (FCH::PM::USBGATING)**

Read-write. Reset: 04h.

\_aliasHOSTLEGACY; PMx000000ED; PM=FED8\_0300h

Bits	Description
7	Reserved.
6	<b>usb_smiact_en</b> . Read-write. Reset: 0. Not used.
5	<b>undo_smi_change</b> . Read-write. Reset: 0. Not used.
4	<b>usb_smi_en</b> . Read-write. Reset: 0. Set to 1 to enable USB <a href="#">SMI</a> #.
3	<b>usb_pme_gate</b> . Read-write. Reset: 0. XHC0/1 PME gate. Set to 1 will block the PME.
2	<b>pmio_ohci_arb_req_q_vld_en</b> . Read-write. Reset: 1. Not used.
1	<b>usb_irq_en</b> . Read-write. Reset: 0. Set to 1 to route IRQ1/IRQ12 from usb to PIC/IOAPIC.
0	<b>usb_a20_en</b> . Read-write. Reset: 0. Set to 1 to enable USB A20#.

**PMx000000EE (FCH::PM::USB3CNTRL)**

Read-write.

\_aliasHOSTLEGACY; PMx000000EE; PM=FED8\_0300h

Bits	Description
7:6	Reserved.
5:4	<b>xhc1powersel.</b> Read-write. Reset: 0h.
	<b>Description:</b> 00: oXhc1S5RstB assert when CF9, KbRst, RsmRst, UsrRstB, S5, S3, Power saving mode. 01: oXhc1S5RstB assert when CF9, KbRst, RsmRst, UsrRstB, S5. 10: oXhc1S5RstB assert when CF9, KbRst, RsmRst, UsrRstB. 11: oXhc1S5RstB assert when CF9, KbRst, RsmRst, UsrRstB.
3	<b>usb3efusstat.</b> Read-write. Reset: X. Read-Only. This bit means "USB3 is Efuse-enabled"
2	Reserved.
1:0	<b>xhc0powersel.</b> Read-write. Reset: 0h.
	<b>Description:</b> 00: oXhc0S5RstB assert when CF9, KbRst, RsmRst, UsrRstB, S5, S3, Power saving mode. 01: oXhc0S5RstB assert when CF9, KbRst, RsmRst, UsrRstB, S5. 10: oXhc0S5RstB assert when CF9, KbRst, RsmRst, UsrRstB. 11: oXhc0S5RstB assert when CF9, KbRst, RsmRst, UsrRstB.

**PMx000000EF (FCH::PM::USBDEBUG)**

Read-write. Reset: 7Fh.

\_aliasHOSTLEGACY; PMx000000EF; PM=FED8\_0300h

Bits	Description
7:0	<b>s3_usbenable.</b> Read-write. Reset: 7Fh. Not used

**PMx000000F0 (FCH::PM::USBCONTROL)**

Read-write. Reset: 739Ch.

\_aliasHOSTLEGACY; PMx000000F0; PM=FED8\_0300h

Bits	Description
15:13	Reserved.
12	<b>usb2blglobalclkgateen.</b> Read-write. Reset: 1. Set to 1 to enable USB2 B-Link Global Clock Gating
11	Reserved.
10:8	<b>usbsleepctrl.</b> Read-write. Reset: 3h. <b>Description:</b> Control on USB advanced async sleep function. Setting of 000b:100b are for the advanced async sleep. 000b: Standard 10s sleep 001b: Advanced sleep up to 2 uframes 010b: Advanced sleep up to 4 uframes 011b: Advanced sleep up to 6 uframes (default) 100b: Advanced sleep up to next uframe 0 101b, 110b: Reserved 111b: EHCI will stop fetching descriptor once it has completed the list while CPU is in C state.
7	<b>usbresumeenable.</b> Read-write. Reset: 1. Set to 1 to enable S3 wakeup on USB device resume.
6	<b>usbs3wakeresumeonlydisable.</b> Read-write. Reset: 0. Default (0) is to support USB Wake-Up event on Resume only. When set to 1, USB can wakeup on all wake events, connection, disconnect, over-current, and/or resume detect.
5	<b>pmio_ohci_mem_slp_dis.</b> Read-write. Reset: 0. <b>Description:</b> 0: enable OHCI memory sleep mode 1: disable OHCI memory sleep mode
4	<b>usb11pdresistorenable.</b> Read-write. Reset: 1. Set to 0 to disconnect pull-down resistors on stand-alone USB1.1 pads.
3	<b>usbs5resetenable.</b> Read-write. Reset: 1. Set to 1 to enable USB reset on S4/S5 resume detection.
2	<b>usbkbresetenable.</b> Read-write. Reset: 1. Set to 1 to enable resetting USB on KB reset.
1	<b>usbforceregenable.</b> Read-write. Reset: 0. This function is not implemented.
0	<b>usbphys5pwrdownenable.</b> Read-write. Reset: 0. <b>Description:</b> Set to 1 to disable S4/S5 USB PHY power down support and to enable S4 USB wakeup support. The bit has to be set to 1 to support S4 USB wakeup.

**PMx000000F2 (FCH::PM::USBCONTROL\_1)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; PMx000000F2; PM=FED8\_0300h

Bits	Description
7:0	Reserved.

**PMx000000F3 (FCH::PM::USBDEBUG\_2)**

Read-write. Reset: 00h.

\_aliasHOSTLEGACY; PMx000000F3; PM=FED8\_0300h

Bits	Description
7	<b>forcephyportreset.</b> Read-write. Reset: 0. Forces USB PHY port reset.
6	<b>forcephyearlyreset.</b> Read-write. Reset: 0. Forces USB PHY early reset.
5	<b>forcephydllreset.</b> Read-write. Reset: 0. Forces USB PHY DLL reset.
4	<b>forcephypllreset.</b> Read-write. Reset: 0. Forces USB PHY PLL reset.
3	<b>forcephyprdown.</b> Read-write. Reset: 0. Forces USB PHY into power down mode.
2:0	<b>forcereset2usb.</b> Read-write. Reset: 0h. These are software control bits that can be used to force resetting of USB host controllers. Each bit corresponds to one USB major function.

**PMx000000F4 (FCH::PM::USBCONTROL\_2)**

Read-write. Reset: 0000h.

\_aliasHOSTLEGACY; PMx000000F4; PM=FED8\_0300h

Bits	Description
15:3	Reserved.
2	<b>usb_s3_ohci_discon_fix</b> . Read-write. Reset: 0. Not used.
1	<b>ohci_hidden_enable</b> . Read-write. Reset: 0. <b>Description:</b> This bit is used to hide OHCI controllers inside USB2.0. 0: USB2.0 contains OHCI and EHCIs. 1: All OHCI controllers inside USB2.0 are hidden and only EHCI controller exist as single function. Not used.
0	<b>usb_s3_dis_con_wo_wakeen</b> . Read-write. Reset: 0. <b>Description:</b> Set to open EHCI/OHCI S3 disconnect and connect fix. Not used.

**PMx000000F6 (FCH::PM::OTGCFG)**

Read-write. Reset: 0000h.

\_aliasHOSTLEGACY; PMx000000F6; PM=FED8\_0300h

Bits	Description
15:2	Reserved.
1:0	<b>otgpowersel</b> . Read-write. Reset: 0h. <b>Description:</b> 00: oOtgS5RstB assert when CF9, KbRst, RsmRst, UsrRstB, S5, S3, Power saving mode. 01: oOtgS5RstB assert when CF9, KbRst, RsmRst, UsrRstB, S5. 10: oOtgS5RstB assert when CF9, KbRst, RsmRst, UsrRstB. 11: oOtgS5RstB assert when CF9, KbRst, RsmRst, UsrRstB.

**PMx000000F8 (FCH::PM::SPBBASE)**

Read-write. Reset: FEF0\_003Fh.

\_aliasHOSTLEGACY; PMx000000F8; PM=FED8\_0300h

Bits	Description
31:0	<b>spbs5cntrl</b> . Read-write. Reset: FEF0_003Fh. Not used.

**PMx000000FC (FCH::PM::TRACEMEMORYEN)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; PMx000000FC; PM=FED8\_0300h

Bits	Description
31:20	<b>tracememorybaseaddr</b> . Read-write. Reset: 000h. The base address of trace memory in ILA (Internal Logic Analyzer) connect to ILA.ILA_Mem_Addr. It is 1M memory space.
19:1	Reserved.
0	<b>tracememoryen</b> . Read-write. Reset: 0. Set to 1 to enable trace memory decoding in ILA (Internal Logic Analyzer), connect to ILA.Acpi2ILA_Enable

**PMx00000500 (FCH::PM::PM1STATUS)**

Read-write.

This register is located at the base address defined by AcpiPm1EvtBlk.

\_aliasHOSTLEGACY; PMx00000500; PM=FED8\_0300h

Bits	Description
15	<b>wakestatus.</b> Read-write. Reset: 0. This bit is set when the system is in the sleep state and a wake-up event occurs.
14	<b>pciexpwakestatus.</b> Read-write. Reset: 0. This bit is set by hardware to indicate that the system wake is due to a PCI Express® wakeup event.
13:11	Reserved.
10	<b>rtcstatus.</b> Read-write. Reset: 0. This bit is set when RTC generates an alarm.
9	Reserved.
8	<b>pwrbtnstatus.</b> Read-write. Reset: 0. Power button status bit
7:6	Reserved.
5	<b>gblstatus.</b> Read-write. Reset: 0. This bit is set when an SCI is generated due to the BIOS wanting the attention of the SCI handler. This is set by writing 1 to PM_Reg: 74h bit [7].
4	<b>bmstatus.</b> Read-write. Reset: 0. Bus master status bit. This bit is set any time a system bus master requests the system bus, and can only be cleared by writing an one to this bit position. Note: this bit is no longer used except for server CPU. For server CPU, this will be used in conjunction with IDLE_EXIT# pin
3:1	Reserved.
0	<b>tmrstatus.</b> Read-write. Reset: 0. Timer carry status bit. This bit gets set anytime the 31st bit of 32 bit counter changes (whenever the MSB changes from low to high or high to low. While TmrEn and TmrStatus are set, an interrupt event is raised). [Read-only]

**PMx00000502 (FCH::PM::PM1ENABLE)**

Read-write.

This register is located at the base address defined by AcpiPm1EvtBlk.

\_aliasHOSTLEGACY; PMx00000502; PM=FED8\_0300h

Bits	Description
15	Reserved.
14	<b>pciexpwakedis.</b> Read-write. Reset: 1. This bit disables the inputs to the PciExpWakeStatus from waking the system.
13:11	Reserved.
10	<b>rtcen.</b> Read-write. Reset: 0. RTC enable. If this bit is set, SCI is generated whenever RtcStatus is true.
9	Reserved.
8	<b>pwrbtnen.</b> Read-write. Reset: 0. If this bit is set, SCI is generated whenever PwrBtnStatus is true.
7:6	Reserved.
5	<b>gblen.</b> Read-write. Reset: 0. If this bit is set, SCI is raised whenever both GblEn and GblStatus are true.
4:1	Reserved.
0	<b>tmren.</b> Read-write. Reset: 0. This is the timer carry interrupt enable bit. When this bit is set then an SCI event is generated anytime the TmrStatus is set. When this bit is reset then no interrupt is generated when the TmrStatus bit is set.



**PMx00000504 (FCH::PM::PMCONTROL)**

Read-write.

This register is located at the base address defined by AcpiPm1CntBlk (PM\_Reg:62h).

\_aliasHOSTLEGACY; PMx00000504; PM=FED8\_0300h

Bits	Description
15:14	Reserved.
13	<b>slp_en.</b> Read-write. Reset: 0. <b>Description:</b> This is a write-only bit and reads from it always return zero. If PM_Reg:Beh bit5 (SLP_TYP_EN) is 1 (default), setting this bit will cause the system to sequence into the sleeping state associated with the SLP_TYP fields programmed. Writing 0 to this bit has no effect.
12:10	<b>slp_typ.</b> Read-write. Reset: 0h. Defines the sleep state the system enters when the SLP_TYPEn is set to one. This design currently implements 5 states: S0, S1, S3, S4, and S5.
9:3	Reserved.
2	<b>gbl_rls.</b> Read-write. Reset: 0. If SMI_Reg:B0h[17:16] is set to 01b, writing 1 to this bit will generate <a href="#">SMI#</a> and set SMI_Reg:88h bit[8]. Reading, this bit will always return 0.
1	<b>bmrlld.</b> Read-write. Reset: 0. If this bit is set, any bus master activity will cause the C state logic to break out from C3. This is no longer needed for current C state implementation
0	<b>sci_en.</b> Read-write. Reset: 0. Selects the power management event to be either an SCI or <a href="#">SMI#</a> interrupt for the following events. When this bit is set, then PM events will generate an SCI interrupt otherwise, it will be SMI#.

**PMx00000508 (FCH::PM::TMRVALUE\_ETMRVALUE)**

Read-only.

AcpiPmTmrBlk is defined in PM\_Reg:64h

\_aliasHOSTLEGACY; PMx00000508; PM=FED8\_0300h

Bits	Description
31:0	<b>tmrvalue.</b> Read-only. Reset: XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXb. This read-only field returns the running count of the power management timer (ACPI timer).

**PMx0000050C (FCH::PM::CLKVALUE)**

Read-write. Reset: 0000\_0000h.

CpuControl Io base is defined in PM\_Reg 0x66

\_aliasHOSTLEGACY; PMx0000050C; PM=FED8\_0300h

Bits	Description
31:0	Reserved.

**PMx00000510 (FCH::PM::PLVL2)**

Read-only. Reset: 00h.

CpuControl Io base is defined in PM\_Reg 0x66

\_aliasHOSTLEGACY; PMx00000510; PM=FED8\_0300h

Bits	Description
7:0	<b>plvl2.</b> Read-only. Reset: 00h. Reads to this register return all zeros and generate a "enter C2" sequence to APU writes to this register have no effect.

**PMx00000511 (FCH::PM::PLVL3)**

Read-only. Reset: 00h.

CpuControl Io base is defined in PM\_Reg 0x66

\_aliasHOSTLEGACY; PMx00000511; PM=FED8\_0300h

Bits	Description
7:0	<b>plvl3.</b> Read-only. Reset: 00h. Reads to this register return all zeros and generate a "enter C3" sequence to APU writes to this register have no effect.

**PMx00000514 (FCH::PM::EVENT\_STATUS\_STDACPI)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; PMx00000514; PM=FED8\_0300h

Bits	Description
31:0	<b>eventstatus.</b> Read-write. Reset: 0000_0000h. Each bit represents an ACPI event status. Writing 1 to any bit clears it. Each event status is set when the selected event input equals to the corresponding value in SciTrig. Note: configuration for EVENTS are located at SMI_Reg: 08h through 70h. The status bits are also mirrored in SMI_Reg: 00h

**PMx00000518 (FCH::PM::EVENT\_ENABLE\_STDACPI)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; PMx00000518; PM=FED8\_0300h

Bits	Description
31:0	<b>eventenable.</b> Read-write. Reset: 0000_0000h. Each bit controls whether ACP should generate wakeup and Sci interrupt. The enable bits are also mirrored in SMI_Reg: 04h

**PMx0000051C (FCH::PM::SMICMDPORT)**

Read-write. Reset: 00h.

This register is located at the base address defined by AcpiSmiCmd [PM\_Reg:6Ah] + offset 0. When **SMI** command port is enabled, write to this port will generate SMI# (only IOW can generate SMI#, MEMW will not generate SMI#). A read of this address will return the previously written value but will not generate SMI. The SMI command port has to be located at an even address (ie, 0, 2, 4, 6, 8, A, C, or E). SmiCmdStatus is always located one byte immediately after the SmiCmdPort. The implementation actually contains four (4) bytes of address space. If SMI command port is assigned to byte 0, then byte 1 is SmiCmdStatus. Byte 2 and 3 can be used as scratch. If SmiCmdPort is assigned to byte 2, then bytes 0 and 1 are not available.

\_aliasHOSTLEGACY; PMx0000051C; PM=FED8\_0300h

Bits	Description
7:0	<b>smicmdport.</b> Read-write. Reset: 00h. Writing the Port can generate Smi.

**PMx0000051D (FCH::PM::SMICMDSTATUS)**

Read-write. Reset: 00h.

This register is located at the base address defined by AcpiSmiCmd [PM\_Reg:6Ah] + offset 1.

\_aliasHOSTLEGACY; PMx0000051D; PM=FED8\_0300h

Bits	Description
7:0	<b>smicmdstatus.</b> Read-write. Reset: 00h. Used by BIOS and OS

**PMx00000524 (FCH::PM::PMACONTROL)**

Read-write.

AcpiPmaCntBlk is defined in PM\_Reg:6Eh

\_aliasHOSTLEGACY; PMx00000524; PM=FED8\_0300h

Bits	Description
7:1	Reserved.
0	<b>arb_dis.</b> Read-write. Reset: 0. System arbiter is disabled when this bit is set. Note: under this current AMD C state implementation, this is no longer used and should not be reported to OS.

**PMx00000528 (FCH::PM::PMACONTROL\_1)**

Read-write.

AcpiPmaCntBlk is defined in PM\_Reg:6Eh

\_aliasHOSTLEGACY; PMx00000528; PM=FED8\_0300h

Bits	Description
7:1	Reserved.
0	<b>arb_dis2.</b> Read-write. Reset: 1. System arbiter is disabled when this bit is set if ARB_DIS is also set. This bit is hidden from OS and meant to be used by BIOS.

## 11.3.9.4 RTC External Registers

PMx5F_x00 [RTCEXT DltSavEn] (FCH::PM::RTCEXT::RTCEXTDltSavEn)	
Read-write.	
_aliasHOSTLEGACY; PMx5F_x00; PM=FED8_0300h; DataPortWrite=FCH::PM::RTCEXTINDEX	
Bits	Description
7:1	Reserved.
0	<b>DltSavEnable</b> . Read-write. Reset: X. 1=Enable RTC daylight saving feature. The value of this register is undefined/non-deterministic when powered up for the first time.

  

PMx5F_x01 [RTCEXT SprFwdCtrl] (FCH::PM::RTCEXT::RTCEXTSprFwdCtrl)											
Read-write.											
_aliasHOSTLEGACY; PMx5F_x01; PM=FED8_0300h; DataPortWrite=FCH::PM::RTCEXTINDEX											
Bits	Description										
7	Reserved.										
6	<b>SprFwdWeek</b> . Read-write. Reset: X. This specifies which Sunday morning to do the "spring forward". Spring forward is usually at the 1st Sunday of April in United States and last Sunday of March in Europe. 0=The 1st Sunday of the month. 1=The last Sunday of the month. The value of this register is undefined/non-deterministic when powered up for the first time.										
5:0	<b>SprFwdHour</b> . Read-write. Reset: XXXXXXb. <b>Description:</b> This Binary-Coded Decimal ( <a href="#">BCD</a> ) value determines which hour (24 hour mode) to do the "spring forward". Setting of 02h means 2am. Default is 00h which also denotes 2am. Spring forward is usually 2am in United States and 1am in Europe. Note: the value of this register is undefined/indeterministic when power up first time. <b>ValidValues:</b> <table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>00h</td><td>2AM.</td></tr> <tr> <td>01h</td><td>1AM.</td></tr> <tr> <td>02h</td><td>2AM.</td></tr> <tr> <td>3Fh-03h</td><td>Reserved.</td></tr> </table>	Value	Description	00h	2AM.	01h	1AM.	02h	2AM.	3Fh-03h	Reserved.
Value	Description										
00h	2AM.										
01h	1AM.										
02h	2AM.										
3Fh-03h	Reserved.										

  

PMx5F_x02 [RTCEXT SprFwdMonth] (FCH::PM::RTCEXT::RTCEXTSprFwdMonth)							
Read-write.							
_aliasHOSTLEGACY; PMx5F_x02; PM=FED8_0300h; DataPortWrite=FCH::PM::RTCEXTINDEX							
Bits	Description						
7:5	Reserved.						
4:0	<b>SprFwdMonth</b> . Read-write. Reset: XXXXXb. This Binary-Coded Decimal ( <a href="#">BCD</a> ) value determines which month to do the "spring forward". The value of this register is undefined/non-deterministic when powered up for the first time. <b>ValidValues:</b> <table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0</td><td>April</td></tr> <tr> <td>1</td><td>March</td></tr> </table>	Value	Description	0	April	1	March
Value	Description						
0	April						
1	March						

**PMx5F\_x03 [RTCEXT FallBackCtrl] (FCH::PM::RTCEXT::RTCEXTFallBackCtrl)**

Read-write.

\_aliasHOSTLEGACY; PMx5F\_x03; PM=FED8\_0300h; DataPortWrite=FCH::PM::RTCEXTINDEX

Bits	Description																																																										
7	Reserved.																																																										
6	<b>FallBackWeek.</b> Read-write. Reset: X. 0=The last week of the month. 1=The first week of the month. This value specifies which Sunday morning to do the "fall back". The value of this register is undefined/non-deterministic when powered up for the first time.																																																										
5:0	<p><b>FallBackHour.</b> Read-write. Reset: XXXXXXb. This Binary-Coded Decimal (<a href="#">BCD</a>) value specifies which hour (24 hour mode) to do the "fall back". Fall back is usually 2 AM in United States and 1 AM in Europe. 02h=2 AM. The value of this register is undefined/non-deterministic when powered up for the first time.</p> <p><b>ValidValues:</b></p> <table> <tr> <th>Value</th><th>Description</th></tr> <tr><td>00h</td><td>2 am</td></tr> <tr><td>01h</td><td>1 am</td></tr> <tr><td>02h</td><td>2 am</td></tr> <tr><td>03h</td><td>3 am</td></tr> <tr><td>04h</td><td>4 am</td></tr> <tr><td>05h</td><td>5 am</td></tr> <tr><td>06h</td><td>6 am</td></tr> <tr><td>07h</td><td>7 am</td></tr> <tr><td>08h</td><td>8 am</td></tr> <tr><td>09h</td><td>9 am</td></tr> <tr><td>0Fh-0Ah</td><td>Reserved.</td></tr> <tr><td>10h</td><td>10 am</td></tr> <tr><td>11h</td><td>11 am</td></tr> <tr><td>12h</td><td>Noon</td></tr> <tr><td>13h</td><td>1 pm</td></tr> <tr><td>14h</td><td>2 pm</td></tr> <tr><td>15h</td><td>3 pm</td></tr> <tr><td>16h</td><td>4 pm</td></tr> <tr><td>17h</td><td>5 pm</td></tr> <tr><td>18h</td><td>6 pm</td></tr> <tr><td>19h</td><td>7 pm</td></tr> <tr><td>1Fh-1Ah</td><td>Reserved.</td></tr> <tr><td>20h</td><td>8 pm</td></tr> <tr><td>21h</td><td>9 pm</td></tr> <tr><td>22h</td><td>10 pm</td></tr> <tr><td>23h</td><td>11 pm</td></tr> <tr><td>24h</td><td>Midnight</td></tr> <tr><td>3Fh-25h</td><td>Reserved.</td></tr> </table>	Value	Description	00h	2 am	01h	1 am	02h	2 am	03h	3 am	04h	4 am	05h	5 am	06h	6 am	07h	7 am	08h	8 am	09h	9 am	0Fh-0Ah	Reserved.	10h	10 am	11h	11 am	12h	Noon	13h	1 pm	14h	2 pm	15h	3 pm	16h	4 pm	17h	5 pm	18h	6 pm	19h	7 pm	1Fh-1Ah	Reserved.	20h	8 pm	21h	9 pm	22h	10 pm	23h	11 pm	24h	Midnight	3Fh-25h	Reserved.
Value	Description																																																										
00h	2 am																																																										
01h	1 am																																																										
02h	2 am																																																										
03h	3 am																																																										
04h	4 am																																																										
05h	5 am																																																										
06h	6 am																																																										
07h	7 am																																																										
08h	8 am																																																										
09h	9 am																																																										
0Fh-0Ah	Reserved.																																																										
10h	10 am																																																										
11h	11 am																																																										
12h	Noon																																																										
13h	1 pm																																																										
14h	2 pm																																																										
15h	3 pm																																																										
16h	4 pm																																																										
17h	5 pm																																																										
18h	6 pm																																																										
19h	7 pm																																																										
1Fh-1Ah	Reserved.																																																										
20h	8 pm																																																										
21h	9 pm																																																										
22h	10 pm																																																										
23h	11 pm																																																										
24h	Midnight																																																										
3Fh-25h	Reserved.																																																										

**PMx5F\_x04 [RTCEXT FallBackMonth] (FCH::PM::RTCEXT::RTCEXTFallBackMonth)**

Read-write.

`_aliasHOSTLEGACY; PMx5F_x04; PM=FED8_0300h; DataPortWrite=FCH::PM::RTCEXTINDEX`

Bits	Description																																
7:5	Reserved.																																
4:0	<b>FallBackMonth.</b> Read-write. Reset: XXXXXb. This Binary-Coded Decimal ( <a href="#">BCD</a> ) value specifies which month to "fall back". The value of this register is undefined/non-deterministic when powered up for the first time. <p><b>ValidValues:</b></p> <table> <tr> <th>Value</th><th>Description</th></tr> <tr><td>00h</td><td>October</td></tr> <tr><td>01h</td><td>January</td></tr> <tr><td>02h</td><td>February</td></tr> <tr><td>03h</td><td>March</td></tr> <tr><td>04h</td><td>April</td></tr> <tr><td>05h</td><td>May</td></tr> <tr><td>06h</td><td>June</td></tr> <tr><td>07h</td><td>July</td></tr> <tr><td>08h</td><td>August</td></tr> <tr><td>09h</td><td>September</td></tr> <tr><td>0Fh-0Ah</td><td>Reserved.</td></tr> <tr><td>10h</td><td>October</td></tr> <tr><td>11h</td><td>November</td></tr> <tr><td>12h</td><td>December</td></tr> <tr><td>1Fh-13h</td><td>Reserved.</td></tr> </table>	Value	Description	00h	October	01h	January	02h	February	03h	March	04h	April	05h	May	06h	June	07h	July	08h	August	09h	September	0Fh-0Ah	Reserved.	10h	October	11h	November	12h	December	1Fh-13h	Reserved.
Value	Description																																
00h	October																																
01h	January																																
02h	February																																
03h	March																																
04h	April																																
05h	May																																
06h	June																																
07h	July																																
08h	August																																
09h	September																																
0Fh-0Ah	Reserved.																																
10h	October																																
11h	November																																
12h	December																																
1Fh-13h	Reserved.																																

**PMx5F\_x10 [RTCEXT WeekTimerControl] (FCH::PM::RTCEXT::RTCEXTWeekTimerCtl)**

Read-write.

The 16-bit Week Timer is a battery-powered down counter timer that supports 1ms, 1 second, and 1minute resolution and auto reloads when the timer reaches 0. The WEEK\_ALRM interrupt is asserted when the timer reaches 0 and stays asserted until the timer is disabled.

`_aliasHOSTLEGACY; PMx5F_x10; PM=FED8_0300h; DataPortWrite=FCH::PM::RTCEXTINDEX`

Bits	Description										
7:3	Reserved.										
2:1	<b>Resolution.</b> Read-write. Reset: XXb. This field specifies the resolution of the Week Timer counter. Before programing this bit, software should program Enable to 0 to disable the Week Timer. The value of this register is undefined/non-deterministic when powered up for the first time. <p><b>ValidValues:</b></p> <table> <tr> <th>Value</th><th>Description</th></tr> <tr><td>0h</td><td>1minute</td></tr> <tr><td>1h</td><td>1second</td></tr> <tr><td>2h</td><td>1ms</td></tr> <tr><td>3h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	1minute	1h	1second	2h	1ms	3h	Reserved.
Value	Description										
0h	1minute										
1h	1second										
2h	1ms										
3h	Reserved.										
0	<b>Enable.</b> Read-write. Reset: X. 0=Disable Week Timer. 1=Enable Week Timer. The value of this register is undefined/non-deterministic when powered up for the first time.										

**PMx5F\_x11 [RTCEXT WeekTimerReloadLow] (FCH::PM::RTCEXT::RTCEXTWeekTimerReloadLo)**

Read-write.

\_aliasHOSTLEGACY; PMx5F\_x11; PM=FED8\_0300h; DataPortWrite=FCH::PM::RTCEXTINDEX

Bits	Description
7:0	<b>WeekTimerReloadLow.</b> Read-write. Reset: XXh. This field is used to program the lower 8 bits of the 16-bit WeekTimerReload register. Writing the WeekTimerReloadLow register causes the 16-bit WeekTimerReload to be written into the Week Timer. Software should program FCH::PM::RTCEXT::RTCEXTWeekTimerCtl[Enable] = 0 before writing to this register. The value of this register is undefined/non-deterministic when powered up for the first time.

**PMx5F\_x12 [RTCEXT WeekTimerReloadHigh] (FCH::PM::RTCEXT::RTCEXTWeekTimerReloadHi)**

Read-write.

\_aliasHOSTLEGACY; PMx5F\_x12; PM=FED8\_0300h; DataPortWrite=FCH::PM::RTCEXTINDEX

Bits	Description
7:0	<b>WeekTimerReloadHigh.</b> Read-write. Reset: XXh. This field is used to program the upper 8 bits of the 16-bit WeekTimerReload register. This field should be programmed before programming FCH::PM::RTCEXT::RTCEXTWeekTimerReloadLo. Software should program FCH::PM::RTCEXT::RTCEXTWeekTimerCtl[Enable] = 0 before writing to this register. The value of this register is undefined/non-deterministic when powered up for the first time.

**PMx5F\_x13 [RTCEXT WeekTimerDataLow] (FCH::PM::RTCEXT::RTCEXTWeekTimerDataLo)**

Read-only.

\_aliasHOSTLEGACY; PMx5F\_x13; PM=FED8\_0300h; DataPortWrite=FCH::PM::RTCEXTINDEX

Bits	Description
7:0	<b>WeekTimerDataLow.</b> Read-only. Reset: XXh. This field is used to read the current state of the 16-bit Week Timer. Reading from the WeekTimerDataLow register returns the lower 8 bits of the 16-bit Week Timer and causes the upper 8 bits to be latched into FCH::PM::RTCEXT::RTCEXTWeekTimerDataHi. The value of this register is undefined/non-deterministic when powered up for the first time.

**PMx5F\_x14 [RTCEXT WeekTimerDataHigh] (FCH::PM::RTCEXT::RTCEXTWeekTimerDataHi)**

Read-only.

\_aliasHOSTLEGACY; PMx5F\_x14; PM=FED8\_0300h; DataPortWrite=FCH::PM::RTCEXTINDEX

Bits	Description
7:0	<b>WeekTimerDataHigh.</b> Read-only. Reset: XXh. This field is used to read the current state of the 16-bit Week Timer. Reading from the WeekTimerDataHigh register returns the upper 8 bits of the 16-bit Week Timer latched by a previous read from FCH::PM::RTCEXT::RTCEXTWeekTimerReloadLo. The value of this register is undefined/non-deterministic when powered up for the first time.

**11.3.10 GPIO Pin control registers****11.3.10.1 IOMUX Registers****11.3.10.1.1 IOMUX Functional Table**

Table 193: IOMUX Function Table

IOMU X#	Bump Pin Name	Domain	GPIO #	GEVENT #	Override_0	Override_1	IOMU X == 0	IOMU X == 1	IOMU X == 2	IOMU X == 3	Default IO State	IOMU X value
---------	---------------	--------	--------	----------	------------	------------	-------------	-------------	-------------	-------------	------------------	--------------

												at reset
IOMU Xx0	BP_P WR_B TN_L/ AGPI O0	S5	0	21			PWR_ BTN_ L	GPIO0	GPIO0	GPIO0	PU	0
IOMU Xx1	BP_S YS_R ESET_ L/ AGPI O1	S5	1	19		RST_s trap	SYS_ RESE T_L	GPIO1	GPIO1	GPIO1	PU	0
IOMU Xx2	BP_W AKE_ L/ AGPI O2	S5	2	8			WAKE _L	GPIO2	GPIO2	GPIO2	PU	0
IOMU Xx3	BP_A GPIO3 / SPD_ HOST _CTR L_L	S5	3	2			GPIO3	GPIO3	GPIO3	GPIO3	PU	0
IOMU Xx4	BP_A GPIO4 / SATA_ ACT_ L	S5	4	4			GPIO4	SATA_ ACT_ L	GPIO4	GPIO4	PU	0
IOMU Xx5	BP_A GPIO5 / DEVS LP0/ SATA_ ZP0_L	S5	5	7			GPIO5	DEVS LP0	GPIO5	GPIO5	PD	0
IOMU Xx6	BP_A GPIO6 / DEVS LP1/ SATA_ ZP1_L	S5	6	10			GPIO6	DEVS LP1	GPIO6	GPIO6	PD	0
IOMU Xx7	BP_A GPIO7	S5	7				GPIO7	GPIO7	GPIO7	GPIO7	PD	0
IOMU XxC	BP_P WRG D_OU T/ AGPI O12	S5	12				PWRG D_OU T	GPIO1 2	GPIO1 2	GPIO1 2	n/a	0

IOMU XxD	BP_I2 C4_SC L/ HP_S CL/ UBM_ SCL/ AGPI O13	S5	13				I2C4_ SCL	GPIO1 3	GPIO1 3	GPIO1 3	n/a	0
IOMU XxE	BP_I2 C4_SD A/ HP_S DA/ UBM_ SDA/ AGPI O14	S5	14				I2C4_ SDA	GPIO1 4	GPIO1 4	GPIO1 4	n/a	0
IOMU Xx10	BP_U SB10_ OC_L/ AGPI O16	S5	16	12			USB10_ OC_ L	GPIO1 6	GPIO1 6	GPIO1 6	PU	0
IOMU Xx11	BP_U SB11_ OC_L/ AGPI O17	S5	17	13			USB11_ OC_ L	GPIO1 7	GPIO1 7	GPIO1 7	PU	0
IOMU Xx13	BP_I2 C5_SC L/ BMC_ SCL/ SMBU S1_SC L/ AGPI O19	S5	19				I2C5_ SCL	SMBU S1_SC L	GPIO1 9	GPIO1 9	n/a	1
IOMU Xx14	BP_I2 C5_SD A/ BMC_ SDA/ SMBU S1_SD A/ AGPI O20	S5	20				I2C5_ SDA	SMBU S1_SD A	GPIO2 0	GPIO2 0	n/a	1
IOMU Xx15	BP_A GPIO2 1	S5	21	5			GPIO2 1	GPIO2 1	GPIO2 1		PD	0
IOMU	BP_A	S5	22	3			GPIO2		GPIO2	GPIO2	PD	0



Xx16	GPIO2 2						2		2	2		
IOMU Xx17	BP_ES PI_RS TOUT _L/ AGPI O23	S5	23	16			ESPI_ RSTO UT_L	GPIO2 3		GPIO2 3	n/a	0
IOMU Xx18	BP_S MERR _L/ AGPI O24	S5	24	14			SMER R_L	GPIO2 4	GPIO2 4	GPIO2 4	PU	0
IOMU Xx1A	BP_PC IE_RS T1_L/ AGPI O26	S5	26	15			PCIE_ RST1_ L	GPIO2 6	GPIO2 6	GPIO2 6	n/a	0
IOMU Xx1C	BP_X4 8M_O UT/ AGPI O28	S5	28	18			X48M _OUT	GPIO2 8	GPIO2 8	GPIO2 8	PD	0
IOMU Xx4A	BP_ES PI_CL K2/ AGPI O74	S0	74				ESPI_ CLK2	GPIO7 4	GPIO7 4	GPIO7 4	PD	0
IOMU Xx4B	BP_ES PI_CL K1/ SPI_C LK1/ AGPI O75	S0	75			SPI32 Bit_str ap	ESPI_ CLK1	GPIO7 5	GPIO7 5		PD	0
IOMU Xx4C	BP_A GPIO7 6/ SPI_T PM_C S_L	S0	76	11			GPIO7 6	SPI_T PM_C S_L	GPIO7 6	GPIO7 6	PU	0
IOMU Xx56	BP_N MI_S YNC_ FLOO D_L/ AGPI O86/ LPC_S MI_L	S0	86	9			GPIO8 6	GPIO8 6	LPC_S MI_L	GPIO8 6	PU	0
IOMU Xx57	BP_A GPIO8	S0	87				GPIO8 7		GPIO8 7	GPIO8 7	PD	0

	7											
IOMU Xx58	BP_A GPIO8 8	S0	88				GPIO8 8		GPIO8 8	GPIO8 8	PD	0
IOMU Xx59	BP_G ENIN T_L/ PM_I NTR_ L/ AGPI O89	S0	89	0			GENI NT_L	PM_I NTR_ L	GPIO8 9	GPIO8 9	PU	0
IOMU Xx68	BP_A GPIO1 04	S0	104	20			GPIO1 04	GPIO1 04		GPIO1 04	PD	0
IOMU Xx69	BP_A GPIO1 05	S0	105	22			GPIO1 05	GPIO1 05		GPIO1 05	PD	0
IOMU Xx6A	BP_A GPIO1 06	S0	106	23			GPIO1 06	GPIO1 06		GPIO1 06	PD	0
IOMU Xx6B	BP_A GPIO1 07	S0	107				GPIO1 07	GPIO1 07		GPIO1 07	PD	0
IOMU Xx6C	BP_ES PI0_A LERT_ L_ESP I_IO1/ AGPI O108	S0	108			ESPI0 _ALE RT_L	ESPI0 _ALE RT_D1	GPIO1 08		GPIO1 08	PU	0
IOMU Xx6D	BP_A GPIO1 09	S0	109		ROMT YPE_s trap		GPIO1 09	GPIO1 09		GPIO1 09	PD	0
IOMU Xx6E	BP_ES PI1_A LERT_ L/ AGPI O110	S0	110			ESPI1 _ALE RT_L	ESPI1 _ALE RT_D1	GPIO1 10	GPIO1 10	GPIO1 10	PU	0
IOMU Xx73	BP_A GPIO1 15/ CLK_ REQ1 1_L	S0	115	1			GPIO1 15	CLK_ REQ1 1_L	GPIO1 15	GPIO1 15	PU	0
IOMU Xx74	BP_A GPIO1 16/ CLK_ REQ1 2_L	S0	116	6			GPIO1 16	CLK_ REQ1 2_L	GPIO1 16	GPIO1 16	PU	0

IOMU Xx75	BP_ES PI_CLK/ SPI_CLK/ AGPIO17	S0	117		CLKG EN_strap		ESPI_CLK0	GPIO1 17	GPIO1 17	GPIO1 17	PD	0
IOMU Xx76	BP_SPI_CS0_L/ AGPIO18	S0	118				SPI_CS0_L	GPIO1 18	GPIO1 18	GPIO1 18	PU	0
IOMU Xx77	BP_SPI_CS1_L/ AGPIO19	S0	119				SPI_CS1_L	GPIO1 19	GPIO1 19	GPIO1 19	PU	0
IOMU Xx78	BP_ESPI0_DAT0/ SPI0_DAT0/ AGPIO120	S0	120				ESPI0_DAT0/ SPI0_DAT0	GPIO1 20	GPIO1 20	GPIO1 20	PU	0
IOMU Xx79	BP_ESPI0_DAT1/ SPI0_DAT1/ AGPIO121	S0	121				ESPI0_DAT1/ SPI0_DAT1	GPIO1 21	GPIO1 21	GPIO1 21	PU	0
IOMU Xx7A	BP_ESPI0_DAT2/ SPI0_DAT2/ AGPIO122	S0	122				ESPI0_DAT2/ SPI0_DAT2	GPIO1 22	GPIO1 22	GPIO1 22	PU	0
IOMU Xx7B	BP_ESPI0_DAT3/ SPI0_DAT3/ AGPIO123	S0	123				ESPI0_DAT3/ SPI0_DAT3	GPIO1 23	GPIO1 23	GPIO1 23	PU	0
IOMU Xx7C	BP_ESPI_CS0_L/ AGPIO124	S0	124				ESPI_CS0_L	GPIO1 24	GPIO1 24	GPIO1 24	PU	0
IOMU Xx7D	BP_ESPI_CS1_L	S0	125				ESPI_CS1_L	GPIO1 25	GPIO1 25	GPIO1 25	PU	0

	1_L/ AGPI O125											
IOMU Xx7E	BP_SP I_CS2 _L/ AGPI O126	S0	126				SPI_C S2_L	GPIO1 26	GPIO1 26	GPIO1 26	PU	0
IOMU Xx81	BP_ES PI_RS TIN_L / KBR S T_L/ AGPI O129	S0	129	17			ESPI_ RSTIN _L	KBR S T_L	GPIO1 29	GPIO1 29	PU	0
IOMU Xx83	BP_ES PI1_D AT0/ SPI1_ DAT0/ AGPI O131	S0	131			WAF L _TIME OUT_s trap	ESPI1 _DAT0 / SPI1_ DAT0	GPIO1 31	GPIO1 31	GPIO1 31	PU	0
IOMU Xx84	BP_ES PI1_D AT1/ SPI1_ DAT1/ AGPI O132	S0	132				ESPI1 _DAT1 / SPI1_ DAT1	GPIO1 32	GPIO1 32	GPIO1 32	PU	0
IOMU Xx85	BP_ES PI1_D AT2/ SPI1_ DAT2/ AGPI O133	S0	133				ESPI1 _DAT2 / SPI1_ DAT2	GPIO1 33	GPIO1 33	GPIO1 33	PU	0
IOMU Xx86	BP_ES PI1_D AT3/ SPI1_ DAT3/ AGPI O134	S0	134				ESPI1 _DAT3 / SPI1_ DAT3	GPIO1 34	GPIO1 34	GPIO1 34	PU	0
IOMU Xx87	BP_U ART0_ CTS_L / UART 2_TX D/ AGPI	S0	135				UART 0_CTS _L	UART 2_TX D	GPIO1 35	GPIO1 35	PD	10

	O135											
IOMU Xx88	BP_U ART0_ RXD/ AGPI O136	S0	136				UART 0_RX D	GPIO1 36	GPIO1 36	GPIO1 36	PD	0
IOMU Xx89	BP_U ART0_ RTS_L / UART 2_RX D/ AGPI O137	S0	137				UART 0_RTS _L	UART 2_RX D	GPIO1 37	GPIO1 37	PU	10
IOMU Xx8A	BP_U ART0_ TXD/ AGPI O138	S0	138				UART 0_TX D	GPIO1 38	GPIO1 38	GPIO1 38	PU	1
IOMU Xx8B	BP_U ART0_ INTR/ AGPI O139	S0	139				UART 0_INT R	GPIO1 39	GPIO1 39	GPIO1 39	PD	0
IOMU Xx8D	BP_U ART1_ RXD/ AGPI O141	S0	141				UART 1_RX D	GPIO1 41	GPIO1 41	GPIO1 41	PD	0
IOMU Xx8E	BP_U ART1_ TXD/ AGPI O142	S0	142			ROMT YPE1_ strap	UART 1_TX D	GPIO1 42	GPIO1 42	GPIO1 42	PU	1
IOMU Xx91	BP_I3 C0_SC L/ I2C0_ SCL/ SPD0_ SCL/ SMBU S0_SC L/ AGPI O145	S0	145				I3C0_ SCL	I2C0_ SCL	SMBU S0_SC L	GPIO1 45	n/a	0
IOMU Xx92	BP_I3 C0_SD A/ I2C0_ SDA/ SDA/	S0	146				I3C0_ SDA	I2C0_ SDA	SMBU S0_SD A	GPIO1 46	n/a	0

	SPD0_ SDA/ SMBU S0_SD A/ AGPI O146											
IOMU Xx93	BP_I3 C1_SC L/ I2C1_ SCL/ SPD1_ SCL/ AGPI O147	S0	147				I3C1_ SCL	I2C1_ SCL	GPIO1 47	GPIO1 47	n/a	0
IOMU Xx94	BP_I3 C1_SD A/ I2C1_ SDA/ SPD1_ SDA/ AGPI O148	S0	148				I3C1_ SDA	I2C1_ SDA	GPIO1 48	GPIO1 48	n/a	0
IOMU Xx95	BP_I3 C2_SC L/ I2C2_ SCL/ SPD2_ SCL/ AGPI O149	S0	149				I3C2_ SCL	I2C2_ SCL	GPIO1 49	GPIO1 49	n/a	0
IOMU Xx96	BP_I3 C2_SD A/ I2C2_ SDA/ SPD2_ SDA/ AGPI O150	S0	150				I3C2_ SDA	I2C2_ SDA	GPIO1 50	GPIO1 50	n/a	0
IOMU Xx97	BP_I3 C3_SC L/ I2C3_ SCL/ SPD3_ SCL/ AGPI O151	S0	151				I3C3_ SCL	I2C3_ SCL	GPIO1 51	GPIO1 51	n/a	0

IOMU Xx98	BP_I3 C3_SD A/ I2C3_ SDA/ SPD3_ SDA/ AGPI O152	S0	152				I3C3_ SDA	I2C3_ SDA	GPIO1 52	GPIO1 52	n/a	0
IOMU Xx100	BP_A GPIO2 56/ SGPIO 0_CL K	S5	256				GPIO2 56	SGPIO 0_CL K	GPIO2 56	GPIO2 56	PU	0
IOMU Xx101	BP_A GPIO2 57/ SGPIO 1_CL K/ CLK_ REQ0 1_L	S5	257				GPIO2 57	SGPIO 1_CL K	CLK_ REQ0 1_L	GPIO2 57	PU	0
IOMU Xx102	BP_A GPIO2 58/ SGPIO 2_CL K/ CLK_ REQ0 2_L	S5	258				GPIO2 58	SGPIO 2_CL K	CLK_ REQ0 2_L	GPIO2 58	PU	0
IOMU Xx103	BP_A GPIO2 59/ SGPIO 3_CL K	S5	259				GPIO2 59	SGPIO 3_CL K	GPIO2 59	GPIO2 59	PU	0
IOMU Xx104	BP_S GPIO_ DATA OUT/ AGPI O260	S5	260				SGPIO _DAT AOUT	GPIO2 60	GPIO2 60	GPIO2 60	PU	0
IOMU Xx105	BP_S GPIO_ LOAD / AGPI O261	S5	261				SGPIO _LOA D	GPIO2 61	GPIO2 61	GPIO2 61	PU	0
IOMU	BP_U	S5	264				USB00	GPIO2	GPIO2	GPIO2	PU	0

Xx108	SB00_ OC_L/ AGPI O264						_OC_ L	64	64	64		
IOMU Xx109	BP_U SB01_ OC_L/ AGPI O265	S5	265				USB01 _OC_ L	GPIO2 65	GPIO2 65	GPIO2 65	PU	0

IOMUX registers are accessed by memory-mapped (or IO-mapped) Ios. And they range from "AcpiMMioAddr" + 0xD00 to "AcpiMMioAddr" + 0xDFF. AcpiMMioAddr is FED8\_0000 or the address defined in PMxD6.

The IOMUX register is used to select the function for multi-function IO pins.

Note:

1. PWR\_BTN\_L\_AGPI00 can only be used as PWR\_BTN\_. Since ACPI5.0 require Power Button be claimed as GPIO, and BIOS need the GPIO number to program its debouncing time, thus AGPI00 is assigned.
2. when UART Input is selected (UART\_CTS\_L, UART\_RXD, UART\_RTS\_N, UART\_INTR), corresponding GPIOOutEn bit need be set to '0'

#### IOMUXx00000000 (FCH::IOMUX::IOMUX0\_GPIO)

Read-write. Reset: 00h.

\*Note:

<N> denotes number in hexadecimal: 00h ~ 90h.

<X> denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000000; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

#### IOMUXx00000001 (FCH::IOMUX::IOMUX1\_GPIO)

Read-write. Reset: 00h.

\*Note:

<N> denotes number in hexadecimal: 00h ~ 90h.

<X> denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000001; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3



**IOMUXx00000002 (FCH::IOMUX::IOMUX2\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000002; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000003 (FCH::IOMUX::IOMUX3\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000003; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000004 (FCH::IOMUX::IOMUX4\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000004; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000005 (FCH::IOMUX::IOMUX5\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000005; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000006 (FCH::IOMUX::IOMUX6\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000006; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000007 (FCH::IOMUX::IOMUX7\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000007; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000008 (FCH::IOMUX::IOMUX8\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000008; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000009 (FCH::IOMUX::IOMUX9\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000009; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx0000000A (FCH::IOMUX::IOMUX10\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000000A; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx0000000B (FCH::IOMUX::IOMUX11\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000000B; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx0000000C (FCH::IOMUX::IOMUX12\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000000C; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx0000000D (FCH::IOMUX::IOMUX13\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000000D; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx0000000E (FCH::IOMUX::IOMUX14\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000000E; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx0000000F (FCH::IOMUX::IOMUX15\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000000F; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000010 (FCH::IOMUX::IOMUX16\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000010; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000011 (FCH::IOMUX::IOMUX17\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000011; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000012 (FCH::IOMUX::IOMUX18\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000012; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000013 (FCH::IOMUX::IOMUX19\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000013; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000014 (FCH::IOMUX::IOMUX20\_GPIO)**

Read-write. Reset: 00h.

**\*Note:**

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000014; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000015 (FCH::IOMUX::IOMUX21\_GPIO)**

Read-write. Reset: 00h.

**\*Note:**

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000015; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000016 (FCH::IOMUX::IOMUX22\_GPIO)**

Read-write. Reset: 00h.

**\*Note:**

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000016; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000017 (FCH::IOMUX::IOMUX23\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000017; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000018 (FCH::IOMUX::IOMUX24\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000018; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000019 (FCH::IOMUX::IOMUX25\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000019; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3



**IOMUXx0000001A (FCH::IOMUX::IOMUX26\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000001A; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx0000001B (FCH::IOMUX::IOMUX27\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000001B; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx0000001C (FCH::IOMUX::IOMUX28\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000001C; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx0000001D (FCH::IOMUX::IOMUX29\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000001D; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx0000001E (FCH::IOMUX::IOMUX30\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000001E; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx0000001F (FCH::IOMUX::IOMUX31\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000001F; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000020 (FCH::IOMUX::IOMUX32\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000020; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000021 (FCH::IOMUX::IOMUX33\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000021; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000022 (FCH::IOMUX::IOMUX34\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000022; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000023 (FCH::IOMUX::IOMUX35\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000023; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x</b> . Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000024 (FCH::IOMUX::IOMUX36\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000024; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x</b> . Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000025 (FCH::IOMUX::IOMUX37\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000025; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x</b> . Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000026 (FCH::IOMUX::IOMUX38\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000026; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000027 (FCH::IOMUX::IOMUX39\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000027; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000028 (FCH::IOMUX::IOMUX40\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000028; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000029 (FCH::IOMUX::IOMUX41\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000029; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx0000002A (FCH::IOMUX::IOMUX42\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000002A; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx0000002B (FCH::IOMUX::IOMUX43\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000002B; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx0000002C (FCH::IOMUX::IOMUX44\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000002C; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx0000002D (FCH::IOMUX::IOMUX45\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000002D; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx0000002E (FCH::IOMUX::IOMUX46\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000002E; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx0000002F (FCH::IOMUX::IOMUX47\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000002F; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000030 (FCH::IOMUX::IOMUX48\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000030; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000031 (FCH::IOMUX::IOMUX49\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000031; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3



**IOMUXx00000032 (FCH::IOMUX::IOMUX50\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000032; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000033 (FCH::IOMUX::IOMUX51\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000033; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000034 (FCH::IOMUX::IOMUX52\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000034; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000035 (FCH::IOMUX::IOMUX53\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000035; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000036 (FCH::IOMUX::IOMUX54\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000036; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000037 (FCH::IOMUX::IOMUX55\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000037; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000038 (FCH::IOMUX::IOMUX56\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000038; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000039 (FCH::IOMUX::IOMUX57\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000039; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx0000003A (FCH::IOMUX::IOMUX58\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000003A; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx0000003B (FCH::IOMUX::IOMUX59\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000003B; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx0000003C (FCH::IOMUX::IOMUX60\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000003C; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx0000003D (FCH::IOMUX::IOMUX61\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000003D; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx0000003E (FCH::IOMUX::IOMUX62\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000003E; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx0000003F (FCH::IOMUX::IOMUX63\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000003F; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000040 (FCH::IOMUX::IOMUX64\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000040; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000041 (FCH::IOMUX::IOMUX65\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000041; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000042 (FCH::IOMUX::IOMUX66\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000042; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000043 (FCH::IOMUX::IOMUX67\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000043; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000044 (FCH::IOMUX::IOMUX68\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000044; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x</b> . Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000045 (FCH::IOMUX::IOMUX69\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000045; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x</b> . Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000046 (FCH::IOMUX::IOMUX70\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000046; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x</b> . Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000047 (FCH::IOMUX::IOMUX71\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000047; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000048 (FCH::IOMUX::IOMUX72\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000048; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000049 (FCH::IOMUX::IOMUX73\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000049; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3



**IOMUXx0000004A (FCH::IOMUX::IOMUX74\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000004A; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x</b> . Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx0000004B (FCH::IOMUX::IOMUX75\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000004B; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x</b> . Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx0000004C (FCH::IOMUX::IOMUX76\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000004C; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x</b> . Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx0000004D (FCH::IOMUX::IOMUX77\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000004D; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx0000004E (FCH::IOMUX::IOMUX78\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000004E; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx0000004F (FCH::IOMUX::IOMUX79\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000004F; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000050 (FCH::IOMUX::IOMUX80\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000050; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000051 (FCH::IOMUX::IOMUX81\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000051; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000052 (FCH::IOMUX::IOMUX82\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000052; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000053 (FCH::IOMUX::IOMUX83\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000053; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000054 (FCH::IOMUX::IOMUX84\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000054; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000055 (FCH::IOMUX::IOMUX85\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000055; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000056 (FCH::IOMUX::IOMUX86\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000056; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000057 (FCH::IOMUX::IOMUX87\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000057; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000058 (FCH::IOMUX::IOMUX88\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000058; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000059 (FCH::IOMUX::IOMUX89\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000059; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx0000005A (FCH::IOMUX::IOMUX90\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000005A; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx0000005B (FCH::IOMUX::IOMUX91\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000005B; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx0000005C (FCH::IOMUX::IOMUX92\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000005C; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x</b> . Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx0000005D (FCH::IOMUX::IOMUX93\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000005D; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x</b> . Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx0000005E (FCH::IOMUX::IOMUX94\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000005E; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x</b> . Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx0000005F (FCH::IOMUX::IOMUX95\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000005F; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000060 (FCH::IOMUX::IOMUX96\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000060; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000061 (FCH::IOMUX::IOMUX97\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000061; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3



**IOMUXx00000062 (FCH::IOMUX::IOMUX98\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000062; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000063 (FCH::IOMUX::IOMUX99\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000063; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000064 (FCH::IOMUX::IOMUX100\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000064; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000065 (FCH::IOMUX::IOMUX101\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000065; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000066 (FCH::IOMUX::IOMUX102\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000066; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000067 (FCH::IOMUX::IOMUX103\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000067; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000068 (FCH::IOMUX::IOMUX104\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000068; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000069 (FCH::IOMUX::IOMUX105\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000069; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx0000006A (FCH::IOMUX::IOMUX106\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000006A; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx0000006B (FCH::IOMUX::IOMUX107\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000006B; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx0000006C (FCH::IOMUX::IOMUX108\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000006C; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx0000006D (FCH::IOMUX::IOMUX109\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000006D; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx0000006E (FCH::IOMUX::IOMUX110\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000006E; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x</b> . Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx0000006F (FCH::IOMUX::IOMUX111\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000006F; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x</b> . Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000070 (FCH::IOMUX::IOMUX112\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000070; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x</b> . Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000071 (FCH::IOMUX::IOMUX113\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000071; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000072 (FCH::IOMUX::IOMUX114\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000072; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000073 (FCH::IOMUX::IOMUX115\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000073; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000074 (FCH::IOMUX::IOMUX116\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000074; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000075 (FCH::IOMUX::IOMUX117\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000075; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000076 (FCH::IOMUX::IOMUX118\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000076; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000077 (FCH::IOMUX::IOMUX119\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000077; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x</b> . Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000078 (FCH::IOMUX::IOMUX120\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000078; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x</b> . Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000079 (FCH::IOMUX::IOMUX121\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000079; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x</b> . Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3



**IOMUXx0000007A (FCH::IOMUX::IOMUX122\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000007A; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx0000007B (FCH::IOMUX::IOMUX123\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000007B; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx0000007C (FCH::IOMUX::IOMUX124\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000007C; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx0000007D (FCH::IOMUX::IOMUX125\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000007D; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx0000007E (FCH::IOMUX::IOMUX126\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000007E; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx0000007F (FCH::IOMUX::IOMUX127\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000007F; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000080 (FCH::IOMUX::IOMUX128\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000080; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000081 (FCH::IOMUX::IOMUX129\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000081; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000082 (FCH::IOMUX::IOMUX130\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000082; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000083 (FCH::IOMUX::IOMUX131\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000083; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000084 (FCH::IOMUX::IOMUX132\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000084; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000085 (FCH::IOMUX::IOMUX133\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000085; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000086 (FCH::IOMUX::IOMUX134\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000086; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000087 (FCH::IOMUX::IOMUX135\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000087; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000088 (FCH::IOMUX::IOMUX136\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000088; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000089 (FCH::IOMUX::IOMUX137\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000089; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx0000008A (FCH::IOMUX::IOMUX138\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000008A; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx0000008B (FCH::IOMUX::IOMUX139\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000008B; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx0000008C (FCH::IOMUX::IOMUX140\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000008C; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx0000008D (FCH::IOMUX::IOMUX141\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000008D; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx0000008E (FCH::IOMUX::IOMUX142\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000008E; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx0000008F (FCH::IOMUX::IOMUX143\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx0000008F; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x</b> . Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000090 (FCH::IOMUX::IOMUX144\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000090; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x</b> . Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000091 (FCH::IOMUX::IOMUX145\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000091; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x</b> . Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3



**IOMUXx00000092 (FCH::IOMUX::IOMUX146\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000092; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000093 (FCH::IOMUX::IOMUX147\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000093; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000094 (FCH::IOMUX::IOMUX148\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000094; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000095 (FCH::IOMUX::IOMUX149\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000095; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000096 (FCH::IOMUX::IOMUX150\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000096; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000097 (FCH::IOMUX::IOMUX151\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000097; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**IOMUXx00000098 (FCH::IOMUX::IOMUX152\_GPIO)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number in hexadecimal: 00h ~ 90h.

&lt;X&gt; denotes number in decimal: 0 ~ 144.

\_aliasHOSTLEGACY; IOMUXx00000098; IOMUX=FED8\_0D00h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**11.3.10.2 GPIO Registers**

The GPIO pins are controlled by a combination of device enables and by their specific GPIO and IOMUX register pair.

GPIO registers are accessed through memory-mapped ACPIMMIO region. The offset is relative to FED8\_0000h+1500h. GPIO bank 0 registers range from FED8\_0000h+1500h to FED8\_0000h+15FFh. GPIO Bank 1 registers range from FED8\_0000h+1600h to FED8\_0000h+16FFh. GPIO Bank 2 registers range from FED8\_0000h+1700h to FED8\_0000h+17FFh. GPIO Bank 3 registers range from FED8\_0000h+1800h to FED8\_0000h+18FFh.

*Table 194: I2C/I3C Pad Configuration Method*

	PAD name	GPIO register(bank, offset) (No use)	Misc_Reg(Control I2C PAD)
I2C0/I3C0	I3C0_SCL_I2C0_SCL_SPD0_SCL_ SMBUS0_SCL_AGPI0145	0x244	0xD8
	I3C0_SDA_I2C0_SDA_SPD0_SDA_ SMBUS0_SDA_AGPI0146	0x248	
I2C1/I3C1	I3C1_SCL_I2C1_SCL_SPD1_SCL_ AGPI0147	0x24C	0xDC
	I3C1_SDA_I2C1_SDA_SPD1_SDA_ AGPI0148	0x250	
I2C2/I3C3	I3C2_SCL_I2C2_SCL_SPD2_SCL_ AGPI0149	0x254	0xE0
	I3C2_SDA_I2C2_SDA_SPD2_SDA_ AGPI0150	0x258	
I2C3/I3C3	I3C3_SCL_I2C3_SCL_SPD3_SCL_ AGPI0151	0x25C	0xE4
	I3C3_SDA_I2C3_SDA_SPD3_SDA_ AGPI0152	0x260	
I2C4	I2C4_SCL_HP_SCL_UBM_SCL_A GPIO13	0x044	0xE8
	I2C4_SDA_HP_SDA_UBM_SDA_ AGPI014	0x048	
I2C5	I2C5_SCL_BMC_SCL_SMBUS1_S CL_AGPI019	0x04C	0xEC
	I2C5_SDA_BMC_SDA_SMBUS1_S	0x050	

	DA_AGPI020		
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Table 195: GPIO BANK0 Register Default Value

Register	Reset Value	Index	Function
GPIOx00000	0014_0000h	0	BP_PWR_BTN_L_AGPI00
GPIOx00004	0014_0000h	1	BP_SYS_RESET_L_AGPI01
GPIOx00008	0014_0000h	2	BP_WAKE_L_AGPI02
GPIOx0000C	0014_0000h	3	BP_AGPI03_SPD_HOST_CTRL_L
GPIOx00010	0014_0000h	4	BP_AGPI04_SATA_ACT_L
GPIOx00014	0024_0000h	5	BP_AGPI05_DEVSLP0_SATA_ZP0_L
GPIOx00018	0024_0000h	6	BP_AGPI06_DEVSLP1_SATA_ZP1_L
GPIOx0001C	0024_0000h	7	BP_AGPI07
GPIOx00020	0024_0000h	8	Reserved
GPIOx00024	0024_0000h	9	Reserved
GPIOx00028	0014_0000h	10	Reserved
GPIOx0002C	0014_0000h	11	Reserved
GPIOx00030	0004_0000h	12	BP_PWRGD_OUT_AGPI012
GPIOx00034	0004_0000h	13	BP_I2C4_SCL_HP_SCL_UBM_SCL_AGPI013
GPIOx00038	0004_0000h	14	BP_I2C4_SDA_HP_SDA_UBM_SDA_AGPI014
GPIOx0003C	0000_0000h	15	Reserved
GPIOx00040	0014_0000h	16	BP_USB10_OC_L_AGPI016
GPIOx00044	0014_0000h	17	BP_USB11_OC_L_AGPI017
GPIOx00048	0014_0000h	18	Reserved
GPIOx0004C	0004_0000h	19	BP_I2C5_SCL_BMC_SCL_SMBUS1_SCL_AGPI019
GPIOx00050	0004_0000h	20	BP_I2C5_SDA_BMC_SDA_SMBUS1_SDA_AGPI020
GPIOx00054	0024_0000h	21	BP_AGPI021
GPIOx00058	0024_0000h	22	BP_AGPI022
GPIOx0005C	0014_0000h	23	BP_ESPI_RSTOUT_L_AGPI023
GPIOx00060	0014_0000h	24	BP_SMERR_L_AGPI024
GPIOx00064	0000_0000h	25	Reserved
GPIOx00068	0004_0000h	26	BP_PCIE_RST1_L_AGPI026
GPIOx0006C	0024_0000h	27	Reserved
GPIOx00070	0024_0000h	28	Reserved
GPIOx00074	0014_0000h	29	Reserved
GPIOx00078	0014_0000h	30	Reserved
GPIOx0007C	0014_0000h	31	Reserved
GPIOx00080	0024_0000h	32	Reserved
GPIOx00084	0000_0000h	33	Reserved
GPIOx00088	0000_0000h	34	Reserved
GPIOx0008C	0000_0000h	35	Reserved
GPIOx00090	0000_0000h	36	Reserved
GPIOx00094	0000_0000h	37	Reserved
GPIOx00098	0000_0000h	38	Reserved
GPIOx0009C	0000_0000h	39	Reserved
GPIOx000A0	0024_0000h	40	Reserved
GPIOx000A4	0000_0000h	41	Reserved
GPIOx000A8	0014_0000h	42	Reserved

GPIOx000AC	0000_0000h	43	Int_FakeSts0
GPIOx000B0	0000_0000h	44	Int_ShdwSysAlarmFire
GPIOx000B4	0000_0000h	45	Int_pwr_bttm (NOTE: This Event needs to debounce.)
GPIOx000B8	0000_0000h	46	Int_FakeSts0
GPIOx000BC	0000_0000h	47	Int_Wake_up_WDTO
GPIOx000C0	0000_0000h	48	Int_DhcpLeaseTimerExpire
GPIOx000C4	0000_0000h	49	Int_ASFSlaveIntr
GPIOx000C8	0000_0000h	50	Int_sm_irq_
GPIOx000CC	0000_0000h	51	Int_WakeFromLLB
GPIOx000D0	0000_0000h	52	Int_AcDcTimerEvent
GPIOx000D4	0000_0000h	53	Int_ALTHPET_TimerSts
GPIOx000D8	0000_0000h	54	Int_iSocEvent[0] (MP2 wakeup event)
GPIOx000DC	0000_0000h	55	Int_iSocEvent[1] (MP2 GPIO[0])
GPIOx000E0	0000_0000h	56	Int_iSocEvent[2] (MP2 GPIO[1])
GPIOx000E4	0000_0000h	57	Reserved
GPIOx000E8	0000_0000h	58	Int_usb_xhc_0_acpi_pme
GPIOx000EC	0000_0000h	59	Int_usb_xhc_1_acpi_pme
GPIOx000F0	0000_0000h	60	Int_RTC_STS_reg
GPIOx000F4	0000_0000h	61	Int_ACP_FCH_AZ_Wake
GPIOx000F8	0000_0000h	62	Int_ACP_FCH_I2S_Wake

Table 196: GPIO BANK1 Register Default Value

Register	Reset Value	Index	Function
GPIOx00100	0000_0000h	64	Reserved
GPIOx00104	0000_0000h	65	Reserved
GPIOx00108	0000_0000h	66	Reserved
GPIOx0010C	0000_0000h	67	Reserved
GPIOx00110	0000_0000h	68	Reserved
GPIOx00114	0000_0000h	69	Reserved
GPIOx00118	0000_0000h	70	Reserved
GPIOx0011C	0000_0000h	71	Reserved
GPIOx00120	0000_0000h	72	Reserved
GPIOx00124	0000_0000h	73	Reserved
GPIOx00128	0024_0000h	74	BP_ESPI_CLK2_AGPIO74
GPIOx0012C	0024_0000h	75	BP_ESPI_CLK1_SPI_CLK1_AGPIO75
GPIOx00130	0014_0000h	76	BP_AGPIO76_SPI_TPM_CS_L
GPIOx00134	0000_0000h	77	Reserved
GPIOx00138	0000_0000h	78	Reserved
GPIOx0013C	0000_0000h	79	Reserved
GPIOx00140	0000_0000h	80	Reserved
GPIOx00144	0000_0000h	81	Reserved
GPIOx00148	0000_0000h	82	Reserved
GPIOx0014C	0000_0000h	83	Reserved
GPIOx00150	0000_0000h	84	Reserved
GPIOx00154	0000_0000h	85	Reserved
GPIOx00158	0024_0000h	86	BP_NMI_SYNC_FLOOD_L
GPIOx0015C	0024_0000h	87	BP_AGPIO87

GPIOx00160	0024_0000h	88	BP_AGPI088
GPIOx00164	0014_0000h	89	BP_GENINT_L_PM_INTR_L_AGPI089
GPIOx00168	0000_0001h	90	Reserved
GPIOx0016C	0000_0000h	91	Reserved
GPIOx00170	0000_0000h	92	Reserved
GPIOx00174	0000_0000h	93	Reserved
GPIOx00178	0000_0000h	94	Reserved
GPIOx0017C	0000_0000h	95	Reserved
GPIOx00180	0000_0000h	96	Reserved
GPIOx00184	0000_0000h	97	Reserved
GPIOx00188	0000_0000h	98	Reserved
GPIOx0018C	0000_0000h	99	Reserved
GPIOx00190	0000_0000h	100	Reserved
GPIOx00194	0000_0000h	101	Reserved
GPIOx00198	0000_0000h	102	Reserved
GPIOx0019C	0000_0000h	103	Reserved
GPIOx001A0	0024_0000h	104	BP_AGPI0104
GPIOx001A4	0024_0000h	105	BP_AGPI0105
GPIOx001A8	0024_0000h	106	BP_AGPI0106
GPIOx001AC	0024_0000h	107	BP_AGPI0107
GPIOx001B0	0014_0000h	108	BP_ESPI0_ALERT_L_ESPI_IO1_AGPI0108
GPIOx001B4	0024_0000h	109	BP_AGPI0109
GPIOx001B8	0000_0000h	110	BP_ESPI1_ALERT_L_AGPI0110
GPIOx001BC	0000_0000h	111	Reserved
GPIOx001C0	0000_0000h	112	Reserved
GPIOx001C4	0000_0000h	113	Reserved
GPIOx001C8	0000_0000h	114	Reserved
GPIOx001CC	0014_0000h	115	BP_AGPI0115_CLK_REQ11_L
GPIOx001D0	0014_0000h	116	BP_AGPI0116_CLK_REQ12_L
GPIOx001D4	0024_0000h	117	BP_ESPI_CLK0_SPI_CLK0_AGPI0117
GPIOx001D8	0014_0000h	118	BP_SPI_CS0_L_AGPI0118
GPIOx001DC	0014_0000h	119	BP_SPI_CS1_L_AGPI0119
GPIOx001E0	0014_0000h	120	BP_ESPI0_DAT0_SPI0_DAT0_AGPI0120
GPIOx001E4	0014_0000h	121	BP_ESPI0_DAT1_SPI0_DAT1_AGPI0121
GPIOx001E8	0014_0000h	122	BP_ESPI0_DAT2_SPI0_DAT2_AGPI0122
GPIOx001EC	0014_0000h	123	BP_ESPI0_DAT3_SPI0_DAT3_AGPI0123
GPIOx001F0	0014_0000h	124	BP_ESPI_CS0_L_AGPI0124
GPIOx001F4	0014_0000h	125	BP_ESPI_CS1_L_AGPI0125
GPIOx001F8	0014_0000h	126	BP_SPI_CS2_L_AGPI0126

Table 197: GPIO BANK2 Register Default Value

Register	Reset Value	Index	Function
GPIOx00200	0000_0000h	128	Reserved
GPIOx00204	0014_0000h	129	BP_ESPI_RSTIN_L_KBRST_L_AGPI0129
GPIOx00208	0000_0000h	130	Reserved
GPIOx0020C	0014_0000h	131	BP_ESPI1_DAT0_SPI1_DAT0_AGPI0131
GPIOx00210	0014_0000h	132	BP_ESPI1_DAT1_SPI1_DAT1_AGPI0132
GPIOx00214	0014_0000h	133	BP_ESPI1_DAT2_SPI1_DAT2_AGPI0133

GPIOx00218	0014_0000h	134	BP_ESPI1_DAT3_SPI1_DAT3_AGPI0134
GPIOx0021C	0024_0000h	135	BP_UART0_CTS_L_UART2_TXD_AGPI0135
GPIOx00220	0024_0000h	136	BP_UART0_RXD_AGPI0136
GPIOx00224	0014_0000h	137	BP_UART0_RTS_L_UART2_RXD_AGPI0137
GPIOx00228	0014_0000h	138	BP_UART0_TXD_AGPI0138
GPIOx0022C	0024_0000h	139	BP_UART0_INTR_AGPI0139
GPIOx00230	0000_0000h	140	Reserved
GPIOx00234	0024_0000h	141	BP_UART1_RXD_AGPI0141
GPIOx00238	0014_0000h	142	BP_UART1_TXD_AGPI0142
GPIOx0023C	0000_0000h	143	Reserved
GPIOx00240	0000_0000h	144	Reserved
GPIOx00244	0004_0000h	145	BP_I3C0_SCL_I2C0_SCL_SPD0_SCL_SMBUS0_SCL_AGPI0145
GPIOx00248	0004_0000h	146	BP_I3C0_SDA_I2C0_SDA_SPD0_SDA_SMBUS0_SDA_AGPI0146
GPIOx0024C	0004_0000h	147	BP_I3C1_SCL_I2C1_SCL_SPD1_SCL_AGPI0147
GPIOx00250	0004_0000h	148	BP_I3C1_SDA_I2C1_SDA_SPD1_SDA_AGPI0148
GPIOx00254	0004_0000h	149	BP_I3C2_SCL_I2C2_SCL_SPD2_SCL_AGPI0149
GPIOx00258	0004_0000h	150	BP_I3C2_SDA_I2C2_SDA_SPD2_SDA_AGPI0150
GPIOx0025C	0004_0000h	151	BP_I3C3_SCL_I2C3_SCL_SPD3_SCL_AGPI0151
GPIOx00260	0004_0000h	152	BP_I3C3_SDA_I2C3_SDA_SPD3_SDA_AGPI0152
GPIOx00264	0000_0000h	153	Reserved
GPIOx00268	0000_0000h	154	Reserved
GPIOx0026C	0000_0000h	155	Reserved
GPIOx00270	0000_0000h	156	Reserved
GPIOx00274	0000_0000h	157	Reserved
GPIOx00278	0000_0000h	158	Reserved
GPIOx0027C	0000_0000h	159	Reserved
GPIOx00280	0000_0000h	160	Reserved
GPIOx00284	0000_0000h	161	Reserved
GPIOx00288	0000_0000h	162	Reserved
GPIOx0028C	0000_0000h	163	Reserved
GPIOx00290	0000_0000h	164	Reserved
GPIOx00294	0000_0000h	165	Reserved
GPIOx00298	0000_0000h	166	Reserved
GPIOx0029C	0000_0000h	167	Reserved
GPIOx002A0	0000_0000h	168	Reserved
GPIOx002A4	0000_0000h	169	Reserved
GPIOx002A8	0000_0000h	170	Reserved
GPIOx002AC	0000_0000h	171	Reserved
GPIOx002B0	0000_0000h	172	NBGppPmePulse
GPIOx002B4	0000_0000h	173	NBGppHpPulse
GPIOx002B8	0000_0000h	174	AcpiPerfIntr
GPIOx002BC	0000_0000h	175	sata_sci_ & sata_sci2_
GPIOx002C0	0000_0000h	176	FanThermal_SCIOut
GPIOx002C4	0000_0000h	177	ASFMasterIntr
GPIOx002C8	0000_0000h	178	Ras_event
GPIOx002CC	0000_0000h	179	GBL_RLS
GPIOx002D0	0000_0000h	180	ShortTimerEvent   LongTimerEvent

GPIOx002D4	0000_0000h	181	NBHwAssertion_r[3]   NBSciAssertion_r[3]
GPIOx002D8	0000_0000h	182	eSPI_WAKE_PME_B
GPIOx002DC	0000_0000h	183	eSPI_SYS_EVT_B
GPIOx002E0	0000_0000h	184	eSPI1_WAKE_PME_B
GPIOx002E4	0000_0000h	185	eSPI1_SYS_EVT_B
GPIOx002E8	0000_0000h	186	Reserved
GPIOx002EC	0000_0000h	187	Reserved
GPIOx002F0	0000_0000h	188	Reserved
GPIOx002F4	0000_0000h	189	Reserved
GPIOx002F8	0000_0000h	190	Reserved

Table 198: GPIO BANK3 Register Default Value

Register	Reset Value	Index	Function
GPIOx00300	0000_0000h	192	
GPIOx00304	0000_0000h	193	
GPIOx00308	0000_0000h	194	
GPIOx0030C	0000_0000h	195	
GPIOx00310	0000_0000h	196	
GPIOx00314	0000_0000h	197	
GPIOx00318	0000_0000h	198	
GPIOx0031C	0000_0000h	199	
GPIOx00320	0000_0000h	200	
GPIOx00324	0000_0000h	201	
GPIOx00328	0000_0000h	202	
GPIOx0032C	0000_0000h	203	
GPIOx00330	0000_0000h	204	
GPIOx00334	0000_0000h	205	
GPIOx00338	0000_0000h	206	
GPIOx0033C	0000_0000h	207	
GPIOx00340	0000_0000h	208	
GPIOx00344	0000_0000h	209	
GPIOx00348	0000_0000h	210	
GPIOx0034C	0000_0000h	211	
GPIOx00350	0000_0000h	212	
GPIOx00354	0000_0000h	213	
GPIOx00358	0000_0000h	214	
GPIOx0035C	0000_0000h	215	
GPIOx00360	0000_0000h	216	
GPIOx00364	0000_0000h	217	
GPIOx00368	0000_0000h	218	
GPIOx0036C	0000_0000h	219	
GPIOx00370	0000_0000h	220	
GPIOx00374	0000_0000h	221	
GPIOx00378	0000_0000h	222	
GPIOx0037C	0000_0000h	223	
GPIOx00380	0000_0000h	224	
GPIOx00384	0000_0000h	225	
GPIOx00388	0000_0000h	226	



GPIOx0038C	0000_0000h	227	
GPIOx00390	0000_0000h	228	
GPIOx00394	0000_0000h	229	
GPIOx00398	0000_0000h	230	
GPIOx0039C	0000_0000h	231	
GPIOx003A0	0000_0000h	232	
GPIOx003A4	0000_0000h	233	
GPIOx003A8	0000_0000h	234	
GPIOx003AC	0000_0000h	235	
GPIOx003B0	0000_0000h	236	
GPIOx003B4	0000_0000h	237	
GPIOx003B8	0000_0000h	238	
GPIOx003BC	0000_0000h	239	
GPIOx003C0	0000_0000h	240	
GPIOx003C4	0000_0000h	241	
GPIOx003C8	0000_0000h	242	
GPIOx003CC	0000_0000h	243	
GPIOx003D0	0000_0000h	244	
GPIOx003D4	0000_0000h	245	
GPIOx003D8	0000_0000h	246	
GPIOx003DC	0000_0000h	247	
GPIOx003E0	0000_0000h	248	
GPIOx003E4	0000_0000h	249	
GPIOx003E8	0000_0000h	250	
GPIOx003EC	0000_0000h	251	
GPIOx003F0	0000_0000h	252	
GPIOx003F4	0000_0000h	253	
GPIOx003F8	0000_0000h	254	
GPIOx003FC	0000_0000h	255	

Table 199: Debounce Timer Definition

DebounceTmrLarge	DebounceTmrOutUnit	Timer Unit	Max Debounce Time
0	0	61 usec (2 RtcClk)	915 usec
0	1	183 usec (6 RtcClk)	2.75 msec
1	0	15.56 msec (510 RtcClk)	233 msec
1	1	62.44 msec (2046 RtcClk)	936 msec

**GPIOx00000000 (FCH::GPIO::PWR\_BTN\_L\_AGPI00)**

Reset: 0014\_0000h.

\_aliasHOSTLEGACY; GPIOx00000000; GPIO=FED8\_1500h

Bits	Description
31	<b>less10secsts.</b> Read-write. Reset: 0. <b>Description:</b> Read-only. This bit is only valid for GPIO0. For other GPIO, this bit is Reserved. When power button is pressed for less than 10 second in S0 state, this bit will become 1. This bit can be cleared by writing 1 to InterruptSts bit.
30	<b>less2secsts.</b> Read-write. Reset: 0. <b>Description:</b> Read-only. This bit is only valid for GPIO0. For other GPIO, this bit is Reserved. When power button is pressed for less than 2 second in S0 state, this bit will become 1. When Less2secSts becomes 1, Less10secSts will also become 1. This bit can be cleared by writing 1 to InterruptSts bit.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h.

	<b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrmlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx00000004 (FCH::GPIO::SYS\_RESET\_L\_AGPI01)**

Reset: 0014\_0000h.

\_aliasHOSTLEGACY; GPIOx00000004; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx00000008 (FCH::GPIO::WAKE\_L\_AGPIO2)**

Reset: 0014\_0000h.

\_aliasHOSTLEGACY; GPIOx00000008; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

GPIOx0000000C (FCH::GPIO::AGPIO3)	
Reset: 0014_0000h.	
_aliasHOSTLEGACY; GPIOx0000000C; GPIO=FED8_1500h	
Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.



	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx00000010 (FCH::GPIO::AGPIO4)**

Reset: 0014\_0000h.

\_aliasHOSTLEGACY; GPIOx00000010; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx00000014 (FCH::GPIO::AGPIO5)**

Reset: 0024\_0000h.

\_aliasHOSTLEGACY; GPIOx00000014; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx00000018 (FCH::GPIO::AGPIO6)**

Reset: 0024\_0000h.

\_aliasHOSTLEGACY; GPIOx00000018; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx0000001C (FCH::GPIO::AGPIO7)**

Reset: 0024\_0000h.

\_aliasHOSTLEGACY; GPIOx0000001C; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.



	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec Debounce
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx00000030 (FCH::GPIO::PWRGD\_OUT\_AGPI012)**

Reset: 0004\_0000h.

\_aliasHOSTLEGACY; GPIOx00000030; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx00000034 (FCH::GPIO::I2C4\_SCL\_HP\_SCL\_UBM\_SCL\_AGPI013)**

Reset: 0004\_0000h.

\_aliasHOSTLEGACY; GPIOx00000034; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx00000038 (FCH::GPIO::I2C4\_SDA\_HP\_SDA\_UBM\_SDA\_AGPI014)**

Reset: 0004\_0000h.

\_aliasHOSTLEGACY; GPIOx00000038; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx00000040 (FCH::GPIO::USB0\_OC\_L\_AGPIO16)**

Reset: 0014\_0000h.

\_aliasHOSTLEGACY; GPIOx00000040; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.



	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx00000044 (FCH::GPIO::USB1\_OC\_L\_AGPI017)**

Reset: 0014\_0000h.

\_aliasHOSTLEGACY; GPIOx00000044; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx0000004C (FCH::GPIO::I2C5\_SCL\_BMC\_SCL\_SMBUS1\_SCL\_AGPI019)**

Reset: 0004\_0000h.

\_aliasHOSTLEGACY; GPIOx0000004C; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx00000050 (FCH::GPIO::I2C5\_SDA\_BMC\_SDA\_SMBUS1\_SDA\_AGPI020)**

Reset: 0004\_0000h.

\_aliasHOSTLEGACY; GPIOx00000050; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx00000054 (FCH::GPIO::AGPIO21)**

Reset: 0024\_0000h.

\_aliasHOSTLEGACY; GPIOx00000054; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.



	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx00000058 (FCH::GPIO::AGPIO22)**

Reset: 0024\_0000h.

\_aliasHOSTLEGACY; GPIOx00000058; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx0000005C (FCH::GPIO::ESPI\_RSTOUT\_L\_AGPI023)**

Reset: 0014\_0000h.

\_aliasHOSTLEGACY; GPIOx0000005C; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx00000060 (FCH::GPIO::SMERR\_L\_AGPI024)**

Reset: 0014\_0000h.

\_aliasHOSTLEGACY; GPIOx00000060; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx00000068 (FCH::GPIO::PCIE\_RST1\_L\_AGPI026)**

Reset: 0004\_0000h.

\_aliasHOSTLEGACY; GPIOx00000068; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.



	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx0000006C (FCH::GPIO::PCIE\_RST0\_L\_AGPIO27)**

Reset: 0004\_0000h.

\_aliasHOSTLEGACY; GPIOx0000006C; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx00000070 (FCH::GPIO::X48M\_OUT\_0\_AGPI028)**

Reset: 0024\_0000h.

\_aliasHOSTLEGACY; GPIOx00000070; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx00000074 (FCH::GPIO::X48M\_OUT\_1\_AGPI029)**

Reset: 0024\_0000h.

\_aliasHOSTLEGACY; GPIOx00000074; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx00000078 (FCH::GPIO::X48M\_OUT\_2\_AGPI030)**

Reset: 0024\_0000h.

\_aliasHOSTLEGACY; GPIOx00000078; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.



	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

GPIOx000000AC (FCH::GPIO::INT_FAKESTS0)	
Reset: 0000_0000h.	
_aliasHOSTLEGACY; GPIOx000000AC; GPIO=FED8_1500h	
Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

**GPIOx000000B0 (FCH::GPIO::INT\_SHDWSYSALARMFIRE)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx000000B0; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

**GPIOx000000B4 (FCH::GPIO::INT\_PWR\_BTN)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx000000B4; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

**GPIOx000000B8 (FCH::GPIO::INT\_FAKESTS0\_2ND)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx000000B8; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

**GPIOx000000BC (FCH::GPIO::INT\_WAKE\_UP\_WDTO)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx000000BC; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

**GPIOx000000C0 (FCH::GPIO::INT\_DHCPLEASETIMEREXPIRE)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx000000C0; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

GPIOx000000C4 (FCH::GPIO::INT_ASFSLAVEINTR)	
Reset: 0000_0000h.	
_aliasHOSTLEGACY; GPIOx000000C4; GPIO=FED8_1500h	
Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.



**GPIOx000000C8 (FCH::GPIO::INT\_SM\_IRQ)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx000000C8; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

GPIOx000000CC (FCH::GPIO::INT_WAKEFROMLLB)	
Reset: 0000_0000h.	
_aliasHOSTLEGACY; GPIOx000000CC; GPIO=FED8_1500h	
Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

**GPIOx000000D0 (FCH::GPIO::INT\_ACDCTIMEREVENT)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx000000D0; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

**GPIOx000000D4 (FCH::GPIO::INT\_ALHPET\_TIMERSTS)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx000000D4; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

GPIOx000000D8 (FCH::GPIO::INT_ISOCEVENT0)	
Reset: 0000_0000h.	
_aliasHOSTLEGACY; GPIOx000000D8; GPIO=FED8_1500h	
Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

**GPIOx000000DC (FCH::GPIO::INT\_ISOCEVENT1)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx000000DC; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

**GPIOx000000E0 (FCH::GPIO::INT\_ISOCEVENT2)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx000000E0; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

**GPIOx000000E8 (FCH::GPIO::INT\_USB\_XHC\_0\_ACPI\_PME)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx000000E8; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.



**GPIOx000000EC (FCH::GPIO::INT\_USB\_XHC\_1\_ACPI\_PME)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx000000EC; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

**GPIOx000000F0 (FCH::GPIO::INT\_RTC\_STS\_REG)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx000000F0; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

**GPIOx000000F4 (FCH::GPIO::INT\_ACP\_FCH\_AZ\_WAKE)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx000000F4; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

**GPIOx000000F8 (FCH::GPIO::INT\_ACP\_FCH\_I2S\_WAKE)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx000000F8; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

**GPIOx000000FC (FCH::GPIO::GPIO\_WAKE\_INTERRUPT\_MASTER\_SWITCH)**

Read-write. Reset: FF00\_0000h.

\_aliasHOSTLEGACY; GPIOx000000FC; GPIO=FED8\_1500h

Bits	Description
31	<b>gpiowakeen.</b> Read-write. Reset: 1. When this bit is 0, all GPIO wake are blocked.
30	<b>gpiointerrupten.</b> Read-write. Reset: 1. When this bit is 0, all GPIO interrupts are blocked.
29	<b>eoi.</b> Read-write. Reset: 1. <b>Description:</b> This bit is set to 1 by SW when it is allowed to send GPIO interrupt. HW clear this bit when interrupt occurs. When this bit is 0, the GPIO interrupt is blocked. (This SW/HW handshake mechanism is the same with EOS of <a href="#">SMI</a> .)
28	<b>mask_sts_en.</b> Read-write. Reset: 1. This bit enables HW to block all wake/intr status generation when SW writes any Debounce* registers. The length of blocking depends on mask_sts_length[3:0].
27:24	<b>mask_sts_length_3_0.</b> Read-write. Reset: Fh. <b>Description:</b> See mask_sts_en as well. The length of blocking = {mask_sts_length[11:0], 14'h3FFF}
23:16	<b>mask_sts_length_11_4.</b> Read-write. Reset: 00h. <b>Description:</b> See mask_sts_en as well. The length of blocking = {mask_sts_length[11:0], 14'h3FFF}
15	<b>enwinbluebtn.</b> Read-write. Reset: 0. <b>Description:</b> 0: GPIO0 detect debounced power button. Power button override is 4 sec. 1: GPIO0 detect debounced power button in S3/S5/Power saving mode, and detect "pressed less than 2sec" and "pressed 2~10sec" in S0. Power button override is 10 sec.
14	<b>introutactivehi.</b> Read-write. Reset: 0. <b>Description:</b> 0: GPIO controller interrupt output is low active 1: GPIO controller interrupt output is high active
13	<b>selgpio0src.</b> Read-write. Reset: 0. <b>Description:</b> Select the source for GPIO0 detection. 0: Power button goes to a processing logic first and then goes to GPIO0 detection logic 1: Power button goes to GPIO0 debounce and then goes to GPIO0 detection logic. Note: The "processing logic" includes 16ms debounce counter and a logic to detect how long the button has been pressed to generate press_less2s_sts and press_less4s_sts. "GPIO0 debounce block" only has debounce function.
12	<b>introutpulse.</b> Read-write. Reset: 0. <b>Description:</b> 0: GPIO controller interrupt output is a level signal 1: GPIO controller interrupt output is pulse signal Note: The polarity is defined by IntrOutActiveHi register bit.
11:0	Reserved.

**GPIOx00000128 (FCH::GPIO::ESPI\_CLK2\_AGPIO74)**

Reset: 0024\_0000h.

\_aliasHOSTLEGACY; GPIOx00000128; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx0000012C (FCH::GPIO::ESPI\_CLK1\_SPI\_CLK1\_AGPIOW5)**

Reset: 0014\_0000h.

\_aliasHOSTLEGACY; GPIOx0000012C; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.



	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx00000130 (FCH::GPIO::AGPIO76\_SPI\_TPM\_CS\_L)**

Reset: 0014\_0000h.

\_aliasHOSTLEGACY; GPIOx00000130; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx00000158 (FCH::GPIO::NMI\_SYNC\_FLOOD\_L)**

Reset: 0024\_0000h.

\_aliasHOSTLEGACY; GPIOx00000158; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx0000015C (FCH::GPIO::AGPIO87)**

Reset: 0024\_0000h.

\_aliasHOSTLEGACY; GPIOx0000015C; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx00000160 (FCH::GPIO::AGPIO88)**

Reset: 0024\_0000h.

\_aliasHOSTLEGACY; GPIOx00000160; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.



	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx00000164 (FCH::GPIO::GENINT\_L\_PM\_INTR\_L\_AGPI089)**

Reset: 0014\_0000h.

\_aliasHOSTLEGACY; GPIOx00000164; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx000001A0 (FCH::GPIO::AGPIO104)**

Reset: 0024\_0000h.

\_aliasHOSTLEGACY; GPIOx000001A0; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx000001A4 (FCH::GPIO::AGPIO105)**

Reset: 0024\_0000h.

\_aliasHOSTLEGACY; GPIOx000001A4; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx000001A8 (FCH::GPIO::AGPIO106)**

Reset: 0024\_0000h.

\_aliasHOSTLEGACY; GPIOx000001A8; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.



	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx000001AC (FCH::GPIO::AGPIO107)**

Reset: 0024\_0000h.

\_aliasHOSTLEGACY; GPIOx000001AC; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx000001B0 (FCH::GPIO::ESPI0\_ALERT\_L\_ESPI\_IO1\_AGPI0108)**

Reset: 0014\_0000h.

\_aliasHOSTLEGACY; GPIOx000001B0; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx000001B4 (FCH::GPIO::AGPIO109)**

Reset: 0024\_0000h.

\_aliasHOSTLEGACY; GPIOx000001B4; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx000001B8 (FCH::GPIO::ESPI1\_ALERT\_L\_AGPIO110)**

Reset: 0014\_0000h.

\_aliasHOSTLEGACY; GPIOx000001B8; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.



	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx000001CC (FCH::GPIO::CLK\_REQ\_11\_L\_AGPI0115)**

Reset: 0014\_0000h.

\_aliasHOSTLEGACY; GPIOx000001CC; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx000001D0 (FCH::GPIO::CLK\_REQ\_12\_L\_AGPI0116)**

Reset: 0014\_0000h.

\_aliasHOSTLEGACY; GPIOx000001D0; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx000001D4 (FCH::GPIO::ESPI\_CLK0\_SPI\_CLK0\_AGPIO117)**

Reset: 0024\_0000h.

\_aliasHOSTLEGACY; GPIOx000001D4; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx000001D8 (FCH::GPIO::SPI\_CS0\_L\_AGPI0118)**

Reset: 0014\_0000h.

\_aliasHOSTLEGACY; GPIOx000001D8; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.



	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx000001DC (FCH::GPIO::SPI\_CS1\_L\_AGPI0119)**

Reset: 0014\_0000h.

\_aliasHOSTLEGACY; GPIOx000001DC; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx000001E0 (FCH::GPIO::ESPI0\_DAT0\_SPI0\_DAT0\_AGPI0120)**

Reset: 0014\_0000h.

\_aliasHOSTLEGACY; GPIOx000001E0; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx000001E4 (FCH::GPIO::ESPI0\_DAT1\_SPI0\_DAT1\_AGPI0121)**

Reset: 0014\_0000h.

\_aliasHOSTLEGACY; GPIOx000001E4; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx000001E8 (FCH::GPIO::ESPI0\_DAT2\_SPI0\_DAT2\_AGPI0122)**

Reset: 0014\_0000h.

\_aliasHOSTLEGACY; GPIOx000001E8; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.



	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx000001EC (FCH::GPIO::ESPI0\_DAT3\_SPI0\_DAT3\_AGPI0123)**

Reset: 0014\_0000h.

\_aliasHOSTLEGACY; GPIOx000001EC; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx000001F0 (FCH::GPIO::ESPI\_CS0\_L\_AGPI0124)**

Reset: 0014\_0000h.

\_aliasHOSTLEGACY; GPIOx000001F0; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx000001F4 (FCH::GPIO::ESPI\_CS1\_L\_AGPI0125)**

Reset: 0014\_0000h.

\_aliasHOSTLEGACY; GPIOx000001F4; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx000001F8 (FCH::GPIO::SPI\_CS2\_L\_AGPI0126)**

Reset: 0014\_0000h.

\_aliasHOSTLEGACY; GPIOx000001F8; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.



	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx00000204 (FCH::GPIO::ESPI\_RSTIN\_L\_KBRST\_L\_AGPI0129)**

Reset: 0014\_0000h.

\_aliasHOSTLEGACY; GPIOx00000204; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx0000020C (FCH::GPIO::ESPI1\_DAT0\_SPI1\_DAT0\_AGPIO131)**

Reset: 0014\_0000h.

\_aliasHOSTLEGACY; GPIOx0000020C; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx00000210 (FCH::GPIO::ESPI1\_DAT1\_SPI1\_DAT1\_AGPI0132)**

Reset: 0014\_0000h.

\_aliasHOSTLEGACY; GPIOx00000210; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx00000214 (FCH::GPIO::ESPI1\_DAT2\_SPI1\_DAT2\_AGPI0133)**

Reset: 0014\_0000h.

\_aliasHOSTLEGACY; GPIOx00000214; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.



	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx00000218 (FCH::GPIO::ESPI1\_DAT3\_SPI1\_DAT3\_AGPI0134)**

Reset: 0014\_0000h.

\_aliasHOSTLEGACY; GPIOx00000218; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx0000021C (FCH::GPIO::UART0\_CTS\_L\_UART2\_TXD\_AGPI0135)**

Reset: 0024\_0000h.

\_aliasHOSTLEGACY; GPIOx0000021C; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx00000220 (FCH::GPIO::UART0\_RXD\_AGPI0136)**

Reset: 0024\_0000h.

\_aliasHOSTLEGACY; GPIOx00000220; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx00000224 (FCH::GPIO::UART0\_RTS\_L\_UART2\_RXD\_AGPIO137)**

Reset: 0014\_0000h.

\_aliasHOSTLEGACY; GPIOx00000224; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.



	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx00000228 (FCH::GPIO::UART0\_TXD\_AGPI0138)**

Reset: 0014\_0000h.

\_aliasHOSTLEGACY; GPIOx00000228; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx0000022C (FCH::GPIO::UART0\_INTR\_AGPIO139)**

Reset: 0024\_0000h.

\_aliasHOSTLEGACY; GPIOx0000022C; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx00000234 (FCH::GPIO::UART1\_RXD\_AGPI0141)**

Reset: 0044\_0000h.

\_aliasHOSTLEGACY; GPIOx00000234; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 1. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx00000238 (FCH::GPIO::UART1\_TXD\_AGPI0142)**

Reset: 0024\_0000h.

\_aliasHOSTLEGACY; GPIOx00000238; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.



	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx00000244 (FCH::GPIO::I3C0\_SCL\_I2C0\_SCL\_SPD0\_SCL\_SMBUS0\_SCL\_AGPIO145)**

Reset: 0004\_0000h.

\_aliasHOSTLEGACY; GPIOx00000244; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx00000248 (FCH::GPIO::I3C0\_SDA\_I2C0\_SDA\_SPD0\_SDA\_SMBUS0\_SDA\_AGPI0146)**

Reset: 0004\_0000h.

\_aliasHOSTLEGACY; GPIOx00000248; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx0000024C (FCH::GPIO::I3C1\_SCL\_I2C1\_SCL\_SPD1\_SCL\_AGPIO147)**

Reset: 0004\_0000h.

\_aliasHOSTLEGACY; GPIOx0000024C; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx00000250 (FCH::GPIO::I3C1\_SDA\_I2C1\_SDA\_SPD1\_SDA\_AGPI0148)**

Reset: 0004\_0000h.

\_aliasHOSTLEGACY; GPIOx00000250; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.



	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx00000254 (FCH::GPIO::I3C2\_SCL\_I2C2\_SCL\_SPD2\_SCL\_AGPI0149)**

Reset: 0004\_0000h.

\_aliasHOSTLEGACY; GPIOx00000254; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx00000258 (FCH::GPIO::I3C2\_SDA\_I2C2\_SDA\_SPD2\_SDA\_AGPI0150)**

Reset: 0004\_0000h.

\_aliasHOSTLEGACY; GPIOx00000258; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx0000025C (FCH::GPIO::I3C3\_SCL\_I2C3\_SCL\_SPD3\_SCL\_AGPI0151)**

Reset: 0004\_0000h.

\_aliasHOSTLEGACY; GPIOx0000025C; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.

	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**GPIOx00000260 (FCH::GPIO::I3C3\_SDA\_I2C3\_SDA\_SPD3\_SDA\_AGPI0152)**

Reset: 0004\_0000h.

\_aliasHOSTLEGACY; GPIOx00000260; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h.



	<b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

GPIOx000002AC (FCH::GPIO::SPI_INT)	
Reset: 0000_0000h.	
_aliasHOSTLEGACY; GPIOx000002AC; GPIO=FED8_1500h	
Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

**GPIOx000002B0 (FCH::GPIO::INT\_NBGPPPMEPULSE)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx000002B0; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

**GPIOx000002B4 (FCH::GPIO::INT\_NBGPPHPULSE)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx000002B4; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

**GPIOx000002B8 (FCH::GPIO::INT ACPIPERFINTR)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx000002B8; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

**GPIOx000002BC (FCH::GPIO::INT\_SATA\_SCI\_SCI2)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx000002BC; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

**GPIOx000002C0 (FCH::GPIO::INT\_FANTHERMAL\_SCIOUT)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx000002C0; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

**GPIOx000002C4 (FCH::GPIO::INT\_ASFMASTERINTR)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx000002C4; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.



**GPIOx000002C8 (FCH::GPIO::INT\_RAS\_EVENT)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx000002C8; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

GPIOx000002CC (FCH::GPIO::INT_GBL_RLS)	
Reset: 0000_0000h.	
_aliasHOSTLEGACY; GPIOx000002CC; GPIO=FED8_1500h	
Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

**GPIOx000002D0 (FCH::GPIO::INT\_SHORTTIMEREVENT\_LONGTIMEREVENT)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx000002D0; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

**GPIOx000002D4 (FCH::GPIO::INT\_NBASSERTION)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx000002D4; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

**GPIOx000002D8 (FCH::GPIO::INT\_ESPIPME)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx000002D8; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic) (NOTE: This Event is low enable)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

**GPIOx000002DC (FCH::GPIO::INT\_ESPISYSEVT)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx000002DC; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic) (NOTE: This Event is low enable)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

**GPIOx000002E0 (FCH::GPIO::INT\_ESPIPME1)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx000002E0; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic) (NOTE: This Event is low enable)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

**GPIOx000002E4 (FCH::GPIO::INT\_ESPISYSEVT1)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx000002E4; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic) (NOTE: This Event is low enable)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.



**GPIOx000002F0 (FCH::GPIO::GPIO\_WAKE\_STATUS\_INDEX\_0)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx000002F0; GPIO=FED8\_1500h

Bits	Description
31:16	<b>wake_status_index_31_16.</b> Read-write. Reset: 0000h. Read-only. When this bit is 1, it means at least one of the wake status of GPIO N*4 ~ N*4+3 is 1. N = 16~31
15	<b>wake_status_index_15.</b> Read-write. Reset: 0. Read-only. When this bit is 1, it means at least one of the wake status of GPIO 60~62 is 1.
14:0	<b>wake_status_index_14_0.</b> Read-write. Reset: 0000h. Read-only. When this bit is 1, it means at least one of the wake status of GPIO N*4 ~ N*4+3 is 1. N = 0~14

**GPIOx000002F4 (FCH::GPIO::GPIO\_WAKE\_STATUS\_INDEX\_1)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx000002F4; GPIO=FED8\_1500h

Bits	Description
31:16	Reserved.
15	<b>nbgpppmewake.</b> Read-write. Reset: 0. <b>Description:</b> Read-only. 1: NBGpp has sent PME to wake the system. (one of wake status is set in Gpio Bank3 register) 0: no NBGpp Pme wake event
14	Reserved.
13:0	<b>wake_status_index_45_32.</b> Read-write. Reset: 0000h. Read-only. When this bit is 1, it means at least one of the wake status of GPIO N*4 ~ N*4+3 is 1. N = 32~45

**GPIOx000002F8 (FCH::GPIO::GPIO\_INTERRUPT\_STATUS\_INDEX\_0)**

Read-write. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx000002F8; GPIO=FED8\_1500h

Bits	Description
31:16	<b>interrupt_status_index_31_16.</b> Read-write. Reset: 0000h. Read-only. When this bit is 1, it means at least one of the interrupt status of GPIO N*4 ~ N*4+3 is 1. N = 16~31
15	<b>interrupt_status_index_15.</b> Read-write. Reset: 0. Read-only. When this bit is 1, it means at least one of the interrupt status of GPIO 60~62 is 1.
14:0	<b>interrupt_status_index_14_0.</b> Read-write. Reset: 0000h. Read-only. When this bit is 1, it means at least one of the interrupt status of GPIO N*4 ~ N*4+3 is 1. N = 0~14

**GPIOx000002FC (FCH::GPIO::GPIO\_INTERRUPT\_STATUS\_INDEX\_1)**

Read-write. Reset: 1F00\_0000h.

\_aliasHOSTLEGACY; GPIOx000002FC; GPIO=FED8\_1500h

Bits	Description
31:29	Reserved.
28	<b>mask_sts_en.</b> Read-write. Reset: 1. This bit enables HW to block all wake/intr status generation when SW writes any Debounce* registers. The length of blocking depends on mask_sts_length[3:0].
27:24	<b>mask_sts_length_3_0.</b> Read-write. Reset: Fh. <b>Description:</b> See mask_sts_en as well. The length of blocking = {mask_sts_length[11:0], 14'h3FFF}
23:16	<b>mask_sts_length_11_4.</b> Read-write. Reset: 00h. <b>Description:</b> See mask_sts_en as well. The length of blocking = {mask_sts_length[11:0], 14'h3FFF}
15	<b>nbgpppmeintr.</b> Read-write. Reset: 0. <b>Description:</b> Read-only. 1: NB GPP has sent PME (one of Intr status is set in Gpio Bank3 register) 0: no NB GPP Pme event
14	Reserved.
13:0	<b>interrupt_status_index_45_32.</b> Read-write. Reset: 0000h. Read-only. When this bit is 1, it means at least one of the interrupt status of GPIO N*4 ~ N*4+3 is 1. N = 32~45

**GPIOx00000300 (FCH::GPIO::INT\_NBGPPORTDEV0PME)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx00000300; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27	Reserved.
26	<b>rxdisable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Enable GPIO PAD receive 1: Disable GPIO PAD receive
25	<b>swcntrlcn.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlcn.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

**GPIOx00000304 (FCH::GPIO::INT\_NBGPPORTDEV1PME)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx00000304; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27:26	Reserved.
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

**GPIOx00000308 (FCH::GPIO::INT\_NBGPPORTDEV2PME)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx00000308; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27:26	Reserved.
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

**GPIOx0000030C (FCH::GPIO::INT\_NBGPPPORTDEV3PME)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx0000030C; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27:26	Reserved.
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

**GPIOx00000310 (FCH::GPIO::INT\_NBGPPORTDEV4PME)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx00000310; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27:26	Reserved.
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

**GPIOx00000314 (FCH::GPIO::INT\_NBGPPORTDEV5PME)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx00000314; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27:26	Reserved.
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.



**GPIOx00000318 (FCH::GPIO::INT\_NBGPPORTDEV6PME)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx00000318; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27:26	Reserved.
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

**GPIOx0000031C (FCH::GPIO::INT\_NBGPPPORTDEV7PME)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx0000031C; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27:26	Reserved.
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

**GPIOx00000320 (FCH::GPIO::INT\_NBGPPORTDEV8PME)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx00000320; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27:26	Reserved.
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

**GPIOx00000324 (FCH::GPIO::INT\_NBGPPORTDEV9PME)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx00000324; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27:26	Reserved.
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

**GPIOx00000328 (FCH::GPIO::INT\_NBGPPORTDEV10PME)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx00000328; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27:26	Reserved.
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

**GPIOx0000032C (FCH::GPIO::INT\_NBGPPPORTDEV11PME)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx0000032C; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27:26	Reserved.
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

**GPIOx00000330 (FCH::GPIO::INT\_NBGPPORTDEV12PME)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx00000330; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27:26	Reserved.
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

**GPIOx00000334 (FCH::GPIO::INT\_NBGPPORTDEV13PME)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx00000334; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27:26	Reserved.
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.



**GPIOx00000338 (FCH::GPIO::INT\_NBGPPORTDEV14PME)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx00000338; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27:26	Reserved.
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

**GPIOx0000033C (FCH::GPIO::INT\_NBGPPPORTDEV15PME)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx0000033C; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27:26	Reserved.
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

**GPIOx00000340 (FCH::GPIO::INT\_NBGPPORTDEV16PME)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx00000340; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27:26	Reserved.
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

**GPIOx00000344 (FCH::GPIO::INT\_NBGPPORTDEV17PME)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx00000344; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27:26	Reserved.
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

**GPIOx00000348 (FCH::GPIO::INT\_NBGPPORTDEV18PME)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx00000348; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27:26	Reserved.
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

**GPIOx0000034C (FCH::GPIO::INT\_NBGPPPORTDEV19PME)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx0000034C; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27:26	Reserved.
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

**GPIOx00000350 (FCH::GPIO::INT\_NBGPPORTDEV20PME)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx00000350; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27:26	Reserved.
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

**GPIOx00000354 (FCH::GPIO::INT\_NBGPPORTDEV21PME)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx00000354; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27:26	Reserved.
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.



**GPIOx00000358 (FCH::GPIO::INT\_NBGPPORTDEV22PME)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx00000358; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27:26	Reserved.
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

**GPIOx0000035C (FCH::GPIO::INT\_NBGPPPORTDEV23PME)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx0000035C; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27:26	Reserved.
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

**GPIOx00000360 (FCH::GPIO::INT\_NBGPPORTDEV24PME)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx00000360; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27:26	Reserved.
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

**GPIOx00000364 (FCH::GPIO::INT\_NBGPPORTDEV25PME)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx00000364; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27:26	Reserved.
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

**GPIOx00000368 (FCH::GPIO::INT\_NBGPPORTDEV26PME)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx00000368; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27:26	Reserved.
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

**GPIOx0000036C (FCH::GPIO::INT\_NBGPPPORTDEV27PME)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx0000036C; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27:26	Reserved.
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

**GPIOx00000370 (FCH::GPIO::INT\_NBGPPORTDEV28PME)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx00000370; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27:26	Reserved.
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

**GPIOx00000374 (FCH::GPIO::INT\_NBGPPORTDEV29PME)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx00000374; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27:26	Reserved.
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.



**GPIOx00000378 (FCH::GPIO::INT\_NBGPPORTDEV30PME)**

Reset: 0000\_0000h.

\_aliasHOSTLEGACY; GPIOx00000378; GPIO=FED8\_1500h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27:26	Reserved.
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

GPIOx0000037C (FCH::GPIO::INT_NBGPPPORTDEV31PME)	
Reset: 0000_0000h.	
_aliasHOSTLEGACY; GPIOx0000037C; GPIO=FED8_1500h	
Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27:26	Reserved.
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23:17	Reserved.
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)
12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7:0	Reserved.

### 11.3.10.3 REMOTE GPIO and IOMUX Registers

Remote GPIO register and Remote IOMUX register (GPIO256 ~ GPIO266) are in the same bank which is different with other GPIO (GPIO0 ~ GPIO255). Each Remote GPIO PAD requires 32-bit GPIO register and 8-bit IOMUX register.

Table 200: Remote GPIO Register Offset and Default Value

Register offset	Reset	Function
0x00	0014_0000h	AGPIO256_SGPIO0_CLK

0x04	0014_0000h	AGPIO257_SGPIO1_CLK_CLK_REQ01_L
0x08	0014_0000h	AGPIO258_SGPIO2_CLK_CLK_REQ02_L
0x0C	0014_0000h	AGPIO259_SGPIO3_CLK
0x10	0014_0000h	SGPIO_DATAOUT_AGPIO260
0x14	0014_0000h	SGPIO_LOAD_AGPIO261
0x18	0024_0000h	Reserved
0x1C	0024_0000h	Reserved
0x20	0014_0000h	USB00_OC_L_AGPIO264
0x24	0014_0000h	USB01_OC_L_AGPIO265
0x28	0004_0000h	PCIE_RST0_L_AGPIO266
0x2C	0000_0000h	Reserved
0x30	0000_0000h	Reserved
0x34	0000_0000h	Reserved
0x38	0024_0000h	Reserved
0x3C	0024_0000h	Reserved
** Offset 0x40 – 0xBF are reserved		

Table 201: Remote IOMUX Register Offset and Default Value

Register offset	Reset	Function
0xC0	00b	GPIO256
0xC1	00b	GPIO257
0xC2	00b	GPIO258
0xC3	00b	GPIO259
0xC4	00b	SGPIO_DATAOUT
0xC5	00b	SGPIO_LOAD
0xC6	00b	Reserved
0xC7	00b	Reserved
0xC8	00b	USB00_OC_L
0xC9	00b	USB01_OC_L
0xCA	00b	PCIE_RST0_L
0xCB	00b	Reserved
0xCC	00b	Reserved
0xCD	00b	Reserved
0xCE	00b	Reserved
0xCF	00b	Reserved
** Offset 0xD0 – 0xEF are reserved		

Table 202: Remote IOMUX Function Table

IOMUX	Pin Name	Do mai n	GP IO	G EV EN T	Ov err ide _0	Ov err ide _1	IOMUX =0	IOMUX =1	IO MU X=2	IO MU X=3	Defau lt	Reset value
IOMUXx 100	AGPIO256_SGPIO0_C LK	S5	256				GPIO25 6	SGPIO0 _CLK	GPI O25 6	GPI O25 6	PU	00
IOMUXx 101	AGPIO257_SGPIO1_C LK_CLK_REQ01_L	S5	257				GPIO25 7	SGPIO1 _CLK	CL K_ RE	GPI O25 7	PU	00

									G01_L			
IOMUXx 102	AGPIO258_SGPIO2_CLK_REQ02_L	S5	258				GPIO258	SGPIO2_CLK	CLK_REQ02_L	GPI O258	PU	00
IOMUXx 103	AGPIO259_SGPIO3_CLK	S5	259				GPIO259	SGPIO3_CLK	GPI O259	GPI O259	PU	00
IOMUXx 104	SGPIO_DATAOUT_A GPIO260	S5	260				SGPIO_DATAOUT	GPIO260	GPI O260	GPI O260	PU	00
IOMUXx 105	SGPIO_LOAD_A GPIO261	S5	261				SGPIO_LOAD	GPIO261	GPI O261	GPI O261	PU	00
IOMUXx 108	USB00_OC_L_A GPIO264	S5	264				USB00_OC_L	GPIO264	GPI O264	GPI O264	PU	00
IOMUXx 109	USB01_OC_L_A GPIO265	S5	265				USB01_OC_L	GPIO265	GPI O265	GPI O265	PU	00
IOMUXx 10A	PCIE_RST0_L_A GPIO266	S5	266				PCIE_RST0_L	GPIO266	GPI O266	GPI O266	N/A	00

**REMOTEGPIOx00000000 (FCH::RMTGPIO::AGPIO256\_SGPIO0\_CLK)**

Reset: 0014\_0000h.

\_aliasHOSTLEGACY; REMOTEGPIOx00000000; REMOTEGPIO=FED8\_1200h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27:26	Reserved.
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)

12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**REMOTEGPIOx00000004 (FCH::RMTGPIO::AGPIO257\_SGPIO1\_CLK\_CLK\_REQ01\_L)**

Reset: 0014\_0000h.

\_aliasHOSTLEGACY; REMOTEGPIOx00000004; REMOTEGPIO=FED8\_1200h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27:26	Reserved.
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)

12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)



**REMOTEGPIOx00000008 (FCH::RMTGPIO::AGPIO258\_SGPIO2\_CLK\_CLK\_REQ02\_L)**

Reset: 0014\_0000h.

\_aliasHOSTLEGACY; REMOTEGPIOx00000008; REMOTEGPIO=FED8\_1200h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27:26	Reserved.
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)

12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**REMOTEGPIOx0000000C (FCH::RMTGPIO::AGPIO259\_SGPIO3\_CLK)**

Reset: 0014\_0000h.

\_aliasHOSTLEGACY; REMOTEGPIOx0000000C; REMOTEGPIO=FED8\_1200h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27:26	Reserved.
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)

12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**REMOTEGPIOx00000010 (FCH::RMTGPIO::SGPIO\_DATAOUT\_AGPIO260)**

Reset: 0014\_0000h.

\_aliasHOSTLEGACY; REMOTEGPIOx00000010; REMOTEGPIO=FED8\_1200h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27:26	Reserved.
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)

12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**REMOTEGPIOx00000014 (FCH::RMTGPIO::SGPIO\_LOAD\_AGPIO261)**

Reset: 0014\_0000h.

\_aliasHOSTLEGACY; REMOTEGPIOx00000014; REMOTEGPIO=FED8\_1200h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27:26	Reserved.
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)

12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)



**REMOTEGPIOx00000020 (FCH::RMTGPIO::USB00\_OC\_L\_AGPI0264)**

Reset: 0024\_0000h.

\_aliasHOSTLEGACY; REMOTEGPIOx00000020; REMOTEGPIO=FED8\_1200h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27:26	Reserved.
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)

12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrmlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**REMOTEGPIOx00000024 (FCH::RMTGPIO::USB01\_OC\_L\_AGPI0265)**

Reset: 0024\_0000h.

\_aliasHOSTLEGACY; REMOTEGPIOx00000024; REMOTEGPIO=FED8\_1200h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27:26	Reserved.
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)

12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**REMOTEGPIOx00000028 (FCH::RMTGPIO::PCIE\_RST0\_L\_AGPI0266)**

Reset: 0024\_0000h.

\_aliasHOSTLEGACY; REMOTEGPIOx00000028; REMOTEGPIO=FED8\_1200h

Bits	Description
31:30	Reserved.
29	<b>wakests.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't generate wake event. 1: the pin is one of wake source Writing 1 to clear the bit to 0.
28	<b>interruptsts.</b> Read-write,Read, <a href="#">Write-1-to-clear</a> . Reset: 0. <b>Description:</b> 0: the pin doesn't cause interrupt. 1: the pin is one of interrupt source Writing 1 to clear the bit to 0.
27:26	Reserved.
25	<b>swcntrlen.</b> Read-write. Reset: 0. <b>Description:</b> 0: Disable software controlled GPIO in 1: Enable software controlled GPIO in
24	<b>swcntrlin.</b> Read-write. Reset: 0. When SwCntrlEn is 1, this bit can be used by software to control the GPIO input to the GPIO controller. This might be useful during debug or work-around.
23	<b>outputenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Output is disabled on the pin 1: Output is enabled on the pin.
22	<b>outputvalue.</b> Read-write. Reset: 0. <b>Description:</b> 0: low. 1: high.
21	<b>pulldownenable.</b> Read-write. Reset: 1. <b>Description:</b> 0: Pull-down is disabled on the pin. 1: Pull-down is enabled on the pin.
20	<b>pullupenable.</b> Read-write. Reset: 0. <b>Description:</b> 0: Pull-up is disabled on the pin. 1: Pull-up is enabled on the pin.
19	Reserved.
18:17	<b>drvstrengthsel.</b> Read-write. Reset: 2h. <b>Description:</b> 3.3V PAD: x0: Z= 40 ohms x1: Z= 80 ohms 1.8V PAD: 00: not supported 01: Z= 60 ohms 10: Z= 40 ohms 11: Z= 80 ohms
16	<b>pinsts.</b> Read-write. Reset: 0. <b>Description:</b> Read only. 0: the pin is low 1: the pin is high (NOTE: the bit doesn't affected by debounce logic)
15:13	<b>wakecntrl_2_0.</b> Read-write. Reset: 0h. <b>Description:</b> WakeCntrl[0] enables wake in Power saving mode state WakeCntrl[1] enables wake in S3 state (SLP_TYP = 3, and !G0_State) WakeCntrl[2] enables wake in S4/S5 state (SLP_TYP = 4 or 5, and !G0_State)

12:11	<b>interruptenable_1_0.</b> Read-write. Reset: 0h. <b>Description:</b> InterruptEnable[0] enables interrupt status InterruptEnable[1] enables interrupt delivery
10:9	<b>activelevel.</b> Read-write. Reset: 0h. <b>Description:</b> 00: Active high 01: Active Low. 10: Active on both of edges if LevelTrig is set to 0 11: reserved
8	<b>leveltrig.</b> Read-write. Reset: 0. <b>Description:</b> 0: Edge trigger 1: Level trigger
7	<b>debouncetmrmlarge.</b> Read-write. Reset: 0. Combined with DebounceTmrOutUnit, this bit change the unit and max debounce time for the debounce timer. Please refer to "DebounceTmrOutUnit" description for details.
6:5	<b>debouncecntrl.</b> Read-write. Reset: 0h. <b>Description:</b> 00: No debounce 01: Preserve low glitch 10: Preserve high glitch 11: Remove glitch
4	<b>debouncetmroutunit.</b> Read-write. Reset: 0. <b>Description:</b> {DebounceTmrLarge, DebounceTmrOutUnit} defines the unit and max debounce time for the debounce timer, 00: Timer Unit = 61 usec (2 RtcClk), Max Debounce Time = 976 usec 01: Timer Unit = 244 usec (8 RtcClk), Max Debounce Time = 3.9 msec 10: Timer Unit = 15.6 msec (512 RtcClk), Max Debounce Time = 250 msec 11: Timer Unit = 62.5 msec (2048 RtcClk), Max Debounce Time = 1.0 sec
3:0	<b>debouncetmrout.</b> Read-write. Reset: 0h. Debounce timer out number ( 0 means that debouncing logic is disabled)

**REMOTEGPIOx000000C0 (FCH::RMTGPIO::IOMUX0\_GPIO256)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number of IoMux, from 0 to 15, IoMux0 for GPIO256, , IoMux register at C0h ~ CFh.

&lt;X&gt; denotes GPIO number in decimal: 256 ~ 271.

\_aliasHOSTLEGACY; REMOTEGPIOx000000C0; REMOTEGPIO=FED8\_1200h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**REMOTEGPIOx000000C1 (FCH::RMTGPIO::IOMUX1\_GPIO257)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number of IoMux, from 0 to 15, IoMux0 for GPIO256, , IoMux register at C0h ~ CFh.

&lt;X&gt; denotes GPIO number in decimal: 256 ~ 271.

\_aliasHOSTLEGACY; REMOTEGPIOx000000C1; REMOTEGPIO=FED8\_1200h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**REMOTEGPIOx000000C2 (FCH::RMTGPIO::IOMUX2\_GPIO258)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number of IoMux, from 0 to 15, IoMux0 for GPIO256, , IoMux register at C0h ~ CFh.

&lt;X&gt; denotes GPIO number in decimal: 256 ~ 271.

\_aliasHOSTLEGACY; REMOTEGPIOx000000C2; REMOTEGPIO=FED8\_1200h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**REMOTEGPIOx000000C3 (FCH::RMTGPIO::IOMUX3\_GPIO259)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number of IoMux, from 0 to 15, IoMux0 for GPIO256, , IoMux register at C0h ~ CFh.

&lt;X&gt; denotes GPIO number in decimal: 256 ~ 271.

\_aliasHOSTLEGACY; REMOTEGPIOx000000C3; REMOTEGPIO=FED8\_1200h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**REMOTEGPIOx000000C4 (FCH::RMTGPIO::IOMUX4\_GPIO260)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number of IoMux, from 0 to 15, IoMux0 for GPIO256, , IoMux register at C0h ~ CFh.

&lt;X&gt; denotes GPIO number in decimal: 256 ~ 271.

\_aliasHOSTLEGACY; REMOTEGPIOx000000C4; REMOTEGPIO=FED8\_1200h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**REMOTEGPIOx000000C5 (FCH::RMTGPIO::IOMUX5\_GPIO261)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number of IoMux, from 0 to 15, IoMux0 for GPIO256, , IoMux register at C0h ~ CFh.

&lt;X&gt; denotes GPIO number in decimal: 256 ~ 271.

\_aliasHOSTLEGACY; REMOTEGPIOx000000C5; REMOTEGPIO=FED8\_1200h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**REMOTEGPIOx000000C6 (FCH::RMTGPIO::IOMUX6\_GPIO262)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number of IoMux, from 0 to 15, IoMux0 for GPIO256, , IoMux register at C0h ~ CFh.

&lt;X&gt; denotes GPIO number in decimal: 256 ~ 271.

\_aliasHOSTLEGACY; REMOTEGPIOx000000C6; REMOTEGPIO=FED8\_1200h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3



**REMOTEGPIOx000000C7 (FCH::RMTGPIO::IOMUX7\_GPIO263)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number of IoMux, from 0 to 15, IoMux0 for GPIO256, , IoMux register at C0h ~ CFh.

&lt;X&gt; denotes GPIO number in decimal: 256 ~ 271.

\_aliasHOSTLEGACY; REMOTEGPIOx000000C7; REMOTEGPIO=FED8\_1200h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**REMOTEGPIOx000000C8 (FCH::RMTGPIO::IOMUX8\_GPIO264)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number of IoMux, from 0 to 15, IoMux0 for GPIO256, , IoMux register at C0h ~ CFh.

&lt;X&gt; denotes GPIO number in decimal: 256 ~ 271.

\_aliasHOSTLEGACY; REMOTEGPIOx000000C8; REMOTEGPIO=FED8\_1200h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**REMOTEGPIOx000000C9 (FCH::RMTGPIO::IOMUX9\_GPIO265)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number of IoMux, from 0 to 15, IoMux0 for GPIO256, , IoMux register at C0h ~ CFh.

&lt;X&gt; denotes GPIO number in decimal: 256 ~ 271.

\_aliasHOSTLEGACY; REMOTEGPIOx000000C9; REMOTEGPIO=FED8\_1200h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**REMOTEGPIOx000000CA (FCH::RMTGPIO::IOMUX10\_GPIO266)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number of IoMux, from 0 to 15, IoMux0 for GPIO256, , IoMux register at C0h ~ CFh.

&lt;X&gt; denotes GPIO number in decimal: 256 ~ 271.

\_aliasHOSTLEGACY; REMOTEGPIOx000000CA; REMOTEGPIO=FED8\_1200h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**REMOTEGPIOx000000CB (FCH::RMTGPIO::IOMUX11\_GPIO267)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number of IoMux, from 0 to 15, IoMux0 for GPIO256, , IoMux register at C0h ~ CFh.

&lt;X&gt; denotes GPIO number in decimal: 256 ~ 271.

\_aliasHOSTLEGACY; REMOTEGPIOx000000CB; REMOTEGPIO=FED8\_1200h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**REMOTEGPIOx000000CC (FCH::RMTGPIO::IOMUX12\_GPIO268)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number of IoMux, from 0 to 15, IoMux0 for GPIO256, , IoMux register at C0h ~ CFh.

&lt;X&gt; denotes GPIO number in decimal: 256 ~ 271.

\_aliasHOSTLEGACY; REMOTEGPIOx000000CC; REMOTEGPIO=FED8\_1200h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**REMOTEGPIOx000000CD (FCH::RMTGPIO::IOMUX13\_GPIO269)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number of IoMux, from 0 to 15, IoMux0 for GPIO256, , IoMux register at C0h ~ CFh.

&lt;X&gt; denotes GPIO number in decimal: 256 ~ 271.

\_aliasHOSTLEGACY; REMOTEGPIOx000000CD; REMOTEGPIO=FED8\_1200h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**REMOTEGPIOx000000CE (FCH::RMTGPIO::IOMUX14\_GPIO270)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number of IoMux, from 0 to 15, IoMux0 for GPIO256, , IoMux register at C0h ~ CFh.

&lt;X&gt; denotes GPIO number in decimal: 256 ~ 271.

\_aliasHOSTLEGACY; REMOTEGPIOx000000CE; REMOTEGPIO=FED8\_1200h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**REMOTEGPIOx000000CF (FCH::RMTGPIO::IOMUX15\_GPIO271)**

Read-write. Reset: 00h.

\*Note:

&lt;N&gt; denotes number of IoMux, from 0 to 15, IoMux0 for GPIO256, , IoMux register at C0h ~ CFh.

&lt;X&gt; denotes GPIO number in decimal: 256 ~ 271.

\_aliasHOSTLEGACY; REMOTEGPIOx000000CF; REMOTEGPIO=FED8\_1200h

Bits	Description
7:2	Reserved.
1:0	<b>iomux_gpio_x.</b> Read-write. Reset: 0h. <b>Description:</b> Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3

**REMOTEGPIOx000000F0 (FCH::RMTGPIO::RMT\_GPIO\_WAKE\_STATUS)**

Read-only. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; REMOTEGPIOx000000F0; REMOTEGPIO=FED8\_1200h

Bits	Description
31:16	Reserved.
15:0	<b>gpioxxx_wake_status.</b> Read-only. Reset: 0000h. Wake status of GPIO256 (bit[0]) GPIO271 (bit[15])

**REMOTEGPIOx000000F4 (FCH::RMTGPIO::RMT\_GPIO\_INTERRUPT\_STATUS)**

Read-only. Reset: 0000\_0000h.

\_aliasHOSTLEGACY; REMOTEGPIOx000000F4; REMOTEGPIO=FED8\_1200h

Bits	Description
31:16	Reserved.
15:0	<b>gpioxxx_intr_status</b> . Read-only. Reset: 0000h. Interrupt status of GPIO256 (bit[0]) GPIO271 (bit[15])

**REMOTEGPIOx000000FC (FCH::RMTGPIO::RMT\_GPIO\_MASTER\_SWITCH)**

Read-write. Reset: 1F00\_0000h.

\_aliasHOSTLEGACY; REMOTEGPIOx000000FC; REMOTEGPIO=FED8\_1200h

Bits	Description
31:29	Reserved.
28	<b>mask_sts_en</b> . Read-write. Reset: 1. This bit enables HW to block all wake/intr status generation when SW writes any Debounce* registers. The length of blocking depends on mask_sts_length[11:0] using pciclk to count, default = $15.15\text{ns} * 0x40000 = 4\text{ms}$
27:24	<b>mask_sts_length_3_0</b> . Read-write. Reset: Fh. <b>Description:</b> See mask_sts_en as well. The length of blocking = {mask_sts_length[11:0], 14'h3FFF}
23:16	<b>mask_sts_length_11_4</b> . Read-write. Reset: 00h. <b>Description:</b> See mask_sts_en as well. The length of blocking = {mask_sts_length[11:0], 14'h3FFF}
15:0	Reserved.