

**Processor Programming
Reference (PPR)
for AMD Family 1Ah
Model 11h, Revision B0
Processors
Volume 3 of 7**

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4 System Management Unit (SMU)

4.1 SMU Overview

The System Management Unit (SMU) is a subcomponent of the SOC that is responsible for a variety of system and power management tasks during boot and runtime.

4.2 Initialization

The SMU does not require software initialization. Upon successful boot-up the SMU is ready for operation.

4.3 SMU Features

This section describes SOC features controlled by the SMU.

4.3.1 Clocking

The processor contains multiple PLLs to create all necessary clock signals. The [PMFW](#) controls all clock frequencies based on current performance and power requirements. Software does not directly control clock frequencies.

4.3.2 Sideband Interface (SBI)

The sideband interface ([SBI](#)) supports the following interface(s):

- The Remote Management Interface ([SB-RMI](#)) (see the Advanced Platform Management Link ([APML](#)) Specification for details 1.2 [[Reference Documents](#)]).
- The Temperature Sensor Interface ([SB-TSI](#)) (see the SBI Temperature Sensor Interface (SB-TSI) for details refer to 6 [[SB Temperature Sensor Interface \(SB-TSI\)](#)]).

4.4 Thermal (THM)

The thermal block contains all the features related to temperature sensing, control, and reporting. It includes:

- Temperature collection and calculation logic.
- Fan speed control for off-chip fans.
- Temperature reporting through the [APML](#) interface.

4.4.1 Registers

SMUTHMx00000000 (SMU::THM::THM_TCON_CUR_TMP)

Reset: 0000_0000h.

TCON Current Temperature Control

_aliasSMN; SMUTHMx00000000; SMUTHM=0005_9800h

Bits	Description
31:21	CUR_TEMP. Read-only. Reset: 000h. Provides current control temperature (Tctl) after the slew-rate controls have been applied.
20	Reserved.
19	CUR_TEMP_RANGE_SEL. Read-write. Reset: 0. 0=Report on 0C to 225C scale range. 1=Report on -49C to 206C scale range.
18:0	Reserved.

SMUTHMx00000410 (SMU::THM::SMUSBI_SBIREGADDR)

Read-write. Reset: 0000_0000h.

_aliasSMN; SMUTHMx00000410; SMUTHM=0005_9800h

Bits	Description
31:19	Reserved.
18:11	SBRMI_HI_Address. Read-write. Reset: 00h. Select SBRMI internal register high byte address for Read or Write.
10:9	SIZE. Read-write. Reset: 0h. N+1 bytes to be read or written
8	TSI_RMI_SEL. Read-write. Reset: 0. When set to 0 selects SB-TSI register set; otherwise selects SB-RMI registers.
7:0	Address. Read-write. Reset: 00h. Select SBI internal register address for Read or Write.

SMUTHMx00000414 (SMU::THM::SMUSBI_SBIREGDATA)

Read-write. Reset: 0000_0000h.

_aliasSMN; SMUTHMx00000414; SMUTHM=0005_9800h

Bits	Description
31:0	SBI_REGDATA. Read-write. Reset: 0000_0000h. Read or Write data for SBI internal register address.

SMUTHMx00000424 (SMU::THM::SMUSBI_ERRATA_STAT_REG)

Read-only. Reset: 0000_0000h.

_aliasSMN; SMUTHMx00000424; SMUTHM=0005_9800h

Bits	Description
31:0	ERRATA_STAT_REG. Read-only. Reset: 0000_0000h. Errata status.