# AMD PENSANDO® 2<sup>ND</sup> GENERATION PLUS ("GIGLIO") DATA PROCESSING UNIT

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# **Overview**

The second-generation plus AMD Pensando<sup>™</sup> data processing unit (DPU), Giglio, is a power- and performance-optimized chip based on the second-generation AMD Pensando "Elba" DPU. It is source-code compatible with its predecessors, making it easy for existing customers to adopt, and simplifying integration with partner products.

It offers advanced capabilities for offloading various data center networking, storage and security services at 2 x 200 Gb/s line rate, at cloud scale. It features a P4-programmable pipeline comprised of 144 custom match processing units (MPUs), combined with a 16x A72 ARM<sup>®</sup> core complex, and dedicated data encryption and storage offload engines, all tied together via a proprietary fast network-on-a-chip interconnect. Giglio's unique architecture allows AMD, its customers, and partners to create highly efficient and scalable solutions deploying a rich set of software-defined networking, storage, and security features in a virtualized, broadly distributed, centrally managed way.

The Giglio DPU is designed to allow the implementation of complex traffic processing and forwarding algorithms, including network virtualization and security, packet encapsulation/decapsulation, inline encryption/decryption, and network address translation.

The Giglio DPU architecture supports stateful packet processing, which can be used for flow monitoring, flow-aware security policies implementation, help against DDoS attacks, and more.

Dedicated offload engines facilitate seamless and efficient processing of computation-heavy operations used in various encryption and storage algorithms, including compression/decompression, checksums, RAID, and deduplication hashing.

AMD Pensando DPUs are programmed using the industry standard P4 language, facilitating the implementation of a wide variety of system solutions. It supports software-defined networking and storage protocols, including NVMe virtualization and transport, and is designed to give developers the agility to develop and deploy new features and modifications to satisfy evolving customer needs throughout its product life cycle. Giglio is source-code compatible with software written for the previous Capri and Elba DPUs.

The Giglio DPU form factor and power profile is designed to support multiple system level implementations, ranging from a half-height, half-length PCIe card that can fit into the power and cooling profiles of any standard server, to network and security



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appliances and Smart Switches. The P4-programmable design enables these applications to dynamically re-configure the data processing inside the DPU.

# **Key Features**

Feature	Description	
Network Interfaces	56 Gb/s PAM4 SerDes supporting Dual 200 GE, Quad- 100/50/25/10 GE 1GE Management Port	
PCIe <sup>®</sup> Interface	16 lanes of PCIe Gen4, configurable as root complex or end- point mode 2x8 or 4x4 with QoS support in multi-host applications	
Data Pipeline	P4 data pipeline comprised of 144 match processing units (MPUs) @ 2 GHz Provides high performance capabilities in packet and message processing, at line rate.	
SOC	16x Arm A72 CPU cores @ 3 GHz with I-Cache, D-Cache, and LLC Cache QSPI Flash, EMMC storage for embedded OS Secure Boot with hardware root of trust	
Memory	Dual DDR5-5600 interfaces supporting 8 - 64 GB system memory	
Offloads	Inline IPsec and DTLS, bulk crypto, PKE, compression, decompression, checksums, deduplication, erasure coding	
Scale	2K VNICs, 16M hardware queues, highly scalable P4 tables (stateful and stateless) accessible at every stage of pipeline	
Scheduling	<ul> <li>Queue Group scheduling with Min/Max rate</li> <li>High Priority Option per queue group</li> <li>P4 meters and QoS priorities</li> <li>DDR Buffer Overflow: Supports 200 Gb/s write</li> </ul>	
RoCEv2	<ul> <li>Memory-based scatter-gather lists (SGL) in DMA commands</li> <li>Latency optimized hardware data path with all context on DPU</li> </ul>	
Single Wire Management	Connects 1 GE BMC controller and uplink ports in standby power mode	



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# **Typical System Configurations**

The Giglio DPU can be deployed in various system configurations. Typical configurations are listed below:

Model	PCle	Notes
Standard PCIe Card	8 lanes Gen3/4	Low Power PCIe card Uplinks: 2x10/25/100 GE + 1x1 GE Mgmt
High Performance PCIe Card	16 lanes Gen4	Single or Multi-host support Uplinks: 2x200 GE + 1x1 GE Mgmt
Data Center Appliance	16 lanes Gen4	Uplinks: 2x200 GE

# **Key Applications**

Application	Details
Advanced Networking	Full support for SDN, Virtual Private Networks (Network Overlays), L3 ECMP, Load Balancing, NAT, PAT
Cutting-Edge Security Features	Stateful Firewall, Security Groups, Stateless and Reflexive ACLs, VPN Termination (IPsec), TLS/DTLS encryption, TLS Proxy
Enhanced Storage	Full support for SDS, NVMe virtualization, NVMe-oF with RDMA or TCP Transport, AES-XTS data-at-rate encryption, compression/decompression, SHA-3 deduplication, CRC-64/CRC-32 and checksum acceleration
Advanced Observability	Flow-based packet telemetry, stateful connection tracking, latency metrics, highly scalable per-packet counters
Cloud Infrastructure	Virtual Private Cloud (VPC), Security Groups, Firewalls, DDoS protection, Transit Gateway and VPC Peering, NAT Gateway, Load Balancer, Metering, Rate Control and QoS marking, SR-IOV for Workload Traffic/resource isolation, IPsec/VPN Gateway



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### **Hardware and Support**

For information about ordering Distributed Services Cards based on the AMD Pensando 2nd generation plus ("Giglio") DPU, and the appropriate support for your deployment, please contact your AMD sales representative.

In addition to the PCIe card-based form factor, DPU-only deployments are also possible; consult your AMD sales or partner representative for further information.

#### **For Developers**

AMD offers a Software-in-Silicon Development Kit (SSDK) to facilitate building customer and partner software solutions leveraging the unique capabilities of the Elba DPU and its existing rich set of software service libraries. Visit <u>amd.com/pensando</u> for details.





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