

Processor Programming Reference (PPR) for AMD Family 19h Model 61h, Revision B1 Processors

Legal Notices

© 2022,2023 Advanced Micro Devices, Inc. All rights reserved.

The information contained herein is for informational purposes only, and is subject to change without notice. While every precaution has been taken in the preparation of this document, it may contain technical inaccuracies, omissions and typographical errors, and AMD is under no obligation to update or otherwise correct this information. Advanced Micro Devices, Inc. makes no representations or warranties with respect to the accuracy or completeness of the contents of this document, and assumes no liability of any kind, including the implied warranties of noninfringement, merchantability or fitness for particular purposes, with respect to the operation or use of AMD hardware, software or other products described herein. No license, including implied or arising by estoppel, to any intellectual property rights is granted by this document. Terms and limitations applicable to the purchase or use of AMD's products are as set forth in a signed agreement between the parties or in AMD's Standard Terms and Conditions of Sale.

Trademarks:

AMD, the AMD Arrow logo, and combinations thereof are trademarks of Advanced Micro Devices, Inc.

AGESA is a trademark of Advanced Micro Devices, Inc.

AMD Virtualization is a trademark of Advanced Micro Devices, Inc.

Adobe is a registered trademark of Adobe.

CXL is a trademark of Compute Express Link Consortium, Inc.

DirectX is a registered trademark of Microsoft Corporation.

HDMI is a trademark of HDMI Licensing, LLC.

Linux is a registered trademark of Linus Torvalds.

Microsoft is a registered trademark of Microsoft Corporation.

OpenCL is a trademark of Apple, Inc. used by permission by Khronos Group, Inc.

OpenGL is a registered trademark of Hewlett Packard Enterprise.

PCI Express is a registered trademark of PCI-SIG Corporation.

PCIe is a registered trademark of PCI-SIG Corporation.

Windows is a registered trademark of Microsoft Corporation.

Other product names used in this publication are for identification purposes only and may be trademarks of their respective companies.

Reverse engineering or disassembly is prohibited.

USE OF THIS PRODUCT IN ANY MANNER THAT COMPLIES WITH THE MPEG ACTUAL OR DE FACTO VIDEO AND/OR AUDIO STANDARDS IS EXPRESSLY PROHIBITED WITHOUT ALL NECESSARY LICENSES UNDER APPLICABLE PATENTS. SUCH LICENSES MAY BE ACQUIRED FROM VARIOUS THIRD PARTIES INCLUDING, BUT NOT LIMITED TO, IN THE MPEG PATENT PORTFOLIO, WHICH LICENSE IS AVAILABLE FROM MPEG LA, L.L.C., 6312 S. FIDDLERS GREEN CIRCLE, SUITE 400E, GREENWOOD VILLAGE, COLORADO 80111.

List of Chapters

- 1 Overview**
- 2 Core Complex (CCX)**
- 3 Reliability, Availability, and Serviceability (RAS) Features**
- 4 Advanced Platform Management Link (APML)**
- 5 SB Temperature Sensor Interface (SB-TSI)**

List of Namespaces

List of Definitions

Memory Map - MSR

Memory Map - SMN

Table of Contents

1	Overview
1.1	Intended Audience
1.2	Reference Documents
1.2.1	Documentation Conventions
1.3	Adobe® Reader
1.3.1	Adobe® Reader Configuration
1.3.1.1	Open Hyperlink Document in New Window
1.3.1.2	Show Toolbars
1.3.1.3	Show "Previous View" and "Next View" Buttons
1.3.2	Adobe® Reader Usage
1.3.2.1	Searching a Multiple Volume PPR
1.3.2.2	Cross-References and Hyperlinks
1.3.2.3	Expand Current Bookmark
1.4	Conventions
1.4.1	Numbering
1.4.2	Arithmetic And Logical Operators
1.4.2.1	Operator Precedence and Associativity
1.4.3	Register Mnemonics
1.4.3.1	Logical Mnemonic
1.4.3.2	Physical Mnemonic
1.4.4	Register Format
1.4.4.1	Register Instances
1.4.4.2	Register Physical Mnemonic, Title, and Name
1.4.4.3	Full Width Register Attributes
1.4.4.4	Register Description
1.4.4.5	Register Instance Table
1.4.4.5.1	Content Ordering in a Row
1.4.4.5.2	Multiple Instances Per Row
1.4.4.5.3	MSR Access Method
1.4.4.5.3.1	MSR Per-Thread Example
1.4.4.5.3.2	MSR Range Example
1.4.4.5.4	BAR Access Method
1.4.4.5.4.1	BAR as a Register Reference
1.4.4.5.5	PCICFG Access Method
1.4.4.5.5.1	PCICFG Bus Implied to be 00h
1.4.4.5.6	Data Port Access Method
1.4.4.6	Register Field Format
1.4.4.7	Simple Register Field Format
1.4.4.8	Complex Register Field Format
1.4.4.9	Field Name is Reserved
1.4.4.10	Field Access Type
1.4.4.10.1	Conditional Access Type Expression
1.4.4.11	Field Reset
1.4.4.12	Field Initialization
1.4.4.13	Field Check
1.4.4.14	Field Valid Values
1.4.5	Revision History and Change Bar Notation
1.5	Definitions
1.6	Changes Between Revisions and Product Variations
1.6.1	Revision Conventions

- 1.7 Package
 - 1.7.1 Package type
- 1.8 Processor Overview
 - 1.8.1 Features
- 2 **Core Complex (CCX)**
 - 2.1 Processor x86 Core
 - 2.1.1 Core Functional Information
 - 2.1.1.1 Core Definitions
 - 2.1.2 Secure Virtual Machine Mode (SVM)
 - 2.1.2.1 BIOS support for SVM Disable
 - 2.1.2.1.1 Enable AMD Virtualization™
 - 2.1.2.1.2 Disable AMD Virtualization™
 - 2.1.2.1.3 Disable AMD Virtualization™, with a user supplied key
 - 2.1.3 Effective Frequency
 - 2.1.4 Address Space
 - 2.1.4.1 Virtual Address Space
 - 2.1.4.2 Physical Address Space
 - 2.1.4.3 System Address Map
 - 2.1.4.3.1 Memory Access to the Physical Address Space
 - 2.1.4.3.1.1 Determining Memory Type
 - 2.1.5 Configuration Space
 - 2.1.5.1 Memory Mapped IO (MMIO) Configuration Coding Requirements
 - 2.1.5.2 MMIO Configuration Ordering
 - 2.1.5.3 Processor Configuration Space
 - 2.1.6 PCI Configuration Legacy Access
 - 2.1.7 System Software Interaction With SMT Enabled
 - 2.1.8 Register Sharing
 - 2.1.9 Timers
 - 2.1.10 Interrupts
 - 2.1.10.1 System Management Mode (SMM)
 - 2.1.10.1.1 SMM Overview
 - 2.1.10.1.2 Mode and Default Register Values
 - 2.1.10.1.3 SMI Sources And Delivery
 - 2.1.10.1.4 SMM Initial State
 - 2.1.10.1.5 SMM Save State
 - 2.1.10.1.6 System Management State
 - 2.1.10.1.7 Exceptions and Interrupts in SMM
 - 2.1.10.1.8 The Protected ASeg and TSeg Areas
 - 2.1.10.1.9 SMM Special Cycles
 - 2.1.10.1.10 Locking SMM
 - 2.1.10.1.11 SMM Page Configuration Lock
 - 2.1.10.2 Local APIC
 - 2.1.10.2.1 Local APIC Functional Description
 - 2.1.10.2.1.1 Detecting and Enabling
 - 2.1.10.2.1.2 APIC Register Space
 - 2.1.10.2.1.3 ApicId Enumeration Requirements
 - 2.1.10.2.1.4 Physical Destination Mode
 - 2.1.10.2.1.5 Logical Destination Mode
 - 2.1.10.2.1.6 Interrupt Delivery
 - 2.1.10.2.1.7 Vectored Interrupt Handling
 - 2.1.10.2.1.8 Interrupt Masking
 - 2.1.10.2.1.9 Spurious Interrupts
 - 2.1.10.2.1.10 Spurious Interrupts Caused by Timer Tick Interrupt

- 2.1.10.2.1.11 Lowest-Priority Interrupt Arbitration
- 2.1.10.2.1.12 Inter-Processor Interrupts
- 2.1.10.2.1.13 APIC Timer Operation
- 2.1.10.2.1.14 Generalized Local Vector Table
- 2.1.10.2.1.15 State at Reset
- 2.1.10.2.2 Local APIC Registers
- 2.1.11 CPUID Instruction
 - 2.1.11.1 CPUID Instruction Functions
- 2.1.12 MSR Registers
 - 2.1.12.1 MSRs - MSR0000_0xxx
 - 2.1.12.2 MSRs - MSRC000_0xxx
 - 2.1.12.3 MSRs - MSRC001_0xxx
 - 2.1.12.4 MSRs - MSRC001_1xxx
 - 2.1.12.5 L3 MSRs - MSRC001_1xxx
- 2.1.13 Performance Monitor Counters
 - 2.1.13.1 RDPMC Assignments
 - 2.1.13.2 Performance Measurement
 - 2.1.13.3 Large Increment per Cycle Events
 - 2.1.13.4 Core Performance Monitor Counters
 - 2.1.13.4.1 Floating-Point (FP) Events
 - 2.1.13.4.2 Load/Store (LS) Events
 - 2.1.13.4.3 Instruction Cache (IC) and Branch Prediction (BP) Events
 - 2.1.13.4.4 DE Events
 - 2.1.13.4.5 EX (SC) Events
 - 2.1.13.4.6 L2 Cache Events
 - 2.1.13.5 L3 Cache Performance Monitor Counters
 - 2.1.13.5.1 L3 Cache PMC Events
- 2.1.14 Instruction Based Sampling (IBS)
- 2.2 L3 Cache
 - 2.2.1 L3 MSR Registers
 - 2.2.2 L3 Clocks and Test (CT) MSR Registers.

3 Reliability, Availability, and Serviceability (RAS) Features

- 3.1 Machine Check Architecture
 - 3.1.1 Overview
 - 3.1.1.1 Legacy Machine Check Architecture
 - 3.1.1.2 Machine Check Architecture Extensions
 - 3.1.1.3 Use of MCA Information
 - 3.1.1.3.1 Error Management
 - 3.1.1.3.2 Fault Management
 - 3.1.2 Machine Check Registers
 - 3.1.2.1 Global Registers
 - 3.1.2.2 Machine Check Banks
 - 3.1.2.2.1 Legacy MCA Registers
 - 3.1.2.2.2 Legacy MCA MSRs
 - 3.1.2.2.3 MCAX Registers
 - 3.1.2.2.4 MCAX MSRs
 - 3.1.2.3 Access Permissions
 - 3.1.3 Machine Check Errors
 - 3.1.3.1 Error Severities
 - 3.1.3.2 Exceptions and Interrupts
 - 3.1.3.3 Error Codes
 - 3.1.3.4 Extended Error Codes
 - 3.1.3.5 DOER and SEER State

- 3.1.3.6 MCA Overflow Recovery
- 3.1.3.7 MCA Recovery
- 3.1.4 Machine Check Features
 - 3.1.4.1 Error Thresholding
 - 3.1.4.2 Error Simulation
- 3.1.5 Software Guidelines
 - 3.1.5.1 Recognizing MCAX Support
 - 3.1.5.2 Communicating MCAX Support
 - 3.1.5.3 Machine Check Initialization
 - 3.1.5.4 Determining Bank Count
 - 3.1.5.5 Determining Bank Type
 - 3.1.5.6 Recognizing Error Type
 - 3.1.5.7 Machine Check Error Handling
- 3.2 Machine Check Architecture Implementation
 - 3.2.1 Implemented Machine Check Banks
 - 3.2.2 Implemented Machine Check Bank Registers
 - 3.2.3 Mapping of Banks to Blocks
 - 3.2.4 Decoding Error Type
 - 3.2.5 MCA Banks
 - 3.2.5.1 LS
 - 3.2.5.2 IF
 - 3.2.5.3 L2
 - 3.2.5.4 DE
 - 3.2.5.5 EX
 - 3.2.5.6 FP
 - 3.2.5.7 L3
 - 3.2.5.8 CS
 - 3.2.5.9 PIE
 - 3.2.5.10 UMC
 - 3.2.5.11 PB
 - 3.2.5.12 MP5
 - 3.2.5.13 NBIO
 - 3.2.5.14 KPX SERDES
 - 3.2.5.15 KPX GMI
 - 3.2.5.16 PCS GMI
- 4 Advanced Platform Management Link (APML)**
 - 4.1 Overview
 - 4.1.1 Definitions
 - 4.2 SBI Bus Characteristics
 - 4.2.1 SMBus Protocol Support
 - 4.2.2 I2C Support
 - 4.3 SBI Processor Information
 - 4.3.1 SBI Processor Pins
 - 4.3.1.1 Physical Layer Characteristics
 - 4.3.2 Processor States
 - 4.4 SBI Protocols
 - 4.4.1 SBI Modified Block Write-Block Read Process Call
 - 4.4.2 SBI Remote Management Interface (SB-RMI)
 - 4.4.2.1 SB-RMI Processor State Access
 - 4.4.2.1.1 SB-RMI Read Processor Register and Read CPUID Commands
 - 4.4.2.1.2 SB-RMI Write Processor Register Command
 - 4.4.2.1.3 SB-RMI Protocol Status Codes
 - 4.4.2.2 SB-RMI Mailbox Service

- 4.4.2.2.1 SB-RMI Mailbox Sequence
- 4.4.2.3 SB-RMI Boot code status
- 4.4.2.4 SB-RMI Register Access
 - 4.4.2.4.1 SB-RMI Register Block Access
 - 4.4.2.4.2 SB-RMI Register Byte Access
- 4.4.2.5 SB-RMI Alert
- 4.4.3 SBI Error Detection and Recovery
 - 4.4.3.1 Error Detection
 - 4.4.3.1.1 ACK/NAK Mechanism
 - 4.4.3.1.2 Packet Error Correction (PEC)
 - 4.4.3.1.3 Bus Timeouts
 - 4.4.3.2 Error Recovery
 - 4.4.3.2.1 SBI Bus Reset
- 4.5 SBI Physical Interface
 - 4.5.1 SBI SMBus Address
 - 4.5.2 SBI Bus Timing
- 4.6 SB-RMI Registers
- 5 SB Temperature Sensor Interface (SB-TSI)**
 - 5.1 Overview
 - 5.1.1 Definitions
 - 5.2 SB-TSI Protocol
 - 5.2.1 SB-TSI Send/Receive Byte Protocol
 - 5.2.1.1 SB-TSI Address Pointer
 - 5.2.2 SB-TSI Read/Write Byte Protocol
 - 5.2.3 Alert Behavior
 - 5.2.4 Atomic Read Mechanism
 - 5.2.5 SB-TSI Temperature and Threshold Encodings
 - 5.2.6 SB-TSI Temperature Offset Encoding
 - 5.3 SB-TSI Physical Interface
 - 5.3.1 SB-TSI SMBus Address
 - 5.3.2 SB-TSI Bus Timing
 - 5.3.3 SB-TSI Bus Electrical Parameters
 - 5.3.4 Pass-FET Option
 - 5.4 SB-TSI Registers

List of Figures

Figure 1:	Adobe® Reader Hyperlink Opens New Window Configuration
Figure 2:	Adobe® Reader Select Between Opened Files
Figure 3:	Adobe® Reader Show Toolbars Configuration
Figure 4:	Adobe® Reader Prev/Next Buttons
Figure 5:	Adobe® Reader Searching a Multiple Volume PPR
Figure 6:	Adobe® Reader Expand Current Bookmark Button
Figure 7:	Register Physical Mnemonic, Title, and Name
Figure 8:	Full Width Register Attributes
Figure 9:	Register Description
Figure 10:	Register Instance Table: Content Ordering in a Row
Figure 11:	Register Instance Table: MSR Example
Figure 12:	Register Instance Table: MSR Range Example
Figure 13:	Register Instance Table: BAR as Register Reference
Figure 14:	Register Instance Table: Bus Implied to be 00h
Figure 15:	Register Instance Table: Data Port Select
Figure 16:	Simple Register Field Example
Figure 17:	Register Field Sub-Row for {Reset,AccessType,Init,Check}
Figure 18:	Register Field Sub-Row for Description
Figure 19:	Register Field Sub-Row for Valid Value Table
Figure 20:	Register Field Sub-Row for Valid Bit Table
Figure 21:	Revision History Format Example
Figure 22:	Change Notation Example
Figure 23:	Overview of Family 19 Core Component Numbering
Figure 24:	Register Sharing Domains
Figure 25:	Instance Parameters
Figure 26:	SBI Transmission Protocol
Figure 27:	RTS Thermal Management Example
Figure 28:	SB-TSI Thermal Management Example
Figure 29:	Alert Assertion Diagram
Figure 30:	Pass FET Implementation

List of Tables

Table 1:	Reference Documents Listing
Table 2:	Arithmetic and Logical Operator Definitions
Table 3:	Function Definitions
Table 4:	Operator Precedence and Associativity
Table 5:	Register Mnemonic Definitions
Table 6:	Logical Mnemonic Definitions
Table 7:	Physical Mnemonic Definitions
Table 8:	AccessType Definitions
Table 9:	Reset Type Definitions
Table 10:	Init Type Definitions
Table 11:	Definitions
Table 12:	Package Definitions
Table 13:	PCI Device ID Assignments.
Table 14:	Definitions
Table 15:	SMM Initial State
Table 16:	SMM Save State
Table 17:	ICR Valid Combinations
Table 18:	Guidance for Common Performance Statistics with Complex Event Selects
Table 19:	Guidance for Pipeline Utilization Analysis Statistics
Table 20:	PMC_Definitions
Table 21:	Machine Check Terms and Acronyms
Table 22:	Legacy MCA MSR Layout
Table 23:	MCAX MSR Layout
Table 24:	MCAX Implementation-Specific Register Layout
Table 25:	Error Overwrite Priorities
Table 26:	Error Scope Hierarchy
Table 27:	Error Code Types
Table 28:	Error code: transaction type (TT)
Table 29:	Error codes: cache level (LL)
Table 30:	Error codes: memory transaction type (RRRR)
Table 31:	Blocks Capable of Supporting MCA Banks
Table 32:	Mapping of Blocks to MCA_IPID[HwId] and MCA_IPID[McaType]
Table 33:	Legacy MCA Registers
Table 34:	MCAX Registers
Table 35:	Core MCA Bank to Block Mapping
Table 36:	Non-core MCA Bank to Block Mapping
Table 37:	MCA_STATUS_LS
Table 38:	MCA_ADDR_LS
Table 39:	MCA_SYND_LS
Table 40:	MCA_STATUS_IF
Table 41:	MCA_ADDR_IF
Table 42:	MCA_SYND_IF
Table 43:	MCA_STATUS_L2
Table 44:	MCA_ADDR_L2
Table 45:	MCA_SYND_L2
Table 46:	MCA_STATUS_DE
Table 47:	MCA_ADDR_DE
Table 48:	MCA_SYND_DE
Table 49:	MCA_STATUS_EX
Table 50:	MCA_ADDR_EX

Table 51:	MCA_SYND_EX
Table 52:	MCA_STATUS_FP
Table 53:	MCA_ADDR_FP
Table 54:	MCA_SYND_FP
Table 55:	MCA_STATUS_L3
Table 56:	MCA_ADDR_L3
Table 57:	MCA_SYND_L3
Table 58:	MCA_STATUS_CS
Table 59:	MCA_ADDR_CS
Table 60:	MCA_SYND_CS
Table 61:	MCA_STATUS_PIE
Table 62:	MCA_ADDR_PIE
Table 63:	MCA_SYND_PIE
Table 64:	MCA_STATUS_UMC
Table 65:	MCA_ADDR_UMC
Table 66:	MCA_SYND_UMC
Table 67:	MCA_STATUS_PB
Table 68:	MCA_ADDR_PB
Table 69:	MCA_SYND_PB
Table 70:	MCA_STATUS_MP5
Table 71:	MCA_ADDR_MP5
Table 72:	MCA_SYND_MP5
Table 73:	MCA_STATUS_NBIO
Table 74:	MCA_ADDR_NBIO
Table 75:	MCA_SYND_NBIO
Table 76:	MCA_STATUS_KPX_SERDES
Table 77:	MCA_ADDR_KPX_SERDES
Table 78:	MCA_SYND_KPX_SERDES
Table 79:	MCA_STATUS_KPX_GMI
Table 80:	MCA_ADDR_KPX_GMI
Table 81:	MCA_SYND_KPX_GMI
Table 82:	MCA_STATUS_PCS_GMI
Table 83:	MCA_ADDR_PCS_GMI
Table 84:	MCA_SYND_PCS_GMI
Table 85:	APML Definitions
Table 86:	SB-RMI Functions
Table 87:	SB-RMI Read Processor Register Command Protocol
Table 88:	SB-RMI Read CUID Command Protocol
Table 89:	SB-RMI Read Data/Status Command Protocol
Table 90:	SB-RMI Load Address Command Protocol
Table 91:	SB-RMI Write Processor Register Command Protocol
Table 92:	SB-RMI Status Codes
Table 93:	SB-RMI Soft Mailbox Message
Table 94:	SB-RMI Soft Mailbox Error Code
Table 95:	SB-RMI Register Block Write Protocol
Table 96:	SB-RMI Register Block Read Protocol
Table 97:	SB-RMI Register Write Byte Protocol
Table 98:	SB-RMI Register Read Byte Protocol
Table 99:	SB-TSI Definitions
Table 100:	SB-TSI CPU Temperature and Threshold Encoding Examples
Table 101:	SB-TSI Temperature Offset Encoding Examples
Table 102:	SB-TSI Address Encodings

1 Overview

1.1 Intended Audience

This document provides the processor behavioral definition and associated design notes. It is intended for platform designers and for programmers involved in the development of BIOS functions, drivers, and operating system kernel modules.

1.2 Reference Documents

Table 1: Reference Documents Listing

Term	Description
docAPM1	AMD64 Architecture Programmer's Manual Volume 1: Application Programming, order# 24592.
docAPM2	AMD64 Architecture Programmer's Manual Volume 2: System Programming, order# 24593.
docAPM3	AMD64 Architecture Programmer's Manual Volume 3: Instruction-Set Reference, order# 24594.
docAPM4	AMD64 Architecture Programmer's Manual Volume 4: 128-Bit and 256-Bit Media Instructions, order# 26568.
docAPM5	AMD64 Architecture Programmer's Manual Volume 5: 64-Bit Media and x87 Floating-Point Instructions, order# 26569.
docACPI	Advanced Configuration and Power Interface (ACPI) Specification. http://www.acpi.info .
docASF	Alert Standard Format Specification. http://dmtf.org/standards/asf .
docATA	AT Attachment with Packet Interface. http://www.t13.org .
docDP	VESA DisplayPort Standard. http://www.vesa.org/vesa-standards .
docIOMMU	AMD I/O Virtualization Technology Specification, order# 48882.
docI2C	I2C Bus Specification. http://www.nxp.com/documents/user_manual/UM10204.pdf
docJEDEC	JEDEC Standards. http://www.jedec.org .
docPCIe	PCI Express® Specification. http://www.pcisig.org .
docPCIb	PCI Local Bus Specification. http://www.pcisig.org .
docRevG	Revision Guide for AMD Family 19h Models 60h-6Fh Processors
docSATA	Serial ATA Specification. http://www.sata-io.org .
docSDHC	Secure Digital Host Controller Standard Specification. https://www.sdcard.org .
docUSB	Universal Serial Bus Specification. http://www.usb.org .

1.2.1 Documentation Conventions

When referencing information found in external documents listed in Reference Documents, the "=>" operator is used. This notation represents the item to be searched for in the reference document. For example:

docExDoc => Header1 => Header2

is to have the reader use the search facility when opening referenced document "docExDoc" and search for "Header2". "Header2" may appear more than once in "docExDoc", therefore, referencing the one that follows "Header1". In that case, the easiest way to get to Header2 is to use the search to locate Header1, then again to locate "Header2".

1.3 Adobe® Reader

This section describes how to configure and use Adobe® Reader for the PPR PDFs.

Adobe Reader is the recommended tool for viewing PPR pdfs and can be downloaded at <https://get.adobe.com/reader/>.

1.3.1 Adobe® Reader Configuration

This section describes how to configure Adobe Reader for the PPR PDFs.

1.3.1.1 Open Hyperlink Document in New Window

The Open Hyperlink Document in New Window setting opens a new window for a hyperlink, instead of opening the hyperlink document in the same window.

- Only when deselected are previously opened files visible in the Windows® pull-down menu.

Edit->Preferences:

- Documents
 - Open Settings:
 - Deselect: Open cross-document links in same window

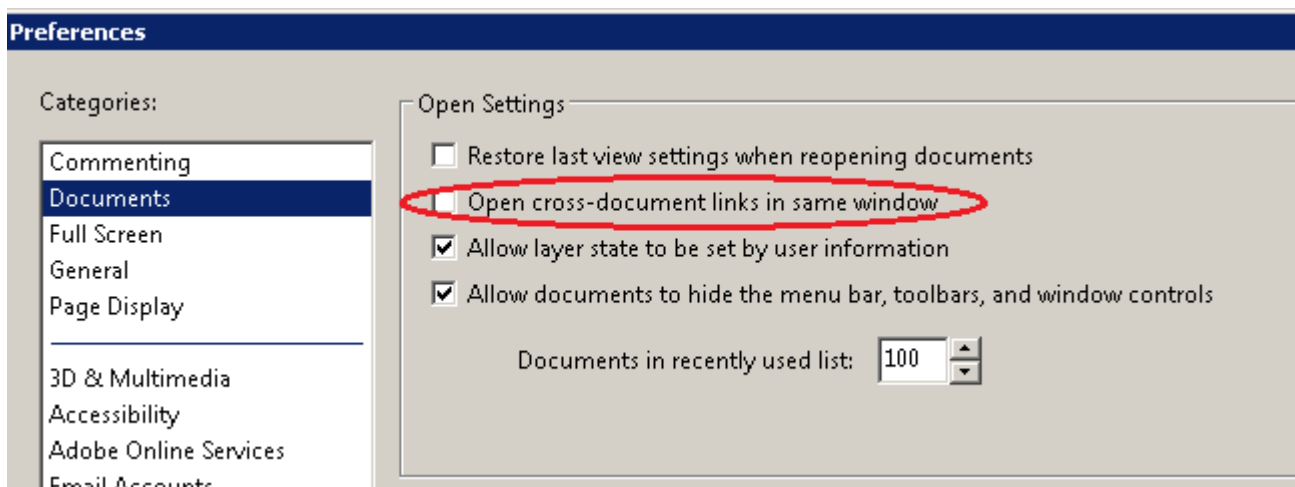


Figure 1: Adobe® Reader Hyperlink Opens New Window Configuration

Figure 2 shows how when hyperlinking from volume 2 to volume 1, that volume 2 is left open. The check indicates the foreground window.

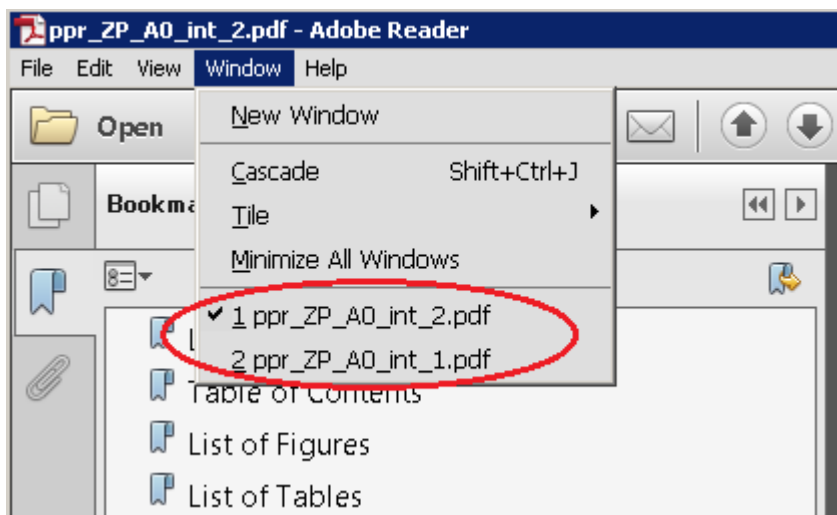


Figure 2: Adobe® Reader Select Between Opened Files

1.3.1.2 Show Toolbars

If Toolbars is not shown:

- View->Show/Hide->Toolbar Items->Show Toolbars
- The toolbar is needed to see the "Previous View" and "Next View" buttons.



Figure 3: Adobe® Reader Show Toolbars Configuration

1.3.1.3 Show "Previous View" and "Next View" Buttons

If the "Previous View" (left arrow) and "Next View" (right arrow) buttons are not shown:

- Right click on toolbar-> Page Navigation-> select "Previous View" and "Next View" items.



Figure 4: Adobe® Reader Prev/Next Buttons

1.3.2 Adobe® Reader Usage

This section describes how to use Adobe Reader for the PPR PDFs.

NOTE: PDF's are distributed in zip format. In order to search and hyperlink between PDF volumes, the zip contents must be extracted to a folder.

1.3.2.1 Searching a Multiple Volume PPR

The PPR is a multiple PDF document and searching all PDFs is performed as follows:

- The zip of PDF files must be extracted to a directory where the search will be performed. A search across multiple PDF files can not be performed from within a zip of PDF's.
- Open search by selecting Edit -> Advanced Search (Shift+Ctrl+F)
- Select "All PDF Documents in" and select "Browse for Location...", which opens the "Browse For Folder" window.
- In the "Browse For Folder" window, select the folder that contains the PPR PDFs that need to be searched, and select OK.

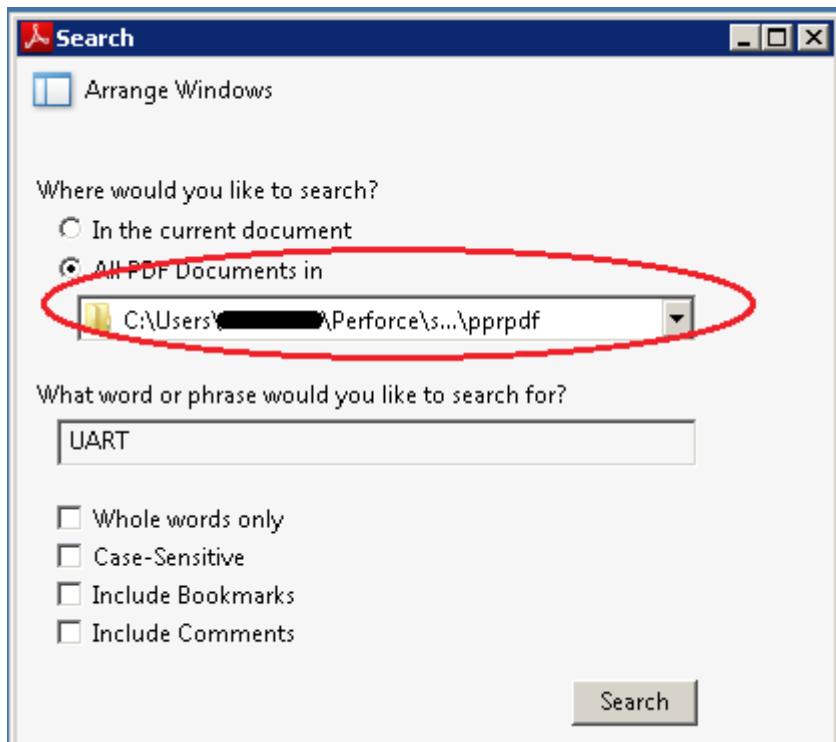


Figure 5: Adobe® Reader Searching a Multiple Volume PPR

1.3.2.2 Cross-References and Hyperlinks

A cross-reference is a link to a location within the same PDF. A hyperlink is a link to a location within a different PDF.

- For cross-references, use "Previous View" to return from the current location to the previous location.
- Hyperlinks between documents leave the current location unchanged in the PDF that contained the hyperlink.
- In order for hyperlinks to work properly the zip of PDF's must be extracted to a directory. Hyperlinks will not function within a zip of PDF's.

1.3.2.3 Expand Current Bookmark

The bookmark pane can highlight the current bookmark associated with the viewer pane by selecting the "expand current bookmark" button, as shown below.

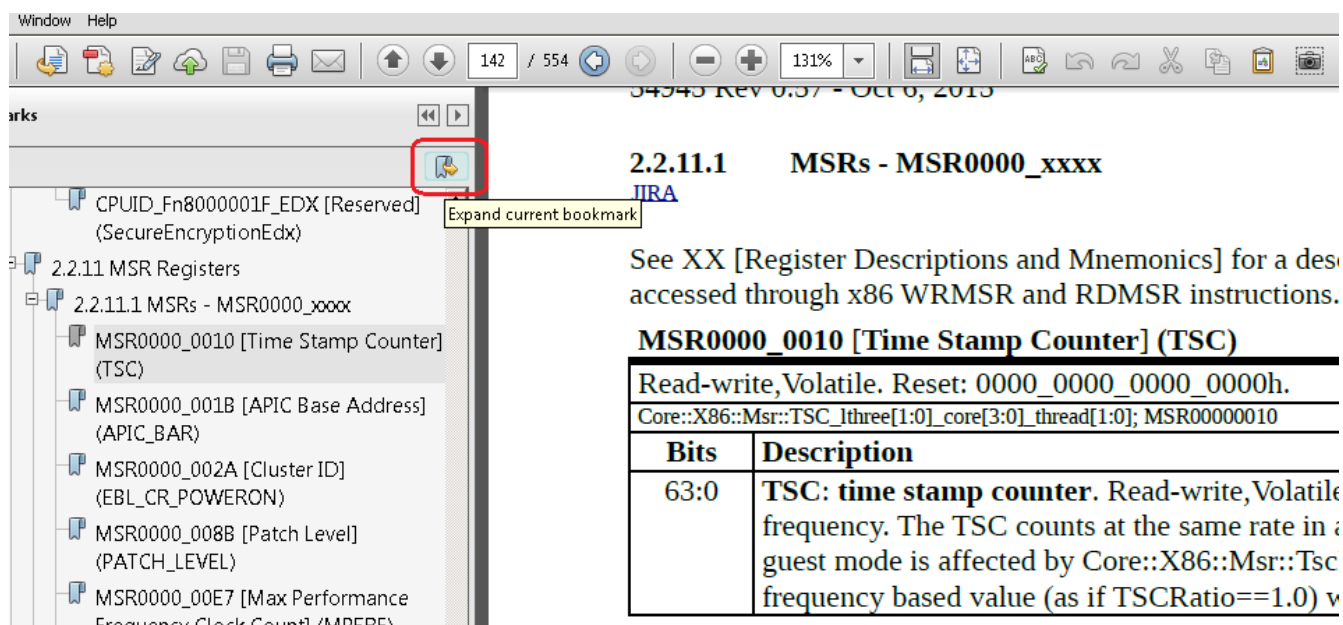


Figure 6: Adobe® Reader Expand Current Bookmark Button

1.4 Conventions

1.4.1 Numbering

- Binary numbers: Binary numbers are indicated either by appending a "b" at the end (e.g., 0110b) or by Verilog syntax (e.g., 4'b0110).
- Hexadecimal numbers: Hexadecimal numbers are indicated by appending an "h" to the end (e.g., 45F8h) or by Verilog syntax (e.g., 16'h45F8).
- Decimal numbers: A number is decimal if not specified to be binary or hex.
- Exception: Physical register mnemonics are implied to be hex without the h suffix.
- Underscores in numbers: Underscores are used to break up numbers to make them more readable. They do not imply any operation (e.g., 0110_1100).

1.4.2 Arithmetic And Logical Operators

In this document, formulas generally follow Verilog conventions for logic equations.

Table 2: Arithmetic and Logical Operator Definitions

Operator	Definition
{}	Concatenation. Curly brackets are used to indicate a group of bits that are concatenated together. Each set of bits is separated by a comma (e.g., {Addr[3:2], Xlate[3:0]} represents a 6-bit values; the two MSBs are Addr[3:2] and the four LSBs are Xlate[3:0]).
	Bitwise OR (e.g., 01b 10b == 11b).
	Logical OR (e.g., 01b 10b == 1b). It treats a multi-bit operand as 1 if >= 1 and produces a 1-bit result.
&	Bitwise AND (e.g., 01b & 10b == 00b).
&&	Logical AND (e.g., 01b && 10b == 1b). It treats a multi-bit operand as 1 if >= 1 and produces a 1-bit result.

\wedge	Bitwise exclusive-OR (e.g., $01b \wedge 10b == 11b$). Sometimes used as "raised to the power of" as well, as indicated by the context in which it is used (e.g., $2^2 == 4$).
\sim	Bitwise NOT (also known as one's complement). (e.g., $\sim 10b == 01b$).
!	Logical NOT (e.g., $!10b == 0b$). It treats a multi-bit operand as 1 if ≥ 1 and produces a 1-bit result.
<, <=, >, >=, ==, !=	Relational. Less than, Less than or equal, greater, greater than or equal, equal, and not equal.
+, -, *, /, %	Arithmetic. Addition, subtraction, multiplication, division, and modulus.
<<	Bitwise left shift. Shift left first operand by the number of bits specified by the 2nd operand (e.g., $01b \ll 01b == 10b$).
>>	Bitwise right shift. Shift right first operand by the number of bits specified by the 2nd operand (e.g., $10b \gg 01b == 01b$).
?:	Ternary conditional (e.g., condition ? value if true : value if false).

Table 3: Function Definitions

Term	Description
ABS	ABS(integer expression): Remove sign from signed value.
FLOOR	FLOOR(integer expression): Rounds real number down to nearest integer.
CEIL	CEIL(real expression): Rounds real number up to nearest integer.
MIN	MIN(integer expression list): Picks minimum integer or real value of comma separated list.
MAX	MAX(integer expression list): Picks maximum integer or real value of comma separated list.
COUNT	COUNT(integer expression): Returns the number of binary 1's in the integer.
ROUND	ROUND(real expression): Rounds to the nearest integer; halfway rounds away from zero.
UNIT	UNIT(register field reference): Input operand is a register field reference that contains a valid values table that defines a value with a unit (e.g., clocks, ns, ms, etc.). This function takes the value in the register field and returns the value associated with the unit (e.g., If the field had a valid value definition where 1010b was defined as 5 ns). Then if the field had the value of 1010b, then UNIT() would return the value 5.
POW	POW(base, exponent): POW(x,y) returns the value x to the power of y.

1.4.2.1 Operator Precedence and Associativity

This document follows C operator precedence and associativity. The following table lists operator precedence (highest to lowest). Their associativity indicates in what order operators of equal precedence in an expression are applied. Parentheses are also used to group subexpressions to force a different precedence; such parenthetical expressions can be nested and are evaluated from inner to outer (e.g., "X = A || !B && C" is the same as "X = A || (!B) && C").

Table 4: Operator Precedence and Associativity

Operator	Description	Associativity
!, ~	Logical negation/bitwise complement	right to left
*, /, %	Multiplication/division/modulus	left to right
+, -	Addition/subtraction	left to right
<<, >>	Bitwise shift left, Bitwise shift right	left to right
<, <=, >, >=, ==, !=	Relational operators	left to right
&	Bitwise AND	left to right
\wedge	Bitwise exclusive OR	left to right
	Bitwise inclusive OR	left to right
&&	Logical AND	left to right

	Logical OR	left to right
?:	Ternary conditional	right to left

1.4.3 Register Mnemonics

A register mnemonic is a short name that uniquely refers to a register, either all instances of that register, some instances, or a single instance.

Every register instance can be expressed in 2 forms, logical and physical, as defined below.

Table 5: Register Mnemonic Definitions

Term	Description
logical mnemonic	The register mnemonic format that describes the register functionally, what namespace to which the register belongs, a name for the register that connotes its function, and optionally, named parameters that indicate the different function of each instance (e.g., Link::Phy::PciDevVendIDF3). See 1.4.3.1 [Logical Mnemonic].
physical mnemonic	The register mnemonic that is formed based on the physical address used to access the register (e.g., D18F3x00). See 1.4.3.2 [Physical Mnemonic].

1.4.3.1 Logical Mnemonic

The logical mnemonic format consists of a register namespace, a register name, and optionally a register instance specifier (e.g., register namespace::register name register instance specifier).

For Unb::PciDevVendIDF3:

- The register namespace is Unb, which is the UNB IP register namespace.
- The register name is PciDevVendIDF3, which reads as PCICFG device and vendor ID in Function 3.
- There is no register instance specifier because there is just a single instance of this register.

For Dct::Phy::CalMisc2_dct[1:0]_chiplet[BCST,3:0]_pad[BCST,11:0]:

- The register namespace is Dct::Phy, which is the DCT PHY register namespace.
- The register name is CalMisc2, which reads as miscellaneous calibration register 2.
- The register instance specifier is _dct[1:0]_chiplet[BCST,3:0]_pad[BCST,11:0], which indicates that there are 2 DCTPHY instances, each IP for this register has 5 chiplets (0-3 and BCST), and for each chiplet 13 pads (0-11 and BCST). This register has 130 instances. (2*5*13)

Table 6: Logical Mnemonic Definitions

Term	Description
register namespace	A namespace for which the register name must be unique. A register namespace indicates to which IP it belongs and an IP may have multiple namespaces. A namespace is a string that supports a list of "::" separated names. The convention is for the list of names to be hierarchical, with the most significant name first and the least significant name last (e.g., Link::Phy::Rx is the RX component in the Link PHY).
register name	A name that connotes the function of the register.
register instance specifier	The register instance specifier exists when there is more than one instance for a register. The register instance specifier consists of one or more register instance parameter specifier (e.g., The register instance specifier <code>_dct[1:0]_chiplet[BCST,3:0]_pad[BCST,11:0]</code> consists of 3 register instance parameter specifiers, <code>_dct[1:0]</code> , <code>_chiplet[BCST,3:0]</code> , and <code>_pad[BCST,11:0]</code>).
register instance parameter specifier	A register instance parameter specifier is of the form <code>_register parameter name[register parameter value list]</code> (e.g., The register instance parameter specifier <code>_dct[1:0]</code> has a register parameter name of <code>dct</code> (The DCT PHY instance name) and a register parameter value list of "1:0" or 2 instances of DCT PHY).
register parameter name	A register parameter name is the name of the number of instances at some level of the logical hierarchy (e.g., The register parameter name <code>dct</code> specifies how many instances of the DCT PHY exist).
register parameter value list	The register parameter value list is the logical name for each instance of the register parameter name (e.g., For <code>_dct[1:0]</code> , there are 2 DCT PHY instances, with the logical names 0 and 1, but it should be noted that the logical names 0 and 1 can correspond to physical values other than 0 and 1). It is the purpose of the <code>AddressMappingTable</code> to map these register parameter values to physical address values for the register.

1.4.3.2 Physical Mnemonic

The physical register mnemonic format varies by the access method. The following table describes the supported physical register mnemonic formats.

Table 7: Physical Mnemonic Definitions

Term	Description
PCICFG	The PCICFG, or PCI defined configuration space, physical register mnemonic format is of the form DXFYxZZZ. X specifies the hexadecimal device number (this may be 1 or 2 digits). Y specifies the function number. ZZZ specifies the hexadecimal byte address (This may be 2 or 3 digits. e.g., D18F3x40 specifies the register at device 18h, function 3, and address 40h).
BAR	The BAR, or base address register, physical register mnemonic format is of the form PREFIXxZZZ. PREFIX is an all capital letter name that connotes the BAR to which the offset is added to get the physical address of the operation. ZZZ is the offset.
MSR	The MSR, or x86 model specific register, physical register mnemonic format is of the form MSRXXXX_XXXX, where XXXX_XXXX is the hexadecimal MSR number. This space is accessed through x86 defined RDMSR and WRMSR instructions.
PMC	The PMC, or x86 performance monitor counter, physical register mnemonic format is any of the forms {PMCxXXX, L2IPMCxXXX, NBPMCxXXX}, where XXX is the performance monitor select.
CPUID	The CPUID, or x86 processor identification state, physical register mnemonic format is of the form CPUID FnXXXX_XXXX_EiX[_xYYY], where XXXX_XXXX is the hex value in the EAX and YYY is the hex value in ECX.

1.4.4 Register Format

A register is a group of register instances that have the same field format (same bit indices and field names).

1.4.4.1 Register Instances

All instances of a register:

- Have the same:
 - Field bit indices and names
 - Field titles, descriptions, valid values.
 - Register title
 - Register description
- Fields may have different: (instance specific)
 - Access Type. See 1.4.4.10 [Field Access Type].
 - Reset. See 1.4.4.11 [Field Reset].
 - Init. See 1.4.4.12 [Field Initialization].
 - Check. See 1.4.4.13 [Field Check].

1.4.4.2 Register Physical Mnemonic, Title, and Name

A register definition is identified by a table that starts with a heavy bold line. The information above the bold line in order is:

1. The physical mnemonic of the register.
 - A register that has multiple instances, may have instances that have different access methods, each with its own physical mnemonic format.
 - In the event that there are multiple physical mnemonic formats, the physical mnemonic format chosen is the most commonly used physical mnemonic.
 - The physical mnemonic is not intended to represent the physical mnemonics of all instances of the register. It is only a visual aid to identify a register when scanning down a list, for readers that prefer to find registers by physical mnemonic. If "..." occurs in the physical mnemonic, the range is first ... last. There is no implication as to how many instances exist between first and last. See 1.4.4.5 [Register

Instance Table].

2. The register title in brackets.
3. The register name in parenthesis.

Physical Mnemonic	Title	Name
MSR0000_0010	[Time Stamp Counter]	(TSC)
Read-write, Volatile. Reset: 0000_0000_0000_0000h.		
Core::X86::Msr::TSC_three[1:0]_core[3:0]_thread[1:0]; MSR00000010		
Bits	Description	
63:0	TSC: time stamp counter. Read-write, Volatile. Reset: 0. The TSC increments at the P0 frequency. The TSC counts at the same rate in all P-states, all C states, S0, or S1. A read of this MSR in guest mode is affected by Core::X86::Msr::TscRateMsr. The value (TSC/TSCRatio) is the TSC P0 frequency based value (as if TSCRatio == 1.0) when (TSCRatio != 1.0).	

Figure 7: Register Physical Mnemonic, Title, and Name

1.4.4.3 Full Width Register Attributes

The first line that follows the bold line contains the attributes that apply to all fields of the register. This row is rendered as a convenience to the reader and replicates content that exists in the register field.

- AccessType: If all non-reserved fields of a register have the same access type, then the access type is rendered in this row.
 - The supported access types are specified by 1.4.4.10 [Field Access Type].
 - The example figure shows that the access type "Read-write, Volatile" applies to all non-reserved fields of the register.
- Reset: If all non-reserved fields of a register have a constant reset and are all the same type (Warm, Cold, Fixed), then the full width register reset is rendered in this row. The example figure shows the reset "0000_0000_0000_0000h". See 1.4.4.11 [Field Reset].
 - The value zero (0) is assumed for display purposes for all reserved fields.
- If none of the above content is rendered, then this row of the register is not rendered.

MSR0000_0010 [Time Stamp Counter] (TSC)

Read-write, Volatile. Reset: 0000_0000_0000_0000h.	
Core::X86::Msr::TSC_three[1:0]_core[3:0]_thread[1:0]; MSR00000010	
Bits	Description
63:0	TSC: time stamp counter. Read-write, Volatile. Reset: 0. The TSC increments at the P0 frequency. The TSC counts at the same rate in all P-states, all C states, S0, or S1. A read of this MSR in guest mode is affected by Core::X86::Msr::TscRateMsr. The value (TSC/TSCRatio) is the TSC P0 frequency based value (as if TSCRatio == 1.0) when (TSCRatio != 1.0).

Figure 8: Full Width Register Attributes

1.4.4.4 Register Description

The register description is optional and appears after the "full width register attributes" row and before the "register instance table" rows. The register description can be one or more paragraphs.

PciDevVendIDF3 [Device/Vendor ID]	
Read-only. Reset: 0000_1022h.	
A register description. That can be multiple paragraphs.	
Link::Phy::Tx::PciDevVendIDF3; D18F3x00	
Bits	Description
31:16	DeviceID: device ID. Read-only. Reset: Fixed,0000h.
15:0	VendorID: vendor ID. Read-only. Reset: Fixed,1022h. Init: 1234h.

Figure 9: Register Description

1.4.4.5 Register Instance Table

The zero or more rows of 8-pt font before the Bits/Description row is the register instance table.

The register instance table can generally be described as follows:

- Each row describes the access method of one or more register instances.
- If a row describes two or more instances, then the logical instance range, left to right, corresponds to the physical range, left to right.
- The absence of register instance rows indicates that the register exists for documentation purposes, and no access method is described for the register.

Because there are multiple access methods for all the registers, each of the following subsections describes an aspect of the register instance table in isolation.

1.4.4.5.1 Content Ordering in a Row

Content in a register instance table row is ordered as follows:

- The text up to the first semicolon is the logical mnemonic.
 - See 1.4.3.1 [Logical Mnemonic].
- The text after the first semicolon is the physical mnemonic.
 - See 1.4.3.2 [Physical Mnemonic].
- Optionally, content after the physical mnemonic provides additional information about the access method for the register instances in the row.

BXXD00F0x000 (NB_VENDOR_ID)	
Read-only. Reset: 1022h.	
Vendor ID Register	
IOHC::NB_VENDOR_ID_aliasHOST; BXXD00F0x000; BXX=IOHC::NB_BUS_NUM_CNTL_aliasSMN[NB_BUS_NUM]	
IOHC::NB_VENDOR_ID_aliasSMN; NBCFGx00000000; NBCFG=13B0_0000h	

Figure 10: Register Instance Table: Content Ordering in a Row

1.4.4.5.2 Multiple Instances Per Row

Multiple instances in a row is represented by a single dimension "range" in the logical mnemonic and the physical mnemonic.

The single dimension order of instances is the same for both the logical and physical mnemonic. The first logical

mnemonic is associated with the first physical mnemonic, so forth for the 2nd, up until the last.

- Brackets indicates a list, most significant to least significant.
- The ":" character indicates a continuous range between 2 values.
- The "," character separates non-contiguous values.
- There are some cases where more than one logical mnemonic maps to a single physical mnemonic.

Note that it is implied that the MSR {lthree,core,thread} parameters are not part of a range.

Example:

NAMESP::REGNAME_inst[BLOCK[5:0],BCST]_aliasHOST; FFF1x00000088_x[000[B:6]_0001,00000000]

- There are 7 instances.
- NAMESP is the namespace.
- 6 instances are represented by the sub-range 000[B:6]_0001.
- _instBCST corresponds to FFF1x00000088_x00000000.
- _inst BLOCK 0 corresponds to FFF1x00000088_x00060001.
- ...
- _inst BLOCK 5 corresponds to FFF1x00000088_x000B0001.

1.4.4.5.3 MSR Access Method

The MSR parameters {lthree,core,thread} are implied by the identity of the core on which the RDMSR/WRMSR is being executed, and therefore are not represented in the physical mnemonic.

MSRs that are:

- per-thread have the {lthree,core,thread} parameters.
- per-core do not have the thread parameter.
- per-L3 do not have the {core,thread} parameters.
- common to all L3's do not have the {lthree,core,thread} parameters.

1.4.4.5.3.1 MSR Per-Thread Example

An MSR that is per-thread has all three {lthree,core,thread} parameters and all instances have the same physical mnemonic.

MSR0000_0010 [Time Stamp Counter] (TSC)

Read-write, Volatile. Reset: 0000_0000_0000_0000h.	
Core::X86::Msr::TSC_lthree[1:0]_core[3:0]_thread[1:0]:[MSR00000010]	
Bits	Description
63:0	TSC: time stamp counter. Read-write, Volatile. Reset: 0. The TSC increments at the P0 frequency. The TSC counts at the same rate in all P-states, all C states, S0, or S1. A read of this MSR in guest mode is affected by Core::X86::Msr::TscRateMsr. The value (TSC/TSCRatio) is the TSC P0 frequency based value (as if TSCRatio == 1.0) when (TSCRatio != 1.0).

Figure 11: Register Instance Table: MSR Example

1.4.4.5.3.2 MSR Range Example

An MSR can exist as a range for a parameter other than the {lthree,core,thread} parameters.

In the following example the n parameter is a range. The _n0 value corresponds to MSR0000_0201, and so on.

MSR0000_0201 [Variable-Size MTRRs Mask] (MtrrVarMask)

Reset: 0000_0000_0000_0000h.
Core::X86::Msr::MtrrVarMask[n[7:0]]three[1:0]_core[3:0]; MSR0000_0201[[F,D,B,9,7,5,3,1]]

Figure 12: Register Instance Table: MSR Range Example

1.4.4.5.4 BAR Access Method

The BAR access method is indicated by a physical mnemonic that has the form PREFIXxNUMBER.

- Example: APICx0000. The BAR prefix is "APIC".

The BAR prefix represents either a constant or an expression that consists of a register reference.

1.4.4.5.4.1 BAR as a Register Reference

A relocatable BAR is when the base of an IP is not a constant.

- The prefix NTBPRIBAR0 represents the base of the IP, the value of which comes from the register NBIFEPFNCFG::BASE_ADDR_1_aliasHOST_instNBIF0_func1[BASE_ADDR].

NTBPRIBAR0x00000 (NTB_SMU_PCTRL0)

Reset: 0000_0000h.
NTB::NTB_SMU_PCTRL0_aliasHOSTPRI; NTBPRIBAR0x00000;
NTBPRIBAR0=NBIFEPFNCFG::BASE_ADDR_1_aliasHOST_instNBIF0_func1[BASE_ADDR]
NTB::NTB_SMU_PCTRL0_aliasHOSTSEC; NTBSECBAR0x00000;
NTBSECBAR0=NBIFEPFNCFG::BASE_ADDR_1_aliasHOST_instNBIF2_func1[BASE_ADDR]
NTB::NTB_SMU_PCTRL0_aliasSMN; NTBx00000000; NTB=0400_0000h

Figure 13: Register Instance Table: BAR as Register Reference

1.4.4.5.5 PCICFG Access Method

The PCICFG access method is indicated by a physical mnemonic that has the form DXXFXxNUMBER. There are 2 cases:

- Bus omitted and implied to be 00h.
- Bus represented as BXX and indicates that the bus is indicated by a register field.

Example:

- Example: D18F0x000. (The bus, when omitted, is implied to be 00h)
- Example: BXXD0F0x000. (The bus as an expression that includes a register reference)

1.4.4.5.5.1 PCICFG Bus Implied to be 00h

Example:

- The absence of a B before the D14 implies that the bus is 0.

FCH::ITF::LPC::PciDevVendID_aliasHOST; D14F3x000
--

Figure 14: Register Instance Table: Bus Implied to be 00h

1.4.4.5.6 Data Port Access Method

A data port requires that the data port select be written before the register is accessed via the data port.

Example:

- The data port select value follows the "_x".
- The data port select register follows the "DataPortWrite=".

DF::FabricBlockInstanceCount_inst[PIE0,BCST]_aliasHOST; D18F0x040_x[00050001,00000000]; DataPortWrite=DF::FabricConfigAccessControl
DF::FabricBlockInstanceCount_inst[PIE0,BCST]_aliasSMN; DFF0x00000040_x[00050001,00000000]; DFF0=0001_C000h;
DataPortWrite=DF::FabricConfigAccessControl

Figure 15: Register Instance Table: Data Port Select

1.4.4.6 Register Field Format

The register field definition are all rows that follow the Bits/Description row. Each field row represents the definition of a bit range, with the bit ranges ordered from most to least significant. There are 2 columns, with the left column defining the field bit range, and the right column containing the field definition.

There are 2 field definition formats, simple and complex. If the description can be described in the simple one paragraph format then the simple format is used, else the complex format is used.

1.4.4.7 Simple Register Field Format

The simple register format compresses all content into a single paragraph with the following implied order:

1. Field Name (required)
 - Allowed to be Reserved. See 1.4.4.9 [Field Name is Reserved].
 - "FFXSE" in the example figure.
2. Field Title
 - "fast FXSAVE/FRSTOR enable" in the example figure.
3. Field Access Type. See 1.4.4.10 [Field Access Type].
 - In the example figure the access type is "Read-write".
4. Field Reset. See 1.4.4.11 [Field Reset].
 - In the example figure the reset is warm reset and "0".
5. Field Init. See 1.4.4.12 [Field Initialization].
6. Field Check. See 1.4.4.13 [Field Check].
7. Field Valid Values. If the valid values are single bit (e.g., 0=, 1=). See 1.4.4.14 [Field Valid Values].
 - In the example figure the 1= definition begins with "Enables" and ends with "mechanism".
 - In the example figure there is no 0= definition.
8. Field Description. If it is a single paragraph.
 - In the example figure the field description begins with "This is" and ends with "afterwards".

All fields that do not exist are omitted.

14	FFXSE: fast FXSAVE/FRSTOR enable Read-write Reset: 0; 1= Enables the fast FXSAVE/FRSTOR mechanism. A 64-bit operating system may enable the fast FXSAVE/FRSTOR mechanism if (Core::X86::CpuId::FeatureExtIdEdx[FFXSr] == 1). This bit is set once by the operating system and its value is not changed afterwards.
----	---

Figure 16: Simple Register Field Example

1.4.4.8 Complex Register Field Format

Content that cannot be expressed in the single paragraph format is broken out to a separate sub-row (a definition column row).

Additional sub-rows are added in the following order:

1. Complex expression for {Reset,AccessType,Init,Check}.
2. Instance specific {Reset,AccessType,Init,Check} values.
3. Description, if more than 1 paragraph.
4. Valid values, if more than 0=1=. Or a Valid bit table. (see figure)

The following figure highlights a complex access type specification.

63:0	APerfReadOnly: read-only actual core clocks counter. Reset: 0. This register increments in proportion to the actual number of core clocks cycles while the core is in C0. See Core::X86::Msr::MPerfReadOnly. This register is not affected by writes to Core::X86::Msr::APERF.
	AccessType: Core::X86::Msr::HWCR[EffFreqReadOnlyLock] ? Read-only, Volatile : Read-write, Volatile.

Figure 17: Register Field Sub-Row for {Reset,AccessType,Init,Check}

The following figure highlights a complex description specification.

4	INVDWBINVD: INVD to WBINVD conversion. Read-write. Reset: 1. Check: 1. 1=Convert INVD to WBINVD.
	Description: This bit is required to be set for normal operation when any of the following are true: <ul style="list-style-type: none"> • An L2 is shared by multiple threads. • An L3 is shared by multiple cores. • CC6 is enabled. • Probe filter is enabled.

Figure 18: Register Field Sub-Row for Description

The following figure highlights a complex valid value table, used either when the field is more than 1 bit or when the definition is more than a single sentence.

2:1	CpuWdtTimeBase: CPU watchdog timer time base. Read-write. Reset: 0. Specifies the time base for the timeout period specified in CpuWdtCountSel.										
	ValidValues:										
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>00b</td><td>1.31ms</td></tr> <tr> <td>01b</td><td>1.28us</td></tr> <tr> <td>10b</td><td>Reserved (5ns)</td></tr> <tr> <td>11b</td><td>Reserved</td></tr> </table>	Value	Description	00b	1.31ms	01b	1.28us	10b	Reserved (5ns)	11b	Reserved
Value	Description										
00b	1.31ms										
01b	1.28us										
10b	Reserved (5ns)										
11b	Reserved										

Figure 19: Register Field Sub-Row for Valid Value Table

The following figure highlights a valid bit table which is used when each bit has a specific function.

55:52	Reserved.
51:48	SliceMask. Read-write. Reset: 0.
	ValidValues:
Bit	Description
[0]	L3 Slice 0 mask.
[1]	L3 Slice 1 mask.
[2]	L3 Slice 2 mask.
[3]	L3 Slice 3 mask.

Figure 20: Register Field Sub-Row for Valid Bit Table

1.4.4.9 Field Name is Reserved

When a register field name is Reserved, and it does not explicitly specify an access type, then the implied access type is "write-as-read".

- Reads must not depend on the read value.
- Writes must only write the value that was read.

1.4.4.10 Field Access Type

The AccessType keyword is optional and specifies the access type for a register field. The access type for a field is a comma separated list of the following access types.

Table 8: AccessType Definitions

Term	Description
Read-only	Readable; writes are ignored.
Read-write	Readable and writable.
Read	Readable; must be associated with one of the following {Write-once, Write-1-only, Write-1-to-clear, Error-on-write}.
Write-once	Capable of being written once; all subsequent writes have no effect. If not associated with Read, then reads are undefined.
Write-only	Writable. Reads are undefined.
Write-1-only	Writing a 1 sets to a 1; Writing a 0 has no effect. If not associated with Read, then reads are undefined.
Write-1-to-clear	Writing a 1 clears to a 0; Writing a 0 has no effect. If not associated with Read, then reads are undefined.
Write-0-only	Writing a 0 clears to a 0; Writing a 1 has no effect. If not associated with Read, then reads are undefined.
Error-on-read	Error occurs on read.
Error-on-write	Error occurs on write.
Error-on-write-0	Error occurs on bitwise write of 0.
Error-on-write-1	Error occurs on bitwise write of 1.
Inaccessible	Not readable or writable (e.g., Hide ? Inaccessible : Read-Write).
Configurable	Indicates that the access type is configurable as described by the documentation.
Unpredictable	The behavior of both reads and writes is unpredictable.
Reserved-write-as-1	Reads are undefined. Must always write 1.
Reserved-write-as-0	Reads are undefined. Must always write 0.
Volatile	Indicates that a register field value may be modified by hardware, firmware, or microcode when fetching the first instruction and/or might have read or write side effects. No read may depend on the results of a previous read and no write may be omitted based on the value of a previous read or write. Not volatile indicates that software may service a read from the results of a previous read and that a write may be dropped if it's value matches the value previously read or written.

1.4.4.10.1 Conditional Access Type Expression

The ternary operator can be used to express an access type that is conditional on an expression that can contain any of the following:

- A register field value
- A constant
- A definition

1.4.4.11 Field Reset

The Reset keyword is optional and specifies the value for a register field at the time that hardware exits reset, before firmware initialization initiates.

Unless preceded by one of the following prefixes, the reset value is called warm reset and the value is applied at both warm and cold reset.

Table 9: Reset Type Definitions

Type	Description
Cold	Cold reset. The value is applied only at cold reset.
Fixed	The read value that applies at all times.

1.4.4.12 Field Initialization

The Init keyword is optional and specifies an initialization recommendation for a register field.

If present, then there is an optional prefix that specifies the owner of the initialization. See Table 10 [Init Type Definitions].

- Example: Init: BIOS,2'b00. //A initialization recommendation for a field to be programmed by BIOS.

Table 10: Init Type Definitions

Type	Description
BIOS	Initialized by AMD provided AMD Generic Encapsulated Software Architecture (AGESA™) x86 software.
SBIOS	Initialized by OEM or IBV provided x86 software, also called Platform BIOS.
OS	Initialized by OS or Driver.

1.4.4.13 Field Check

The Check keyword is optional and specifies the value that is recommended for firmware/software to write for a register field. It is a recommendation, not a requirement, and may not under all circumstances be what software programs.

1.4.4.14 Field Valid Values

A register can optionally have either a valid values table or a valid bit table:

- A valid values table specifies the definition for specific field values.
- A valid bit table specifies the definition for specific field bits.

1.4.5 Revision History and Change Bar Notation

If a set of PDFs is generated to show differences with respect to a previous release, then:

- A revision history table is generated and exists before the Overview section. (highlighted in red in the following figure)
- The top line indicates what release the changes are in reference to.
- Changes in the revision history have 3 types:
 - Add. A heading, register or field is added.
 - Delete. A heading, register, or field is deleted.
 - Updated. A heading, register, or field is updated.

Table of Contents	
List of Figures	
List of Tables	
Revision History	
> 1 Overview	
> 2 Core Complex (CCX)	
> 3 Reliability, Availability, and Serviceability (RAS) Features	
> 4 System Management Network (SMN)	
> 5 Remote System Management Unit (RSMU)	
> 6 Security	
> 7 System Management Unit (SMU)	
> 8 Advanced Platform Management Link (APML)	

Revision History

ZP PPR Revision 3.03 Changes with respect to 3.02, Jun 14, 2019, NDA release:

- 2.1.2 [Core Definitions]: Updated.
- 2.1.16.2.1.3 [ApicId Enumeration Requirements]: Updated.
- Core::X86::Cpuid::PerfOptId: Updated.
- Core::X86::Msr::SYS_CFG: Updated.
- Core::X86::Pmc::Core::ExRetBmResync: Deleted.
- Core::X86::Pmc::Core::L2FillPending: Added.
- Core::X86::Pmc::Core::L2Latency: Added.
- Core::X86::Pmc::Core::L2WcbReq: Deleted.
- 9.1.1 [Definitions]: Updated.
- 12.1.1 [Definitions]: Updated.
- FCH::PM::LpcMisc: Updated.
- FCH::PM::ResetCmd: Updated.
- 13.2.16.2 [GPIO Registers]: Updated.
- FCH::GPIO::GPIOBank0Ctl: Updated.
- (9 Registers Total)
- FCH::GPIO::GPIOBank3Ctl: Updated.**

Figure 21: Revision History Format Example

The following diagram shows the notation for changes:

- If a change exists on a line then a thin vertical bar is rendered in the left margin, as circled in blue.
- Deleted text is indicated with amber and strike-through, as circled in red.
- Added text is indicated with amber and underlined, as circled in green.

GPIOx003[00...FC] [GPIO Bank 3 Control Register] (FCH::GPIO::GPIOBank3Ctl)	
	Each GPIO pin is controlled by 4 bytes. These registers control GPIO bank 3 pins: GPIO[224:193- GPIO224].
	_link[63:0]_aliasHOST; GPIOx003[FC,F8,F4,F0,EC,E8,E4,E0,DC,D8,D4,D0,CC,C8,C4,C0,BC,B8,B4,B0,AC,A8,A4,A0,9C,98,94,90,8C,88,84,80,7C,78,74,70,6C,68,64,60,5C,58,54,50,4C,48,44,40,3C,38,34,30,2C,28,24,20,1C,18,14,10,0C,08,04,00]; GPIO=FED8_1500h
Bits	Description
31:30	Reserved.
29	WakeSts. Read,Write-1-to-clear. Reset: X. 0=The pin did not generate a wake event. 1=The pin is a wake source. Wake Sts-Register status.
28	InterruptSts. Read,Write-1-to-clear. Reset: X. 0=The pin did not generate an interrupt. 1=The pin is an interrupt

Figure 22: Change Notation Example

1.5 Definitions

Table 11: Definitions

Term	Description
AGESA™	AMD Generic Encapsulated Software Architecture.
AP	Applications Processor.
APML	Advanced Platform Management Link.
BCD	Binary Coded Decimal number format.
BCS	Base Configuration Space.
BIST	Built-In Self-Test. Hardware within the processor that generates test patterns and verifies that they are stored correctly (in the case of memories) or received without error (in the case of links).
Boot VID	Boot Voltage ID. This is the VDD and VDDNB voltage level that the processor requests from the external voltage regulator during the initial phase of the cold boot sequence.
C-states	These are ACPI defined core power states. C0 is operational. All other C-states are low-power states in which the processor is not executing code. See docACPI.
Cold reset	PWROK is de-asserted and RESET_L is asserted.
COF	Current operating frequency of a given clock domain.
DID	Divisor Identifier. Specifies the post-PLL divisor used to reduce the COF.
Doubleword	A 32-bit value.
DW	Doubleword.
ECS	Extended Configuration Space.
FCH	The integrated platform subsystem that contains the IO interfaces and bridges them to the system BIOS. Previously included in the Southbridge.
FID	Frequency Identifier. Specifies the PLL frequency multiplier for a given clock domain.
GB	Gbyte or Gigabyte; 1,073,741,824 bytes.
GT/s	Giga-Transfers per second.
IFCM	Isochronous flow-control mode, as defined in the link specification.
IO configuration	Access to configuration space through IO ports CF8h and CFCh.
IP	In electronic design, a semiconductor Intellectual Property, IP, or IP block is a reusable unit of logic, cell, or integrated circuit layout design that is the intellectual property of one party.
KB	Kbyte or Kilobyte; 1024 bytes.
Master abort	This is a PCI-defined term that is applied to transactions on other than PCI buses. It indicates that the transaction is terminated without affecting the intended target; Reads return all 1s; Writes are discarded; the master abort error code is returned in the response, if applicable; master abort error bits are set if applicable.
MB	Megabyte; 1024 KB.
MMIO	Memory-Mapped Input-Output range. This is physical address space that is mapped to the IO functions such as the IO links or MMIO configuration.
MMIO configuration	Access to configuration space through memory space.
OW	Octword. An 128-bit value.
PCIe®	PCI Express.
PCS	Physical Coding Sublayer.
Processor	System on Chip (SoC) covered by this PPR. See 1.8 [Processor Overview].
P-state	Performance state.
QW	Quadword. A 64-bit value.
RAS	Reliability, availability and serviceability (industry term). See 3.1 [Machine Check Architecture].
REFCLK	Reference clock. Refers to the clock frequency (100 MHz) or the clock period (10 ns) depending on the context used.
RX	Receiver.
Shutdown	A state in which the affected core waits for either INIT, RESET, or NMI. When shutdown state is entered, a shutdown special cycle is sent on the IO links.

SMAF	System Management Action Field. This is the code passed from the SMC to the processors in STPCLK assertion messages.
SMC	System Management Controller. This is the platform device that communicates system management state information to the processor through an IO link, typically the system IO hub.
Speculative event	A performance monitor event counter that counts all occurrences of the event even if the event occurs during speculative code execution.
SSC	Spread Spectrum Clocking.
TDC	Thermal Design Current.
TDP	Thermal Design Power. A power consumption parameter that is used in conjunction with thermal specifications to design appropriate cooling solutions for the processor.
TOM	Top of Memory.
TOM2	Top of extended Memory.
TX	Transmitter.
UMI	Unified Media Interface. The link between the processor and the FCH.
VID	Voltage level identifier.
Warm reset	RESET_L is asserted only (while PWROK stays high).
XBAR	Cross bar; command packet switch.

1.6 Changes Between Revisions and Product Variations

1.6.1 Revision Conventions

The processor revision is specified by CPUID_Fn00000001_EAX (FamModStep) or CPUID_Fn80000001_EAX (FamModStepExt). This document uses a revision letter instead of specific model numbers. Where applicable, the processor stepping is indicated after the revision letter. All behavior marked with a revision letter apply to future revisions unless they are superseded by a change in a later revision. See the revision guide in 1.2 [Reference Documents] for additional information about revision determination.

1.7 Package

1.7.1 Package type

The following packages are supported.

Table 12: Package Definitions

Term	Description
AM5	Desktop, single socket. For client desktop platform (LGA) with DDR5. AM5 = (Core::X86::Cpuid::BrandId[PkgType] == 00h).
FL1	Notebook and mobile workstations. FL1 = (Core::X86::Cpuid::BrandId[PkgType] == 01h).

1.8 Processor Overview

1.8.1 Features

Family 19h Models 60h-6Fh are microprocessor System-On-a-Chip (SOC) multi-chip module (MCM). It is built using a

mixed-technology chiplet approach - up to two core/cache complex dies (CCD) and a single I/O die (IOD).

The table, Table 13 [PCI Device ID Assignments.], shows the Family 19h, Models 60h-6Fh PCI Vendor ID and Device ID assignments. Graphics uses the ATI Vendor ID of 1002h, the others use the AMD Vendor ID of 1022h.

Table 13: PCI Device ID Assignments.

Vendor ID	Device ID	Bus	Device	Function	Component
1022h	14D8h	0	0	0	Root Complex
1022h	14D9h	0	0	2	IOMMU
1022h	14DAh	0	1, 2, 3, 4, 8	0	PCIe® Dummy Host Bridge
1022h	14DBh	0	1	1	PCIe® GPP Bridge 0
1022h	14DBh	0	1	2	PCIe® GPP Bridge 1
1022h	14DBh	0	1	3	PCIe® GPP Bridge 2
1022h	14DBh	0	1	4	PCIe® GPP Bridge 3
1022h	14DBh	0	1	5	PCIe® GPP Bridge 4
1022h	14DBh	0	1	6	PCIe® GPP Bridge 5
1022h	14DBh	0	1	7	PCIe® GPP Bridge 6
1022h	14DBh	0	2	1	PCIe® GPP Bridge 7
1022h	14DBh	0	2	2	PCIe® GPP Bridge 8
1022h	14DBh	0	3	1	PCIe® GPP Bridge 0
1022h	14DBh	0	3	2	PCIe® GPP Bridge 1
1022h	14DBh	0	3	3	PCIe® GPP Bridge 2
1022h	14DBh	0	3	4	PCIe® GPP Bridge 3
1022h	14DBh	0	3	5	PCIe® GPP Bridge 4
1022h	14DBh	0	3	6	PCIe® GPP Bridge 5
1022h	14DBh	0	3	7	PCIe® GPP Bridge 6
1022h	14DBh	0	4	1	PCIe® GPP Bridge 7
1022h	14DBh	0	4	2	PCIe® GPP Bridge 8
1022h	14DDh	0	8	1	Internal PCIe® GPP Bridge 0 to Bus A
1022h	14DDh	0	8	2	Internal PCIe® GPP Bridge 1 to Bus B
1022h	14DDh	0	8	3	Internal PCIe® GPP Bridge 2 to Bus C
1022h	14DEh	A	0	0	PCIe® Dummy Function
1022h	14DEh	B	0	0	PCIe® Dummy Function
1022h	14DEh	C	0	0	PCIe® Dummy Function
1022h	14E0h	0	24	0	Data Fabric: Device 18h; Function 0
1022h	14E1h	0	24	1	Data Fabric: Device 18h; Function 1
1022h	14E2h	0	24	2	Data Fabric: Device 18h; Function 2
1022h	14E3h	0	24	3	Data Fabric: Device 18h; Function 3
1022h	14E4h	0	24	4	Data Fabric: Device 18h; Function 4
1022h	14E5h	0	24	5	Data Fabric: Device 18h; Function 5
1022h	14E6h	0	24	6	Data Fabric: Device 18h; Function 6

1022h	14E7h	0	24	7	Data Fabric: Device 18h; Function 7
1022h	15B6h	A	0	3	USB3.1 (USB0)
1022h	15B7h	A	0	4	USB3.1 (USB1)
1022h	15B8h	C	0	0	USB2 (USB BIO) secure
1022h	15E2h	A	0	5	Audio Processor (ACP)
1022h	15E3h	A	0	6	Audio Processor – HD Audio Controller (Standalone AZ)
1002h	164Eh	A	0	0	Internal GPU (GFX)
1002h	1640h	A	0	1	Display HD Audio Controller (GFXAZ)

Note: In Table 13 [PCI Device ID Assignments.], programmable bus numbers are labeled A and B. Buses with different labels cannot be assigned the same bus number.

Note: Vendor ID 1002h is used for Internal GPU (164Eh) and Display HD Audio Controller (1640h).

2 Core Complex (CCX)

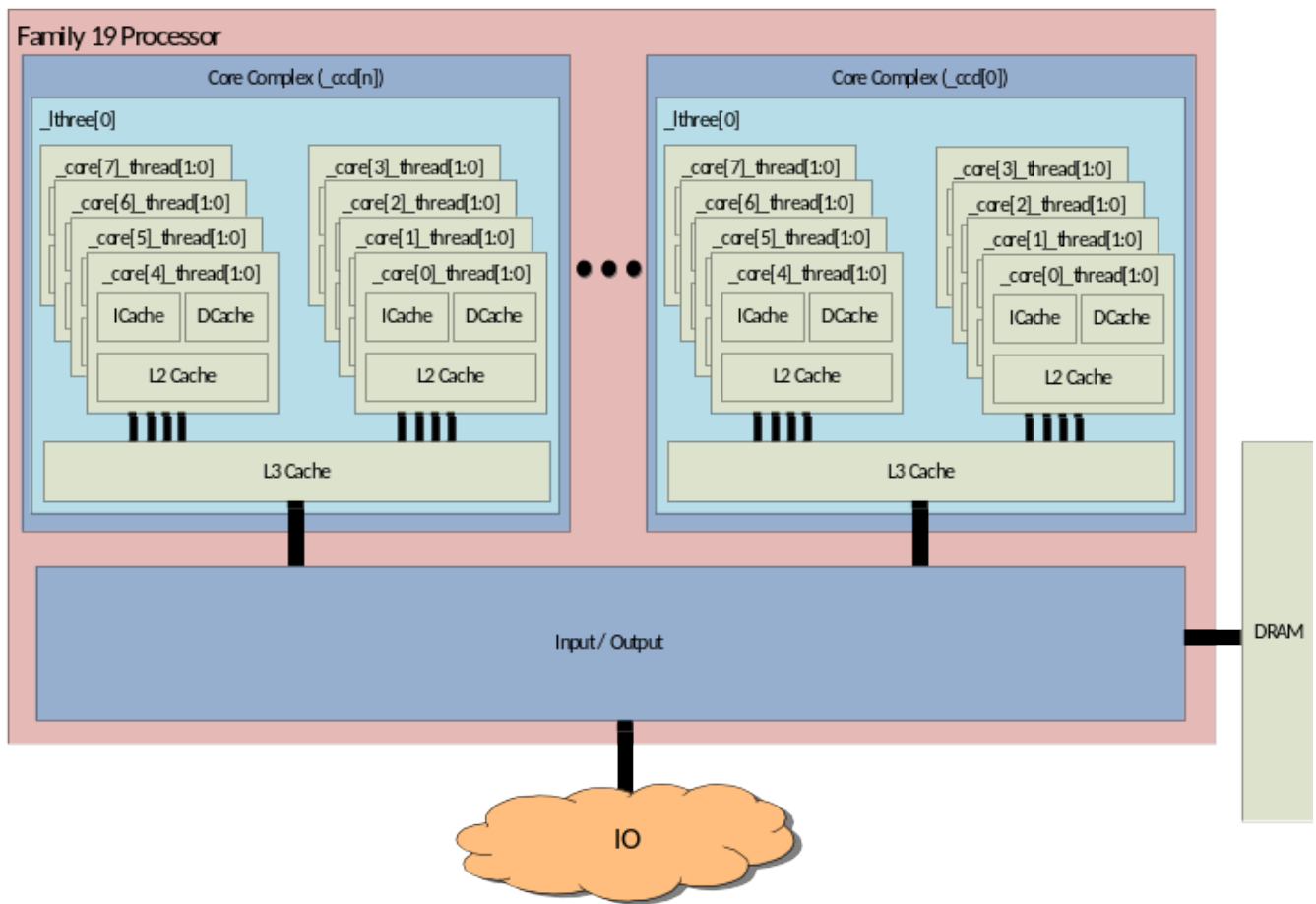


Figure 23: Overview of Family 19 Core Component Numbering

2.1 Processor x86 Core

2.1.1 Core Functional Information

2.1.1.1 Core Definitions

Table 14: Definitions

Term	Description
BSC	Boot strap core. Core 0 of the BSP.
BSP	Boot strap processor.
Canonical-address	An address in which the state of the most-significant implemented bit is duplicated in all the remaining higher-order bits, up to bit[63].
CCX	Core Complex where more than one core shares L3 resources.
CMP	Specifies the core number.
Core	The instruction execution unit of the processor when the term Core is used in a x86 core context.
CoreCOF	Core current operating frequency in MHz. CoreCOF = (Core::X86::Msr::PStateDef[CpuFid[7:0]]/Core::X86::Msr::PStateDef[CpuDfsId])*200. A nominal frequency reduction can occur if spread spectrum clocking is enabled.
CPL	Current Privilege Level of the running task when the term CPL is used in a x86 core context.
CpuCoreNum	Specifies the core number.
#GP	A general-protection exception.
#GP(0)	Notation indicating a general-protection exception (#GP) with error code of 0.
HWPF	Hardware Prefetcher.
IBS	Instruction based sampling.
IO configuration	Access to configuration space through IO ports CF8h and CFCh.
IORR	IO range register.
L1 cache	The level 1 caches (instruction cache and the data cache).
L2 cache	The level 2 caches.
L3	Level 3 Cache. The L3 term is also in Addrmaps to enumerate CCX units.
L3 cache	Level 3 Cache.
Linear (virtual) address	The address generated by a core after the segment is applied.
LINT	Local interrupt.
Logical address	The address generated by a core before the segment is applied.
LRU	Least recently used.
LVT	Local vector table. A collection of APIC registers that define interrupts for local events (e.g., APIC[530:500] [Extended Interrupt [3:0] Local Vector Table]).
Macro-op	The front-end of the pipeline breaks instructions into macro-ops and transfers (dispatches) them to the back-end of the pipeline for scheduling and execution. See Software Optimization Guide.
Micro-op	Processor schedulers break down macro-ops into sequences of even simpler instructions called micro-ops, each of which specifies a single primitive operation. See Software Optimization Guide.
NBC	NBC=(CPUID Fn00000001_EBX[LocalApicId[3:0]] == 0). Node Base Core. The lowest numbered core in the node.
MTRR	Memory-type range register. The MTRRs specify the type of memory associated with various memory ranges.
NTA	Non-Temporal Access.
PPIN	Protected Processor Inventory Number.
PTE	Page table entry.
SMI	System management interrupt.
SMM	System Management Mode.
SMT	Simultaneous multithreading. See Core::X86::Cpuid::CoreId[ThreadsPerCore].
Speculative event	A performance monitor event counter that counts all occurrences of the event even if the event occurs during speculative code execution.
SVM	Secure virtual machine.
Thread	One architectural context for instruction execution.

WDT	Watchdog timer. A timer that detects activity and triggers an error if a specified period of time expires without the activity.
X2APICEN	x2 APIC is enabled. X2APICEN = (Core::X86::Msr::APIC_BAR[ApicEn] && Core::X86::Msr::APIC_BAR[x2ApicEn]).

2.1.2 Secure Virtual Machine Mode (SVM)

Support for SVM mode is indicated by Core::X86::Cpuid::FeatureExtIdEcX[SVM].

2.1.2.1 BIOS support for SVM Disable

The BIOS should include the following user setup options to enable and disable AMD Virtualization™ technology.

2.1.2.1.1 Enable AMD Virtualization™

- Core::X86::Msr::VM_CR[SvmeDisable] = 0.
- Core::X86::Msr::VM_CR[Lock] = 1.
- Core::X86::Msr::SvmLockKey[SvmLockKey] = 0000_0000_0000_0000h.

2.1.2.1.2 Disable AMD Virtualization™

- Core::X86::Msr::SvmLockKey[SvmLockKey] = 0000_0000_0000_0000h.
- Core::X86::Msr::VM_CR[SvmeDisable] = 1.
- Core::X86::Msr::VM_CR[Lock] = 1.

The BIOS may also include the following user setup options to disable AMD Virtualization technology.

2.1.2.1.3 Disable AMD Virtualization™, with a user supplied key

- Core::X86::Msr::VM_CR[SvmeDisable] = 1.
- Core::X86::Msr::VM_CR[Lock] = 1.
- Core::X86::Msr::SvmLockKey[SvmLockKey] programmed with value supplied by user. This value should be stored in NVRAM.

2.1.3 Effective Frequency

The effective frequency interface allows software to discern the average, or effective, frequency of a given core over a configurable window of time. This provides software a measure of actual performance rather than forcing software to assume the current frequency of the core is the frequency of the last P-state requested. Core::X86::Msr::MPERF is incremented by hardware at the P0 frequency while the core is in C0. Core::X86::Msr::APERF increments in proportion to the actual number of core clocks cycles while the core is in C0.

The following procedure calculates effective frequency using Core::X86::Msr::MPERF and Core::X86::Msr::APERF:

1. At some point in time, write 0 to both MSRs.
2. At some later point in time, read both MSRs.
3. Effective frequency = (value read from Core::X86::Msr::APERF / value read from Core::X86::Msr::MPERF) * P0 frequency.

Additional notes:

- The amount of time that elapses between steps 1 and 2 is determined by software.

- It is software's responsibility to disable interrupts or any other events that may occur in between the Write of Core::X86::Msr::MPERF and the Write of Core::X86::Msr::APERF in step 1 or between the Read of Core::X86::Msr::MPERF and the Read of Core::X86::Msr::APERF in step 2.
- The behavior of Core::X86::Msr::MPERF and Core::X86::Msr::APERF may be modified by Core::X86::Msr::HWCER[EffFreqCntMwait].
- The effective frequency interface provides +/- 50MHz accuracy if the following constraints are met:
 - Effective frequency is read at most one time per millisecond.
 - When reading or writing Core::X86::Msr::MPERF and Core::X86::Msr::APERF software executes only MOV instructions, and no more than 3 MOV instructions, between the two RDMSR or WRMSR instructions.
 - Core::X86::Msr::MPERF and Core::X86::Msr::APERF are invalid if an overflow occurs.

2.1.4 Address Space

2.1.4.1 Virtual Address Space

The processor supports 48-bit address bits of virtual memory space (256 TB) as indicated by Core::X86::Cpuid::LongModeInfo.

2.1.4.2 Physical Address Space

The processor supports a 48-bit physical address space. See Core::X86::Cpuid::LongModeInfo. The processor master aborts the following upper-address transactions (to address PhysAddr):

- Link or core requests with non-zero PhysAddr[63:48].

2.1.4.3 System Address Map

The processor defines a Reserved memory address region starting at FFFD_0000_0000h and extending up to FFFF_FFFF_FFFFh. System software must not map memory into this region. Downstream host accesses to the Reserved address region results in a page fault. Upstream system device accesses to the reserved address region results in an undefined operation.

2.1.4.3.1 Memory Access to the Physical Address Space

All memory accesses to the physical address space from a core are sent to its associated Data Fabric (DF). All memory accesses from a link are routed through the DF. An IO link access to physical address space indicates to the DF the cache attribute (Coherent or Non-coherent, based on bit[0] of the Sized Read and Write commands).

A core access to physical address space has two important attributes that must be determined before issuing the access to the NB: the memory type (e.g., WB, WC, UC; as described in the MTRRs) and the access destination (DRAM or MMIO).

If the memory map maps a region as DRAM that is not populated with real storage behind it, then that area of DRAM must be mapped as UC memtype.

This mechanism is managed by the BIOS and does not require any setup or changes by system software.

2.1.4.3.1.1 Determining Memory Type

The memory type for a core access is determined by the highest priority of the following ranges that the access falls in: 1=Lowest priority.

1. The memory type as determined by architectural mechanisms.
 - See the docAPM2 chapter titled "Memory System", sections "Memory-Type Range Registers" and "Page-Attribute Table Mechanism".
 - See the docAPM2 chapter titled "Nested Paging", section "Combining Memory Types, MTRRs".
 - See Core::X86::Msrb::MTRRdefType, Core::X86::Msrb::MtrrVarBase, Core::X86::Msrb::MtrrVarMask, Core::X86::Msrb::MtrrFix_64K and Core::X86::Msrb::MtrrFix_16K_0 through Core::X86::Msrb::MtrrFix_4K_7.
2. TSeg & ASeg SMM mechanism (See Core::X86::Msrb::SMMAddr and Core::X86::Msrb::SMMMMask).
3. CR0[CD]: If (CR0[CD] == 1) then MemType = CD.
4. MMIO configuration space, APIC space.
 - MMIO APIC space and MMIO config space must not overlap.
 - MemType = UC.
5. If ("In SMM Mode" && ~((Core::X86::Msrb::SMMMMask[AValid] && "The address falls within the ASeg region") || (Core::X86::Msrb::SMMMMask[TValid] && "The address falls within the TSeg region"))) then MemType = CD.

2.1.5 Configuration Space

PCI-defined configuration space was originally defined to allow up to 256 bytes of register space for each function of each device; these first 256 bytes are called base configuration space (BCS). It was expanded to support up to 4096 bytes per function; bytes 256 through 4095 are called extended configuration space (ECS).

The processor includes configuration space registers located in both BCS and ECS. Processor configuration space is accessed through bus 0, devices 18h to 1Fh, where device 18h corresponds to node 0 and device 1Fh corresponds to node 7. See 2.1.5.3 [Processor Configuration Space].

Configuration space is accessed by the processor through two methods as follows:

- IO-space configuration: IO instructions to addresses CF8h and CFCh.
 - Enabled through IO::IoCfgAddr[ConfigEn], which allows access to BCS.
 - Use of IO-space configuration can be programmed to generate GP faults through Core::X86::Msrb::HWCR[IoCfgGpFault].
 - SMI trapping for these accesses is specified by Core::X86::Msrb::SMI_ON_IO_TRAP_CTL_STS and Core::X86::Msrb::SMI_ON_IO_TRAP.
- Memory Mapped IO (MMIO) configuration: configuration space is a region of memory space.
 - The base address and size of this range is specified by Core::X86::Msrb::MmioCfgBaseAddr. The size is controlled by the number of configuration-space bus numbers supported by the system. Accesses to this range are converted configuration space as follows:
- Address[31:0] = {0h, segment[6:0], bus[7:0], device[4:0], function[2:0], offset[11:0]}.

The BIOS may use either configuration space access mechanism during boot. Before booting the OS, BIOS must disable IO access to ECS, enable MMIO configuration and build an ACPI defined MCFG table. BIOS ACPI code must use MMIO to access configuration space.

2.1.5.1 Memory Mapped IO (MMIO) Configuration Coding Requirements

MMIO configuration space accesses must use the uncacheable (UC) memory type.

Instructions used to read MMIO configuration space are required to take the following form:

```
mov eax/ax/al, any_address_mode;
```

Instructions used to write MMIO configuration space are required to take the following form:

```
mov any_address_mode, eax/ax/al;
```

No other source/target registers may be used other than eax/ax/al.

In addition, all such accesses are required not to cross any naturally aligned DW boundary. Access to MMIO configuration space registers that do not meet these requirements result in undefined behavior.

2.1.5.2 MMIO Configuration Ordering

Since MMIO configuration cycles are not serializing in the way that IO configuration cycles are, their ordering rules relative to posted may result in unexpected behavior.

Therefore, processor MMIO configuration space is designed to match the following ordering relationship that exists naturally with IO-space configuration: if a core generates a configuration cycle followed by a posted Write cycle, then the posted Write is held in the processor until the configuration cycle completes. As a result, any unexpected behavior that might have resulted if the posted Write cycle were to pass MMIO configuration cycle is avoided.

2.1.5.3 Processor Configuration Space

Accesses to unimplemented registers of implemented functions are ignored: Writes dropped; Reads return 0. Accesses to unimplemented functions also ignored: Writes are dropped; however, Reads return all F's. The processor does not log any master abort events for accesses to unimplemented registers or functions.

Accesses to device numbers of devices not implemented in the processor are routed based on the configuration map registers. If such requests are master aborted, then the processor can log the event.

2.1.6 PCI Configuration Legacy Access

IOx0CF8 [IO-Space Configuration Address] (IO::IoCfgAddr)

Read-write. Reset: 0000_0000h.

IO::IoCfgAddr, and IO::IoCfgData are used to access system configuration space, as defined by the PCI specification. IO::IoCfgAddr provides the address register and IO::IoCfgData provides the data port. Software sets up the configuration address by writing to IO::IoCfgAddr. Then, when an access is made to IO::IoCfgData, the processor generates the corresponding configuration access to the address specified in IO::IoCfgAddr. See 2.1.5 [Configuration Space].

IO::IoCfgAddr may only be accessed through aligned, DW IO Reads and Writes; otherwise, the accesses are passed to the appropriate IO link. Accesses to IO::IoCfgAddr and IO::IoCfgData received from an IO link are treated as all other IO transactions received from an IO link. IO::IoCfgAddr and IO::IoCfgData in the processor are not accessible from an IO link.

_aliasIO; IOx0CF8; IO=0000_0000h

Bits	Description
31	ConfigEn: configuration space enable. Read-write. Reset: 0. 0=IO Read and Write accesses are passed to the appropriate IO link and no configuration access is generated. 1=IO Read and Write accesses to IO::IoCfgData are translated into configuration cycles at the configuration address specified by this register.
30:28	Reserved.
27:24	ExtRegNo: extended register number. Read-write. Reset: 0h. ExtRegNo provides bits[11:8] and RegNo provides bits[7:2] of the byte address of the configuration register.
23:16	BusNo: bus number. Read-write. Reset: 00h. Specifies the bus number of the configuration cycle.
15:11	Device: device number. Read-write. Reset: 00h. Specifies the device number of the configuration cycle.
10:8	Function. Read-write. Reset: 0h. Specifies the function number of the configuration cycle.
7:2	RegNo: register address. Read-write. Reset: 00h. See IO::IoCfgAddr[ExtRegNo].
1:0	Reserved.

IOx0CFC [IO-Space Configuration Data Port] (IO::IoCfgData)

Read-write. Reset: 0000_0000h.

_aliasIO; IOx0CFC; IO=0000_0000h

Bits	Description
31:0	Data. Read-write. Reset: 0000_0000h. See IO::IoCfgAddr.

2.1.7 System Software Interaction With SMT Enabled

If Core::X86::Cpuid::CoreId[ThreadsPerCore] > 0, then SMT is enabled in all cores in the system. When SMT is enabled, the resources of each core are dynamically balanced among the hardware threads executing on that core. The number of hardware threads (hereafter "threads") supported by a single core when SMT is enabled is reported in Core::X86::Cpuid::CoreId[ThreadsPerCore]. System software that is SMT-aware may take advantage of the knowledge that core resources are being shared among multiple threads when scheduling tasks to be run by each thread on each core. System software that is not SMT-aware sees each thread as an independent core.

2.1.8 Register Sharing

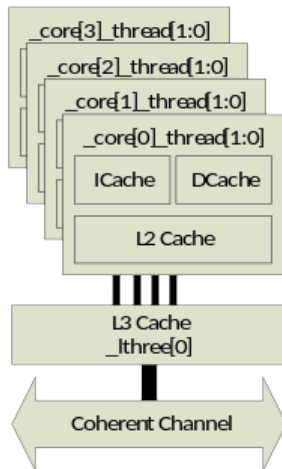


Figure 24: Register Sharing Domains

MSR0000_0010 [Time Stamp Counter] (TSC)

Read-write, Volatile. Reset: 0000_0000_0000_0000h.	
Core::X86::Msr::TSC_lthree0_core[3:0]_thread[1:0]; MSR00000010	
Bits	Description
63:0	TSC: time stamp counter. Read-write, Volatile. Reset: 0. The TSC increments at the P0 frequency. The TSC counts at the same rate in all P-states, all C states, S0, or S1. A read of this MSR in guest mode is affected by Core::X86::Msr::TscRateMsr. The value (TSC/TSCRatio) is the TSC P0 frequency based value (as if TSCRatio == 1.0) when (TSCRatio != 1.0).

Figure 25: Instance Parameters

Instances of core registers are designated as ccd[n:0]_lthree[n:0]_core[n:0]_thread[1:0]. Core registers may be shared at various levels of hierarchy as one register instance per node, per L3 complex, per core or per thread. The absence of the instance parameter _thread[1:0] signifies that there is not a specific instance of said register per thread and thus the register is shared between thread[1] and thread[0]. Similarly, the absence of the instance parameter _core[n:0] signifies that there is not a specific instance of said register per core and thus the register is shared by all cores in that L3 complex, and so on. The absence of instance parameters indicate there is one shared register at the node level. Software must coordinate writing to shared registers with other threads in the same sharing hierarchy level.

2.1.9 Timers

Each core includes the following timers. These timers do not vary in frequency regardless of the current P-state or C-state.

- Core::X86::Msr::TSC; the TSC increments at the rate specified by the P0 Pstate.
- The APIC timer (Core::X86::Apic::TimerInitialCount and Core::X86::Apic::TimerCurrentCount), which increments at the rate of 2xCLKIN; the APIC timer may increment in units of between 1 and 8.

2.1.10 Interrupts

2.1.10.1 System Management Mode (SMM)

System management mode (SMM) is typically used for system control activities such as power management. These activities are typically transparent to the operating system.

2.1.10.1.1 SMM Overview

SMM is entered by a core on the next instruction boundary after a system management interrupt (SMI) is received and recognized. A core may be programmed to broadcast a special cycle to the system, indicating that it is entering SMM mode. The core then saves its state into the SMM memory state save area and jumps to the SMI service routine (or SMI handler). The pointer to the SMI handler is specified by MSRs. The code and data for the SMI handler are stored in the SMM memory area, which may be isolated from the main memory accesses.

The core returns from SMM by executing the RSM instruction from the SMI handler. The core restores its state from the SMM state save area and resumes execution of the instruction following the point where it entered SMM. The core may be programmed to broadcast a special bus cycle to the system, indicating that it is exiting SMM mode.

2.1.10.1.2 Mode and Default Register Values

The software environment after entering SMM has the following characteristics:

- Addressing and operation is in Real mode.
 - A far jump, call or return in the SMI handler can only address the lower 1M of memory, unless the SMI handler first switches to protected mode.
 - If (Core::X86::Msrr::SMM_BASE[SmmBase] >= 0010_0000h) then:
 - The value of the CS selector is undefined upon SMM entry.
 - The undefined CS selector value should not be used as the target of a far jump, call, or return.
- 4-Gbyte segment limits.
- Default 16-bit operand, address, and stack sizes (instruction prefixes can override these defaults).
- Control transfers that do not override the default operand size truncate the EIP to 16 bits.
- Far jumps or calls cannot transfer control to a segment with a base address requiring more than 20 bits, as in Real mode segment-base addressing, unless a change is made into protected mode.
- Interrupt vectors use the Real mode interrupt vector table.
- The IF flag in EFLAGS is cleared (INTR is not recognized).
- The TF flag in EFLAGS is cleared.
- The NMI and INIT interrupts are masked.
- Debug register DR7 is cleared (debug traps are disabled).

The SMM base address is specified by Core::X86::Msrr::SMM_BASE[SmmBase]. Important offsets to the base address pointer are:

- Core::X86::Msrr::SMM_BASE[SmmBase] + 8000h: SMI handler entry point.
- Core::X86::Msrr::SMM_BASE[SmmBase] + FE00h - FFFFh: SMM state save area.

2.1.10.1.3 SMI Sources And Delivery

The processor accepts SMIs as link-defined interrupt messages only. The core/node destination of these SMIs is a function of the destination field of these messages. However, the expectation is that all such SMI messages are specified to be delivered globally (to all cores of all nodes).

There are also several local events that can trigger SMIs. However, these local events do not generate SMIs directly. Each of them triggers a programmable IO cycle that is expected to target the SMI command port in the IO hub and trigger a global SMI interrupt message back to the coherent fabric.

Local sources of SMI events that generate the IO cycle specified in Core::X86::Msrr::SmiTrigIoCycle are:

- In the core, as specified by:
 - Core::X86::Msrr::McExcepRedir.
 - Core::X86::Msrr::SMI_ON_IO_TRAP.
- All local APIC LVT registers programmed to generate SMIs.

The status for these are stored in Core::X86::Smm::LocalSmiStatus.

2.1.10.1.4 SMM Initial State

After storing the save state, execution starts at Core::X86::Msrr::SMM_BASE[SmmBase] + 08000h. The SMM initial state is specified in the following table.

Table 15: SMM Initial State

Register	SMM Initial State
CS	SmmBase[19:4]
DS	0000h
ES	0000h
FS	0000h
GS	0000h
SS	0000h
General-Purpose Registers	Unmodified.
EFLAGS	0000_0002h
RIP	0000_0000_0000_8000h
CR0	Bits[0,2,3,31] cleared (PE, EM, TS, and PG); remainder is unmodified.
CR4	0000_0000_0000_0000h
GDTR	Unmodified.
LDTR	Unmodified.
IDTR	Unmodified.
TR	Unmodified.
DR6	Unmodified.
DR7	0000_0000_0000_0400h
EFER	All bits are cleared except bit[12] (SVME) which is unmodified.

2.1.10.1.5 SMM Save State

In the following table, the offset field provides the offset from the SMM base address specified by Core::X86::Msrr::SMM_BASE[SmmBase].

Table 16: SMM Save State

Offset	Size	Contents	Access
FE00h	Word	ES Selector	Read-only
FE02h	6 Bytes		
FE08h	Quadword		
FE10h	Word	CS Selector	Read-only
FE12h	6 Bytes		
FE18h	Quadword		

FE20h	Word	SS	Selector	Read-only
FE22h	6 Bytes		Reserved	
FE28h	Quadword		Descriptor in memory format	
FE30h	Word	DS	Selector	Read-only
FE32h	6 Bytes		Reserved	
FE38h	Quadword		Descriptor in memory form	
FE40h	Word	FS	Selector	Read-only
FE42h	2 Bytes		Reserved	
FE44h	Doubleword		FS Base {16'b[47], 47:32}(note 1)	
FE48h	Quadword		Descriptor in memory format	
FE50h	Word	GS	Selector	Read-only
FE52h	2 Bytes		Reserved	
FE54h	Doubleword		GS Base {16'b[47], 47:32}(note 1)	
FE58h	Quadword		Descriptor in memory format	
FE60h	4 Bytes	GDTR	Reserved	Read-only
FE64h	Word		Limit	
FE66h	2 Bytes		Reserved	
FE68h	Quadword		Descriptor in memory format	
FE70h	Word	LDTR	Selector	Read-only
FE72h	Word		Attributes	
FE74h	Doubleword		Limit	
FE78h	Quadword		Base	
FE80h	4 Bytes	IDTR	Reserved	Read-only
FE84h	Word		Limit	
FE86h	2 Bytes		Reserved	
FE88h	Quadword		Base	
FE90h	Word	TR	Selector	Read-only
FE92h	Word		Attributes	
FE94h	Doubleword		Limit	
FE98h	Quadword		Base	
FEA0h	Quadword	IO_RESTART_RIP		
FEA8h	Quadword	IO_RESTART_RCX		
FEB0h	Quadword	IO_RESTART_RSI		
FEB8h	Quadword	IO_RESTART_RDI		
FEC0h	Doubleword	Core::X86::Smm::TrapOffset [SMM IO Trap Offset]		Read-only
FEC4	Doubleword	Core::X86::Smm::LocalSmiStatus		Read-only
FEC8h	Byte	Core::X86::Smm::IoRestart		Read-write
FEC9h	Byte	Core::X86::Smm::AutoHalt		Read-write
FECAh	Byte	Core::X86::Smm::NmiMask		Read-write
FECBh	5 Bytes	Reserved		
FED0h	Quadword	EFER		Read-only
FED8h	Quadword	Core::X86::Smm::SvmState		Read-only
FEE0h	Quadword	Guest VMCB physical address		Read-only

FEE8h	Quadword	SVM Virtual Interrupt Control	Read-only
FEF0h	16 Bytes	Reserved	
FEFCh	Doubleword	Core::X86::Smm::SmmRevID	Read-only
FF00h	Doubleword	Core::X86::Smm::SmmBase	Read-write
FF04h	28 Bytes	Reserved	
FF20h	Quadword	Guest PAT	Read-only
FF28h	Quadword	Host EFER (note 2)	
FF30h	Quadword	Host CR4 (note 2)	
FF38h	Quadword	Nested CR3 (note 2)	
FF40h	Quadword	Host CR0 (note 2)	
FF48h	Quadword	CR4	
FF50h	Quadword	CR3	
FF58h	Quadword	CR0	
FF60h	Quadword	DR7	Read-only
FF68h	Quadword	DR6	
FF70h	Quadword	RFLAGS	Read-write
FF78h	Quadword	RIP	Read-write
FF80h	Quadword	R15	
FF88h	Quadword	R14	
FF90h	Quadword	R13	
FF98h	Quadword	R12	
FFA0h	Quadword	R11	
FFA8h	Quadword	R10	
FFB0h	Quadword	R9	
FFB8h	Quadword	R8	
FFC0h	Quadword	RDI	Read-write
FFC8h	Quadword	RSI	
FFD0h	Quadword	RBP	
FFD8h	Quadword	RSP	
FFE0h	Quadword	RBX	
FFE8h	Quadword	RDX	
FFF0h	Quadword	RCX	
FFF8h	Quadword	RAX	
Notes: 1. This notation specifies that bit[47] is replicated in each of the 16 MSBs of the DW (sometimes called sign extended). The 16 LSBs contain bits[47:32]. 2. Only used for an SMI in guest mode with nested paging enabled.			

The SMI save state includes most of the integer execution unit. Not included in the save state are: the floating-point state, MSRs, and CR2. In order to be used by the SMI handler, these must be saved and restored. The save state is the same, regardless of the operating mode (32-bit or 64-bit).

2.1.10.1.6 System Management State

The following are offsets in the SMM save state area.

SMMxFEC0 [SMM IO Trap Offset] (Core::X86::Smm::TrapOffset)

Read-only, Volatile. Reset: 0000_0000h.

If the assertion of SMI is recognized on the boundary of an IO instruction, Core::X86::Smm::TrapOffset contains information about that IO instruction. For example, if an IO access targets an unavailable device, the system can assert SMI and trap the IO instruction. Core::X86::Smm::TrapOffset then provides the SMI handler with information about the IO instruction that caused the trap. After the SMI handler takes the appropriate action, it can reconstruct and then re-execute the IO instruction from SMM. Or, more likely, it can use Core::X86::Smm::IoRestart to cause the core to re-execute the IO instruction immediately after resuming from SMM.

Bits	Description
31:16	Port: trapped IO port address. Read-only, Volatile. Reset: 0000h. This provides the address of the IO instruction.
15:12	BPR: IO breakpoint match. Read-only, Volatile. Reset: 0h.
11	TF: EFLAGS TF value. Read-only, Volatile. Reset: 0.
10:7	Reserved.
6	SZ32: size 32 bits. Read-only, Volatile. Reset: 0. 1=Port access was 32 bits.
5	SZ16: size 16 bits. Read-only, Volatile. Reset: 0. 1=Port access was 16 bits.
4	SZ8: size 8 bits. Read-only, Volatile. Reset: 0. 1=Port access was 8 bits.
3	REP: repeated port access. Read-only, Volatile. Reset: 0.
2	STR: string-based port access. Read-only, Volatile. Reset: 0.
1	V: IO trap word valid. Read-only, Volatile. Reset: 0. 0=The other fields of this offset are not valid. 1=The core entered SMM on an IO instruction boundary; all information in this offset is valid.
0	RW: port access type. Read-only, Volatile. Reset: 0. 0=IO Write (OUT instruction). 1=IO Read (IN instruction).

SMMxFEC4 [Local SMI Status] (Core::X86::Smm::LocalSmiStatus)

Read-only, Volatile. Reset: 0000_0000h.

This offset stores status bits associated with SMI sources local to the core. For each of these bits, 1=The associated mechanism generated an SMI.

Bits	Description
31:9	Reserved.
8	MceRedirSts: machine check exception redirection status. Read-only, Volatile. Reset: 0. This bit is associated with the SMI source specified in Core::X86::Msr::McExcepRedir[RedirSmiEn].
7:4	Reserved.
3:0	IoTrapSts: IO trap status. Read-only, Volatile. Reset: 0h. Each of these bits is associated with each of the respective SMI sources specified in Core::X86::Msr::SMI_ON_IO_TRAP.

SMMxFEC8 [IO Restart Byte] (Core::X86::Smm::IoRestart)

Read-write. Reset: 00h.

If the core entered SMM on an IO instruction boundary, the SMI handler may write this to FFh. This causes the core to re-execute the trapped IO instruction immediately after resuming from SMM. The SMI handler should only write to this byte if Core::X86::Smm::TrapOffset[V] == 1; otherwise, the behavior is undefined.

If a second SMI is asserted while a valid IO instruction is trapped by the first SMI handler, the core services the second SMI prior to re-executing the trapped IO instruction. Core::X86::Smm::TrapOffset[V] == 0 during the second entry into SMM, and the second SMI handler must not rewrite this byte.

If there is a simultaneous SMI IO instruction trap and debug breakpoint trap, the processor first responds to the SMI and postpones recognizing the debug exception until after resuming from SMM. If debug registers other than DR6 and DR7 are used while in SMM, they must be saved and restored by the SMI handler. If Core::X86::Smm::IoRestart is set to FFh when the RSM instruction is executed, the debug trap does not occur until after the IO instruction is re-executed.

Bits	Description
7:0	RST: SMM IO Restart Byte. Read-write. Reset: 00h.

SMMxFEC9 [Auto Halt Restart Offset] (Core::X86::Smm::AutoHalt)

Read-write. Reset: 00h.

Bits	Description
7:1	Reserved.
0	HLT: halt restart. Read-write. Reset: 0. 0=Entered SMM on a normal x86 instruction boundary. 1=Entered SMM from the Halt state. Upon SMM entry, this bit indicates whether SMM was entered from the Halt state. Before returning from SMM, this bit can be written by the SMI handler to specify whether the return from SMM should take the processor back to the Halt state or to the instruction-execution state specified by the SMM state save area (normally, the instruction after the halt). Clearing this bit the returns to the instruction specified in the SMM save state. Setting this bit returns to the halt state. If the return from SMM takes the processor back to the Halt state, the HLT instruction is not refetched and re-executed. However, the Halt special bus cycle is broadcast and the processor enters the Halt state.

SMMxFECA [NMI Mask] (Core::X86::Smm::NmiMask)

Read-write. Reset: 00h.

Bits	Description
7:1	Reserved.
0	NmiMask: NMI Mask. Read-write. Reset: 0. 0=NMI not masked. 1=NMI masked. Specifies whether NMI was masked upon entry to SMM.

SMMxFED8 [SMM SVM State] (Core::X86::Smm::SvmState)

Read-only, Volatile. Reset: 0000_0000_0000_0000h.

This offset stores the SVM state of the processor upon entry into SMM.

Bits	Description														
63:4	Reserved.														
3	HostEflagsIF: host EFLAGS IF. Read-only, Volatile. Reset: 0.														
2:0	SvmState. Read-only, Volatile. Reset: 0h. ValidValues:														
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>SMM entered from a non-guest state.</td></tr> <tr> <td>1h</td><td>Reserved.</td></tr> <tr> <td>2h</td><td>SMM entered from a guest state.</td></tr> <tr> <td>5h-3h</td><td>Reserved.</td></tr> <tr> <td>6h</td><td>SMM entered from a guest state with nested paging enabled.</td></tr> <tr> <td>7h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	SMM entered from a non-guest state.	1h	Reserved.	2h	SMM entered from a guest state.	5h-3h	Reserved.	6h	SMM entered from a guest state with nested paging enabled.	7h	Reserved.
Value	Description														
0h	SMM entered from a non-guest state.														
1h	Reserved.														
2h	SMM entered from a guest state.														
5h-3h	Reserved.														
6h	SMM entered from a guest state with nested paging enabled.														
7h	Reserved.														

SMMxFEFC [SMM Revision Identifier] (Core::X86::Smm::SmmRevID)

Read-only. Reset: 0003_0064h.

This offset stores the SVM state of the processor upon entry into SMM.

Bits	Description
31:18	Reserved.
17	BRL. Read-only. Reset: 1. 1=Base relocation supported.
16	IOTrap. Read-only. Reset: 1. 1=IO trap supported.
15:0	Revision. Read-only. Reset: 0064h.

SMMxFE00 [SMM Base Address] (Core::X86::Smm::SmmBase)	
Read-write, Volatile. Reset: 0000_0000_0000_0000h.	
This offset stores the base of the SMM-State of the processor upon entry into SMM.	
Bits	Description
63:32	Reserved.
31:0	SmmBase. Read-write, Volatile. Reset: 0000_0000h. See Core::X86::Msr::SMM_BASE[SmmBase].

2.1.10.1.7 Exceptions and Interrupts in SMM

When SMM is entered, the core masks INTR, NMI, SMI, and INIT interrupts. The core clears the IF flag to disable INTR interrupts. To enable INTR interrupts within SMM, the SMM handler must set the IF flag to 1.

Generating an INTR interrupt can be used for unmasking NMI interrupts in SMM. The core recognizes the assertion of NMI within SMM immediately after the completion of an IRET instruction. Once NMI is recognized within SMM, NMI recognition remains enabled until SMM is exited, at which point NMI masking is restored to the state it was in before entering SMM.

While in SMM, the core responds to STPCLK interrupts, as well as to all exceptions that may be caused by the SMI handler.

2.1.10.1.8 The Protected ASeg and TSeg Areas

These ranges are controlled by Core::X86::Msr::SMMAddr and Core::X86::Msr::SMMMask; see those registers for details.

2.1.10.1.9 SMM Special Cycles

Special cycles can be initiated on entry and exit from SMM to acknowledge to the system that these transitions are occurring. These are controlled by Core::X86::Msr::HWCR[RsmSpCycDis, SmiSpCycDis].

2.1.10.1.10 Locking SMM

The SMM registers (Core::X86::Msr::SMMAddr and Core::X86::Msr::SMMMask) can be locked from being altered by setting Core::X86::Msr::HWCR[SmmLock]. SBIOS must lock the SMM registers after initialization to prevent unexpected changes to these registers.

2.1.10.1.11 SMM Page Configuration Lock

The SMM Page Configuration Lock feature allows SMM handler code to lock the paging configuration. Once locked, the paging configuration cannot be modified until RSM completes.

Core::X86::CpuId::FeatureExt2Eax[SmmPgCfgLock] Specifies SMM page configuration locking is supported.

Core::X86::Msr::HWCR[SmmPgCfgLock] locks registers related to page configuration. If not in SMM mode, Error-on-write-1. Cleared on RSM instruction.

If Core::X86::Msr::HWCR[SmmPgCfgLock], WRMSR of Core::X86::Msr::EFER results in an error.

If Core::X86::Msr::HWCR[SmmPgCfgLock], MOV CR0, CR3 and CR4 instructions result in an error.

2.1.10.2 Local APIC

The processor supports the APIC interrupt controller and the X2APIC interrupt controllers.

See 2.1.10.2.2 [Local APIC Registers] for the APIC registers and Core::X86::Msr::APIC_ID through

Core::X86::Msr::ExtendedInterruptLvtEntries for the X2APIC registers.

2.1.10.2.1 Local APIC Functional Description

The local APIC contains logic to receive interrupts from a variety of sources and to send interrupts to other local APICs, as well as registers to control its behavior and report status. Interrupts can be received from:

- IO devices including the IO hub (IO APICs)
- Other local APICs (inter-processor interrupts)
- APIC timer
- Thermal events
- Performance counters
- Legacy local interrupts from the IO hub (INTR and NMI)
- APIC internal errors

The APIC timer, thermal events, performance counters, local interrupts, and internal errors are all considered local interrupt sources, and their routing is controlled by local vector table entries. These entries assign a message type and vector to each interrupt, allow them to be masked, and track the status of the interrupt.

IO and inter-processor interrupts have their message type and vector assigned at the source and are unaltered by the local APIC. They carry a destination field and a mode bit that together determine which local APIC(s) accepts them. The destination mode (DM) bit specifies if the interrupt request packet should be handled in physical or logical destination mode.

2.1.10.2.1.1 Detecting and Enabling

The presence of APIC is detected via Core::X86::Cpuid::FeatureIdEdx[APIC], and the presence of X2APIC is detected via Core::X86::Cpuid::FeatureIdEcX[X2APIC].

The local APIC is enabled via Core::X86::Msr::APIC_BAR[ApicEn]. The X2APIC is enabled via Core::X86::Msr::APIC_BAR[x2ApicEn]. Reset forces the APIC and X2APIC disabled.

2.1.10.2.1.2 APIC Register Space

MMIO APIC space:

- Memory mapped to a 4-KB range. The memory type of this space is the UC memory type. The base address of this range is specified by {Core::X86::Msr::APIC_BAR[ApicBar[47:12]],000h}.
- The mnemonic is defined to be APICxXXX; where XXX is the byte address offset from the base address starting with APICx020 through APICx530 (Core::X86::Apic::ApicId - Core::X86::Apic::ExtendedInterruptLvtEntries).
- Treated as normal memory space when APIC is disabled, as specified by Core::X86::Msr::APIC_BAR[ApicEn].

MSR X2APIC space:

- The local APIC register space in x2APIC mode.
- MMIO APIC registers in x2APIC mode is defined by the register from MSR0000_0802 to MSR0000_08[53:50] (Core::X86::Msr::APIC_ID through Core::X86::Msr::ExtendedInterruptLvtEntries).
- If (Core::X86::Msr::APIC_BAR[x2ApicEn] == 0) then GP-read-write.
- RDMSR/WRMSR will occur in program order.

2.1.10.2.1.3 ApicId Enumeration Requirements

Note: Family 19h processors do not require contiguous ApicId assignments.

Operating systems are expected to use Core::X86::Cpuid::SizeId[ApicIdSize], the number of least significant bits in the Initial APIC ID that indicate core ID within a processor, in constructing per-core CPUID

masks. Core::X86::Cpuid::SizeId[ApicIdSize] determines the maximum number of cores (MNC) that the processor could theoretically support, not the actual number of cores that are actually implemented or enabled on the processor, as indicated by Core::X86::Cpuid::SizeId[NC].

2.1.10.2.1.4 Physical Destination Mode

The interrupt is only accepted by the local APIC whose Core::X86::Apic::ApicId[ApicId] matches the destination field of the interrupt. Physical mode allows up to 255 APICs to be addressed individually.

2.1.10.2.1.5 Logical Destination Mode

A local APIC accepts interrupts selected by Core::X86::Apic::LocalDestination and the destination field of the interrupt using either cluster or flat format as configured by Core::X86::Apic::DestinationFormat[Format].

If flat destinations are in use, bits[7:0] of Core::X86::Apic::LocalDestination[Destination] are checked against bits[7:0] of the arriving interrupt's destination field. If any bit position is set in both fields, the local APIC is a valid destination. Flat format allows up to 8 APICs to be addressed individually.

If cluster destinations are in use, bits[7:4] of Core::X86::Apic::LocalDestination[Destination] are checked against bits[7:4] of the arriving interrupt's destination field to identify the cluster. If all of bits[7:4] match, then bits[3:0] of Core::X86::Apic::LocalDestination[Destination] and the interrupt destination are checked for any bit positions that are set in both fields to identify processors within the cluster. If both conditions are met, the local APIC is a valid destination. Cluster format allows 15 clusters of 4 APICs each to be addressed.

2.1.10.2.1.6 Interrupt Delivery

SMI, NMI, INIT, Startup, and External interrupts are classified as non-vectored interrupts.

When an APIC accepts a non-vectored interrupt, it is handled directly by the processor instead of being queued in the APIC. When an APIC accepts a fixed or lowest-priority interrupt, it sets the bit in Core::X86::Apic::InterruptRequest corresponding to the vector in the interrupt. For local interrupt sources, this comes from the vector field in that interrupt's local vector table entry. The corresponding bit in Core::X86::Apic::TriggerMode is set if the interrupt is level-triggered and cleared if edge-triggered. If a subsequent interrupt with the same vector arrives when the corresponding bit in Core::X86::Apic::InterruptRequest[RequestBits] is already set, the two interrupts are collapsed into one. Vectors[15:0] are Reserved.

2.1.10.2.1.7 Vectored Interrupt Handling

Core::X86::Apic::TaskPriority and Core::X86::Apic::ProcessorPriority each contain an 8-bit priority divided into a main priority (bits[7:4]) and a priority sub-class (bits[3:0]). The task priority is assigned by software to set a threshold priority at which the processor is interrupted.

The processor priority is calculated by comparing the main priority (bits[7:4]) of Core::X86::Apic::TaskPriority[Priority] to bits[7:4] of the 8-bit encoded value of the highest bit set in Core::X86::Apic::InService. The processor priority is the higher of the two main priorities.

The processor priority is used to determine if any accepted interrupts (indicated by Core::X86::Apic::InterruptRequest[RequestBits]) are high enough priority to be serviced by the processor. When the processor is ready to service an interrupt, the highest bit in Core::X86::Apic::InterruptRequest[RequestBits] is cleared, and the corresponding bit is set in Core::X86::Apic::InService[InServiceBits].

When the processor has completed service for an interrupt, it performs a Write to Core::X86::Apic::EndOfInterrupt, clearing the highest bit in Core::X86::Apic::InService[InServiceBits] and causing the next-highest interrupt to be serviced. If the corresponding bit in Core::X86::Apic::TriggerMode[TriggerModeBits] is set, a Write to Core::X86::Apic::EndOfInterrupt is performed on all APICs to complete service of the interrupt at the source.

2.1.10.2.1.8 Interrupt Masking

Interrupt masking is controlled by the Core::X86::Apic::ExtendedApicControl. If Core::X86::Apic::ExtendedApicControl[IerEn] is set, Core::X86::Apic::InterruptEnable are used to mask interrupts. Any bit in Core::X86::Apic::InterruptEnable[InterruptEnableBits] that is clear indicates the corresponding interrupt is masked. A masked interrupt is not serviced and the corresponding bit in Core::X86::Apic::InterruptRequest[RequestBits] remains set.

2.1.10.2.1.9 Spurious Interrupts

In the event that the task priority is set to or above the level of the interrupt to be serviced, the local APIC delivers a spurious interrupt vector to the processor, as specified by Core::X86::Apic::SpuriousInterruptVector. Core::X86::Apic::InService is not changed and no Write to Core::X86::Apic::EndOfInterrupt occurs.

2.1.10.2.1.10 Spurious Interrupts Caused by Timer Tick Interrupt

A typical interrupt is asserted until it is serviced. An interrupt is de-asserted when software clears the interrupt status bit within the interrupt service routine. Timer tick interrupt is an exception since it is de-asserted regardless of whether it is serviced or not.

The processor is not always able to service interrupts immediately (i.e., when interrupts are masked by clearing EFLAGS.IM).

If the processor is not able to service the timer tick interrupt for an extended period of time, the INTR caused by the first timer tick interrupt asserted during that time is delivered to the local APIC in ExtInt mode and latched, and the subsequent timer tick interrupts are lost. The following cases are possible when the processor is ready to service interrupts:

- An ExtInt interrupt is pending, and INTR is asserted. This results in timer tick interrupt servicing. This occurs 50 percent of the time.
- An ExtInt interrupt is pending, and INTR is de-asserted. The processor sends the interrupt acknowledge cycle, but when the PIC receives it, INTR is de-asserted, and the PIC sends a spurious interrupt vector. This occurs 50 percent of the time.

There is a 50 percent probability of spurious interrupts to the processor.

2.1.10.2.1.11 Lowest-Priority Interrupt Arbitration

Fixed and non-vectored interrupts are accepted by their destination APICs without arbitration.

Delivery of lowest-priority interrupts requires all APICs to arbitrate to determine which one accepts the interrupt. If Core::X86::Apic::SpuriousInterruptVector[FocusDisable] is clear, then the focus processor for an interrupt always accepts the interrupt. A processor is the focus of an interrupt if it is already servicing that interrupt (corresponding bit in Core::X86::Apic::InService[InServiceBits] is set) or if it already has a pending request for that interrupt (corresponding bit in Core::X86::Apic::InterruptRequest[RequestBits] is set). If Core::X86::Apic::ExtendedApicControl[IerEn] is set, the interrupt must also be enabled in Core::X86::Apic::InterruptEnable[InterruptEnableBits] for a processor to be the focus processor. If there is no focus processor for an interrupt, or focus processor checking is disabled, then each APIC calculates an arbitration priority value, stored in Core::X86::Apic::ArbitrationPriority, and the one with the lowest result

accepts the interrupt.

The arbitration priority value is calculated by comparing Core::X86::Apic::TaskPriority[Priority] with the 8-bit encoded value of the highest bit set in Core::X86::Apic::InterruptRequest[RequestBits] (IRRVec) and the 8-bit encoded value of the highest bit set Core::X86::Apic::InService[InServiceBits] (ISRVec). If Core::X86::Apic::ExtendedApicControl[IerEn] is set the IRRVec and ISRVec are based off the highest enabled interrupt. The main priority bits[7:4] are compared as follows:

```
if ((TaskPriority[Priority[7:4]] >= InterruptRequest[IRRVec[7:4]])
&&(TaskPriority[Priority[7:4]] > InService[ISRVec[7:4]]) {
ArbitrationPriority[Priority] = TaskPriority[Priority]
} elseif { (InterruptRequest[IRRVec[7:4]] > InService[ISRVec[7:4]])
ArbitrationPriority[Priority] = {InterruptRequest[IRRVec[7:4]], 0h}
} else {
ArbitrationPriority[Priority] = {InService[ISRVec[7:4]], 0h}
}
```

2.1.10.2.1.12 Inter-Processor Interrupts

The Core::X86::Apic::InterruptCommandLow and Core::X86::Apic::InterruptCommandHigh provide a mechanism for generating interrupts in order to redirect an interrupt to another processor, originate an interrupt to another processor, or allow a processor to interrupt itself. A Write to register Core::X86::Apic::InterruptCommandLow causes an interrupt to be generated with the properties specified by the Core::X86::Apic::InterruptCommandLow and Core::X86::Apic::InterruptCommandHigh fields.

Message type (bits[10:8]) == 011b (Remote Read) is deprecated.

Not all combinations of ICR fields are valid. Only the following combinations are valid:

Note: x indicates a don't care.

Table 17: ICR Valid Combinations

Message Type	Trigger Mode	Level	Destination Shorthand
Fixed	Edge	x	x
	Level	Assert	x
Lowest Priority, SMI, NMI, INIT	Edge	x	Destination or all excluding self
	Level	Assert	Destination or all excluding self
Startup	x	x	Destination or all excluding self

2.1.10.2.1.13 APIC Timer Operation

The local APIC contains a 32-bit timer, controlled by Core::X86::Apic::TimerLvtEntry, Core::X86::Apic::TimerInitialCount, and Core::X86::Apic::TimerDivideConfiguration. The processor bus clock is divided by the value in Core::X86::Apic::TimerDivideConfiguration[Div[3:0]] to obtain a time base for the timer. When Core::X86::Apic::TimerInitialCount[Count] is written, the value is copied into Core::X86::Apic::TimerCurrentCount. Core::X86::Apic::TimerCurrentCount[Count] is decremented at the rate of the divided clock. When the count reaches 0, a timer interrupt is generated with the vector specified in Core::X86::Apic::TimerLvtEntry[Vector]. If Core::X86::Apic::TimerLvtEntry[Mode] specifies periodic operation, Core::X86::Apic::TimerCurrentCount[Count] is reloaded with the Core::X86::Apic::TimerInitialCount[Count] value, and it continues to decrement at the rate of the

divided clock. If Core::X86::Apic::TimerLvtEntry[Mask] is set, timer interrupts are not generated.

2.1.10.2.1.14 Generalized Local Vector Table

All LVTs (Core::X86::Apic::ThermalLvtEntry to Core::X86::Apic::LVTINT, and Core::X86::Apic::ExtendedInterruptLvtEntries) support a generalized message type as follows:

- 000b=Fixed
- 010b=SMI
- 100b=NMI
- 111b=ExtINT
- All other messages types are Reserved.

2.1.10.2.1.15 State at Reset

At power-up or reset, the APIC is hardware disabled (Core::X86::Msr::APIC_BAR[ApicEn] == 0) so only SMI, NMI, INIT, and ExtInt interrupts may be accepted.

The APIC can be software disabled through Core::X86::Apic::SpuriousInterruptVector[APICSWEn]. The software disable has no effect when the APIC is hardware disabled.

When a processor accepts an INIT interrupt, the APIC is reset as at power-up, with the exception that:

- Core::X86::Apic::ApicId is unaffected.
- Pending APIC register writes complete.

2.1.10.2.2 Local APIC Registers

APICx020 [APIC ID] (Core::X86::Apic::ApicId)	
Read-only.	
_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; APICx020; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}	
Bits	Description
31:24	ApicId: APIC ID. Read-only. Reset: XXh. The reset value varies based on core number. See 2.1.10.2.1.3 [ApicId Enumeration Requirements].
23:0	Reserved.
APICx030 [APIC Version] (Core::X86::Apic::ApicVersion)	
Read-only.	
_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; APICx030; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}	
Bits	Description
31	ExtApicSpace: extended APIC register space present. Read-only. Reset: 1. 1=Indicates the presence of extended APIC register space starting at Core::X86::Apic::ExtendedApicFeature.
30:25	Reserved.
24	DirectedEoiSupport: directed EOI support. Read-only. Reset: Fixed,1. 0=Directed EOI capability not supported.
23:16	MaxLvtEntry. Read-only. Reset: XXh. Specifies the number of entries in the local vector table minus one.
15:8	Reserved.
7:0	Version. Read-only. Reset: 10h. Indicates the version number of this APIC implementation.

APICx080 [Task Priority] (Core::X86::Apic::TaskPriority)

Read-write. Reset: 0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; APICx080; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}

Bits	Description
31:8	Reserved.
7:0	Priority. Read-write. Reset: 00h. This field is assigned by software to set a threshold priority at which the core is interrupted.

APICx090 [Arbitration Priority] (Core::X86::Apic::ArbitrationPriority)

Read-only, Volatile. Reset: 0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; APICx090; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}

Bits	Description
31:8	Reserved.
7:0	Priority. Read-only, Volatile. Reset: 00h. Indicates the current priority for a pending interrupt, or a task or interrupt being serviced by the core. The priority is used to arbitrate between cores to determine which accepts a lowest-priority interrupt request.

APICx0A0 [Processor Priority] (Core::X86::Apic::ProcessorPriority)

Read-only, Volatile. Reset: 0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; APICx0A0; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}

Bits	Description
31:8	Reserved.
7:0	Priority. Read-only, Volatile. Reset: 00h. Indicates the core's current priority servicing a task or interrupt, and is used to determine if any pending interrupts should be serviced. It is the higher value of the task priority value and the current highest in-service interrupt.

APICx0B0 [End of Interrupt] (Core::X86::Apic::EndOfInterrupt)

Write-only.

This register is written by the software interrupt handler to indicate the servicing of the current interrupt is complete.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; APICx0B0; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}

Bits	Description
31:0	Reserved.

APICx0C0 [Reserved] (Core::X86::Apic::RemoteRead)

Read-only. Reset: 0000_0000h.

Remote Read is deprecated.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; APICx0C0; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}

Bits	Description
31:0	Reserved.

APICx0D0 [Logical Destination] (Core::X86::Apic::LocalDestination)

Read-write, Volatile. Reset: 0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; APICx0D0; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}

Bits	Description
31:24	Destination. Read-write, Volatile. Reset: 00h. This APIC's destination identification. Used to determine which interrupts should be accepted.
23:0	Reserved.

APICx0E0 [Destination Format] (Core::X86::Apic::DestinationFormat)

Read-write. Reset: F000_0000h.

Only supported in xAPIC mode.

`_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; APICx0E0; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}`

Bits	Description								
31:28	Format. Read-write. Reset: Fh. Controls which format to use when accepting interrupts with a logical destination mode. ValidValues:								
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>Cluster destinations are used.</td></tr> <tr> <td>Eh-1h</td><td>Reserved.</td></tr> <tr> <td>Fh</td><td>Flat destinations are used.</td></tr> </table>	Value	Description	0h	Cluster destinations are used.	Eh-1h	Reserved.	Fh	Flat destinations are used.
Value	Description								
0h	Cluster destinations are used.								
Eh-1h	Reserved.								
Fh	Flat destinations are used.								
27:0	Reserved.								

APICx0F0 [Spurious-Interrupt Vector] (Core::X86::Apic::SpuriousInterruptVector)

Reset: 0000_00FFh.

`_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; APICx0F0; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}`

Bits	Description
31:10	Reserved.
9	FocusDisable. Read-write. Reset: 0. 1=Disable focus core checking during lowest-priority arbitrated interrupts.
8	APICSWEn: APIC software enable. Read-write, Volatile. Reset: 0. 0=SMI, NMI, INIT, LINT[1:0], and Startup interrupts may be accepted; pending interrupts in Core::X86::Apic::InService and Core::X86::Apic::InterruptRequest are held, but further fixed, lowest-priority, and ExtInt interrupts are not accepted. All LVT entry mask bits are set and cannot be cleared.
7:0	Vector. Read-write, Volatile. Reset: FFh. The vector that is sent to the core in the event of a spurious interrupt.

APICx1[0...7]0 [In-Service] (Core::X86::Apic::InService)

Read-only, Volatile. Reset: 0000_0000h.

The in-service registers provide a bit per interrupt to indicate that the corresponding interrupt is being serviced by the core. The first 16 InServiceBits of the first Core::X86::Apic::InService register are Reserved.

`_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n0; APICx100; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}``_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n1; APICx110; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}``_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n2; APICx120; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}``_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n3; APICx130; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}``_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n4; APICx140; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}``_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n5; APICx150; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}``_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n6; APICx160; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}``_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n7; APICx170; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}`

Bits	Description
31:0	InServiceBits. Read-only, Volatile. Reset: 0000_0000h. These bits are set when the corresponding interrupt is being serviced by the core.

APICx1[8...F]0 [Trigger Mode] (Core::X86::Apic::TriggerMode)

Read-only, Volatile. Reset: 0000_0000h.

The trigger mode registers provide a bit per interrupt to indicate the assertion mode of each interrupt. The first 16 TriggerModeBits of the each thread's APIC[1F0:180] registers are Reserved.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n0; APICx180; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n1; APICx190; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n2; APICx1A0; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n3; APICx1B0; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n4; APICx1C0; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n5; APICx1D0; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n6; APICx1E0; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n7; APICx1F0; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}

Bits	Description
31:0	TriggerModeBits. Read-only, Volatile. Reset: 0000_0000h. The corresponding trigger mode bit is updated when an interrupt is accepted. 1=Level-triggered interrupt. 0=Edge-triggered interrupt. ValidValues: See: Core::X86::Apic::TriggerMode[TriggerModeBits] Valid Values.

Core::X86::Apic::TriggerMode[TriggerModeBits] Valid Values

Bit	Description
[0]	0=Edge-triggered interrupt. 1=Level-triggered interrupt.
[1]	0=Edge-triggered interrupt. 1=Level-triggered interrupt.
[2]	0=Edge-triggered interrupt. 1=Level-triggered interrupt.
[3]	0=Edge-triggered interrupt. 1=Level-triggered interrupt.
[4]	0=Edge-triggered interrupt. 1=Level-triggered interrupt.
[5]	0=Edge-triggered interrupt. 1=Level-triggered interrupt.
[6]	0=Edge-triggered interrupt. 1=Level-triggered interrupt.
[7]	0=Edge-triggered interrupt. 1=Level-triggered interrupt.
[8]	0=Edge-triggered interrupt. 1=Level-triggered interrupt.
[9]	0=Edge-triggered interrupt. 1=Level-triggered interrupt.
[10]	0=Edge-triggered interrupt. 1=Level-triggered interrupt.
[11]	0=Edge-triggered interrupt. 1=Level-triggered interrupt.
[12]	0=Edge-triggered interrupt. 1=Level-triggered interrupt.
[13]	0=Edge-triggered interrupt. 1=Level-triggered interrupt.
[14]	0=Edge-triggered interrupt. 1=Level-triggered interrupt.
[15]	0=Edge-triggered interrupt. 1=Level-triggered interrupt.
[16]	0=Edge-triggered interrupt. 1=Level-triggered interrupt.
[17]	0=Edge-triggered interrupt. 1=Level-triggered interrupt.
[18]	0=Edge-triggered interrupt. 1=Level-triggered interrupt.
[19]	0=Edge-triggered interrupt. 1=Level-triggered interrupt.
[20]	0=Edge-triggered interrupt. 1=Level-triggered interrupt.
[21]	0=Edge-triggered interrupt. 1=Level-triggered interrupt.
[22]	0=Edge-triggered interrupt. 1=Level-triggered interrupt.
[23]	0=Edge-triggered interrupt. 1=Level-triggered interrupt.
[24]	0=Edge-triggered interrupt. 1=Level-triggered interrupt.
[25]	0=Edge-triggered interrupt. 1=Level-triggered interrupt.
[26]	0=Edge-triggered interrupt. 1=Level-triggered interrupt.
[27]	0=Edge-triggered interrupt. 1=Level-triggered interrupt.
[28]	0=Edge-triggered interrupt. 1=Level-triggered interrupt.
[29]	0=Edge-triggered interrupt. 1=Level-triggered interrupt.
[30]	0=Edge-triggered interrupt. 1=Level-triggered interrupt.

[31]	0=Edge-triggered interrupt. 1=Level-triggered interrupt.
APICx2[0...7]0 [Interrupt Request] (Core::X86::Apic::InterruptRequest)	
Read-only. Reset: 0000_0000h.	
The interrupt request registers provide a bit per interrupt to indicate that the corresponding interrupt has been accepted by the APIC. The first 16 RequestBits of the first Core::X86::Apic::InterruptRequest register are Reserved.	
_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n0; APICx200; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}	
_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n1; APICx210; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}	
_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n2; APICx220; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}	
_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n3; APICx230; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}	
_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n4; APICx240; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}	
_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n5; APICx250; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}	
_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n6; APICx260; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}	
_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n7; APICx270; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}	
Bits	Description
31:0	RequestBits. Read-only. Reset: 0000_0000h. The corresponding request bit is set when the an interrupt is accepted by the APIC.
	ValidValues: See: Core::X86::Apic::InterruptRequest[RequestBits] Valid Values.

Core::X86::Apic::InterruptRequest[RequestBits] Valid Values

Bit	Description
[0]	0=Request bit not set. 1=Request bit set.
[1]	0=Request bit not set. 1=Request bit set.
[2]	0=Request bit not set. 1=Request bit set.
[3]	0=Request bit not set. 1=Request bit set.
[4]	0=Request bit not set. 1=Request bit set.
[5]	0=Request bit not set. 1=Request bit set.
[6]	0=Request bit not set. 1=Request bit set.
[7]	0=Request bit not set. 1=Request bit set.
[8]	0=Request bit not set. 1=Request bit set.
[9]	0=Request bit not set. 1=Request bit set.
[10]	0=Request bit not set. 1=Request bit set.
[11]	0=Request bit not set. 1=Request bit set.
[12]	0=Request bit not set. 1=Request bit set.
[13]	0=Request bit not set. 1=Request bit set.
[14]	0=Request bit not set. 1=Request bit set.
[15]	0=Request bit not set. 1=Request bit set.
[16]	0=Request bit not set. 1=Request bit set.
[17]	0=Request bit not set. 1=Request bit set.
[18]	0=Request bit not set. 1=Request bit set.
[19]	0=Request bit not set. 1=Request bit set.
[20]	0=Request bit not set. 1=Request bit set.
[21]	0=Request bit not set. 1=Request bit set.
[22]	0=Request bit not set. 1=Request bit set.
[23]	0=Request bit not set. 1=Request bit set.
[24]	0=Request bit not set. 1=Request bit set.
[25]	0=Request bit not set. 1=Request bit set.
[26]	0=Request bit not set. 1=Request bit set.
[27]	0=Request bit not set. 1=Request bit set.
[28]	0=Request bit not set. 1=Request bit set.
[29]	0=Request bit not set. 1=Request bit set.

[30]	0=Request bit not set. 1=Request bit set.
[31]	0=Request bit not set. 1=Request bit set.

APICx280 [Error Status] (Core::X86::Apic::ErrorStatus)

Writes to this register trigger an update of the register state. The value written by software is arbitrary. Each write causes the internal error state to be loaded into this register, clearing the internal error state. Consequently, a second write prior to the occurrence of another error causes the register to be overwritten with cleared data.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; APICx280; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}

Bits	Description
31:8	Reserved.
7	IllegalRegAddr: illegal register address. Read-write. Reset: 0. This bit indicates that an access to a nonexistent register location within this APIC was attempted. Can only be set in xAPIC mode.
6	RcvdIllegalVector: received illegal vector. Read-write. Reset: 0. This bit indicates that this APIC has received a message with an illegal vector (00h to 0Fh for fixed and lowest priority interrupts).
5	SentIllegalVector. Read-write. Reset: 0. This bit indicates that this APIC attempted to send a message with an illegal vector (00h to 0Fh for fixed and lowest priority interrupts).
4	Reserved.
3	RcvAcceptError: receive accept error. Read-write. Reset: 0. This bit indicates that a message received by this APIC was not accepted by this or any other APIC.
2	SendAcceptError. Read-write. Reset: 0. This bit indicates that a message sent by this APIC was not accepted by any APIC.
1:0	Reserved.

APICx300 [Interrupt Command Low] (Core::X86::Apic::InterruptCommandLow)

Reset: 0000_0000h.																			
_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; APICx300; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}																			
Bits	Description																		
31:20	Reserved.																		
19:18	DestShrthnd: destination shorthand. Read-write. Reset: 0h. Description: Provides a quick way to specify a destination for a message. If all including self or all excluding self is used, then destination mode is ignored and physical is automatically used. ValidValues: <table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>No shorthand (Destination field).</td></tr> <tr> <td>1h</td><td>Self.</td></tr> <tr> <td>2h</td><td>All including self.</td></tr> <tr> <td>3h</td><td>All excluding self (This sends a message with a destination encoding of all 1s, so if lowest priority is used the message could end up being reflected back to this APIC).</td></tr> </table>	Value	Description	0h	No shorthand (Destination field).	1h	Self.	2h	All including self.	3h	All excluding self (This sends a message with a destination encoding of all 1s, so if lowest priority is used the message could end up being reflected back to this APIC).								
Value	Description																		
0h	No shorthand (Destination field).																		
1h	Self.																		
2h	All including self.																		
3h	All excluding self (This sends a message with a destination encoding of all 1s, so if lowest priority is used the message could end up being reflected back to this APIC).																		
17:16	RemoteRdStat. Read-only. Reset: 0h. ValidValues: <table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>Read was invalid.</td></tr> <tr> <td>1h</td><td>Delivery pending.</td></tr> <tr> <td>2h</td><td>Delivery complete and access was valid.</td></tr> <tr> <td>3h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	Read was invalid.	1h	Delivery pending.	2h	Delivery complete and access was valid.	3h	Reserved.								
Value	Description																		
0h	Read was invalid.																		
1h	Delivery pending.																		
2h	Delivery complete and access was valid.																		
3h	Reserved.																		
15	TM: trigger mode. Read-write. Reset: 0. 0=Edge triggered. 1=Level triggered. Indicates how this interrupt is triggered.																		
14	Level. Read-write. Reset: 0. 0=De-asserted. 1=Asserted.																		
13	Reserved.																		
12	DS: interrupt delivery status. Read-only. Reset: 0. 0=Idle. 1=Send pending. In xAPIC mode this bit is set to indicate that the interrupt has not yet been accepted by the destination core(s). Software may repeatedly write Core::X86::Apic::InterruptCommandLow without polling the DS bit; all requested IPIs are delivered.																		
11	DM: destination mode. Read-write. Reset: 0. 0=Physical. 1=Logical.																		
10:8	MsgType. Read-write. Reset: 0h. The message types are encoded as follows: ValidValues: <table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>Fixed.</td></tr> <tr> <td>1h</td><td>Lowest Priority.</td></tr> <tr> <td>2h</td><td>SMI.</td></tr> <tr> <td>3h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>NMI.</td></tr> <tr> <td>5h</td><td>INIT.</td></tr> <tr> <td>6h</td><td>Startup.</td></tr> <tr> <td>7h</td><td>External interrupt.</td></tr> </table>	Value	Description	0h	Fixed.	1h	Lowest Priority.	2h	SMI.	3h	Reserved.	4h	NMI.	5h	INIT.	6h	Startup.	7h	External interrupt.
Value	Description																		
0h	Fixed.																		
1h	Lowest Priority.																		
2h	SMI.																		
3h	Reserved.																		
4h	NMI.																		
5h	INIT.																		
6h	Startup.																		
7h	External interrupt.																		
7:0	Vector. Read-write. Reset: 00h. The vector that is sent for this interrupt source.																		

APICx310 [Interrupt Command High] (Core::X86::Apic::InterruptCommandHigh)

Read-write. Reset: 0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; APICx310; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}

Bits	Description
31:24	DestinationField. Read-write. Reset: 00h. The destination encoding used when Core::X86::Apic::InterruptCommandLow[DestShrthnd] is 00b.
23:0	Reserved.

APICx320 [LVT Timer] (Core::X86::Apic::TimerLvtEntry)

Reset: 0001_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; APICx320; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}

Bits	Description
31:18	Reserved.
17	Mode. Read-write. Reset: 0. 0=One-shot. 1=Periodic.
16	Mask. Read-write. Reset: 1. 0=Not masked. 1=Masked.
15:13	Reserved.
12	DS: interrupt delivery status. Read-only,Volatile. Reset: 0. 0=Idle. 1=Send pending. (Indicates that the interrupt has not yet been accepted by the core.)
11	Reserved.
10:8	MsgType: message type. Read-write. Reset: 0h. See 2.1.10.2.1.14 [Generalized Local Vector Table].
7:0	Vector. Read-write. Reset: 00h. Interrupt vector number.

APICx330 [LVT Thermal Sensor] (Core::X86::Apic::ThermalLvtEntry)

Reset: 0001_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; APICx330; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}

Bits	Description
31:17	Reserved.
16	Mask. Read-write. Reset: 1. 0=Not masked. 1=Masked.
15:13	Reserved.
12	DS: interrupt delivery status. Read-only,Volatile. Reset: 0. 0=Idle. 1=Send pending. (Indicates that the interrupt has not yet been accepted by the core.)
11	Reserved.
10:8	MsgType: message type. Read-write. Reset: 0h. See 2.1.10.2.1.14 [Generalized Local Vector Table].
7:0	Vector. Read-write. Reset: 00h. Interrupt vector number.

APICx340 [LVT Performance Monitor] (Core::X86::Apic::PerformanceCounterLvtEntry)

Reset: 0001_0000h.

Interrupts for this local vector table are caused by overflows of:

- Core::X86::Msr::PERF_LEGACY_CTL0..3(Performance Event Select [3:0]).
- Core::X86::Msr::PERF_CTL0..5(Performance Event Select [5:0]).

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; APICx340; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}

Bits	Description
31:17	Reserved.
16	Mask. Read-write. Reset: 1. 0=Not masked. 1=Masked.
15:13	Reserved.
12	DS: interrupt delivery status. Read-only,Volatile. Reset: 0. 0=Idle. 1=Send pending. (Indicates that the interrupt has not yet been accepted by the core.)
11	Reserved.
10:8	MsgType: message type. Read-write. Reset: 0h. See 2.1.10.2.1.14 [Generalized Local Vector Table].
7:0	Vector. Read-write. Reset: 00h. Interrupt vector number.

APICx3[5...6]0 [LVT LINT[1:0]] (Core::X86::Apic::LVTINT)

Reset: 0001_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n0; APICx350; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]], 000h}

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n1; APICx360; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]], 000h}

Bits	Description
31:17	Reserved.
16	Mask. Read-write. Reset: 1. 0=Not masked. 1=Masked.
15	TM: trigger mode. Read-write. Reset: 0. 0=Edge. 1=Level.
14	RmtIRR. Read-only, Volatile. Reset: 0. If trigger mode is level, remote Core::X86::Apic::InterruptRequest is set when the interrupt has begun service. Remote Core::X86::Apic::InterruptRequest is cleared when the end of interrupt has occurred.
13	Reserved.
12	DS: interrupt delivery status. Read-only, Volatile. Reset: 0. 0=Idle. 1=Send pending. (Indicates that the interrupt has not yet been accepted by the core.)
11	Reserved.
10:8	MsgType: message type. Read-write. Reset: 0h. See 2.1.10.2.1.14 [Generalized Local Vector Table].
7:0	Vector. Read-write. Reset: 00h. Interrupt vector number.

APICx370 [LVT Error] (Core::X86::Apic::ErrorLvtEntry)

Reset: 0001_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; APICx370; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]], 000h}

Bits	Description
31:17	Reserved.
16	Mask. Read-write. Reset: 1. 0=Not masked. 1=Masked.
15:13	Reserved.
12	DS: interrupt delivery status. Read-only, Volatile. Reset: 0. 0=Idle. 1=Send pending. (Indicates that the interrupt has not yet been accepted by the core.)
11	Reserved.
10:8	MsgType: message type. Read-write. Reset: 0h. See 2.1.10.2.1.14 [Generalized Local Vector Table].
7:0	Vector. Read-write. Reset: 00h. Interrupt vector number.

APICx380 [Timer Initial Count] (Core::X86::Apic::TimerInitialCount)

Read-write, Volatile. Reset: 0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; APICx380; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]], 000h}

Bits	Description
31:0	Count. Read-write, Volatile. Reset: 0000_0000h. The value copied into the current count register when the timer is loaded or reloaded.

APICx390 [Timer Current Count] (Core::X86::Apic::TimerCurrentCount)

Read-only, Volatile. Reset: 0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; APICx390; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]], 000h}

Bits	Description
31:0	Count. Read-only, Volatile. Reset: 0000_0000h. The current value of the counter.

APICx3E0 [Timer Divide Configuration] (Core::X86::Apic::TimerDivideConfiguration)

Read-write. Reset: 0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; APICx3E0; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}

Bits	Description
31:4	Reserved.
3:0	Div[3:0] . Read-write. Reset: 0h. Div[2] is unused.
	ValidValues:
Value	Description
0h	Divide by 2.
1h	Divide by 4.
2h	Divide by 8.
3h	Divide by 16.
7h-4h	Reserved.
8h	Divide by 32.
9h	Divide by 64.
Ah	Divide by 128.
Bh	Divide by 1.
Fh-Ch	Reserved.

APICx400 [Extended APIC Feature] (Core::X86::Apic::ExtendedApicFeature)

Read-only. Reset: 0004_0007h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; APICx400; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}

Bits	Description
31:24	Reserved.
23:16	ExtLvtCount: extended local vector table count . Read-only. Reset: 04h. This specifies the number of extended LVT registers (Core::X86::Apic::ExtendedInterruptLvtEntries) in the local APIC.
15:3	Reserved.
2	ExtApicIdCap: extended APIC ID capable . Read-only. Reset: 1. 1=The processor is capable of supporting an 8-bit APIC ID, as controlled by Core::X86::Apic::ExtendedApicControl[ExtApicIdEn].
1	SeoiCap: specific end of interrupt capable . Read-only. Reset: 1. 1=The Core::X86::Apic::SpecificEndOfInterrupt is present.
0	IerCap: interrupt enable register capable . Read-only. Reset: 1. This bit indicates that the Core::X86::Apic::InterruptEnable are present. See 2.1.10.2.1.8 [Interrupt Masking].

APICx410 [Extended APIC Control] (Core::X86::Apic::ExtendedApicControl)

Read-write. Reset: 0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; APICx410; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}

Bits	Description
31:3	Reserved.
2	ExtApicIdEn: extended APIC ID enable . Read-write. Reset: 0. 1=Enable 8-bit APIC ID; Core::X86::Apic::ApicId[ApicId] supports an 8-bit value; an interrupt broadcast in physical destination mode requires that the IntDest[7:0] == 1111_1111b (instead of XXXX_1111b); a match in physical destination mode occurs when (IntDest[7:0] == ApicId[7:0]) instead of (IntDest[3:0] == ApicId[3:0]).
1	SeoiEn . Read-write. Reset: 0. 1=Enable SEOI generation when a Write to Core::X86::Apic::SpecificEndOfInterrupt is received.
0	IerEn . Read-write. Reset: 0. 1=Enable writes to the interrupt enable registers.

APICx420 [Specific End Of Interrupt] (Core::X86::Apic::SpecificEndOfInterrupt)

Read-write. Reset: 0000_0000h.

`_ccd[1:0]_lthree0_core[7:0]_thread[1:0]`; APICx420; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}

Bits	Description
31:8	Reserved.
7:0	EoiVec: end of interrupt vector. Read-write. Reset: 00h. A Write to this field causes an end of interrupt cycle to be performed for the vector specified in this field. The behavior is undefined if no interrupt is pending for the specified interrupt vector.

APICx4[8...F]0 [Interrupt Enable] (Core::X86::Apic::InterruptEnable)

Read-write. Reset: FFFF_FFFFh.

`_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n0`; APICx480; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}`_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n1`; APICx490; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}`_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n2`; APICx4A0; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}`_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n3`; APICx4B0; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}`_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n4`; APICx4C0; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}`_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n5`; APICx4D0; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}`_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n6`; APICx4E0; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}`_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n7`; APICx4F0; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}

Bits	Description
31:0	InterruptEnableBits. Read-write. Reset: FFFF_FFFFh. The interrupt enable bits can be used to enable each of the 256 interrupts.

APICx5[0...3]0 [Extended Interrupt Local Vector Table] (Core::X86::Apic::ExtendedInterruptLvtEntries)

Reset: 0001_0000h.

Assignments conventions:

- APIC500 provides a local vector table entry for IBS.
- APIC510 provides a local vector table entry for error thresholding. See Core::X86::Msr::McaIntrCfg[ThresholdLvtOffset].
- APIC520 provides a local vector table entry for Deferred errors. See MCI_CONFIG[DeferredIntType].

`_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n0`; APICx500; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}`_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n1`; APICx510; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}`_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n2`; APICx520; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}`_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n3`; APICx530; APIC={Core::X86::Msr::APIC_BAR[ApicBar[47:12]] , 000h}

Bits	Description
31:17	Reserved.
16	Mask. Read-write. Reset: 1. 0=Not masked. 1=Masked.
15:13	Reserved.
12	DS: interrupt delivery status. Read-only, Volatile. Reset: 0. 0=Idle. 1=Send pending. (Indicates that the interrupt has not yet been accepted by the core.)
11	Reserved.
10:8	MsgType: message type. Read-write. Reset: 0h. See 2.1.10.2.1.14 [Generalized Local Vector Table].
7:0	Vector. Read-write. Reset: 00h. Interrupt vector number.

2.1.11 CPUID Instruction

Processor feature capabilities and configuration information are provided through the CPUID instruction. The information is accessed by (1) selecting the CPUID function setting EAX and optionally ECX for some functions, (2) executing the CPUID instruction, and (3) reading the results in the EAX, EBX, ECX, and EDX registers. The syntax CPUID FnXXXXXXXX_EiX[_xYYY] refers to the function where EAX == X, and optionally ECX == Y, and the registers specified by EiX. EiX can be any single register such as {EAX, EBX, ECX, and EDX}, or a range of registers, such as E[C,B,A]X. Undefined function numbers return 0's in all 4 registers.

Unless otherwise specified, single-bit feature fields are encoded as 1=Feature is supported by the processor; 0=Feature is

not supported by the processor. CPUID functions not listed are reserved.

2.1.11.1 CPUID Instruction Functions

The following provides processor specific details about CPUID.

CPUID_Fn00000000_EAX [Processor Vendor and Largest Standard Function Number] (Core::X86::Cpuid::LargFuncNum)	
Read-only. Reset: Fixed,0000_0010h.	
_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn00000000_EAX	
Bits	Description
31:0	LFuncStd: largest standard function. Read-only. Reset: Fixed,0000_0010h. The largest CPUID standard function input value supported by the processor implementation.
CPUID_Fn00000000_EBX [Processor Vendor (ASCII Bytes [3:0])] (Core::X86::Cpuid::ProcVendEbx)	
Read-only. Reset: Fixed,6874_7541h.	
Core::X86::Cpuid::ProcVendEbx and Core::X86::Cpuid::ProcVendExtEbx return the same value.	
_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn00000000_EBX	
Bits	Description
31:0	Vendor. Read-only. Reset: Fixed,6874_7541h. ASCII Bytes [3:0] ("h t u A") of the string "AuthenticAMD".
CPUID_Fn00000000_ECX [Processor Vendor (ASCII Bytes [11:8])] (Core::X86::Cpuid::ProcVendEcx)	
Read-only. Reset: Fixed,444D_4163h.	
Core::X86::Cpuid::ProcVendEcx and Core::X86::Cpuid::ProcVendExtEcx return the same value.	
_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn00000000_ECX	
Bits	Description
31:0	Vendor. Read-only. Reset: Fixed,444D_4163h. ASCII Bytes [11:8] ("D M A c") of the string "AuthenticAMD".
CPUID_Fn00000000_EDX [Processor Vendor (ASCII Bytes [7:4])] (Core::X86::Cpuid::ProcVendEdx)	
Read-only. Reset: Fixed,6974_6E65h.	
Core::X86::Cpuid::ProcVendEdx and Core::X86::Cpuid::ProcVendExtEdx return the same value.	
_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn00000000_EDX	
Bits	Description
31:0	Vendor. Read-only. Reset: Fixed,6974_6E65h. ASCII Bytes [7:4] ("i t n e") of the string "AuthenticAMD".

CPUID_Fn00000001_EAX [Family, Model, Stepping Identifiers] (Core::X86::Cpuid::FamModStep)

Read-only.

Core::X86::Cpuid::FamModStep and Core::X86::Cpuid::FamModStepExt return the same value.

Family: Is an 8-bit value and is defined as: Family[7:0]={0000b,BaseFamily[3:0]}+ExtendedFamily[7:0].

- E.g., If BaseFamily[3:0] == Fh and ExtendedFamily[7:0] == 08h, then Family[7:0] = 17h.

Model: Is an 8-bit value and is defined as: Model[7:0]={ExtendedModel[3:0],BaseModel[3:0]}.

- E.g., If ExtendedModel[3:0] == 1h and BaseModel[3:0] == 8h, then Model[7:0] = 18h.
- Model numbers vary with product.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn00000001_EAX

Bits	Description
31:28	Reserved.
27:20	ExtFamily: extended family. Read-only. Reset: 0Ah. See Family above.
19:16	ExtModel: extended model. Read-only. Reset: 6h. See Model above.
15:12	Reserved.
11:8	BaseFamily. Read-only. Reset: Fh. See Family description above.
7:4	BaseModel. Read-only. Reset: Xh. Model numbers vary with product.
3:0	Stepping. Read-only. Reset: Xh. Processor stepping (revision) for a specific model.

CPUID_Fn00000001_EBX [LocalApicId, LogicalProcessorCount, CLFlush] (Core::X86::Cpuid::FeatureIdEbx)

Read-only.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn00000001_EBX

Bits	Description
31:24	LocalApicId. Read-only. Reset: XXh. Initial local APIC physical ID.
23:16	LogicalProcessorCount: logical processor count. Read-only. Reset: Fixed,(Core::X86::Cpuid::SizeId[NC] + 1). Specifies the number of threads in the processor as Core::X86::Cpuid::SizeId[NC]+1.
15:8	CLFlush. Read-only. Reset: Fixed,08h. CLFLUSH size in quadwords.
7:0	Reserved.

CPUID_Fn00000001_ECX [Feature Identifiers] (Core::X86::Cpuid::FeatureIdEcX)

Read-only.

These values can be over-written by Core::X86::Msr::CPUID_Features.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn00000001_ECX

Bits	Description
31	Reserved.
30	RDRAND . Read-only. Reset: Fixed,1. RDRAND instruction support.
29	F16C . Read-only. Reset: Fixed,1. Half-precision convert instruction support.
28	AVX . Read-only. Reset: Fixed,1. AVX instruction support.
27	OSXSAVE . Read-only. Reset: X. 1=The OS has enabled support for XGETBV/XSETBV instructions to query processor extended states. OS enabled support for XGETBV/XSETBV.
26	XSAVE . Read-only. Reset: Fixed,1. 1=Support provided for the XSAVE, XRESTOR, XSETBV, and XGETBV instructions and the XFEATURE_ENABLED_MASK register. XSAVE (and related) instruction support.
25	AES: AES instruction support . Read-only. Reset: X. AES instruction support.
24	Reserved.
23	POPCNT . Read-only. Reset: Fixed,1. POPCNT instruction.
22	MOVBE . Read-only. Reset: Fixed,1. MOVBE instruction support.
21	X2APIC . Read-only. Reset: Fixed,1. x2APIC capability.
20	SSE42 . Read-only. Reset: Fixed,1. SSE4.2 instruction support.
19	SSE41 . Read-only. Reset: Fixed,1. SSE4.1 instruction support.
18	Reserved.
17	PCID . Read-only. Reset: Fixed,0. Process context identifiers support.
16:14	Reserved.
13	CMPXCHG16B . Read-only. Reset: Fixed,1. CMPXCHG16B instruction.
12	FMA . Read-only. Reset: Fixed,1. FMA instruction support.
11:10	Reserved.
9	SSSE3 . Read-only. Reset: Fixed,1. Supplemental SSE3 extensions.
8:4	Reserved.
3	Monitor . Read-only. Reset: !Core::X86::Msr::HWCR[MonMwaitDis]. Monitor/Mwait instructions.
2	Reserved.
1	PCLMULQDQ . Read-only. Reset: X. PCLMULQDQ instruction support.
0	SSE3 . Read-only. Reset: Fixed,1. SSE3 extensions.

CPUID_Fn00000001_EDX [Feature Identifiers] (Core::X86::Cpuid::FeatureIdEdx)

Read-only.

These values can be over-written by Core::X86::Msr::CPUID_Features.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn00000001_EDX

Bits	Description
31:29	Reserved.
28	HTT. Read-only. Reset: Fixed,(Core::X86::Cpuid::SizeId[NC] != 0). 0=Single thread product (Core::X86::Cpuid::SizeId[NC] == 0). 1=Multi thread product (Core::X86::Cpuid::SizeId[NC] != 0). Hyper-threading technology.
27	Reserved.
26	SSE2. Read-only. Reset: Fixed,1. SSE2: SSE2 extensions.
25	SSE. Read-only. Reset: Fixed,1. SSE extensions.
24	FXSR. Read-only. Reset: Fixed,1. FXSAVE and FXRSTOR instructions.
23	MMX. Read-only. Reset: Fixed,1. MMX instructions
22:20	Reserved.
19	CLFSH. Read-only. Reset: Fixed,1. CLFLUSH instruction.
18	Reserved.
17	PSE36. Read-only. Reset: Fixed,1. Page-size extensions.
16	PAT. Read-only. Reset: Fixed,1. Page attribute table.
15	CMOV. Read-only. Reset: Fixed,1. Conditional move instructions, CMOV, FCOMI, FCMOV.
14	MCA. Read-only. Reset: Fixed,1. Machine check architecture, MCG_CAP.
13	PGE. Read-only. Reset: Fixed,1. Page global extension, CR4.PGE.
12	MTRR. Read-only. Reset: Fixed,1. Memory-type range registers.
11	SysEnterSysExit. Read-only. Reset: Fixed,1. SYSENTER and SYSEXIT instructions.
10	Reserved.
9	APIC: advanced programmable interrupt controller (APIC) exists and is enabled. Read-only. Reset: X. Core::X86::Msr::APIC_BAR[ApicEn].
8	CMPXCHG8B. Read-only. Reset: Fixed,1. CMPXCHG8B instruction.
7	MCE. Read-only. Reset: Fixed,1. Machine check exception, CR4.MCE.
6	PAE. Read-only. Reset: Fixed,1. Physical-address extensions (PAE).
5	MSR. Read-only. Reset: Fixed,1. AMD model-specific registers (MSRs), with RDMSR and WRMSR instructions.
4	TSC. Read-only. Reset: Fixed,1. Time Stamp Counter, RDTSC/RDTSCP instructions, CR4.TSD.
3	PSE. Read-only. Reset: Fixed,1. Page-size extensions (4 MB pages).
2	DE. Read-only. Reset: Fixed,1. Debugging extensions, IO breakpoints, CR4.DE.
1	VME. Read-only. Reset: Fixed,1. Virtual-mode enhancements.
0	FPU. Read-only. Reset: Fixed,1. x87 floating point unit on-chip.

CPUID_Fn00000005_EAX [Monitor/MWait] (Core::X86::Cpuid::MonMWaitEax)

Read-only. Reset: Fixed,0000_0040h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn00000005_EAX

Bits	Description
31:16	Reserved.
15:0	MonLineSizeMin. Read-only. Reset: Fixed,0040h. Smallest monitor-line size in bytes.

CPUID_Fn00000005_EBX [Monitor/MWait] (Core::X86::Cpuid::MonMWaitEbx)

Read-only. Reset: Fixed,0000_0040h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn00000005_EBX

Bits	Description
31:16	Reserved.
15:0	MonLineSizeMax . Read-only. Reset: Fixed,0040h. Largest monitor-line size in bytes.

CPUID_Fn00000005_ECX [Monitor/MWait] (Core::X86::Cpuid::MonMWaitEcX)

Read-only. Reset: Fixed,0000_0003h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn00000005_ECX

Bits	Description
31:2	Reserved.
1	IBE . Read-only. Reset: Fixed,1. Interrupt break-event.
0	EMX . Read-only. Reset: Fixed,1. Enumerate MONITOR/MWAIT extensions.

CPUID_Fn00000005_EDX [Monitor/MWait] (Core::X86::Cpuid::MonMWaitEdx)

Read-only. Reset: Fixed,0000_0011h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn00000005_EDX

Bits	Description
31:8	Reserved.
7:4	MWaitC1SubStates . Read-only. Reset: Fixed,1h. Number of C1 sub-cstates supported by MWAIT.
3:0	MWaitC0SubStates . Read-only. Reset: Fixed,1h. Number of C0 sub-cstates supported by MWAIT.

CPUID_Fn00000006_EAX [Thermal and Power Management] (Core::X86::Cpuid::ThermalPwrMgmtEax)

Read-only. Reset: Fixed,0000_0004h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn00000006_EAX

Bits	Description
31:3	Reserved.
2	ARAT: always running APIC timer . Read-only. Reset: Fixed,1. 1=Indicates support for APIC timer always running feature.
1:0	Reserved.

CPUID_Fn00000006_EBX [Thermal and Power Management] (Core::X86::Cpuid::ThermalPwrMgmtEbx)

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn00000006_EBX

Bits	Description
31:0	Reserved.

CPUID_Fn00000006_ECX [Thermal and Power Management] (Core::X86::Cpuid::ThermalPwrMgmtEcX)

Read-only. Reset: Fixed,0000_0001h.

These values can be over-written by Core::X86::Msrr::CPUID_PWR_THERM.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn00000006_ECX

Bits	Description
31:1	Reserved.
0	EffFreq: effective frequency interface . Read-only. Reset: Fixed,1. 1=Indicates presence of Core::X86::Msrr::MPERF and Core::X86::Msrr::APERF.

CPUID_Fn00000006_EDX [Thermal and Power Management] (Core::X86::Cpuid::ThermalPwrMgmtEdx)

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn00000006_EDX

Bits	Description
31:0	Reserved.

**CPUID_Fn00000007_EAX_x00 [Structured Extended Feature Identifiers]
(Core::X86::Cpuid::StructExtFeatIdEax0)**

Read-only. Reset: Fixed, 0000_0001h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn00000007_EAX_x00

Bits	Description
31:0	StructExtFeatIdMax. Read-only. Reset: Fixed, 0000_0001h. The largest CPUID Fn0000_0007 sub-function supported by the processor implementation.

**CPUID_Fn00000007_EBX_x00 [Structured Extended Feature Identifiers]
(Core::X86::Cpuid::StructExtFeatIdEbx0)**

Read-only. Reset: Fixed, F1BF_97A9h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn00000007_EBX_x00

Bits	Description
31	AVX512VL. Read-only. Reset: Fixed, 1. 1=Extends AVX512 instructions to 128 and 256 bits.
30	AVX512BW. Read-only. Reset: Fixed, 1. 1=AVX512BW packed integer instructions.
29	SHA. Read-only. Reset: Fixed, 1. 1=SHA Extensions available.
28	AVX512CD. Read-only. Reset: Fixed, 1. 1=AVX512 Conflict Detection for vectorizing loops supported.
27:25	Reserved.
24	CLWB. Read-only. Reset: Fixed, 1. Cache line write back.
23	CLFSHOPT. Read-only. Reset: Fixed, 1. Optimized Cache Line Flush.
22	Reserved.
21	AVX512_IFMA. Read-only. Reset: Fixed, 1. 1=AVX512 integer fused mul-add instructions supported.
20	SMAP. Read-only. Reset: Fixed, 1. Secure Mode Access Prevention is supported.
19	ADX. Read-only. Reset: Fixed, 1. ADCX and ADOX are present.
18	RDSEED. Read-only. Reset: Fixed, 1. RDSEED is present.
17	AVX512DQ. Read-only. Reset: Fixed, 1. 1=AVX512DQ packed integer instructions supported.
16	AVX512F. Read-only. Reset: Fixed, 1. 1=AVX512 Foundation supported.
15	PQE. Read-only. Reset: Fixed, 1. The processor supports Cache Allocation Technology.
14:13	Reserved.
12	PQM. Read-only. Reset: Fixed, 1. Platform QoS Monitoring.
11	Reserved.
10	INVPCID. Read-only. Reset: Fixed, 1. INVPCID instruction support.
9	ERMS. Read-only. Reset: Fixed, 1. Enhanced REP MOVSB/STOSB.
8	BMI2. Read-only. Reset: Fixed, 1. Bit manipulation group 2 instruction support.
7	SMEP. Read-only. Reset: Fixed, 1. Supervisor Mode Execution protection.
6	Reserved.
5	AVX2. Read-only. Reset: Fixed, 1. AVX extension support.
4	Reserved.
3	BMI1. Read-only. Reset: Fixed, 1. Bit manipulation group 1 instruction support.
2:1	Reserved.
0	FSGSBASE. Read-only. Reset: Fixed, 1. FS and GS base read write instruction support.

**CPUID_Fn00000007_ECX_x00 [Structured Extended Feature Identifier]
(Core::X86::Cpuid::StructExtFeatIdEc0)**

Read-only.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn00000007_ECX_x00

Bits	Description
31:23	Reserved.
22	RDPID . Read-only. Reset: Fixed,1. Read Processor ID instruction support.
21:15	Reserved.
14	AVX512_VPOPCNTDQ . Read-only. Reset: Fixed,1.
13	Reserved.
12	AVX512_BITALG . Read-only. Reset: Fixed,1.
11	AVX512_VNNI . Read-only. Reset: Fixed,1. 1=AVX512 vector neural network instructions.
10	VPCLMULQDQ . Read-only. Reset: X. Vector VPCLMULQDQ instruction support
9	VAES . Read-only. Reset: X. Vector VAES(ENC DEC), VAES(ENC DEC)LAST instruction support.
8	GFNI . Read-only. Reset: Fixed,1.
7	CET_SS . Read-only. Reset: 1. 1=Shadow stack supported.
6	AVX512_VBMI2 . Read-only. Reset: Fixed,1. 1=AVX512 vector byte permutation instruction 2.
5:4	Reserved.
3	PKU . Read-only. Reset: Fixed,1. Protection keys support.
2	UMIP . Read-only. Reset: Fixed,1. User Mode Instruction Prevention enable.
1	AVX512_VBMI . Read-only. Reset: Fixed,1. 1=AVX512 vector byte permutation instruction.
0	Reserved.

**CPUID_Fn00000007_EDX_x00 [Structured Extended Feature Identifiers]
(Core::X86::Cpuid::StructExtFeatIdEdx0)**

Read-only. Reset: Fixed,1000_0010h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn00000007_EDX_x00

Bits	Description
31:29	Reserved.
28	L1D_FLUSH . Read-only. Reset: Fixed,1. L1D_FLUSH supported in FLUSH_CMD MSR.
27:5	Reserved.
4	FSRM . Read-only. Reset: Fixed,1. Fast Short Rep Movsb supported.
3:0	Reserved.

**CPUID_Fn00000007_EAX_x01 [Structured Extended Feature Identifiers]
(Core::X86::Cpuid::StructExtFeatIdEax1)**

Read-only. Reset: Fixed,0000_0020h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn00000007_EAX_x01

Bits	Description
31:6	Reserved.
5	AVX512_BF16 . Read-only. Reset: Fixed,1. 1=BFLOAT16 instructions supported.
4:0	Reserved.

**CPUID_Fn00000007_EBX_x01 [Structured Extended Feature Identifiers]
(Core::X86::Cpuid::StructExtFeatIdEbx1)**

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn00000007_EBX_x01

Bits	Description
31:0	Reserved.

**CPUID_Fn00000007_ECX_x01 [Structured Extended Feature Identifier]
(Core::X86::Cpuid::StructExtFeatIdEcX1)**

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn00000007_ECX_x01

Bits	Description
------	-------------

31:0	Reserved.
------	-----------

**CPUID_Fn00000007_EDX_x01 [Structured Extended Feature Identifiers]
(Core::X86::Cpuid::StructExtFeatIdEdx1)**

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn00000007_EDX_x01

Bits	Description
------	-------------

31:0	Reserved.
------	-----------

CPUID_Fn0000000B_EAX_x00 [Extended Topology Enumeration] (Core::X86::Cpuid::ExtTopEnumEax0)

Read-only. Enable: (Core::X86::Cpuid::ExtTopEnumEbx0 > 0).

CPUID Fn0000_000B_E[D,C,B,A]X_x[2:0] specifies the hierarchy of logical cores from the SMT level through the processor socket level.

Software determines the presence of CPUID Fn0000_000B if (CPUID Fn0000_000B_EBX_x0[31:0] != 0). Software reads CPUID Fn0000_000B_E[C,B,A]X for ascending values of ECX until (CPUID Fn0000_000B_EBX[LogProcAtThisLevel] == 0).

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000B_EAX_x00

Bits	Description
------	-------------

31:5	Reserved.
------	-----------

4:0	CoreMaskWidth. Read-only. Number of bits to shift ExtendedApicId right to get unique topology ID of the next level type.
-----	---

Reset: SMT ? 01h : 00h.

CPUID_Fn0000000B_EBX_x00 [Extended Topology Enumeration] (Core::X86::Cpuid::ExtTopEnumEbx0)

Read-only.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000B_EBX_x00

Bits	Description
------	-------------

31:16	Reserved.
-------	-----------

15:0	LogProcAtThisLevel. Read-only. Number of threads in a core.
------	--

Reset: SMT ? 2 : 0001h.

CPUID_Fn0000000B_ECX_x00 [Extended Topology Enumeration] (Core::X86::Cpuid::ExtTopEnumEcX0)

Read-only. Reset: Fixed,0000_0100h. Enable: (Core::X86::Cpuid::ExtTopEnumEbx0 > 0).

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000B_ECX_x00

Bits	Description
------	-------------

31:16	Reserved.
-------	-----------

15:8	LevelType. Read-only. Reset: Fixed,01h.
------	--

ValidValues:

Value	Description
00h	Invalid
01h	Thread
02h	Processor
FFh-03h	Reserved.

7:0	EcXVal. Read-only. Reset: Fixed,00h. ECX input value.
-----	--

CPUID_Fn0000000B_EAX_x01 [Extended Topology Enumeration] (Core::X86::Cpuid::ExtTopEnumEax1)

Read-only. Enable: (Core::X86::Cpuid::ExtTopEnumEbx1 > 0).

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000B_EAX_x01

Bits	Description
31:5	Reserved.
4:0	CoreMaskWidth . Read-only. Reset: XXXXXb. ExtendedApicId right shift value.

CPUID_Fn0000000B_EBX_x01 [Extended Topology Enumeration] (Core::X86::Cpuid::ExtTopEnumEbx1)

Read-only.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000B_EBX_x01

Bits	Description
31:16	Reserved.
15:0	LogProcAtThisLevel . Read-only. Reset: XXXXh. Number of logical cores in processor socket.

CPUID_Fn0000000B_ECX_x01 [Extended Topology Enumeration] (Core::X86::Cpuid::ExtTopEnumEcxc1)

Read-only. Reset: Fixed,0000_0201h. Enable: (Core::X86::Cpuid::ExtTopEnumEbx1 > 0).

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000B_ECX_x01

Bits	Description										
31:16	Reserved.										
15:8	LevelType . Read-only. Reset: Fixed,02h. ValidValues: <table border="1"> <thead> <tr> <th>Value</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00h</td><td>Invalid</td></tr> <tr> <td>01h</td><td>Thread</td></tr> <tr> <td>02h</td><td>Processor</td></tr> <tr> <td>FFh-03h</td><td>Reserved.</td></tr> </tbody> </table>	Value	Description	00h	Invalid	01h	Thread	02h	Processor	FFh-03h	Reserved.
Value	Description										
00h	Invalid										
01h	Thread										
02h	Processor										
FFh-03h	Reserved.										
7:0	EcxcVal . Read-only. Reset: Fixed,01h. ECX input value.										

CPUID_Fn0000000B_EAX_x02 [Extended Topology Enumeration] (Core::X86::Cpuid::ExtTopEnumEax2)

Read-only. Reset: Fixed,0000_0000h. Enable: (Core::X86::Cpuid::ExtTopEnumEbx2 > 0).

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000B_EAX_x02

Bits	Description
31:5	Reserved.
4:0	CoreMaskWidth . Read-only. Reset: Fixed,00h. Zero indicates no more levels.

CPUID_Fn0000000B_EBX_x02 [Extended Topology Enumeration] (Core::X86::Cpuid::ExtTopEnumEbx2)

Read-only. Reset: 0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000B_EBX_x02

Bits	Description
31:16	Reserved.
15:0	LogProcAtThisLevel . Read-only. Reset: 0000h. Zero indicates no more levels.

CPUID_Fn0000000B_ECX_x02 [Extended Topology Enumeration] (Core::X86::Cpuid::ExtTopEnumEc2)

Read-only. Reset: Fixed,0000_0002h. Enable: (Core::X86::Cpuid::ExtTopEnumEbx2 > 0).

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000B_ECX_x02

Bits	Description										
31:16	Reserved.										
15:8	LevelType. Read-only. Reset: Fixed,00h. ValidValues:										
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>00h</td><td>Invalid</td></tr> <tr> <td>01h</td><td>Thread</td></tr> <tr> <td>02h</td><td>Processor</td></tr> <tr> <td>FFh-03h</td><td>Reserved.</td></tr> </table>	Value	Description	00h	Invalid	01h	Thread	02h	Processor	FFh-03h	Reserved.
Value	Description										
00h	Invalid										
01h	Thread										
02h	Processor										
FFh-03h	Reserved.										
7:0	EcxFVal. Read-only. Reset: Fixed,02h. ECX input value.										

CPUID_Fn0000000B_EDX [Extended Topology Enumeration] (Core::X86::Cpuid::ExtTopEnumEdx)

Read-only.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000B_EDX

Bits	Description
31:0	ExtendedLocalApicId: extended APIC ID. Read-only. Reset: XXXX_XXXXh. Extended APIC_ID.

CPUID_Fn0000000D_EAX_x00 [Processor Extended State Enumeration] (Core::X86::Cpuid::ProcExtStateEnumEax00)

Read-only. Reset: Fixed,0000_02E7h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000D_EAX_x00

Bits	Description		
31:0	XFeatureSupportedMask[31:0]. Read-only. Reset: Fixed,0000_02E7h. Each set bit indicates the corresponding bit in register XCR0[31:0] is settable.		
	ValidValues:		
	Bit	Name	Description
	[0]	X87	X87 Support.
	[1]	SSE	128-bit SSE Support.
	[2]	AVX	256-bit AVX support.
	[4:3]		Reserved.
	[5]	KREGS	KREGS
	[6]	ZMMHI	ZMMHI
	[7]	HIZMM	HIZMM
	[8]		Reserved.
	[9]	MPK	Memory Protection Keys. See Core::X86::Cpuid::StructExtFeatIdEc0[PKU] for the availability of MPK feature support.
[31:10]		Reserved.	

**CPUID_Fn0000000D_EBX_x00 [Processor Extended State Enumeration]
(Core::X86::Cpuid::ProcExtStateEnumEbx00)**

Read-only, Volatile.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000D_EBX_x00

Bits	Description
31:0	XFeatureEnabledSizeMax. Read-only, Volatile. Reset: XXXX_XXXXh. Description: Size in bytes of an uncompact XSAVE/XRSTOR area for all features enabled in the XCR0 register. IF (XCR0[MPK] == 1) return EBX=0000_0988h ELSIF (XCR0[HIZMM] == 1) return EBX=0000_0980h ELSIF (XCR0[ZMMHI] == 1) return EBX=0000_0580h ELSIF (XCR0[KREGS] == 1) return EBX=0000_0380h ELSIF (XCR0[AVX] == 1) return EBX=0000_0340h ELSIF (XCR0[SSE] == 1) or (XCR0[X87] == 1) return EBX=0000_0240h // legacy header + X87/SSE size END

**CPUID_Fn0000000D_ECX_x00 [Processor Extended State Enumeration]
(Core::X86::Cpuid::ProcExtStateEnumEcx00)**

Read-only. Reset: Fixed, 0000_0988h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000D_ECX_x00

Bits	Description
31:0	XFeatureSupportedSizeMax. Read-only. Reset: Fixed, 0000_0988h. Size of legacy header + X87/SSE + AVX + KREGS + ZMMHI + HIZMM + MPK.

**CPUID_Fn0000000D_EDX_x00 [Processor Extended State Enumeration]
(Core::X86::Cpuid::ProcExtStateEnumEdx00)**

Read-only. Reset: Fixed, 0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000D_EDX_x00

Bits	Description
31:0	XFeatureSupportedMask[63:32]. Read-only. Reset: Fixed, 0000_0000h. Each set bit indicates the corresponding bit in register XCR0[63:32] is settable.

**CPUID_Fn0000000D_EAX_x01 [Processor Extended State Enumeration]
(Core::X86::Cpuid::ProcExtStateEnumEax01)**

Read-only. Reset: Fixed, 0000_000Fh.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000D_EAX_x01

Bits	Description
31:4	Reserved.
3	XSAVES. Read-only. Reset: Fixed, 1. XSAVES, XRSTORS, and XSS supported.
2	XGETBV. Read-only. Reset: Fixed, 1. XGETBV with ECX=1 supported.
1	XSAVEC. Read-only. Reset: Fixed, 1. XSAVEC and compact XRSTOR supported.
0	XSAVEOPT. Read-only. Reset: Fixed, 1. XSAVEOPT is available.

**CPUID_Fn0000000D_EBX_x01 [Processor Extended State Enumeration]
(Core::X86::Cpuid::ProcExtStateEnumEbx01)**

Read-only, Volatile.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000D_EBX_x01

Bits	Description
31:0	XFeatureEnabledSizeMax. Read-only, Volatile. Reset: XXXX_XXXXh. Description: Reset is EBX = 0000_0240h + ((XCR0[AVX] == 1) ? 0000_0100h : 0) + ((XCR0[KREGS] == 1) ? 0000_0040h : 0) + ((XCR0[ZMMHI] == 1) ? 0000_0200h : 0) + ((XCR0[HIZMM] == 1) ? 0000_0400h : 0) + ((XCR0[MPK] == 1) ? 0000_0008h : 0) + ((XSS[CET_U] == 1) ? 0000_0010h : 0) + ((XSS[CET_S] == 1) ? 0000_0018h : 0).

**CPUID_Fn0000000D_ECX_x01 [Processor Extended State Enumeration]
(Core::X86::Cpuid::ProcExtStateEnumEcX01)**

Read-only. Reset: Fixed, 0000_1800h.

Each set bit indicates the corresponding bit in register XSS[31:0] is settable.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000D_ECX_x01

Bits	Description										
31:0	MaskXss. Read-only. Reset: Fixed, 0000_1800h. Mask[31:0] of settable XSS bits. ValidValues:										
	<table> <tr> <th>Bit</th><th>Description</th></tr> <tr> <td>[10:0]</td><td>Reserved.</td></tr> <tr> <td>[11]</td><td>CET for user mode.</td></tr> <tr> <td>[12]</td><td>CET for supervisor mode.</td></tr> <tr> <td>[31:13]</td><td>Reserved.</td></tr> </table>	Bit	Description	[10:0]	Reserved.	[11]	CET for user mode.	[12]	CET for supervisor mode.	[31:13]	Reserved.
Bit	Description										
[10:0]	Reserved.										
[11]	CET for user mode.										
[12]	CET for supervisor mode.										
[31:13]	Reserved.										

**CPUID_Fn0000000D_EDX_x01 [Processor Extended State Enumeration]
(Core::X86::Cpuid::ProcExtStateEnumEdx01)**

Read-only. Reset: Fixed, 0000_0000h.

Each set bit indicates the corresponding bit in register XSS[63:32] is settable.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000D_EDX_x01

Bits	Description
31:0	MaskXss. Read-only. Reset: Fixed, 0000_0000h. Mask[63:32] of settable XSS bits.

**CPUID_Fn0000000D_EAX_x02 [Processor Extended State Enumeration]
(Core::X86::Cpuid::ProcExtStateEnumEax02)**

Read-only. Reset: Fixed, 0000_0100h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000D_EAX_x02

Bits	Description
31:0	YmmHiSaveStateOffset. Read-only. Reset: Fixed, 0000_0100h. YMM[31:16] save state byte size.

**CPUID_Fn0000000D_EBX_x02 [Processor Extended State Enumeration]
(Core::X86::Cpuid::ProcExtStateEnumEbx02)**

Read-only. Reset: Fixed, 0000_0240h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000D_EBX_x02

Bits	Description
31:0	YmmHiSaveStateOffset. Read-only. Reset: Fixed, 0000_0240h. YMM[31:16] save state uncompact byte offset.

**CPUID_Fn0000000D_ECX_x02 [Processor Extended State Enumeration]
(Core::X86::Cpuid::ProcExtStateEnumEcxE02)**

Read-only. Reset: Fixed,0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000D_ECX_x02

Bits	Description
31:2	Reserved.
1	YmmHiAligned. Read-only. Reset: Fixed,0. 0=YMM_hi state (YMM[31:16]) is not automatically aligned to a 64-byte boundary on compacted saves/restores. 1=YMM_hi state (YMM[31:16]) is automatically aligned to a 64-byte boundary on compacted saves/restores.
0	XStateSupervisor. Read-only. Reset: Fixed,0. 1=This xstate is Supervisor State.

**CPUID_Fn0000000D_EDX_x02 [Processor Extended State Enumeration]
(Core::X86::Cpuid::ProcExtStateEnumEdxE02)**

Read-only. Reset: Fixed,0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000D_EDX_x02

Bits	Description
31:0	Reserved.

**CPUID_Fn0000000D_EAX_x05 [Processor Extended State Enumeration]
(Core::X86::Cpuid::ProcExtStateEnumEaxE05)**

Read-only. Reset: Fixed,0000_0040h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000D_EAX_x05

Bits	Description
31:0	KREGSSaveStateSize. Read-only. Reset: Fixed,0000_0040h. KREGS save state byte size.

**CPUID_Fn0000000D_EBX_x05 [Processor Extended State Enumeration]
(Core::X86::Cpuid::ProcExtStateEnumEbxE05)**

Read-only. Reset: Fixed,0000_0340h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000D_EBX_x05

Bits	Description
31:0	KREGSSaveStateOffset. Read-only. Reset: Fixed,0000_0340h. KREGS save state uncompact byte offset.

**CPUID_Fn0000000D_ECX_x05 [Processor Extended State Enumeration]
(Core::X86::Cpuid::ProcExtStateEnumEcxE05)**

Read-only. Reset: Fixed,0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000D_ECX_x05

Bits	Description
31:2	Reserved.
1	KREGSAligned. Read-only. Reset: Fixed,0. 0=KREGS state is not automatically aligned to a 64-byte boundary on compacted saves/restores. 1=KREGS state is automatically aligned to a 64-byte boundary on compacted saves/restores.
0	XStateSupervisor. Read-only. Reset: Fixed,0. 1=This xstate is Supervisor State.

**CPUID_Fn0000000D_EDX_x05 [Processor Extended State Enumeration]
(Core::X86::Cpuid::ProcExtStateEnumEdxE05)**

Read-only. Reset: Fixed,0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000D_EDX_x05

Bits	Description
31:0	Reserved.

**CPUID_Fn0000000D_EAX_x06 [Processor Extended State Enumeration]
(Core::X86::Cpuid::ProcExtStateEnumEax06)**

Read-only. Reset: Fixed,0000_0200h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000D_EAX_x06

Bits	Description
31:0	ZMMHISaveStateSize. Read-only. Reset: Fixed,0000_0200h. ZMMHI save state byte size.

**CPUID_Fn0000000D_EBX_x06 [Processor Extended State Enumeration]
(Core::X86::Cpuid::ProcExtStateEnumEbx06)**

Read-only. Reset: Fixed,0000_0380h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000D_EBX_x06

Bits	Description
31:0	ZMMHISaveStateOffset. Read-only. Reset: Fixed,0000_0380h. ZMMHI save state uncompact byte offset.

**CPUID_Fn0000000D_ECX_x06 [Processor Extended State Enumeration]
(Core::X86::Cpuid::ProcExtStateEnumEcx06)**

Read-only. Reset: Fixed,0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000D_ECX_x06

Bits	Description
31:2	Reserved.
1	ZMMHISAligned. Read-only. Reset: Fixed,0. 0=ZMMHI state is not automatically aligned to a 64-byte boundary on compacted saves/restores. 1=ZMMHI is automatically aligned to a 64-byte boundary on compacted saves/restores.
0	XStateSupervisor. Read-only. Reset: Fixed,0. 1=This xstate is Supervisor State.

**CPUID_Fn0000000D_EDX_x06 [Processor Extended State Enumeration]
(Core::X86::Cpuid::ProcExtStateEnumEdx06)**

Read-only. Reset: Fixed,0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000D_EDX_x06

Bits	Description
31:0	Reserved.

**CPUID_Fn0000000D_EAX_x07 [Processor Extended State Enumeration]
(Core::X86::Cpuid::ProcExtStateEnumEax07)**

Read-only. Reset: Fixed,0000_0400h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000D_EAX_x07

Bits	Description
31:0	HIZMMSaveStateSize. Read-only. Reset: Fixed,0000_0400h. HIZMM save state byte size.

**CPUID_Fn0000000D_EBX_x07 [Processor Extended State Enumeration]
(Core::X86::Cpuid::ProcExtStateEnumEbx07)**

Read-only. Reset: Fixed,0000_0580h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000D_EBX_x07

Bits	Description
31:0	HIZMMSaveStateOffset. Read-only. Reset: Fixed,0000_0580h. HIZMM save state uncompact byte offset.

**CPUID_Fn0000000D_ECX_x07 [Processor Extended State Enumeration]
(Core::X86::Cpuid::ProcExtStateEnumEcX07)**

Read-only. Reset: Fixed,0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000D_ECX_x07

Bits	Description
31:2	Reserved.
1	HIZMMAligned. Read-only. Reset: Fixed,0. 0=HIZMM state is not automatically aligned to a 64-byte boundary on compacted saves/restores. 1=HIZMM state is automatically aligned to a 64-byte boundary on compacted saves/restores.
0	XStateSupervisor. Read-only. Reset: Fixed,0. 1=This xstate is Supervisor State.

**CPUID_Fn0000000D_EDX_x07 [Processor Extended State Enumeration]
(Core::X86::Cpuid::ProcExtStateEnumEdx07)**

Read-only. Reset: Fixed,0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000D_EDX_x07

Bits	Description
31:0	Reserved.

**CPUID_Fn0000000D_EAX_x09 [Processor Extended State Enumeration]
(Core::X86::Cpuid::ProcExtStateEnumEax09)**

Read-only. Reset: Fixed,0000_0008h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000D_EAX_x09

Bits	Description
31:0	MpkSaveStateSize. Read-only. Reset: Fixed,0000_0008h. MPK save state byte size.

**CPUID_Fn0000000D_EBX_x09 [Processor Extended State Enumeration]
(Core::X86::Cpuid::ProcExtStateEnumEbx09)**

Read-only. Reset: Fixed,0000_0980h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000D_EBX_x09

Bits	Description
31:0	MpKSaveStateOffset. Read-only. Reset: Fixed,0000_0980h. MPK save state uncompact byte offset.

**CPUID_Fn0000000D_ECX_x09 [Processor Extended State Enumeration]
(Core::X86::Cpuid::ProcExtStateEnumEcX09)**

Read-only. Reset: Fixed,0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000D_ECX_x09

Bits	Description
31:2	Reserved.
1	XState64ByteAligned. Read-only. Reset: Fixed,0. 1=This xstate will always be 64-byte aligned in compacted memops.
0	XStateSupervisor. Read-only. Reset: Fixed,0. 1=This xstate is Supervisor State.

**CPUID_Fn0000000D_EDX_x09 [Processor Extended State Enumeration]
(Core::X86::Cpuid::ProcExtStateEnumEdx09)**

Read-only. Reset: Fixed,0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000D_EDX_x09

Bits	Description
31:0	Reserved.

**CPUID_Fn0000000D_EAX_x0B [Processor Extended State Enumeration]
(Core::X86::Cpuid::ProcExtStateEnumEax0B)**

Read-only. Reset: Fixed,0000_0010h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000D_EAX_x0B

Bits	Description
------	-------------

31:0	CetUserSize. Read-only. Reset: Fixed,0000_0010h. : CET user size.
------	--

**CPUID_Fn0000000D_EBX_x0B [Processor Extended State Enumeration]
(Core::X86::Cpuid::ProcExtStateEnumEbx0B)**

Read-only. Reset: Fixed,0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000D_EBX_x0B

Bits	Description
------	-------------

31:0	CetUserOffset. Read-only. Reset: Fixed,0000_0000h. CET user byte offset.
------	---

**CPUID_Fn0000000D_ECX_x0B [Processor Extended State Enumeration]
(Core::X86::Cpuid::ProcExtStateEnumEcxB)**

Read-only. Reset: Fixed,0000_0001h.

Processor Extended State Enumeration for CET_U.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000D_ECX_x0B

Bits	Description
------	-------------

31:2	Reserved.
------	-----------

1	XState64ByteAligned. Read-only. Reset: Fixed,0. 1=This xstate will always be 64-byte aligned in compacted memops.
---	--

0	XStateSupervisor. Read-only. Reset: Fixed,1. 1=This xstate is Supervisor State.
---	--

**CPUID_Fn0000000D_EDX_x0B [Processor Extended State Enumeration]
(Core::X86::Cpuid::ProcExtStateEnumEdxB)**

Read-only. Reset: Fixed,0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000D_EDX_x0B

Bits	Description
------	-------------

31:0	Reserved.
------	-----------

**CPUID_Fn0000000D_EAX_x0C [Processor Extended State Enumeration]
(Core::X86::Cpuid::ProcExtStateEnumEax0C)**

Read-only. Reset: Fixed,0000_0018h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000D_EAX_x0C

Bits	Description
------	-------------

31:0	CetSprvrSize. Read-only. Reset: Fixed,0000_0018h. CET supervisor size.
------	---

**CPUID_Fn0000000D_EBX_x0C [Processor Extended State Enumeration]
(Core::X86::Cpuid::ProcExtStateEnumEbx0C)**

Read-only. Reset: Fixed,0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000D_EBX_x0C

Bits	Description
------	-------------

31:0	CetSprvrOffset. Read-only. Reset: Fixed,0000_0000h. CET supervisor byte offset.
------	--

**CPUID_Fn0000000D_ECX_x0C [Processor Extended State Enumeration]
(Core::X86::Cpuid::ProcExtStateEnumEcxC)**

Read-only. Reset: Fixed,0000_0001h.

Processor Extended State Enumeration for CET_S.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000D_ECX_x0C

Bits	Description
31:2	Reserved.
1	XState64ByteAligned . Read-only. Reset: Fixed,0. 1=This xstate will always be 64-byte aligned in compacted memops.
0	XStateSupervisor . Read-only. Reset: Fixed,1. 1=This xstate is Supervisor State.

**CPUID_Fn0000000D_EDX_x0C [Processor Extended State Enumeration]
(Core::X86::Cpuid::ProcExtStateEnumEdxC)**

Read-only. Reset: Fixed,0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000D_EDX_x0C

Bits	Description
31:0	Reserved.

**CPUID_Fn0000000F_EAX_x00 [Resource Director Technology Monitor Capability]
(Core::X86::Cpuid::RsrcDirTechMonCapEax0)**

Read-only. Reset: Fixed,0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000F_EAX_x00

Bits	Description
31:0	Reserved.

**CPUID_Fn0000000F_EBX_x00 [Resource Director Technology Monitor Capability]
(Core::X86::Cpuid::RsrcDirTechMonCapEbx0)**

Read-only. Reset: Fixed,0000_00FFh.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000F_EBX_x00

Bits	Description
31:0	RmidMaxRange . Read-only. Reset: Fixed,0000_00FFh. RMID maximum within this processor for all types.

**CPUID_Fn0000000F_ECX_x00 [Resource Director Technology Monitor Capability]
(Core::X86::Cpuid::RsrcDirTechMonCapEcxC)**

Read-only. Reset: Fixed,0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000F_ECX_x00

Bits	Description
31:0	Reserved.

**CPUID_Fn0000000F_EDX_x00 [Resource Director Technology Monitor Capability]
(Core::X86::Cpuid::RsrcDirTechMonCapEdxC)**

Read-only. Reset: Fixed,0000_0002h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000F_EDX_x00

Bits	Description
31:2	Reserved.
1	L3CacheRDT . Read-only. Reset: Fixed,1. L3 Cache RDT Monitoring.
0	Reserved.

**CPUID_Fn0000000F_EAX_x01 [Resource Director Technology L3 Monitor Capability]
(Core::X86::Cpuid::RsrcDirTechMonCapEax1)**

Read-only.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000F_EAX_x01

Bits	Description
31:9	Reserved.
8	OverflowBit. Read-only. Reset: Fixed,0. 1=Indicates Core::X86::Msr::QM_CTR bit[61] is an overflow bit.
7:0	CounterSize. Read-only. Reset: Fixed,20. Encode counter width offset from bit 24.
ValidValues:	
Value	Description
00h	Family/Model/Stepping should be used to determine counter size.
26h-01h	<Value>+24-bit counters.
FFh-27h	Reserved.

**CPUID_Fn0000000F_EBX_x01 [Resource Director Technology L3 Monitor Capability]
(Core::X86::Cpuid::RsrcDirTechMonCapEbx1)**

Read-only. Reset: Fixed,0000_0040h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000F_EBX_x01

Bits	Description
31:0	ConverFactor. Read-only. Reset: Fixed,0000_0040h. Conversion Factor.

**CPUID_Fn0000000F_ECX_x01 [Resource Director Technology L3 Monitor Capability]
(Core::X86::Cpuid::RsrcDirTechMonCapEcxc1)**

Read-only. Reset: Fixed,0000_00FFh.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000F_ECX_x01

Bits	Description
31:0	RmidMaxRange. Read-only. Reset: Fixed,0000_00FFh. RMID Maximum Range of this resource.

**CPUID_Fn0000000F_EDX_x01 [Resource Director Technology L3 Monitor Capability]
(Core::X86::Cpuid::RsrcDirTechMonCapEdxc1)**

Read-only. Reset: Fixed,0000_0007h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn0000000F_EDX_x01

Bits	Description
31:3	Reserved.
2	L3CacheLocalBndwdthMon. Read-only. Reset: Fixed,1. L3 Local Bandwidth monitoring.
1	L3CacheTotalBndwdthMon. Read-only. Reset: Fixed,1. L3 Total Bandwidth monitoring.
0	L3CacheOccpncyMon. Read-only. Reset: Fixed,1. L3 occupancy monitoring.

**CPUID_Fn00000010_EAX_x00 [Resource Director Technology Allocation Enumeration]
(Core::X86::Cpuid::RsrcDirTechAllocEnumEax0)**

Read-only. Reset: Fixed,0000_0000h. Enable: (Core::X86::Cpuid::RsrcDirTechAllocEnumEbx0 > 0).

Software determines the presence of CPUID Fn0000_0010 if (CPUID Fn0000_0010_EBX_x0[31:0] != 0). Software reads CPUID Fn0000_0010_E[D,C,B,A]X for ascending values of ECX until (CPUID Fn0000_0010_EBX[LogProcAtThisLevel] == 0).

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn00000010_EAX_x00

Bits	Description
31:0	Reserved.

**CPUID_Fn00000010_EBX_x00 [Resource Director Technology Allocation Enumeration]
(Core::X86::Cpuid::RsrcDirTechAllocEnumEbx0)**

Read-only. Reset: 0000_0002h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn00000010_EBX_x00

Bits	Description
31:3	Reserved.
2	L2CacheAllocTech. Read-only. Reset: 0. L2 Cache Allocation Technology.
1	L3CacheAllocTech. Read-only. Reset: 1. L3 Cache Allocation Technology.
0	Reserved.

**CPUID_Fn00000010_ECX_x00 [Resource Director Technology Allocation Enumeration]
(Core::X86::Cpuid::RsrcDirTechAllocEnumEcx0)**

Read-only. Reset: Fixed,0000_0000h. Enable: (Core::X86::Cpuid::RsrcDirTechAllocEnumEbx0 > 0).

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn00000010_ECX_x00

Bits	Description
31:0	Reserved.

**CPUID_Fn00000010_EDX_x00 [Resource Director Technology Allocation Enumeration]
(Core::X86::Cpuid::RsrcDirTechAllocEnumEdx0)**

Read-only. Reset: Fixed,0000_0000h. Enable: (Core::X86::Cpuid::RsrcDirTechAllocEnumEbx0 > 0).

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn00000010_EDX_x00

Bits	Description
31:0	Reserved.

**CPUID_Fn00000010_EAX_x01 [Resource Director Technology L3 Allocation Enumeration]
(Core::X86::Cpuid::RsrcDirTechAllocEnumEax1)**

Read-only. Enable: (Core::X86::Cpuid::RsrcDirTechAllocEnumEbx1 > 0).

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn00000010_EAX_x01

Bits	Description
31:5	Reserved.
4:0	CapacityMask. Read-only. Reset: Fixed,0Fh. Capacity bitmask length.

**CPUID_Fn00000010_EBX_x01 [Resource Director Technology L3 Allocation Enumeration]
(Core::X86::Cpuid::RsrcDirTechAllocEnumEbx1)**

Read-only. Reset: 0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn00000010_EBX_x01

Bits	Description
31:0	AllocUnits. Read-only. Reset: 0000_0000h. Allocation Units.

**CPUID_Fn00000010_ECX_x01 [Resource Director Technology L3 Allocation Enumeration]
(Core::X86::Cpuid::RsrcDirTechAllocEnumEcx1)**

Read-only. Reset: Fixed,0000_0004h. Enable: (Core::X86::Cpuid::RsrcDirTechAllocEnumEbx1 > 0).

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn00000010_ECX_x01

Bits	Description
31:3	Reserved.
2	CDP. Read-only. Reset: Fixed,1. Code and data prioritization.
1:0	Reserved.

CPUID_Fn00000010_EDX_x01 [Resource Director Technology L3 Allocation Enumeration] (Core::X86::Cpuid::RsrcDirTechAllocEnumEdx1)

Read-only. Reset: Fixed,0000_000Fh. Enable: (Core::X86::Cpuid::RsrcDirTechAllocEnumEbx1 > 0).

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn00000010_EDX_x01

Bits	Description
31:16	Reserved.
15:0	HCS. Read-only. Reset: Fixed,000Fh. Highest Class Of Service (COS) supported.

CPUID_Fn80000000_EAX [Largest Extended Function Number] (Core::X86::Cpuid::LargExtFuncNum)

Read-only. Reset: Fixed,8000_0028h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000000_EAX

Bits	Description
31:0	LFuncExt: largest extended function. Read-only. Reset: Fixed,8000_0028h. The largest CPUID extended function input value supported by the processor implementation.

CPUID_Fn80000000_EBX [Processor Vendor (ASCII Bytes [3:0])] (Core::X86::Cpuid::ProcVendExtEbx)

Read-only. Reset: Fixed,6874_7541h.

Core::X86::Cpuid::ProcVendEbx and Core::X86::Cpuid::ProcVendExtEbx return the same value.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000000_EBX

Bits	Description
31:0	Vendor. Read-only. Reset: Fixed,6874_7541h. ASCII Bytes [3:0] ("h t u A") of the string "AuthenticAMD".

CPUID_Fn80000000_ECX [Processor Vendor (ASCII Bytes [11:8])] (Core::X86::Cpuid::ProcVendExtEcx)

Read-only. Reset: Fixed,444D_4163h.

Core::X86::Cpuid::ProcVendEcx and Core::X86::Cpuid::ProcVendExtEcx return the same value.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000000_ECX

Bits	Description
31:0	Vendor. Read-only. Reset: Fixed,444D_4163h. ASCII Bytes [11:8] ("D M A c") of the string "AuthenticAMD".

CPUID_Fn80000000_EDX [Processor Vendor (ASCII Bytes [7:4])] (Core::X86::Cpuid::ProcVendExtEdx)

Read-only. Reset: Fixed,6974_6E65h.

Core::X86::Cpuid::ProcVendEdx and Core::X86::Cpuid::ProcVendExtEdx return the same value.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000000_EDX

Bits	Description
31:0	Vendor. Read-only. Reset: Fixed,6974_6E65h. ASCII Bytes [7:4] ("i t n e") of the string "AuthenticAMD".

CPUID_Fn80000001_EAX [Family, Model, Stepping Identifiers] (Core::X86::Cpuid::FamModStepExt)

Read-only.

Core::X86::Cpuid::FamModStep and Core::X86::Cpuid::FamModStepExt return the same value. See Core::X86::Cpuid::FamModStep.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000001_EAX

Bits	Description
31:28	Reserved.
27:20	ExtFamily: extended family. Read-only. Reset: 0Ah. See Core::X86::Cpuid::FamModStep description of Family.
19:16	ExtModel: extended model. Read-only. Reset: 6h. See Core::X86::Cpuid::FamModStep description of ExtModel.
15:12	Reserved.
11:8	BaseFamily. Read-only. Reset: Fh. See Core::X86::Cpuid::FamModStep description of Family.
7:4	BaseModel. Read-only. Reset: Xh. Model numbers vary with product.
3:0	Stepping. Read-only. Reset: Xh. Processor stepping (revision) for a specific model.

CPUID_Fn80000001_EBX [BrandId Identifier] (Core::X86::Cpuid::BrandId)

Read-only.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000001_EBX

Bits	Description								
31:28	PkgType: package type. Read-only. Reset: Xh. Specifies the package type. ValidValues: <table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>3h-0h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>SP5</td></tr> <tr> <td>Fh-5h</td><td>Reserved.</td></tr> </table>	Value	Description	3h-0h	Reserved.	4h	SP5	Fh-5h	Reserved.
Value	Description								
3h-0h	Reserved.								
4h	SP5								
Fh-5h	Reserved.								
27:0	Reserved.								

CPUID_Fn80000001_ECX [Feature Identifiers] (Core::X86::Cpuid::FeatureExtIdEcx)	
Read-only.	
These values can be over-written by Core::X86::Msr::CPUID_ExtFeatures.	
_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000001_ECX	
Bits	Description
31	Reserved.
30	AdMskExtn: address mask extension support for instruction breakpoint. Read-only. Reset: Fixed,1. Indicates support for address mask extension (to 32 bits and to all 4 DRs) for instruction breakpoints.
29	MwaitExtended. Read-only. Reset: !Core::X86::Msr::HWCR[MonMwaitDis]. 1=MWAITX and MONITORX capability is supported.
28	PerfCtrExtLLC: Last Level Cache performance counter extensions. Read-only. Reset: Fixed,1. 1=Indicates support for L3 performance counter extensions.
27	PerfTsc. Read-only. Reset: Fixed,0. Performance time-stamp counter supported.
26	DataBreakpointExtension. Read-only. Reset: Fixed,1. 1=Indicates data breakpoint support for Core::X86::Msr::DR0_ADDR_MASK, Core::X86::Msr::DR1_ADDR_MASK, Core::X86::Msr::DR2_ADDR_MASK and Core::X86::Msr::DR3_ADDR_MASK.
25	Reserved.
24	PerfCtrExtDF: data fabric performance counter extensions support. Read-only. Reset: Fixed,1. 1=Indicates support for Core::X86::Msr::DF_PERF_CTL and Core::X86::Msr::DF_PERF_CTR.
23	PerfCtrExtCore: core performance counter extensions support. Read-only. Reset: Fixed,1. 1=Indicates support for Core::X86::Msr::PERF_CTL0 - 5 and Core::X86::Msr::PERF_CTR.
22	TopologyExtensions: topology extensions support. Read-only. Reset: Fixed,1. 1=Indicates support for Core::X86::Cpuid::CachePropEax0 and Core::X86::Cpuid::ExtApicId.
21:18	Reserved.
17	TCE. Read-only. Reset: Fixed,1. Translation cache extension.
16	FMA4. Read-only. Reset: Fixed,0. Four-operand FMA instruction support.
15	LWP. Read-only. Reset: Fixed,0. Lightweight profiling support.
14	Reserved.
13	WDT. Read-only. Reset: Fixed,1. Watchdog timer support.
12	SKINIT. Read-only. Reset: Fixed,1. SKINIT and STGI support.
11	XOP. Read-only. Reset: Fixed,0. Extended operation support.
10	IBS. Read-only. Reset: Fixed,1. Instruction Based Sampling.
9	OSVW. Read-only. Reset: Fixed,1. OS Visible Work-around support.
8	ThreeDNowPrefetch. Read-only. Reset: Fixed,1. Prefetch and PrefetchW instructions.
7	MisAlignSse. Read-only. Reset: Fixed,1. Misaligned SSE Mode.
6	SSE4A. Read-only. Reset: Fixed,1. EXTRQ, INSERTQ, MOVNTSS, and MOVNTSD instruction support.
5	ABM: advanced bit manipulation. Read-only. Reset: Fixed,1. LZCNT instruction support.
4	AltMovCr8. Read-only. Reset: Fixed,1. LOCK MOV CR0 means MOV CR8.
3	ExtApicSpace. Read-only. Reset: Fixed,1. Extended APIC register space.
2	SVM: Secure Virtual Mode feature. Read-only. Reset: Fixed,1. Indicates support for: VMRUN, VMLOAD, VMSAVE, CLGI, VMMCALL, and INVLPGA.
1	CmpLegacy. Read-only. Reset: Fixed,(Core::X86::Cpuid::SizeId[NC] > 0). 0=Single core product (Core::X86::Cpuid::SizeId[NC] == 0). 1=Multi core product (Core::X86::Cpuid::SizeId[NC] != 0). Core multi-processing legacy mode.
0	LahfSahf. Read-only. Reset: Fixed,1. LAHF and SAHF instruction support in 64-bit mode.

CPUID_Fn80000001_EDX [Feature Identifiers] (Core::X86::Cpuid::FeatureExtIdEdx)

Read-only.

These values can be over-written by Core::X86::Msr::CPUID_ExtFeatures.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000001_EDX

Bits	Description
31	ThreeDNow . Read-only. Reset: Fixed,0. 3DNow! instructions.
30	ThreeDNowExt . Read-only. Reset: Fixed,0. AMD extensions to 3DNow! instructions.
29	LM . Read-only. Reset: Fixed,1. Long Mode.
28	Reserved.
27	RDTSCP . Read-only. Reset: Fixed,1. RDTSCP instruction.
26	Page1GB . Read-only. Reset: Fixed,1. 1-GB large page support.
25	FFXSR . Read-only. Reset: Fixed,1. FXSAVE and FXRSTOR instruction optimizations.
24	FXSR . Read-only. Reset: Fixed,1. FXSAVE and FXRSTOR instructions.
23	MMX . Read-only. Reset: Fixed,1. MMX instructions.
22	MmxExt . Read-only. Reset: Fixed,1. AMD extensions to MMX instructions.
21	Reserved.
20	NX . Read-only. Reset: Fixed,1. No-execute page protection.
19:18	Reserved.
17	PSE36 . Read-only. Reset: Fixed,1. Page-size extensions.
16	PAT . Read-only. Reset: Fixed,1. Page attribute table.
15	CMOV . Read-only. Reset: Fixed,1. Conditional move instructions, CMOV, FCOMI, FCMOV.
14	MCA . Read-only. Reset: Fixed,1. Machine check architecture, MCG_CAP.
13	PGE . Read-only. Reset: Fixed,1. Page global extension, CR4.PGE.
12	MTRR . Read-only. Reset: Fixed,1. Memory-type range registers.
11	SysCallSysRet . Read-only. Reset: Fixed,1. SYSCALL and SYSRET instructions.
10	Reserved.
9	APIC: advanced programmable interrupt controller (APIC) exists and is enabled . Read-only. Reset: X. Reset is Core::X86::Msr::APIC_BAR[ApicEn].
8	CMPXCHG8B . Read-only. Reset: Fixed,1. CMPXCHG8B instruction.
7	MCE . Read-only. Reset: Fixed,1. Machine Check Exception, CR4.MCE.
6	PAE . Read-only. Reset: Fixed,1. Physical-address extensions (PAE).
5	MSR . Read-only. Reset: Fixed,1. Model-specific registers (MSRs), with RDMSR and WRMSR instructions.
4	TSC . Read-only. Reset: Fixed,1. Time stamp counter, RDTSC/RDTSCP instructions, CR4.TSD.
3	PSE . Read-only. Reset: Fixed,1. Page-size extensions (4 MB pages).
2	DE . Read-only. Reset: Fixed,1. Debugging extensions, IO breakpoints, CR4.DE.
1	VME . Read-only. Reset: Fixed,1. Virtual-mode enhancements.
0	FPU . Read-only. Reset: Fixed,1. x87 floating point unit on-chip.

**CPUID_Fn80000002_EAX [Processor Name String Identifier (Bytes [3:0])]
(Core::X86::Cpuid::ProcNameStr0Eax)**

Read-only.

Is an alias of Core::X86::Msr::ProcNameString_n0.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000002_EAX

Bits	Description
31:24	ProcNameByte3. Read-only. Reset: Core::X86::Msr::ProcNameString_n0[CpuNameString3]. Processor name, byte3.
23:16	ProcNameByte2. Read-only. Reset: Core::X86::Msr::ProcNameString_n0[CpuNameString2]. Processor name, byte2.
15:8	ProcNameByte1. Read-only. Reset: Core::X86::Msr::ProcNameString_n0[CpuNameString1]. Processor name, byte1.
7:0	ProcNameByte0. Read-only. Reset: Core::X86::Msr::ProcNameString_n0[CpuNameString0]. Processor name, byte0.

**CPUID_Fn80000002_EBX [Processor Name String Identifier (Bytes [7:4])]
(Core::X86::Cpuid::ProcNameStr0Ebx)**

Read-only.

Is an alias of Core::X86::Msr::ProcNameString_n0.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000002_EBX

Bits	Description
31:24	ProcNameByte7. Read-only. Reset: Core::X86::Msr::ProcNameString_n0[CpuNameString7]. Processor name, byte 7.
23:16	ProcNameByte6. Read-only. Reset: Core::X86::Msr::ProcNameString_n0[CpuNameString6]. Processor name, byte 6.
15:8	ProcNameByte5. Read-only. Reset: Core::X86::Msr::ProcNameString_n0[CpuNameString5]. Processor name, byte 5.
7:0	ProcNameByte4. Read-only. Reset: Core::X86::Msr::ProcNameString_n0[CpuNameString4]. Processor name, byte 4.

**CPUID_Fn80000002_ECX [Processor Name String Identifier (Bytes [11:8])]
(Core::X86::Cpuid::ProcNameStr0Ecx)**

Read-only.

Is an alias of Core::X86::Msr::ProcNameString_n1.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000002_ECX

Bits	Description
31:24	ProcNameByte11. Read-only. Reset: Core::X86::Msr::ProcNameString_n1[CpuNameString3]. Processor name, byte 11.
23:16	ProcNameByte10. Read-only. Reset: Core::X86::Msr::ProcNameString_n1[CpuNameString2]. Processor name, byte 10.
15:8	ProcNameByte9. Read-only. Reset: Core::X86::Msr::ProcNameString_n1[CpuNameString1]. Processor name, byte 9.
7:0	ProcNameByte8. Read-only. Reset: Core::X86::Msr::ProcNameString_n1[CpuNameString0]. Processor name, byte 8.

**CPUID_Fn80000002_EDX [Processor Name String Identifier (Bytes [15:12])]
(Core::X86::Cpuid::ProcNameStr0Edx)**

Read-only.

Is an alias of Core::X86::Msr::ProcNameString_n1.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000002_EDX

Bits	Description
31:24	ProcNameByte15. Read-only. Reset: Core::X86::Msr::ProcNameString_n1[CpuNameString7]. Processor name, byte 15.
23:16	ProcNameByte14. Read-only. Reset: Core::X86::Msr::ProcNameString_n1[CpuNameString6]. Processor name, byte 14.
15:8	ProcNameByte13. Read-only. Reset: Core::X86::Msr::ProcNameString_n1[CpuNameString5]. Processor name, byte 13.
7:0	ProcNameByte12. Read-only. Reset: Core::X86::Msr::ProcNameString_n1[CpuNameString4]. Processor name, byte 12.

**CPUID_Fn80000003_EAX [Processor Name String Identifier (Bytes [19:16])]
(Core::X86::Cpuid::ProcNameStr1Eax)**

Read-only.

Is an alias of Core::X86::Msr::ProcNameString_n2.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000003_EAX

Bits	Description
31:24	ProcNameByte19. Read-only. Reset: Core::X86::Msr::ProcNameString_n2[CpuNameString3]. Processor name, byte 19.
23:16	ProcNameByte18. Read-only. Reset: Core::X86::Msr::ProcNameString_n2[CpuNameString2]. Processor name, byte 18.
15:8	ProcNameByte17. Read-only. Reset: Core::X86::Msr::ProcNameString_n2[CpuNameString1]. Processor name, byte 17.
7:0	ProcNameByte16. Read-only. Reset: Core::X86::Msr::ProcNameString_n2[CpuNameString0]. Processor name, byte 16.

**CPUID_Fn80000003_EBX [Processor Name String Identifier (Bytes [23:20])]
(Core::X86::Cpuid::ProcNameStr1Ebx)**

Read-only.

Is an alias of Core::X86::Msr::ProcNameString_n2.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000003_EBX

Bits	Description
31:24	ProcNameByte23. Read-only. Reset: Core::X86::Msr::ProcNameString_n2[CpuNameString7]. Processor name, byte 23.
23:16	ProcNameByte22. Read-only. Reset: Core::X86::Msr::ProcNameString_n2[CpuNameString6]. Processor name, byte 22.
15:8	ProcNameByte21. Read-only. Reset: Core::X86::Msr::ProcNameString_n2[CpuNameString5]. Processor name, byte 21.
7:0	ProcNameByte20. Read-only. Reset: Core::X86::Msr::ProcNameString_n2[CpuNameString4]. Processor name, byte 20.

**CPUID_Fn80000003_ECX [Processor Name String Identifier (Bytes [27:24])]
(Core::X86::Cpuid::ProcNameStr1EcX)**

Read-only.

Is an alias of Core::X86::Msr::ProcNameString_n3.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000003_ECX

Bits	Description
31:24	ProcNameByte27. Read-only. Reset: Core::X86::Msr::ProcNameString_n3[CpuNameString3]. Processor name, byte 27.
23:16	ProcNameByte26. Read-only. Reset: Core::X86::Msr::ProcNameString_n3[CpuNameString2]. Processor name, byte 26.
15:8	ProcNameByte25. Read-only. Reset: Core::X86::Msr::ProcNameString_n3[CpuNameString1]. Processor name, byte 25.
7:0	ProcNameByte24. Read-only. Reset: Core::X86::Msr::ProcNameString_n3[CpuNameString0]. Processor name, byte 24.

**CPUID_Fn80000003_EDX [Processor Name String Identifier (Bytes [31:28])]
(Core::X86::Cpuid::ProcNameStr1EdX)**

Read-only.

Is an alias of Core::X86::Msr::ProcNameString_n3.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000003_EDX

Bits	Description
31:24	ProcNameByte31. Read-only. Reset: Core::X86::Msr::ProcNameString_n3[CpuNameString7]. Processor name, byte 31.
23:16	ProcNameByte30. Read-only. Reset: Core::X86::Msr::ProcNameString_n3[CpuNameString6]. Processor name, byte 30.
15:8	ProcNameByte29. Read-only. Reset: Core::X86::Msr::ProcNameString_n3[CpuNameString5]. Processor name, byte 29.
7:0	ProcNameByte28. Read-only. Reset: Core::X86::Msr::ProcNameString_n3[CpuNameString4]. Processor name, byte 28.

**CPUID_Fn80000004_EAX [Processor Name String Identifier (Bytes [35:32])]
(Core::X86::Cpuid::ProcNameStr2Eax)**

Read-only.

Is an alias of Core::X86::Msr::ProcNameString_n4.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000004_EAX

Bits	Description
31:24	ProcNameByte35. Read-only. Reset: Core::X86::Msr::ProcNameString_n4[CpuNameString3]. Processor name, byte 35.
23:16	ProcNameByte34. Read-only. Reset: Core::X86::Msr::ProcNameString_n4[CpuNameString2]. Processor name, byte 34.
15:8	ProcNameByte33. Read-only. Reset: Core::X86::Msr::ProcNameString_n4[CpuNameString1]. Processor name, byte 33.
7:0	ProcNameByte32. Read-only. Reset: Core::X86::Msr::ProcNameString_n4[CpuNameString0]. Processor name, byte 32.

**CPUID_Fn80000004_EBX [Processor Name String Identifier (Bytes [39:36])]
(Core::X86::Cpuid::ProcNameStr2Ebx)**

Read-only.

Is an alias of Core::X86::Msr::ProcNameString_n4.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000004_EBX

Bits	Description
31:24	ProcNameByte39. Read-only. Reset: Core::X86::Msr::ProcNameString_n4[CpuNameString7]. Processor name, byte 39.
23:16	ProcNameByte38. Read-only. Reset: Core::X86::Msr::ProcNameString_n4[CpuNameString6]. Processor name, byte 38.
15:8	ProcNameByte37. Read-only. Reset: Core::X86::Msr::ProcNameString_n4[CpuNameString5]. Processor name, byte 37.
7:0	ProcNameByte36. Read-only. Reset: Core::X86::Msr::ProcNameString_n4[CpuNameString4]. Processor name, byte 36.

**CPUID_Fn80000004_ECX [Processor Name String Identifier (Bytes [43:40])]
(Core::X86::Cpuid::ProcNameStr2EcX)**

Read-only.

Is an alias of Core::X86::Msr::ProcNameString_n5.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000004_ECX

Bits	Description
31:24	ProcNameByte43. Read-only. Reset: Core::X86::Msr::ProcNameString_n5[CpuNameString3]. Processor name, byte 43.
23:16	ProcNameByte42. Read-only. Reset: Core::X86::Msr::ProcNameString_n5[CpuNameString2]. Processor name, byte 42.
15:8	ProcNameByte41. Read-only. Reset: Core::X86::Msr::ProcNameString_n5[CpuNameString1]. Processor name, byte 41.
7:0	ProcNameByte40. Read-only. Reset: Core::X86::Msr::ProcNameString_n5[CpuNameString0]. Processor name, byte 40.

**CPUID_Fn80000004_EDX [Processor Name String Identifier (Bytes [47:44])]
(Core::X86::Cpuid::ProcNameStr2Edx)**

Read-only.

Is an alias of Core::X86::Msr::ProcNameString_n5.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000004_EDX

Bits	Description
31:24	ProcNameByte47. Read-only. Reset: Core::X86::Msr::ProcNameString_n5[CpuNameString7]. Processor name, byte 47.
23:16	ProcNameByte46. Read-only. Reset: Core::X86::Msr::ProcNameString_n5[CpuNameString6]. Processor name, byte 46.
15:8	ProcNameByte45. Read-only. Reset: Core::X86::Msr::ProcNameString_n5[CpuNameString5]. Processor name, byte 45.
7:0	ProcNameByte44. Read-only. Reset: Core::X86::Msr::ProcNameString_n5[CpuNameString4]. Processor name, byte 44.

CPUID_Fn80000005_EAX [L1 TLB 2M/4M Identifiers] (Core::X86::Cpuid::L1Tlb2M4M)

Read-only.

This function provides the processor's first level cache and TLB characteristics for each core.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000005_EAX

Bits	Description
31:24	L1DTlb2and4MAssoc: data TLB associativity for 2 MB and 4 MB pages. Read-only. Reset: Fixed,FFh. See Core::X86::Cpuid::L1DcId[L1DcAssoc].
23:16	L1DTlb2and4MSize: data TLB number of entries for 2 MB and 4 MB pages. Read-only. Reset: Fixed,72. The value returned is for the number of entries available for the 2 MB page size; 4 MB pages require two 2 MB entries, so the number of entries available for the 4 MB page size is one-half the returned value.
15:8	L1ITlb2and4MAssoc: instruction TLB associativity for 2 MB and 4 MB pages. Read-only. Reset: Fixed,FFh. See Core::X86::Cpuid::L1DcId[L1DcAssoc].
7:0	L1ITlb2and4MSize: instruction TLB number of entries for 2 MB and 4 MB pages. Read-only. Reset: Fixed,64. The value returned is for the number of entries available for the 2 MB page size; 4 MB pages require two 2 MB entries, so the number of entries available for the 4 MB page size is one-half the returned value.

CPUID_Fn80000005_EBX [L1 TLB 4K Identifiers] (Core::X86::Cpuid::L1Tlb4K)

Read-only.

See Core::X86::Cpuid::L1Tlb2M4M.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000005_EBX

Bits	Description
31:24	L1DTlb4KAssoc. Read-only. Reset: Fixed,FFh. Data TLB associativity for 4 KB pages. See Core::X86::Cpuid::L1DcId[L1DcAssoc].
23:16	L1DTlb4KSize. Read-only. Reset: Fixed,72. Data TLB number of entries for 4 KB pages.
15:8	L1ITlb4KAssoc. Read-only. Reset: Fixed,FFh. Instruction TLB associativity for 4 KB pages. See Core::X86::Cpuid::L1DcId[L1DcAssoc].
7:0	L1ITlb4KSize. Read-only. Reset: Fixed,64. Instruction TLB number of entries for 4 KB pages.

CPUID_Fn80000005_ECX [L1 Data Cache Identifiers] (Core::X86::Cpuid::L1DcId)

Read-only.

This function provides first level cache characteristics for each core.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000005_ECX

Bits	Description														
31:24	L1DcSize. Read-only. Reset: Fixed,32. L1 data cache size in KB.														
23:16	L1DcAssoc. Read-only. Reset: Fixed,08h. L1 data cache associativity. ValidValues:														
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>00h</td><td>Reserved</td></tr> <tr> <td>01h</td><td>1 way (direct mapped)</td></tr> <tr> <td>02h</td><td>2 way</td></tr> <tr> <td>03h</td><td>3 way</td></tr> <tr> <td>FEh-04h</td><td><Value> way</td></tr> <tr> <td>FFh</td><td>Fully associative</td></tr> </table>	Value	Description	00h	Reserved	01h	1 way (direct mapped)	02h	2 way	03h	3 way	FEh-04h	<Value> way	FFh	Fully associative
Value	Description														
00h	Reserved														
01h	1 way (direct mapped)														
02h	2 way														
03h	3 way														
FEh-04h	<Value> way														
FFh	Fully associative														
15:8	L1DcLinesPerTag. Read-only. Reset: Fixed,01h. L1 data cache lines per tag.														
7:0	L1DcLineSize. Read-only. Reset: Fixed,64. L1 data cache line size in bytes.														

CPUID_Fn80000005_EDX [L1 Instruction Cache Identifiers] (Core::X86::Cpuid::L1CId)

Read-only.

This function provides first level cache characteristics for each core.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000005_EDX

Bits	Description																
31:24	L1CSize. Read-only. Reset: Fixed,32. L1 instruction cache size KB.																
23:16	L1CAssoc. Read-only. Reset: Fixed,8. L1 instruction cache associativity. ValidValues: <table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>00h</td><td>Reserved</td></tr> <tr> <td>01h</td><td>1 way (direct mapped)</td></tr> <tr> <td>02h</td><td>2 way</td></tr> <tr> <td>03h</td><td>3 way</td></tr> <tr> <td>04h</td><td>4 way</td></tr> <tr> <td>FEh-05h</td><td><Value> way</td></tr> <tr> <td>FFh</td><td>Fully associative</td></tr> </table>	Value	Description	00h	Reserved	01h	1 way (direct mapped)	02h	2 way	03h	3 way	04h	4 way	FEh-05h	<Value> way	FFh	Fully associative
Value	Description																
00h	Reserved																
01h	1 way (direct mapped)																
02h	2 way																
03h	3 way																
04h	4 way																
FEh-05h	<Value> way																
FFh	Fully associative																
15:8	L1CLinesPerTag. Read-only. Reset: Fixed,01h. L1 instruction cache lines per tag.																
7:0	L1CLineSize. Read-only. Reset: Fixed,64. L1 instruction cache line size in bytes.																

CPUID_Fn80000006_EAX [L2 TLB 2M/4M Identifiers] (Core::X86::Cpuid::L2Tlb2M4M)

Read-only.

This function provides the processor's second level cache and TLB characteristics for each core.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000006_EAX

Bits	Description								
31:28	L2DTlb2and4MAssoc: L2 data TLB associativity for 2 MB and 4 MB pages. Read-only. Reset: Fixed,5h. ValidValues: <table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>4h-0h</td><td>Reserved.</td></tr> <tr> <td>5h</td><td>6 – 7 ways</td></tr> <tr> <td>Fh-6h</td><td>Reserved.</td></tr> </table>	Value	Description	4h-0h	Reserved.	5h	6 – 7 ways	Fh-6h	Reserved.
Value	Description								
4h-0h	Reserved.								
5h	6 – 7 ways								
Fh-6h	Reserved.								
27:16	L2DTlb2and4MSize: L2 data TLB number of entries for 2 MB and 4 MB pages. Read-only. Reset: Fixed,3072. The value returned is for the number of entries available for the 2 MB page size; 4 MB pages require two 2 MB entries, so the number of entries available for the 4 MB page size is one-half the returned value.								
15:12	L2ITlb2and4MAssoc: L2 instruction TLB associativity for 2 MB and 4 MB pages. Read-only. Reset: Fixed,2. ValidValues: <table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>1h-0h</td><td>Reserved.</td></tr> <tr> <td>2h</td><td>2 ways</td></tr> <tr> <td>Fh-3h</td><td>Reserved.</td></tr> </table>	Value	Description	1h-0h	Reserved.	2h	2 ways	Fh-3h	Reserved.
Value	Description								
1h-0h	Reserved.								
2h	2 ways								
Fh-3h	Reserved.								
11:0	L2ITlb2and4MSize: L2 instruction TLB number of entries for 2 MB and 4 MB pages. Read-only. Reset: Fixed,512. The value returned is for the number of entries available for the 2 MB page size; 4 MB pages require two 2 MB entries, so the number of entries available for the 4 MB page size is one-half the returned value.								

CPUID_Fn80000006_EBX [L2 TLB 4K Identifiers] (Core::X86::Cpuid::L2Tlb4K)

Read-only.

This function provides the processor's second level cache and TLB characteristics for each core.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000006_EBX

Bits	Description								
31:28	L2DTlb4KAssoc. Read-only. Reset: Fixed,6h. L2 data TLB associativity for 4 KB pages. ValidValues:								
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>5h-0h</td><td>Reserved.</td></tr> <tr> <td>6h</td><td>8 – 15 ways</td></tr> <tr> <td>Fh-7h</td><td>Reserved.</td></tr> </table>	Value	Description	5h-0h	Reserved.	6h	8 – 15 ways	Fh-7h	Reserved.
Value	Description								
5h-0h	Reserved.								
6h	8 – 15 ways								
Fh-7h	Reserved.								
27:16	L2DTlb4KSize. Read-only. Reset: Fixed,3072. L2 data TLB number of entries for 4 KB pages.								
15:12	L2ITlb4KAssoc. Read-only. Reset: Fixed,4. L2 instruction TLB associativity for 4 KB pages. ValidValues:								
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>3h-0h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>4 – 5 ways</td></tr> <tr> <td>Fh-5h</td><td>Reserved.</td></tr> </table>	Value	Description	3h-0h	Reserved.	4h	4 – 5 ways	Fh-5h	Reserved.
Value	Description								
3h-0h	Reserved.								
4h	4 – 5 ways								
Fh-5h	Reserved.								
11:0	L2ITlb4KSize. Read-only. Reset: Fixed,512. L2 instruction TLB number of entries for 4 KB pages.								

CPUID_Fn80000006_ECX [L2 Cache Identifiers] (Core::X86::Cpuid::L2CacheId)

Read-only.

This function provides second level cache characteristics for each core.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000006_ECX

Bits	Description																				
31:16	L2Size. Read-only. Reset: Fixed,0400h. L2 cache size in KB. ValidValues: <table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>00FFh-0000h</td><td>Reserved.</td></tr> <tr> <td>0100h</td><td>256 KB</td></tr> <tr> <td>01FFh-0101h</td><td>Reserved.</td></tr> <tr> <td>0200h</td><td>512 KB</td></tr> <tr> <td>03FFh-0201h</td><td>Reserved.</td></tr> <tr> <td>0400h</td><td>1 MB</td></tr> <tr> <td>07FFh-0401h</td><td>Reserved.</td></tr> <tr> <td>0800h</td><td>2 MB</td></tr> <tr> <td>FFFFh-0801h</td><td>Reserved.</td></tr> </table>	Value	Description	00FFh-0000h	Reserved.	0100h	256 KB	01FFh-0101h	Reserved.	0200h	512 KB	03FFh-0201h	Reserved.	0400h	1 MB	07FFh-0401h	Reserved.	0800h	2 MB	FFFFh-0801h	Reserved.
Value	Description																				
00FFh-0000h	Reserved.																				
0100h	256 KB																				
01FFh-0101h	Reserved.																				
0200h	512 KB																				
03FFh-0201h	Reserved.																				
0400h	1 MB																				
07FFh-0401h	Reserved.																				
0800h	2 MB																				
FFFFh-0801h	Reserved.																				
15:12	L2Assoc. Read-only. Reset: Fixed,6. L2 cache associativity. ValidValues: <table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>5h-0h</td><td>Reserved.</td></tr> <tr> <td>6h</td><td>8 – 15 ways</td></tr> <tr> <td>Fh-7h</td><td>Reserved.</td></tr> </table>	Value	Description	5h-0h	Reserved.	6h	8 – 15 ways	Fh-7h	Reserved.												
Value	Description																				
5h-0h	Reserved.																				
6h	8 – 15 ways																				
Fh-7h	Reserved.																				
11:8	L2LinesPerTag. Read-only. Reset: Fixed,1h. L2 cache lines per tag.																				
7:0	L2LineSize. Read-only. Reset: Fixed,64. L2 cache line size in bytes.																				

CPUID_Fn80000006_EDX [L3 Cache Identifiers] (Core::X86::Cpuid::L3CacheId)

Read-only.

This function provides third level cache characteristics shared by all cores of a processor.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000006_EDX

Bits Description31:18 **L3Size: L3 cache size.** Read-only. Reset: XXXXh. The L3 cache size in 512 KB units.**ValidValues:**

Value	Description
0000h	Disabled.
3FFFh-0001h	(<Value> * 0.5) MB

17:16 Reserved.

15:12 **L3Assoc.** Read-only. Reset: Fixed,9h. There are insufficient available encodings to represent all possible L3 associativities. Please refer to Core::X86::Cpuid::CachePropEbx3[CacheNumWays].**ValidValues:**

Value	Description
8h-0h	Reserved.
9h	Invalid, not reported here.
Fh-Ah	Reserved.

11:8 **L3LinesPerTag.** Read-only. Reset: Fixed,1h. L3 cache lines per tag.7:0 **L3LineSize.** Read-only. Reset: Fixed,64. L3 cache line size in bytes.**CPUID_Fn80000007_EAX [Reserved] (Core::X86::Cpuid::ProcFeedbackCap)**

Read-only. Reset: Fixed,0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000007_EAX

Bits Description

31:0 Reserved.

CPUID_Fn80000007_EBX [RAS Capabilities] (Core::X86::Cpuid::RasCap)

Read-only.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000007_EBX

Bits Description

31:4 Reserved.

3 **ScalableMca.** Read-only. Reset: Fixed,1. 0=Scalable MCA is not supported. 1=Scalable MCA is supported.2 **HWA.** Read-only. Reset: Fixed,0. Hardware assert supported.1 **SUCCOR: Software uncorrectable error containment and recovery capability.** Read-only. Reset: X. The processor supports software containment of uncorrectable errors through context synchronizing data poisoning and deferred error interrupts; MSR Core::X86::Msr::McaIntrCfg, MCA_STATUS[Deferred] and MCA_STATUS[Poisson] exist.0 **McaOverflowRecov: MCA overflow recovery support.** Read-only. Reset: Fixed,1. 0=MCA overflow conditions require software to shutdown the system. 1=MCA overflow conditions (MCA_STATUS[Overflow] == 1) are not fatal; software may safely ignore such conditions.**CPUID_Fn80000007_ECX [Advanced Power Management Information] (Core::X86::Cpuid::ApmInfoEcX)**

Read-only. Reset: Fixed,0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000007_ECX

Bits Description31:0 **CpuPwrSampleTimeRatio.** Read-only. Reset: Fixed,0000_0000h. Specifies the ratio of the compute unit power accumulator sample period to the TSC counter period.

CPUID_Fn80000007_EDX [Advanced Power Management Information] (Core::X86::Cpuid::ApmInfoEdx)

Read-only.

This function provides advanced power management feature identifiers.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000007_EDX

Bits	Description
31:16	Reserved.
15	FastCPPC . Read-only. Reset: Fixed,1. When set, indicates that Fast CPPC is supported.
14	RAPL . Read-only. Reset: Fixed,1. Running average power limit.
13	ConnectedStandby . Read-only. Reset: Fixed,1. Connected Standby.
12	ProcPowerReporting . Read-only. Reset: Fixed,0. Core power reporting interface supported.
11	ProcFeedbackInterface: processor feedback interface . Read-only. Reset: Fixed,0. 1=Indicates support for processor feedback interface; Core::X86::Cpuid::ProcFeedbackCap.
10	EffFreqRO: read-only effective frequency interface . Read-only. Reset: Fixed,1. Indicates presence of Core::X86::Msr::MPerfReadOnly and Core::X86::Msr::APerfReadOnly.
9	CPB: core performance boost . Read-only. Reset: X. 1=Indicates presence of Core::X86::Msr::HWCR[CpbDis] and support for core performance boost.
8	TscInvariant: TSC invariant . Read-only. Reset: Fixed,1. The TSC rate is invariant.
7	HwPstate: hardware P-state control . Read-only. Reset: Fixed,1. Core::X86::Msr::PStateCurLim, Core::X86::Msr::PStateCtl and Core::X86::Msr::PStateStat exist.
6	OneHundredMHzSteps . Read-only. Reset: Fixed,0. 100 MHz multiplier Control.
5	Reserved.
4	TM . Read-only. Reset: Fixed,1. Hardware thermal control (HTC)
3	TTP . Read-only. Reset: Fixed,1. THERMTRIP.
2:1	Reserved.
0	TS . Read-only. Reset: Fixed,1. Temperature sensor.

CPUID_Fn80000008_EAX [Long Mode Address Size Identifiers] (Core::X86::Cpuid::LongModeInfo)

Read-only. Reset: Fixed,0000_3030h.

This provides information about the maximum physical and linear address width supported by the processor.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000008_EAX

Bits	Description						
31:24	Reserved.						
23:16	GuestPhysAddrSize . Read-only. Reset: Fixed,00h. Maximum guest physical byte address size in bits. ValidValues:						
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>00h</td><td>The maximum guest physical address size defined by PhysAddrSize.</td></tr> <tr> <td>FFh-01h</td><td>The maximum guest physical address size defined by GuestPhysAddrSize.</td></tr> </table>	Value	Description	00h	The maximum guest physical address size defined by PhysAddrSize.	FFh-01h	The maximum guest physical address size defined by GuestPhysAddrSize.
Value	Description						
00h	The maximum guest physical address size defined by PhysAddrSize.						
FFh-01h	The maximum guest physical address size defined by GuestPhysAddrSize.						
15:8	LinAddrSize . Read-only. Reset: Fixed,30h. Maximum linear byte address size in bits.						
7:0	PhysAddrSize . Read-only. Reset: Fixed,30h. Maximum physical byte address size in bits.						

CPUID_Fn80000008_EBX [Extended Feature Extensions ID EBX] (Core::X86::Cpuid::FeatureExtIdEbx)

Read-only.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000008_EBX

Bits	Description
31:29	Reserved.
28	PSFD . Read-only. Reset: Fixed,1. Predictive Store Forward Disable. See Core::X86::Msr::SPEC_CTRL[PSFD].
27	CPPC . Read-only. Reset: 1. Collaborative Processor Performance Control.
26:25	Reserved.
24	SSBD: Speculative Store Bypass Disable . Read-only. Reset: Fixed,1.
23	PPIN: PPIN support . Read-only. Reset: X. 0=PPIN capability is not supported; Core::X86::Msr::PPIN_CTL and Core::X86::Msr::PPIN are treated as RAZ. 1=Indicates that Protected Processor Inventory Number (PPIN) capability can be enabled for privileged system inventory agent to read PPIN from Core::X86::Msr::PPIN. Protected Processor Inventory Number support.
22:21	Reserved.
20	EferLmsleUnsupported . Read-only. Reset: Fixed,1. 1=Core::X86::Msr::EFER[LMSLE] is not supported, and MBZ.
19	IbrrProvidesSameModeProtection . Read-only. Reset: 1. IBRS provides Same Mode Protection.
18	IbrrPreferred . Read-only. Reset: 1. 1=IBRS is preferred over software solution.
17	StibpAlwaysOn . Read-only. Reset: 1. Single Thread Indirect Branch Prediction Mode has Enhanced Performance and may be left Always On.
16	Reserved.
15	STIBP . Read-only. Reset: 1. Single Thread Indirect Branch Prediction.
14	IBRS . Read-only. Reset: 1. Indirect Branch Restricted Speculation.
13	INT_WBINVD . Read-only. Reset: 1. Interruptible WBINVD, WBNOINVD.
12	IBPB . Read-only. Reset: 1. Indirect Branch Prediction Barrier.
11:10	Reserved.
9	WBNOINVD . Read-only. Reset: 1. WBNOINVD writes all modified cache lines in the internal caches of the processor back to memory leaving the line valid (clean) in the internal caches.
8	MCOMMIT: memory commit . Read-only. Reset: 0. Memory commit instruction support.
7	Reserved.
6	MBE . Read-only. Reset: Fixed,1. Memory Bandwidth Enforcement.
5	Reserved.
4	RDPRU: read processor register at user level . Read-only. Reset: Fixed,1. RDPRU instruction allows reading MPERF and APERF at user level.
3	INVLPG . Read-only. Reset: Fixed,0. INVLPG instruction broadcasts a TLB invalidate to all threads in the system.
2	RstrFpErrPtrs . Read-only. Reset: Fixed,1. 1=FXSAVE, XSAVE, FXSAVEOPT, XSAVEC, XSAVES always save error pointers and FXRSTOR, XRSTOR, XRSTORS always restore error pointers is supported.
1	InstRetCntMsr: instructions retired count support . Read-only. Reset: Fixed,1. 1=Core::X86::Msr::IRPerfCount supported.
0	CLZERO: Clear Zero Instruction . Read-only. Reset: Fixed,1. CLZERO instruction zero's out the 64 byte cache line specified in RAX. Note: CLZERO instruction operations are cache-line aligned and RAX[5:0] is ignored.

CPUID_Fn80000008_ECX [Size Identifiers] (Core::X86::Cpuid::SizeId)

Read-only.

This provides information about the number of threads supported by the processor.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000008_ECX

Bits	Description
31:18	Reserved.
17:16	PerfTscSize: performance time-stamp counter size. Read-only. Reset: Fixed,0h.
15:12	ApicIdSize: APIC ID size. Read-only. Reset: Xh. The number of bits in the initial Core::X86::Apic::ApicId[ApicId] value that indicate thread ID within a package.
11:8	Reserved.
7:0	NC: number of threads - 1. Read-only. Reset: XXh. The number of threads in the package is NC+1 (e.g., if NC=0, then there is one thread).

CPUID_Fn80000008_EDX [Feature Extended Size Edx] (Core::X86::Cpuid::FeatureExtSizeEdx)

Read-only. Reset: Fixed,0001_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000008_EDX

Bits	Description
31:24	Reserved.
23:16	RdpruMax. Read-only. Reset: Fixed,01h. RDPRU Instruction max input supported.
15:0	Reserved.

CPUID_Fn8000000A_EAX [SVM Revision and Feature Identification] (Core::X86::Cpuid::SvmRevFeatIdEax)

Read-only. Reset: Fixed,0000_0001h. Enable: Core::X86::Cpuid::FeatureExtIdEcx[SVM].

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn8000000A_EAX

Bits	Description
31:8	Reserved.
7:0	SvmRev. Read-only. Reset: Fixed,01h. SVM revision.

CPUID_Fn8000000A_EBX [SVM Revision and Feature Identification] (Core::X86::Cpuid::SvmRevFeatIdEbx)

Read-only, Volatile. Reset: 0000_8000h. Enable: Core::X86::Cpuid::FeatureExtIdEcx[SVM].

This provides SVM revision and feature information.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn8000000A_EBX

Bits	Description
31:0	NASID: number of address space identifiers (ASID). Read-only, Volatile. Reset: 0000_8000h.

CPUID_Fn8000000A_EDX [SVM Revision and Feature Identification] (Core::X86::Cpuid::SvmRevFeatIdEdx)

Read-only. Enable: Core::X86::Cpuid::FeatureExtIdEcX[SVM].

This provides SVM feature information.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn8000000A_EDX

Bits	Description
31:29	Reserved.
28	VmcbAddrChkChg. Read-only. Reset: Fixed,1. VMCB address check change
27	ExtLvtOffsetFaultChg. Read-only. Reset: Fixed,1. 1=Read/Write fault behavior for the extended LVT offsets (APIC addresses 0x500-0x530) changed to Read Allowed, Write #MVEXIT (trap).
26	IbsVirt. Read-only. Reset: Fixed,1. IBS Virtualization
25	NmiVirt. Read-only. Reset: Fixed,1. Guest NMI Virtualization
24	Reserved.
23	HOST_MCE_OVERRIDE. Read-only. Reset: Fixed,1. 1=If hCR4:MCE == 1 and gCR4:MCE == 0, machine check exceptions (#MC) in guest do not cause shutdown and are always intercepted.
22	Reserved.
21	AllowNonWriteAbleGPT. Read-only. Reset: Fixed,1. 1=Indicates support for Non-Writeable Guest Pages for NPT.
20	GuestSpecCtrl. Read-only. Reset: Fixed,1. 1=Indicates support for Guest Spec_ctl.
19	SupervisorShadowStack. Read-only. Reset: Fixed,1. Supervisor Shadow Stack.
18	X2AVIC: virtualized X2APIC. Read-only. Reset: 0. 1=Virtualized X2APIC is supported.
17	GMET. Read-only. Reset: Fixed,1. Guest Mode Execute Trap.
16	vGIF. Read-only. Reset: Fixed,1. Virtualized GIF.
15	V_VMSAVE_VMLOAD. Read-only. Reset: Fixed,1. Virtualized VMLOAD and VMSAVE.
14	Reserved.
13	AVIC: AMD virtual interrupt controller. Read-only. Reset: 0. 1=Support indicated for SVM mode virtualized interrupt controller; Indicates support for Core::X86::Msr::AvicDoorbell.
12	PauseFilterThreshold. Read-only. Reset: Fixed,1. PAUSE filter threshold.
11	Reserved.
10	PauseFilter. Read-only. Reset: Fixed,1. Pause intercept filter.
9:8	Reserved.
7	DecodeAssists. Read-only. Reset: Fixed,1. Decode assists.
6	FlushByAsid. Read-only. Reset: Fixed,1. Flush by ASID.
5	VmcbClean. Read-only. Reset: Fixed,1. VMCB clean bits.
4	TscRateMsr: MSR based TSC rate control. Read-only. Reset: Fixed,1. 1=Indicates support for TSC ratio Core::X86::Msr::TscRateMsr.
3	NRIPS. Read-only. Reset: Fixed,1. NRIP Save.
2	SVML. Read-only. Reset: Fixed,1. SVM lock.
1	LbrVirt. Read-only. Reset: Fixed,1. LBR virtualization.
0	NP. Read-only. Reset: Fixed,1. Nested Paging.

CPUID_Fn80000019_EAX [L1 TLB 1G Identifiers] (Core::X86::Cpuid::L1Tlb1G)

Read-only.

This function provides first level TLB characteristics for 1GB pages.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000019_EAX

Bits	Description
31:28	L1DTlb1GAssoc : L1 data TLB associativity for 1 GB pages. Read-only. Reset: Fixed,Fh. See Core::X86::Cpuid::L2CacheId[L2Assoc].
27:16	L1DTlb1GSize . Read-only. Reset: Fixed,72. L1 data TLB number of entries for 1 GB pages.
15:12	L1ITlb1GAssoc . Read-only. Reset: Fixed,Fh. L1 instruction TLB associativity for 1 GB pages. See Core::X86::Cpuid::L2CacheId[L2Assoc].
11:0	L1ITlb1GSize . Read-only. Reset: Fixed,64. L1 instruction TLB number of entries for 1 GB pages.

CPUID_Fn80000019_EBX [L2 TLB 1G Identifiers] (Core::X86::Cpuid::L2Tlb1G)

Read-only. Reset: Fixed,F040_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000019_EBX

Bits	Description
31:28	L2DTlb1GAssoc . Read-only. Reset: Fixed,Fh. L2 data TLB associativity for 1 GB pages.
27:16	L2DTlb1GSize . Read-only. Reset: Fixed,040h. L2 data TLB number of entries for 1 GB pages.
15:12	L2ITlb1GAssoc . Read-only. Reset: Fixed,0h. L2 instruction TLB associativity for 1 GB pages.
11:0	L2ITlb1GSize . Read-only. Reset: Fixed,000h. L2 instruction TLB number of entries for 1 GB pages.

CPUID_Fn8000001A_EAX [Performance Optimization Identifiers] (Core::X86::Cpuid::PerfOptId)

Read-only. Reset: Fixed,0000_0006h.

This function returns performance related information.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn8000001A_EAX

Bits	Description
31:3	Reserved.
2	FP256 . Read-only. Reset: Fixed,1. When set, the internal FP/SIMD execution datapath is 256-bits wide.
1	MOVU . Read-only. Reset: Fixed,1. MOVU SSE instructions are more efficient and should be preferred to SSE MOVL/MOVH. MOVUPS is more efficient than MOVLPS/MOVHPS. MOVUPD is more efficient than MOVLPS/MOVHPS.
0	FP128 . Read-only. Reset: Fixed,0. When set, the internal FP/SIMD execution datapath is 128-bits wide.

CPUID_Fn8000001B_EAX [Instruction Based Sampling Identifiers] (Core::X86::Cpuid::IbsIdEax)

Read-only. Reset: Fixed, 0000_0BFFh.

This function returns IBS feature information.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn8000001B_EAX

Bits	Description
31:12	Reserved.
11	Zen4IbsExtensions. Read-only. Reset: Fixed, 1. Fetch and Op IBS support IBS extensions added with Zen4: Core::X86::Msr::IBS_FETCH_CTL[IbsFetchL3Miss], Core::X86::Msr::IBS_FETCH_CTL[IbsFetchOcMiss], Core::X86::Msr::IBS_FETCH_CTL[IbsL3MissOnly] and Core::X86::Msr::IBS_OP_DATA2 DataSrc extension.
10	IbsOpData4. Read-only. Reset: Fixed, 0. IBS op data 4 MSR supported.
9	IbsFetchCtlExtd: IBS fetch control extended MSR supported. Read-only. Reset: Fixed, 1. Indicates support for Core::X86::Msr::IC_IBS_EXTD_CTL.
8	OpFuse: fused branch op indication supported. Read-only. Reset: Fixed, 1. Indicates support for Core::X86::Msr::IBS_OP_DATA[IbsOpFuse].
7	RipInvalidChk: invalid RIP indication supported. Read-only. Reset: Fixed, 1. Indicates support for Core::X86::Msr::IBS_OP_DATA[IbsRipInvalid].
6	OpCntExt: IbsOpCurCnt and IbsOpMaxCnt extend by 7 bits. Read-only. Reset: Fixed, 1. Indicates support for Core::X86::Msr::IBS_OP_CTL[IbsOpCurCnt[26:20], IbsOpMaxCnt[26:20]].
5	BrnTrgt. Read-only. Reset: Fixed, 1. Branch target address reporting supported.
4	OpCnt. Read-only. Reset: Fixed, 1. Op counting mode supported.
3	RdWrOpCnt. Read-only. Reset: Fixed, 1. Read write of op counter supported.
2	OpSam. Read-only. Reset: Fixed, 1. IBS execution sampling supported.
1	FetchSam. Read-only. Reset: Fixed, 1. IBS fetch sampling supported.
0	IBSFFV. Read-only. Reset: Fixed, 1. IBS feature flags valid.

CPUID_Fn8000001D_EAX_x00 [Cache Properties (DC)] (Core::X86::Cpuid::CachePropEax0)

Enable: Core::X86::Cpuid::FeatureExtIdEcx[TopologyExtensions].

Core::X86::Cpuid::CachePropEax0 reports topology information for the DC.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn8000001D_EAX_x00

Bits	Description
31:26	Reserved.
25:14	NumSharingCache: number of logical processors sharing cache. Read-only. Reset: XXXh. The number of logical processors sharing this cache is NumSharingCache + 1.
13:10	Reserved.
9	FullyAssociative: fully associative cache. Read-only. Reset: Fixed,0. 1=Cache is fully associative.
8	SelfInitialization: cache is self-initializing. Read-only. Reset: Fixed,1. 1=Cache is self initializing; cache does not need software initialization.
7:5	CacheLevel: cache level. Read-only. Reset: Fixed,1h. Identifies the cache level.
ValidValues:	
Value	Description
0h	Reserved.
1h	Level 1
2h	Level 2
3h	Level 3
7h-4h	Reserved.
4:0	CacheType: cache type. Read-only. Reset: Fixed,01h. Identifies the type of cache.
ValidValues:	
Value	Description
00h	Null; no more caches.
01h	Data cache.
02h	Instruction cache.
03h	Unified cache.
1Fh-04h	Reserved.

CPUID_Fn8000001D_EAX_x01 [Cache Properties (IC)] (Core::X86::Cpuid::CachePropEax1)

Read-only. Enable: Core::X86::Cpuid::FeatureExtIdEcx[TopologyExtensions].

Core::X86::Cpuid::CachePropEax1 reports topology information for the IC. See Core::X86::Cpuid::CachePropEax0.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn8000001D_EAX_x01

Bits	Description
31:26	Reserved.
25:14	NumSharingCache: number of logical processors sharing cache. Read-only. Reset: XXXh. See Core::X86::Cpuid::CachePropEax0[NumSharingCache].
13:10	Reserved.
9	FullyAssociative: fully associative cache. Read-only. Reset: Fixed,0. See Core::X86::Cpuid::CachePropEax0[FullyAssociative].
8	SelfInitialization: cache is self-initializing. Read-only. Reset: Fixed,1. See Core::X86::Cpuid::CachePropEax0[SelfInitialization].
7:5	CacheLevel: cache level. Read-only. Reset: Fixed,1h. Identifies the cache level. See Core::X86::Cpuid::CachePropEax0[CacheLevel].
4:0	CacheType: cache type. Read-only. Reset: Fixed,02h. See Core::X86::Cpuid::CachePropEax0[CacheType].

CPUID_Fn8000001D_EAX_x02 [Cache Properties (L2)] (Core::X86::Cpuid::CachePropEax2)

Read-only. Enable: Core::X86::Cpuid::FeatureExtIdEcx[TopologyExtensions].

Core::X86::Cpuid::CachePropEax2 reports topology information for the L2. See Core::X86::Cpuid::CachePropEax0.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn8000001D_EAX_x02

Bits	Description
31:26	Reserved.
25:14	NumSharingCache: number of logical processors sharing cache. Read-only. Reset: XXXh. Core::X86::Cpuid::CachePropEax0[NumSharingCache].
13:10	Reserved.
9	FullyAssociative: fully associative cache. Read-only. Reset: Fixed,0. Core::X86::Cpuid::CachePropEax0[FullyAssociative].
8	SelfInitialization: cache is self-initializing. Read-only. Reset: Fixed,1. Core::X86::Cpuid::CachePropEax0[SelfInitialization].
7:5	CacheLevel: cache level. Read-only. Reset: Fixed,2h. Identifies the cache level. Core::X86::Cpuid::CachePropEax0[CacheLevel].
4:0	CacheType: cache type. Read-only. Reset: Fixed,03h. Core::X86::Cpuid::CachePropEax0[CacheType].

CPUID_Fn8000001D_EAX_x03 [Cache Properties (L3)] (Core::X86::Cpuid::CachePropEax3)

Read-only. Enable: Core::X86::Cpuid::FeatureExtIdEcx[TopologyExtensions].

Core::X86::Cpuid::CachePropEax3 reports topology information for the L3.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn8000001D_EAX_x03

Bits	Description
31:26	Reserved.
25:14	NumSharingCache: number of logical processors sharing cache. Read-only. Reset: XXXh. The number of logical processors sharing this cache is NumSharingCache + 1.
13:10	Reserved.
9	FullyAssociative: fully associative cache. Read-only. Reset: Fixed,0. Core::X86::Cpuid::CachePropEax0[FullyAssociative].
8	SelfInitialization: cache is self-initializing. Read-only. Reset: Fixed,1. Core::X86::Cpuid::CachePropEax0[SelfInitialization].
7:5	CacheLevel: cache level. Read-only. Reset: Fixed,3h. Identifies the cache level. Core::X86::Cpuid::CachePropEax0[CacheLevel].
4:0	CacheType: cache type. Read-only. Reset: Fixed,03h. Core::X86::Cpuid::CachePropEax0[CacheType].

CPUID_Fn8000001D_EAX_x04 [Cache Properties Null] (Core::X86::Cpuid::CachePropEax4)

Read-only. Reset: Fixed,0000_0000h. Enable: Core::X86::Cpuid::FeatureExtIdEcx[TopologyExtensions].

Core::X86::Cpuid::CachePropEax4 reports done/null. See Core::X86::Cpuid::CachePropEax0.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn8000001D_EAX_x04

Bits	Description
31:5	Reserved.
4:0	CacheType: cache type. Read-only. Reset: Fixed,00h. Core::X86::Cpuid::CachePropEax0[CacheType].

CPUID_Fn8000001D_EBX_x00 [Cache Properties (DC)] (Core::X86::Cpuid::CachePropEbx0)

Read-only. Reset: Fixed,01C0_003Fh. Enable: Core::X86::Cpuid::FeatureExtIdEcx[TopologyExtensions].

Core::X86::Cpuid::CachePropEbx0 reports topology information for the DC. See Core::X86::Cpuid::CachePropEax0.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn8000001D_EBX_x00

Bits	Description
31:22	CacheNumWays: cache number of ways. Read-only. Reset: Fixed,007h. Cache number of ways is CacheNumWays + 1.
21:12	CachePhysPartitions: cache physical line partitions. Read-only. Reset: Fixed,000h. Cache partitions is CachePhysPartitions + 1.
11:0	CacheLineSize: cache line size in bytes. Read-only. Reset: Fixed,03Fh. Cache line size in bytes is CacheLineSize + 1.

CPUID_Fn8000001D_EBX_x01 [Cache Properties (IC)] (Core::X86::Cpuid::CachePropEbx1)

Read-only. Reset: Fixed,01C0_003Fh. Enable: Core::X86::Cpuid::FeatureExtIdEcx[TopologyExtensions].

Core::X86::Cpuid::CachePropEbx1 reports topology information for the IC. See Core::X86::Cpuid::CachePropEax0.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn8000001D_EBX_x01

Bits	Description
31:22	CacheNumWays: cache number of ways. Read-only. Reset: Fixed,007h. Core::X86::Cpuid::CachePropEbx0[CacheNumWays].
21:12	CachePhysPartitions: cache physical line partitions. Read-only. Reset: Fixed,000h. Core::X86::Cpuid::CachePropEbx0[CachePhysPartitions].
11:0	CacheLineSize: cache line size in bytes. Read-only. Reset: Fixed,03Fh. Core::X86::Cpuid::CachePropEbx0[CacheLineSize].

CPUID_Fn8000001D_EBX_x02 [Cache Properties (L2)] (Core::X86::Cpuid::CachePropEbx2)

Read-only. Reset: Fixed,01C0_003Fh. Enable: Core::X86::Cpuid::FeatureExtIdEcx[TopologyExtensions].

Core::X86::Cpuid::CachePropEbx2 reports topology information for the L2. See Core::X86::Cpuid::CachePropEax0.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn8000001D_EBX_x02

Bits	Description
31:22	CacheNumWays: cache number of ways. Read-only. Reset: Fixed,007h. See Core::X86::Cpuid::CachePropEbx0[CacheNumWays].
21:12	CachePhysPartitions: cache physical line partitions. Read-only. Reset: Fixed,000h. See Core::X86::Cpuid::CachePropEbx0[CachePhysPartitions].
11:0	CacheLineSize: cache line size in bytes. Read-only. Reset: Fixed,03Fh. See Core::X86::Cpuid::CachePropEbx0[CacheLineSize].

CPUID_Fn8000001D_EBX_x03 [Cache Properties (L3)] (Core::X86::Cpuid::CachePropEbx3)

Read-only. Reset: Fixed,03C0_003Fh. Enable: Core::X86::Cpuid::FeatureExtIdEcx[TopologyExtensions].

Core::X86::Cpuid::CachePropEbx3 reports topology information for the L3. See Core::X86::Cpuid::CachePropEax0.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn8000001D_EBX_x03

Bits	Description
31:22	CacheNumWays: cache number of ways. Read-only. Reset: Fixed,00Fh. See Core::X86::Cpuid::CachePropEbx0[CacheNumWays].
21:12	CachePhysPartitions: cache physical line partitions. Read-only. Reset: Fixed,000h. See Core::X86::Cpuid::CachePropEbx0[CachePhysPartitions].
11:0	CacheLineSize: cache line size in bytes. Read-only. Reset: Fixed,03Fh. See Core::X86::Cpuid::CachePropEbx0[CacheLineSize].

CPUID_Fn8000001D_EBX_x04 [Cache Properties Null] (Core::X86::Cpuid::CachePropEbx4)

Read-only. Reset: Fixed,0000_0000h. Enable: Core::X86::Cpuid::FeatureExtIdEcX[TopologyExtensions].

Core::X86::Cpuid::CachePropEax4 reports done/null. See Core::X86::Cpuid::CachePropEax0.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn8000001D_EBX_x04

Bits Description

31:0 Reserved.

CPUID_Fn8000001D_ECX_x00 [Cache Properties (DC)] (Core::X86::Cpuid::CachePropEcX0)

Read-only. Reset: Fixed,0000_003Fh. Enable: Core::X86::Cpuid::FeatureExtIdEcX[TopologyExtensions].

Core::X86::Cpuid::CachePropEcX0 reports topology information for the DC. See Core::X86::Cpuid::CachePropEax0.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn8000001D_ECX_x00

Bits Description31:0 **CacheNumSets: cache number of sets.** Read-only. Reset: Fixed,0000_003Fh. Cache number of sets is CacheNumSets + 1.**CPUID_Fn8000001D_ECX_x01 [Cache Properties (IC)] (Core::X86::Cpuid::CachePropEcX1)**

Read-only. Reset: Fixed,0000_003Fh. Enable: Core::X86::Cpuid::FeatureExtIdEcX[TopologyExtensions].

Core::X86::Cpuid::CachePropEcX1 reports topology information for the IC. See Core::X86::Cpuid::CachePropEax0.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn8000001D_ECX_x01

Bits Description31:0 **CacheNumSets: cache number of sets.** Read-only. Reset: Fixed,0000_003Fh. See Core::X86::Cpuid::CachePropEcX0[CacheNumSets].**CPUID_Fn8000001D_ECX_x02 [Cache Properties (L2)] (Core::X86::Cpuid::CachePropEcX2)**

Read-only. Reset: Fixed,0000_07FFh. Enable: Core::X86::Cpuid::FeatureExtIdEcX[TopologyExtensions].

Core::X86::Cpuid::CachePropEcX2 reports topology information for the L2. See Core::X86::Cpuid::CachePropEax0.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn8000001D_ECX_x02

Bits Description31:0 **CacheNumSets: cache number of sets.** Read-only. Reset: Fixed,0000_07FFh. See Core::X86::Cpuid::CachePropEcX0[CacheNumSets].

CPUID_Fn8000001D_ECX_x03 [Cache Properties (L3)] (Core::X86::Cpuid::CachePropEc3)

Read-only. Enable: Core::X86::Cpuid::FeatureExtIdEc3[TopologyExtensions].

Core::X86::Cpuid::CachePropEc3 reports topology information for the L3.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn8000001D_ECX_x03

Bits	Description												
31:0	CacheNumSets: cache number of sets. Read-only. Reset: 0000_XXXXh. See Core::X86::Cpuid::CachePropEc0[CacheNumSets].												
	ValidValues:												
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0000_3 FFeh- 0000_0 000h</td><td>Reserved.</td></tr> <tr> <td>0000_3 FFFh</td><td>16384 L3 Cache Sets.</td></tr> <tr> <td>0000_7 FFeh- 0000_4 000h</td><td>Reserved.</td></tr> <tr> <td>0000_7 FFFh</td><td>32768 L3 Cache Sets.</td></tr> <tr> <td>FFFF_F FFFh- 0000_8 000h</td><td>Reserved.</td></tr> </table>	Value	Description	0000_3 FFeh- 0000_0 000h	Reserved.	0000_3 FFFh	16384 L3 Cache Sets.	0000_7 FFeh- 0000_4 000h	Reserved.	0000_7 FFFh	32768 L3 Cache Sets.	FFFF_F FFFh- 0000_8 000h	Reserved.
Value	Description												
0000_3 FFeh- 0000_0 000h	Reserved.												
0000_3 FFFh	16384 L3 Cache Sets.												
0000_7 FFeh- 0000_4 000h	Reserved.												
0000_7 FFFh	32768 L3 Cache Sets.												
FFFF_F FFFh- 0000_8 000h	Reserved.												

CPUID_Fn8000001D_ECX_x04 [Cache Properties Null] (Core::X86::Cpuid::CachePropEc4)

Read-only. Reset: Fixed,0000_0000h. Enable: Core::X86::Cpuid::FeatureExtIdEc3[TopologyExtensions].

Core::X86::Cpuid::CachePropEc4 reports done/null. See Core::X86::Cpuid::CachePropEc0.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn8000001D_ECX_x04

Bits	Description
31:0	CacheNumSets. Read-only. Reset: Fixed,0000_0000h. Cache number of sets.

CPUID_Fn8000001D_EDX_x00 [Cache Properties (DC)] (Core::X86::Cpuid::CachePropEdx0)

Read-only. Reset: Fixed,0000_0000h. Enable: Core::X86::Cpuid::FeatureExtIdEc3[TopologyExtensions].

Core::X86::Cpuid::CachePropEdx0 reports topology information for the DC. See Core::X86::Cpuid::CachePropEc0.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn8000001D_EDX_x00

Bits	Description
31:2	Reserved.
1	CacheInclusive: cache inclusive. Read-only. Reset: Fixed,0. 0=Cache is not inclusive of lower cache levels. 1=Cache is inclusive of lower cache levels.
0	WBINVD: Write-Back Invalidate/Invalidate. Read-only. Reset: Fixed,0. 0=WBINVD/INVD invalidates all lower level caches of non-originating cores sharing this cache. 1=WBINVD/INVD not ensured to invalidate all lower level caches of non-originating cores sharing this cache.

CPUID_Fn8000001D_EDX_x01 [Cache Properties (IC)] (Core::X86::Cpuid::CachePropEdx1)

Read-only. Reset: Fixed,0000_0000h. Enable: Core::X86::Cpuid::FeatureExtIdEcx[TopologyExtensions].

Core::X86::Cpuid::CachePropEdx1 reports topology information for the IC. See Core::X86::Cpuid::CachePropEax0.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn8000001D_EDX_x01

Bits	Description
31:2	Reserved.
1	CacheInclusive: cache inclusive. Read-only. Reset: Fixed,0. See Core::X86::Cpuid::CachePropEdx0[CacheInclusive].
0	WBINVD: Write-Back Invalidate/Invalidate. Read-only. Reset: Fixed,0. 0=WBINVD/INVD invalidates all lower level caches of non-originating cores sharing this cache. 1=WBINVD/INVD may not invalidate all lower level caches of non-originating cores sharing this cache. See Core::X86::Cpuid::CachePropEdx0[WBINVD].

CPUID_Fn8000001D_EDX_x02 [Cache Properties (L2)] (Core::X86::Cpuid::CachePropEdx2)

Read-only. Reset: Fixed,0000_0002h. Enable: Core::X86::Cpuid::FeatureExtIdEcx[TopologyExtensions].

Core::X86::Cpuid::CachePropEdx2 reports topology information for the L2. See Core::X86::Cpuid::CachePropEax0.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn8000001D_EDX_x02

Bits	Description
31:2	Reserved.
1	CacheInclusive: cache inclusive. Read-only. Reset: Fixed,1. See Core::X86::Cpuid::CachePropEdx0[CacheInclusive].
0	WBINVD: Write-Back Invalidate/Invalidate. Read-only. Reset: Fixed,0. 0=WBINVD/INVD invalidates all lower level caches of non-originating cores sharing this cache. 1=WBINVD/INVD may not invalidate all lower level caches of non-originating cores sharing this cache.

CPUID_Fn8000001D_EDX_x03 [Cache Properties (L3)] (Core::X86::Cpuid::CachePropEdx3)

Read-only. Reset: Fixed,0000_0001h. Enable: Core::X86::Cpuid::FeatureExtIdEcx[TopologyExtensions].

Core::X86::Cpuid::CachePropEdx3 reports reports topology information for the L3. See

Core::X86::Cpuid::CachePropEax0.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn8000001D_EDX_x03

Bits	Description
31:2	Reserved.
1	CacheInclusive: cache inclusive. Read-only. Reset: Fixed,0. See Core::X86::Cpuid::CachePropEdx0[CacheInclusive].
0	WBINVD: Write-Back Invalidate/Invalidate. Read-only. Reset: Fixed,1. 0=WBINVD/INVD invalidates all lower level caches of non-originating cores sharing this cache. 1=WBINVD/INVD may not invalidate all lower level caches of non-originating cores sharing this cache.

CPUID_Fn8000001D_EDX_x04 [Cache Properties Null] (Core::X86::Cpuid::CachePropEdx4)

Read-only. Reset: Fixed,0000_0000h. Enable: Core::X86::Cpuid::FeatureExtIdEcx[TopologyExtensions].

Core::X86::Cpuid::CachePropEax3 reports done/null. See Core::X86::Cpuid::CachePropEax0.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn8000001D_EDX_x04

Bits	Description
31:0	Reserved.

CPUID_Fn8000001E_EAX [Extended APIC ID] (Core::X86::Cpuid::ExtApicId)

Read-only. Enable: (Core::X86::Cpuid::FeatureExtIdEcX[TopologyExtensions] && Core::X86::Msr::APIC_BAR[ApicEn]).

If Core::X86::Cpuid::FeatureExtIdEcX[TopologyExtensions] == 0 then CPUID Fn8000001E_E[D,C,B,A]X are reserved.
If (Core::X86::Msr::APIC_BAR[ApicEn] == 0) then Core::X86::Cpuid::ExtApicId[ExtendedApicId] is Reserved.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn8000001E_EAX

Bits	Description
31:0	ExtendedApicId: extended APIC ID. Read-only. Reserved. Reset: (Core::X86::Msr::APIC_BAR[ApicEn] && Core::X86::Msr::APIC_BAR[x2ApicEn]) ? Core::X86::Msr::APIC_ID[ApicId[31:0]] : Core::X86::Msr::APIC_BAR[ApicEn] ? {00_0000h , Core::X86::Apic::ApicId[ApicId]} : 0000_0000h.

CPUID_Fn8000001E_EBX [Core Identifiers] (Core::X86::Cpuid::CoreId)

Read-only. Enable: Core::X86::Cpuid::FeatureExtIdEcX[TopologyExtensions].

See Core::X86::Cpuid::ExtApicId.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn8000001E_EBX

Bits	Description
31:16	Reserved.
15:8	ThreadsPerCore: threads per core. Read-only. Reset: XXh. The number of threads per core is ThreadsPerCore+1.
7:0	CoreId: core ID. Read-only. Reset: XXh. Identifies the unique per-socket logical core unit ID.

CPUID_Fn8000001E_ECX [Node Identifiers] (Core::X86::Cpuid::NodeId)

Read-only. Enable: Core::X86::Cpuid::FeatureExtIdEcX[TopologyExtensions].

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn8000001E_ECX

Bits	Description						
31:11	Reserved.						
10:8	NodesPerProcessor: Node per processor. Read-only. Reset: XXXb. ValidValues:						
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>1 node per processor.</td></tr> <tr> <td>7h-1h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	1 node per processor.	7h-1h	Reserved.
Value	Description						
0h	1 node per processor.						
7h-1h	Reserved.						
7:0	NodeId: Node ID. Read-only. Reset: Fixed,XXh.						

CPUID_Fn8000001F_EAX [AMD Secure Encryption EAX] (Core::X86::Cpuid::SecureEncryptionEax)

Read-only.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn8000001F_EAX

Bits	Description
31:25	Reserved.
24	VmsaRegProt. Read-only. Reset: Fixed,0. VMSA Register Protection is supported.
23:20	Reserved.
19	IbsVirtualization. Read-only. Reset: Fixed,0. IBS state virtualization is supported for SEV-ES guests via opt-in control in SEV_FEATURES.
18	VirtualTomMsr. Read-only. Reset: Fixed,0. Virtual TOM MSR is supported.
17	VmexitParameter. Read-only. Reset: Fixed,0. VmexitParameter is supported in SEV_FEATURES.
16	VTE: Virtual Transparent Encryption for SEV. Read-only. Reset: Fixed,0. The Virtual Transparent Encryption feature can be enabled to force all memory accesses within an SEV guest to be encrypted with the guest's key. When enabled the hardware pretends that the C-bits for all guest mode accesses are 1 regardless of the actual guest page tables.
15	PreventHostIBS. Read-only. Reset: Fixed,0. Prevent host IBS for a SEV-ES guest.
14	DebugStateSwap. Read-only. Reset: Fixed,0. 1=DR0-3 and DR0-3_MASK can be saved/restored on world switches.
13	AlternateInjection. Read-only. Reset: Fixed,0. 1=SEV-ES guests can use an encrypted vmcb field for event injection.
12	RestrictInjection. Read-only. Reset: Fixed,0. 1=SEV-ES guests can refuse all event-injections except #HV.
11	Req64BitHypervisor. Read-only. Reset: Fixed,0. Require 64-Bit Hypervisor.
10	CoherencyEnforced. Read-only. Reset: Fixed,0. Hardware enforces cache coherency.
9	TscAuxVirtualization. Read-only. Reset: Fixed,0. Hardware virtualizes TSC_AUX.
8	SecureTsc. Read-only. Reset: Fixed,0. Support for Secure TSC.
7	VmplSSS. Read-only. Reset: 0. The Supervisor Shadow Stack bit is supported in the VMPL permission set.
6	RMPQUERY. Read-only. Reset: 0. The RMPQUERY instruction is supported.
5	VMPL. Read-only. Reset: Fixed,0. Multiple SNP guests can share memory using differing permissions.
4	SNP. Read-only. Reset: Fixed,0. RMP table can be enabled to protect memory even from hypervisor.
3	SevEs. Read-only. Reset: Fixed,0. Secure Encrypted ES.
2	VmPgFlush: VM Page Flush MSR support. Read-only. Reset: Fixed,0. Core::X86::Msr::VMPAGE_FLUSH is no longer supported.
1	SEV. Read-only. Reset: Fixed,0. Secure Encrypted Virtualization supported.
0	SME. Read-only. Reset: Fixed,1. Secure Memory Encryption supported.

CPUID_Fn8000001F_EBX [AMD Secure Encryption EBX] (Core::X86::Cpuid::SecureEncryptionEbx)

Read-only.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn8000001F_EBX

Bits	Description																		
31:16	Reserved.																		
15:12	VmplSupported. Read-only. Reset: Fixed, 0h. Number of VMPLs supported.																		
11:6	MemEncryptPhysAddWidth. Read-only. Reset: 000XXXb. Reduction of physical address space in bits when memory encryption is enabled (0 indicates no reduction). Valid Values:																		
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>00h</td><td>Physical Address width is not reduced.</td></tr> <tr> <td>01h</td><td>Physical Address width is reduced by one.</td></tr> <tr> <td>02h</td><td>Physical Address width is reduced by two.</td></tr> <tr> <td>03h</td><td>Physical Address width is reduced by three.</td></tr> <tr> <td>04h</td><td>Physical Address width is reduced by four.</td></tr> <tr> <td>05h</td><td>Physical Address width is reduced by five.</td></tr> <tr> <td>06h</td><td>Physical Address width is reduced by six.</td></tr> <tr> <td>3Fh-07h</td><td>Reserved.</td></tr> </table>	Value	Description	00h	Physical Address width is not reduced.	01h	Physical Address width is reduced by one.	02h	Physical Address width is reduced by two.	03h	Physical Address width is reduced by three.	04h	Physical Address width is reduced by four.	05h	Physical Address width is reduced by five.	06h	Physical Address width is reduced by six.	3Fh-07h	Reserved.
Value	Description																		
00h	Physical Address width is not reduced.																		
01h	Physical Address width is reduced by one.																		
02h	Physical Address width is reduced by two.																		
03h	Physical Address width is reduced by three.																		
04h	Physical Address width is reduced by four.																		
05h	Physical Address width is reduced by five.																		
06h	Physical Address width is reduced by six.																		
3Fh-07h	Reserved.																		
5:0	CBit. Read-only. Reset: 33h. Page table bit number used to enable memory encryption.																		

CPUID_Fn8000001F_ECX [AMD Secure Encryption ECX] (Core::X86::Cpuid::SecureEncryptionEcX)

Read-only.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn8000001F_ECX

Bits	Description
31:0	NumEncryptedGuests. Read-only. Reset: XXXX_XXXXh. Indicates the maximum ASID value that may be used for an SEV-enabled guest.

CPUID_Fn8000001F_EDX [Minimum ASID] (Core::X86::Cpuid::SecureEncryptionEdx)

Read-only.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn8000001F_EDX

Bits	Description
31:0	MinimumSEVASID: Minimum SEV enabled, SEV-ES disabled ASID. Read-only. Reset: 0000_000Xh. Indicates the minimum ASID value that must be used for an SEV-enabled, SEV-ES-disabled guest.

CPUID_Fn80000020_EAX_x00 [Platform QoS Extended Feature Identifiers] (Core::X86::Cpuid::AmdQosExtEax0)

Read-only. Reset: 0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000020_EAX_x00

Bits	Description
31:0	Reserved.

**CPUID_Fn80000020_EBX_x00 [Platform QoS Extended Feature Identifiers]
(Core::X86::Cpuid::AmdQosExtEbx0)**

Read-only. Reset: 0000_001Eh.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000020_EBX_x00

Bits	Description
31:5	Reserved.
4	L3RR. Read-only. Reset: 1. AMD L3 Range Reservation.
3	EVT_CFG. Read-only. Reset: 1. AMD Bandwidth Monitoring Event Configuration.
2	SMBE. Read-only. Reset: 1. Slow Memory Bandwidth Enforcement. See Core::X86::Cpuid::PqeBandwidthEax2 - Core::X86::Cpuid::PqeBandwidthEdx2.
1	MBE. Read-only. Reset: 1. Memory Bandwidth Enforcement.
0	Reserved.

**CPUID_Fn80000020_ECX_x00 [Platform QoS Extended Feature Identifiers]
(Core::X86::Cpuid::AmdQosExtEcxc0)**

Read-only. Reset: 0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000020_ECX_x00

Bits	Description
31:0	Reserved.

**CPUID_Fn80000020_EDX_x00 [Platform QoS Extended Feature Identifiers]
(Core::X86::Cpuid::AmdQosExtEdxc0)**

Read-only. Reset: 0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000020_EDX_x00

Bits	Description
31:0	Reserved.

**CPUID_Fn80000020_EAX_x01 [Platform QoS Enforcement for Memory Bandwidth]
(Core::X86::Cpuid::PqeBandwidthEax1)**

Read-only. Reset: 0000_000Bh.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000020_EAX_x01

Bits	Description
31:0	BW_LEN: QOS Memory Bandwidth Enforcement Limit Size. Read-only. Reset: 0000_000Bh. Size of the QOS Memory Bandwidth Enforcement Limit.

**CPUID_Fn80000020_EBX_x01 [Platform QoS Enforcement for Memory Bandwidth]
(Core::X86::Cpuid::PqeBandwidthEbx1)**

Read-only. Reset: 0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000020_EBX_x01

Bits	Description
31:0	Reserved.

**CPUID_Fn80000020_ECX_x01 [Platform QoS Enforcement for Memory Bandwidth]
(Core::X86::Cpuid::PqeBandwidthEcxc1)**

Read-only. Reset: 0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000020_ECX_x01

Bits	Description
31:0	Reserved.

**CPUID_Fn80000020_EDX_x01 [Platform QoS Enforcement for Memory Bandwidth]
(Core::X86::Cpuid::PqeBandwidthEdx1)**

Read-only. Reset: 0000_000Fh.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000020_EDX_x01

Bits	Description
31:0	NumClassService. Read-only. Reset: 0000_000Fh. Number of classes of service.

**CPUID_Fn80000020_EAX_x02 [Enforcement for Slow Memory Bandwidth]
(Core::X86::Cpuid::PqeBandwidthEax2)**

Read-only. Reset: 0000_000Bh.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000020_EAX_x02

Bits	Description
31:0	BW_LEN. Read-only. Reset: 0000_000Bh. Slow Memory Bandwidth Enforcement Bit Range Length.

**CPUID_Fn80000020_EBX_x02 [Enforcement for Slow Memory Bandwidth]
(Core::X86::Cpuid::PqeBandwidthEbx2)**

Read-only. Reset: 0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000020_EBX_x02

Bits	Description
31:0	Reserved.

**CPUID_Fn80000020_ECX_x02 [Enforcement for Slow Memory Bandwidth]
(Core::X86::Cpuid::PqeBandwidthEcx2)**

Read-only. Reset: 0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000020_ECX_x02

Bits	Description
31:0	Reserved.

**CPUID_Fn80000020_EDX_x02 [Enforcement for Slow Memory Bandwidth]
(Core::X86::Cpuid::PqeBandwidthEdx2)**

Read-only. Reset: 0000_000Fh.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000020_EDX_x02

Bits	Description
31:0	COS_MAX. Read-only. Reset: 0000_000Fh. Maximum Class Of Service (COS) number for Memory Bandwidth Enforcement.

**CPUID_Fn80000020_EBX_x03 [Platform QoS Monitoring Bandwidth Event Configuration]
(Core::X86::Cpuid::PqeBandwidthEvtCfgEbx3)**

Read-only. Reset: 0000_0002h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000020_EBX_x03

Bits	Description
31:8	Reserved.
7:0	EVT_NUM. Read-only. Reset: 02h. Reports the number of bandwidth events that can be configured.

**CPUID_Fn80000020_ECX_x03 [Platform QoS Monitoring Bandwidth Event Configuration]
(Core::X86::Cpuid::PqeBandwidthEvtCfgEc3)**

Read-only. Reset: 0000_007Fh.

Identifies the bandwidth sources that can be tracked.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000020_ECX_x03

Bits	Description
31:7	Reserved.
6	L3CacheBwVicMon. Read-only. Reset: 1. Dirty victims to all types of memory.
5	L3CacheRmtSlowBwFillMon. Read-only. Reset: 1. Reads from remote memory the system identifies as slow memory.
4	L3CacheLclSlowBwFillMon. Read-only. Reset: 1. Reads from local memory the system identifies as slow memory.
3	L3CacheRmtBwNtWrMon. Read-only. Reset: 1. Non-temporal writes to remote memory.
2	L3CacheLclBwNtWrMon. Read-only. Reset: 1. Non-temporal writes to local memory.
1	L3CacheRmtBwFillMon. Read-only. Reset: 1. Reads from remote memory.
0	L3CacheLclBwFillMon. Read-only. Reset: 1. Reads from local memory.

CPUID_Fn80000021_EAX [Extended Feature 2 EAX] (Core::X86::Cpuid::FeatureExt2Eax)

Read-only.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000021_EAX

Bits	Description
31:19	Reserved.
18	EPSF. Read-only. Reset: 1. Enhanced Predictive Store Forwarding supported.
17	GpOnUserCpuid. Read-only. Reset: 1. Indicates support for #GP when executing CPUID at CPL > 0.
16:14	Reserved.
13	PrefetchCtlMsr. Read-only. Reset: 1. 1=Prefetch control MSR supported. See Core::X86::Msr::PrefetchControl.
12	Reserved.
11	FSRC. Read-only. Reset: Fixed,1. Fast Short Repe Cmpsb supported.
10	FSRS. Read-only. Reset: Fixed,1. Fast Short Rep Stosb supported.
9	NoSmmCtlMSR. Read-only. Reset: Fixed,1. Indicates that MSRC001_0116 (SMM_CTL) is not present.
8	AutomaticIBRS. Read-only. Reset: Fixed,1. Indicates that Core::X86::Msr::EFER[AutomaticIBRSEn] can be set to automatically toggle IBRS protection when CPL changes.
7	UpperAddressIgnore. Read-only. Reset: Fixed,1. Indicates that Core::X86::Msr::EFER[UAIE] bit controls canonical check for upper address bits for certain types of accesses.
6	NullSelectorClearsBase. Read-only. Reset: 1. 1=Null Selector Clears Base. When this bit is set, a null segment load clears the segment base.
5:4	Reserved.
3	SmmPgCfgLock. Read-only. Reset: Fixed,1. 1=SMM paging configuration lock supported.
2	LFenceAlwaysSerializing. Read-only. Reset: Fixed,1. LFENCE is always serializing.
1	FsGsKernelGsBaseNonSerializing. Read-only. Reset: Fixed,1. WRMSR to Core::X86::Msr::FS_BASE, Core::X86::Msr::GS_BASE, and Core::X86::Msr::KernelGSbase are non-serializing.
0	NoNestedDataBp. Read-only. Reset: Fixed,1. New data-breakpoints are ignored while switching to data-breakpoint handler.

CPUID_Fn80000021_EBX [Extended Feature 2 EBX] (Core::X86::Cpuid::FeatureExt2Ebx)

Read-only.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000021_EBX

Bits	Description
31:12	Reserved.
11:0	MicrocodePatchSize. Read-only. Reset: XXXh. Reports the size of the Microcode patch in 16-byte multiples. If 0, the size of the patch is at most 5568 (15C0h) bytes.

**CPUID_Fn80000022_EAX [Extended Performance Monitoring and Debug EAX]
(Core::X86::Cpuid::ExtPerfMonAndDbgEax)**

Read-only. Reset: Fixed,0000_0007h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000022_EAX

Bits	Description
31:3	Reserved.
2	LbrAndPmcFreeze . Read-only. Reset: Fixed,1. 1=PMC and LBR freeze is supported in Core::X86::Msr::DBG_CTL_MSR.
1	LbrExtV2 . Read-only. Reset: Fixed,1. 1=LBR extension Version 2 supported.
0	PerfMonV2 . Read-only. Reset: Fixed,1. 1=Performance Monitoring Version 2 supported.

**CPUID_Fn80000022_EBX [Extended Performance Monitoring and Debug EBX]
(Core::X86::Cpuid::ExtPerfMonAndDbgEbx)**

Read-only.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000022_EBX

Bits	Description
31:22	Reserved.
21:16	NumPerfCtrUmc . Read-only. Reset: Fixed,XXXXXXb. Number of available UMC PMCs.
15:10	NumPerfCtrNB . Read-only. Reset: Fixed,10h. Number of available Data Fabric (Northbridge) Performance Monitor Counters.
9:4	LbrV2StackSz . Read-only. Reset: Fixed,10h. Number of available LBR stack entries.
3:0	NumPerfCtrCore . Read-only. Reset: Fixed,6h. Number of Core Performance Counters.

**CPUID_Fn80000022_ECX [Extended Performance Monitoring and Debug ECX]
(Core::X86::Cpuid::ExtPerfMonAndDbgEcX)**

Read-only.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000022_ECX

Bits	Description
31:0	ActiveUmcMask . Read-only. Reset: Fixed,XXXX_XXXXh. Bitmask representing active UMCs. Calculate the number of PMCs per UMC as CPUID_8000_0022_EBX[21:16] / POPCNT(CPUID_8000_0022_ECX[31:0]).

**CPUID_Fn80000023_EAX [AMD Secure Multi-Key Encryption EAX]
(Core::X86::Cpuid::SecureMultiKeyEncryptionEax)**

Read-only. Reset: Fixed,0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000023_EAX

Bits	Description
31:1	Reserved.
0	MemHmkSupport . Read-only. Reset: Fixed,0. 1=MEM-HMK mode is supported.

**CPUID_Fn80000023_EBX [AMD Secure Multi-Key Encryption EBX]
(Core::X86::Cpuid::SecureMultiKeyEncryptionEbx)**

Read-only. Reset: Fixed,0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000023_EBX

Bits	Description
31:16	Reserved.
15:0	MaxMemHmkEncrKeyID . Read-only. Reset: Fixed,0000h. Total number of available encryption keys in MEM-HMK mode.

**CPUID_Fn80000023_ECX [AMD Secure Multi-Key Encryption ECX]
(Core::X86::Cpuid::SecureMultiKeyEncryptionEcx)**

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000023_ECX

Bits	Description
------	-------------

31:0	Reserved.
------	-----------

**CPUID_Fn80000023_EDX [AMD Secure Multi-Key Encryption EDX]
(Core::X86::Cpuid::SecureMultiKeyEncryptionEdx)**

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000023_EDX

Bits	Description
------	-------------

31:0	Reserved.
------	-----------

CPUID_Fn80000026_EAX_x0[0...3] [Extended CPU Topology] (Core::X86::Cpuid::ExtCpuTopologyEax)

Read-only.

CPUID Fn8000_0026_E[D,C,B,A]X_x[3:0] specifies the hierarchy of logical cores from the SMT level through the processor socket level. Software reads CPUID Fn8000_0026_E[C,B,A]X for ascending values of ECX until (CPUID Fn8000_0026_EBX[LogProcAtThisLevel] == 0).

Note: While CPUID Fn8000_0026 is a preferred superset to CPUID_Fn0000000B, CPUID_Fn0000000B information is valid for software for the supported levels on AMD.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n0; CPUID_Fn80000026_EAX_x00

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n1; CPUID_Fn80000026_EAX_x01

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n2; CPUID_Fn80000026_EAX_x02

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n3; CPUID_Fn80000026_EAX_x03

Bits	Description
------	-------------

31	AsymmetricCores. Read-only. Reset: Fixed,X. When set, not all cores in the system report the same value in Core::X86::Cpuid::ExtCpuTopologyEbx[LogProcThisLevel] for Core::X86::Cpuid::ExtCpuTopologyEcx[LevelType]=0x1. When cleared, all cores in the system report the same value in Core::X86::Cpuid::ExtCpuTopologyEbx[LogProcThisLevel] for Core::X86::Cpuid::ExtCpuTopologyEcx[LevelType]=0x1.
----	--

30	HeterogeneousCoreTopology. Read-only. Reset: Fixed,0. When set, not all instances at the current hierarchy level have the same Core Type topology. The core type is reported in Core::X86::Cpuid::ExtCpuTopologyEbx[CoreType].
----	---

29	EfficiencyRankingAvailable. Read-only. Reset: Fixed,0. When set, Core::X86::Cpuid::ExtCpuTopologyEbx[ProcessorPowerEfficiencyRanking] is valid and varies between individual cores.
----	--

28:5	Reserved.
------	-----------

4:0	CoreMaskWidth. Read-only. Reset: Fixed,XXh. Number of bits to shift Core::X86::Cpuid::ExtCpuTopologyEdx[ExtendedLocalApicId] right to get unique topology ID of the next level type. All logical processors with the same next level ID share current level.
-----	---

CPUID_Fn80000026_EBX_x0[0...3] [Extended CPU Topology] (Core::X86::Cpuid::ExtCpuTopologyEbx)

Read-only.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n0; CPUID_Fn80000026_EBX_x00

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n1; CPUID_Fn80000026_EBX_x01

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n2; CPUID_Fn80000026_EBX_x02

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n3; CPUID_Fn80000026_EBX_x03

Bits	Description								
31:28	CoreType. Read-only. Reset: Fixed,Xh. Defines per-core architectural feature differentiation (microarchitectural resources, etc.) that may lead to a different performance, core clock boost, and power characteristic. Only valid while LevelType=Core. ValidValues: <table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>Performance Core.</td></tr> <tr> <td>1h</td><td>Efficiency Core.</td></tr> <tr> <td>Fh-2h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	Performance Core.	1h	Efficiency Core.	Fh-2h	Reserved.
Value	Description								
0h	Performance Core.								
1h	Efficiency Core.								
Fh-2h	Reserved.								
27:24	NativeModelId. Read-only. Reset: Fixed,0h. Context sensitive to CPUID_Fn00000001_EAX and CPUID_Fn80000001_EAX [Family, Model, Stepping Identifiers] (Core::X86::Cpuid::FamModStep). Only valid while Level Type=Core. This value is used by software to further differentiate implementation specific software visible properties between the cores. ValidValues: <table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>Zen4 Core.</td></tr> <tr> <td>Fh-1h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	Zen4 Core.	Fh-1h	Reserved.		
Value	Description								
0h	Zen4 Core.								
Fh-1h	Reserved.								
23:16	ProcessorPowerEfficiencyRanking. Read-only. Reset: Fixed,XXh. Identifies a static efficiency ranking between each of the cores of a specific CoreType, where a core with a lower value has intrinsically better power, but potentially lower performance potential vs cores with a higher value.								
15:0	LogProcThisLevel. Read-only. Reset: Fixed,XXXh. Number of logical processors at this level type.								

CPUID_Fn80000026_ECX_x0[0...3] [Extended CPU Topology] (Core::X86::Cpuid::ExtCpuTopologyEcX)

Read-only.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n0; CPUID_Fn80000026_ECX_x00

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n1; CPUID_Fn80000026_ECX_x01

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n2; CPUID_Fn80000026_ECX_x02

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n3; CPUID_Fn80000026_ECX_x03

Bits	Description														
31:16	Reserved.														
15:8	LevelType. Read-only. Reset: Fixed,XXh. ValidValues: <table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>00h</td><td>Reserved.</td></tr> <tr> <td>01h</td><td>Core</td></tr> <tr> <td>02h</td><td>Complex</td></tr> <tr> <td>03h</td><td>CCD (Die)</td></tr> <tr> <td>04h</td><td>Socket</td></tr> <tr> <td>FFh-05h</td><td>Reserved.</td></tr> </table>	Value	Description	00h	Reserved.	01h	Core	02h	Complex	03h	CCD (Die)	04h	Socket	FFh-05h	Reserved.
Value	Description														
00h	Reserved.														
01h	Core														
02h	Complex														
03h	CCD (Die)														
04h	Socket														
FFh-05h	Reserved.														
7:0	EcXVal. Read-only. Reset: Fixed,XXh. ECX input value.														

CPUID_Fn80000026_EDX [Extended CPU Topology] (Core::X86::Cpuid::ExtCpuTopologyEdx)

Read-only.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; CPUID_Fn80000026_EDX

Bits Description31:0 **ExtendedLocalApicId.** Read-only. Reset: Fixed,XXXX_XXXXh. Extended APIC ID.**2.1.12 MSR Registers****2.1.12.1 MSRs - MSR0000_xxxx****MSR0000_0010 [Time Stamp Counter] (Core::X86::Msr::TSC)**

Read-write, Volatile. Reset: 0000_0000_0000_0000h.

The TSC uses a common reference for all sockets, cores and threads.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSR0000_0010

Bits Description63:0 **TSC: time stamp counter.** Read-write, Volatile. Reset: 0000_0000_0000_0000h. The TSC increments at the P0 frequency. The TSC counts at the same rate in all P-states, all C states, S0, or S1. A Read of this MSR in guest mode is affected by Core::X86::Msr::TscRateMsr. The value (TSC/TSCRatio) is the TSC P0 frequency based value (as if TSCRatio == 1.0) when (TSCRatio != 1.0).**MSR0000_001B [APIC Base Address] (Core::X86::Msr::APIC_BAR)**

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSR0000_001B

Bits Description

63:48 Reserved.

47:12 **ApicBar[47:12]: APIC base address register.** Read-write. Reset: 0_000F_EE00h. Specifies the base address, physical address [47:12], for the APICXX register set in xAPIC mode. See 2.1.10.2.1.2 [APIC Register Space].11 **ApicEn: APIC enable.** Read-write. Reset: 0. 0=Disable Local APIC. 1=Local APIC is enabled in xAPIC mode. See 2.1.10.2.1.2 [APIC Register Space].10 **x2ApicEn: Extended APIC enable.** Read-write. Reset: 0. 0=Disable Extended Local APIC. 1=Extended Local APIC is enabled in x2APIC mode. Clearing this bit after it has been set results in a #GP.

9 Reserved.

8 **BSC: boot strap core.** Read-write, Volatile. Reset: X. 0=The core is not the boot core of the BSP. 1=The core is the boot core of the BSP.

7:0 Reserved.

MSR0000_002A [Cluster ID] (Core::X86::Msr::EBL_CR_POWERON)

Writes to this register result in a GP fault with error code 0.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSR0000_002A

Bits Description

63:18 Reserved.

17:16 **ClusterID.** Read, Error-on-write. Reset: 0h. The field does not affect hardware.

15:0 Reserved.

MSR0000_0048 [Speculative Control] (Core::X86::Msr::SPEC_CTRL)

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSR0000_0048

Bits	Description
63:8	Reserved.
7	PSFD: Predictive Store Forwarding Disable. Read-write. Reset: 0. 1=Disable predictive store forwarding.
6:3	Reserved.
2	SSBD. Read-write. Reset: 0. Speculative Store Bypass Disable.
1	STIBP. Read-write. Reset: 0. Single thread indirect branch predictor.
0	IBRS. Read-write. Reset: 0. Indirect branch restriction speculation.

MSR0000_0049 [Prediction Command] (Core::X86::Msr::PRED_CMD)

_ccd[1:0]_lthree0_core[7:0]; MSR0000_0049

Bits	Description
63:1	Reserved.
0	IBPB: indirect branch prediction barrier. Write-only, Error-on-read. Reset: 0. Supported if Core::X86::Cpuid::FeatureExtIdEbx[IBPB] == 1.

MSR0000_008B [Patch Level] (Core::X86::Msr::PATCH_LEVEL)

Read, Error-on-write, Volatile. Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]; MSR0000_008B

Bits	Description
63:32	Reserved.
31:0	PatchLevel. Read, Error-on-write, Volatile. Reset: 0000_0000h. This returns an identification number for the microcode patch that has been loaded. If no patch has been loaded, this returns 0.

MSR0000_00E7 [Max Performance Frequency Clock Count] (Core::X86::Msr::MPERF)

Read-write, Volatile. Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSR0000_00E7

Bits	Description
63:0	MPERF: maximum core clocks counter. Read-write, Volatile. Reset: 0000_0000_0000_0000h. Incremented by hardware at the P0 frequency while the core is in C0. This register does not increment when the core is in the stop-grant state. In combination with Core::X86::Msr::APERF, this is used to determine the effective frequency of the core. A Read of this MSR in guest mode is affected by Core::X86::Msr::TscRateMsr. This field uses software P-state numbering. See Core::X86::Msr::HWCR[EffFreqCntMwait], 2.1.3 [Effective Frequency]

MSR0000_00E8 [Actual Performance Frequency Clock Count] (Core::X86::Msr::APERF)

Read-write, Volatile. Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSR0000_00E8

Bits	Description
63:0	APERF: actual core clocks counter. Read-write, Volatile. Reset: 0000_0000_0000_0000h. This register increments in proportion to the actual number of core clocks cycles while the core is in C0. The register does not increment when the core is in the stop-grant state. See Core::X86::Msr::MPERF.

MSR0000_00FE [MTRR Capabilities] (Core::X86::Msrr::MTRRcap)

Read,Error-on-write. Reset: 0000_0000_0000_0508h.

_ccd[1:0]_lthree0_core[7:0]; MSR0000_00FE

Bits	Description
63:11	Reserved.
10	MtrrCapWc: write-combining memory type. Read,Error-on-write. Reset: 1. 1=The write combining memory type is supported.
9	Reserved.
8	MtrrCapFix: fixed range register. Read,Error-on-write. Reset: 1. 1=Fixed MTRRs are supported.
7:0	MtrrCapVCnt: variable range registers count. Read,Error-on-write. Reset: 08h. Specifies the number of variable MTRRs supported.

MSR0000_010B [Flush Command] (Core::X86::Msrr::FLUSH_CMD)

Writes to this register do not execute until all prior instructions finished execution and have completed locally. Later instructions do not execute until the Write completes.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSR0000_010B

Bits	Description
63:1	Reserved.
0	L1D_FLUSH. Write-only, Volatile. Reset: 0. When written to 1, performs a write-back and invalidate of the L1 data cache.

MSR0000_0174 [SYSENTER CS] (Core::X86::Msrr::SYSENTER_CS)

Read-write. Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSR0000_0174

Bits	Description
63:16	Reserved.
15:0	SysEnterCS: SYSENTER target CS. Read-write. Reset: 0000h. Holds the called procedure code segment.

MSR0000_0175 [SYSENTER ESP] (Core::X86::Msrr::SYSENTER_ESP)

Read-write. Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSR0000_0175

Bits	Description
63:32	Reserved.
31:0	SysEnterESP: SYSENTER target SP. Read-write. Reset: 0000_0000h. Holds the called procedure stack pointer.

MSR0000_0176 [SYSENTER EIP] (Core::X86::Msrr::SYSENTER_EIP)

Read-write. Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSR0000_0176

Bits	Description
63:32	Reserved.
31:0	SysEnterEIP: SYSENTER target IP. Read-write. Reset: 0000_0000h. Holds the called procedure instruction pointer.

MSR0000_0179 [Global Machine Check Capabilities] (Core::X86::Msrr::MCG_CAP)

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSR0000_0179

Bits	Description
63:9	Reserved.
8	McgCtlP: MCG_CTL register present. Read-only, Error-on-write. Reset: Fixed, 1. 1=The machine check control registers (MCI_CTL) are present. See 3.1 [Machine Check Architecture].
7:0	Count. Read-only, Error-on-write, Volatile. Reset: XXh. Indicates the number of error reporting banks visible to the core. This value may differ from core to core.

MSR0000_017A [Global Machine Check Status] (Core::X86::Msr::MCG_STAT)

Read-write, Volatile. Reset: 0000_0000_0000_0000h.

See 3.1 [Machine Check Architecture].

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSR0000_017A

Bits	Description
63:3	Reserved.
2	MCIP. Read-write, Volatile. Reset: 0. 1=A machine check is in progress. Machine check in progress.
1	EIPV: error instruction pointer valid. Read-write, Volatile. Reset: 0. 1=The instruction pointer that was pushed onto the stack by the machine check mechanism references the instruction that caused the machine check error.
0	RIPV: restart instruction pointer valid. Read-write, Volatile. Reset: 0. 0=The interrupt was not precise and/or the process (task) context may be corrupt; continued operation of this process may not be possible without intervention, however system processing or other processes may be able to continue with appropriate software clean up. 1=Program execution can be reliably restarted at the EIP address on the stack.

MSR0000_017B [Global Machine Check Exception Reporting Control] (Core::X86::Msr::MCG_CTL)

Reset: 0000_0000_0000_0000h.

This register controls enablement of the individual error reporting banks; see 3.1 [Machine Check Architecture] and 3.1.2.1 [Global Registers]. When a machine check register bank is not enabled in MCG_CTL, errors for that bank are not logged or reported, and actions enabled through the MCA are not taken; each MCi_CTL register identifies which errors are still corrected when MCG_CTL[i] is disabled.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSR0000_017B

Bits	Description																
63:7	MCnEn. Configurable. Reset: 000_0000_0000_0000h. Description: 1=The MC machine check register bank is enabled. Width of this field is SOC implementation and configuration specific. See 3.1.2.1 [Global Registers].																
6:0	MCnEnCore. Read-write. Reset: 00h. 1=The MC machine check register bank is enabled. ValidValues: <table border="1"> <thead> <tr> <th>Bit</th><th>Description</th></tr> </thead> <tbody> <tr> <td>[0]</td><td>Enable MCA for LSDC</td></tr> <tr> <td>[1]</td><td>Enable MCA for ICBP</td></tr> <tr> <td>[2]</td><td>Enable MCA for L2</td></tr> <tr> <td>[3]</td><td>Enable MCA for DE</td></tr> <tr> <td>[4]</td><td>Reserved.</td></tr> <tr> <td>[5]</td><td>Enable MCA for SCEX</td></tr> <tr> <td>[6]</td><td>Enable MCA for FP</td></tr> </tbody> </table>	Bit	Description	[0]	Enable MCA for LSDC	[1]	Enable MCA for ICBP	[2]	Enable MCA for L2	[3]	Enable MCA for DE	[4]	Reserved.	[5]	Enable MCA for SCEX	[6]	Enable MCA for FP
Bit	Description																
[0]	Enable MCA for LSDC																
[1]	Enable MCA for ICBP																
[2]	Enable MCA for L2																
[3]	Enable MCA for DE																
[4]	Reserved.																
[5]	Enable MCA for SCEX																
[6]	Enable MCA for FP																

MSR0000_01D9 [Debug Control] (Core::X86::Msr::DBG_CTL_MSR)

Read-write. Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSR0000_01D9

Bits	Description
63:13	Reserved.
12	FPMCI. Read-write. Reset: 0. 1=Freeze PMCs on PMC interrupt.
11	FLBRI. Read-write. Reset: 0. 1=Freeze LBR on PMC interrupt.
10:6	Reserved.
5:2	PB: performance monitor pin control. Read-write. Reset: 0h. This field does not control any hardware.
1	BTF. Read-write. Reset: 0. 1=Enable branch single step.
0	LBR. Read-write. Reset: 0. 1=Enable last branch record.

MSR0000_01DB [Last Branch From IP] (Core::X86::Msr::BR_FROM)

Read,Error-on-write,Volatile. Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSR0000_01DB

Bits	Description
63	Reserved.
62:0	LastBranchFromIP . Read,Error-on-write,Volatile. Reset: 0000_0000_0000_0000h. Loaded with the segment offset of the branch instruction.

MSR0000_01DC [Last Branch To IP] (Core::X86::Msr::BR_TO)

Read,Error-on-write,Volatile. Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSR0000_01DC

Bits	Description
63:61	Reserved.
60:0	LastBranchToIP . Read,Error-on-write,Volatile. Reset: 0000_0000_0000_0000h. Holds the target RIP of the last branch that occurred before an exception or interrupt.

MSR0000_01DD [Last Exception From IP] (Core::X86::Msr::LastExcpFromIp)

Read,Error-on-write,Volatile. Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSR0000_01DD

Bits	Description
63:0	LastIntFromIP . Read,Error-on-write,Volatile. Reset: 0000_0000_0000_0000h. Holds the source RIP of the last branch that occurred before the exception or interrupt.

MSR0000_01DE [Last Exception To IP] (Core::X86::Msr::LastExcpToIp)

Read,Error-on-write,Volatile. Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSR0000_01DE

Bits	Description
63:0	LastIntToIP . Read,Error-on-write,Volatile. Reset: 0000_0000_0000_0000h. Holds the target RIP of the last branch that occurred before the exception or interrupt.

MSR0000_020[0...E] [Variable-Size MTRRs Base] (Core::X86::Msrr::MtrrVarBase)

Each MTRR (Core::X86::Msrr::MtrrVarBase, Core::X86::Msrr::MtrrFix_64K through Core::X86::Msrr::MtrrFix_4K_7, or Core::X86::Msrr::MTRRdefType) specifies a physical address range and a corresponding memory type (MemType) associated with that range. Setting the memory type to an unsupported value will result in a #GP.

The variable-size MTRRs come in pairs of base and mask registers (MSR0000_0200 and MSR0000_0201 are the first pair, etc.). Variables MTRRs are enabled through Core::X86::Msrr::MTRRdefType[MtrrDefTypeEn]. A core access--with address CPUAddr--is determined to be within the address range of a variable-size MTRR if the following equation is true:

$$\text{CPUAddr}[47:12] \& \text{PhyMask}[47:12] == \text{PhyBase}[47:12] \& \text{PhyMask}[47:12].$$

For example, if the variable MTRR spans 256 KB and starts at the 1 MB address the PhyBase would be set to 0_0010_0000h and the PhyMask to F_FFFC_0000h (with zeros filling in for bits[11:0]). This results in a range from 0_0010_0000h to 0_0013_FFFFh.

_ccd[1:0]_lthree0_core[7:0]_n0; MSR0000_0200
 _ccd[1:0]_lthree0_core[7:0]_n1; MSR0000_0202
 _ccd[1:0]_lthree0_core[7:0]_n2; MSR0000_0204
 _ccd[1:0]_lthree0_core[7:0]_n3; MSR0000_0206
 _ccd[1:0]_lthree0_core[7:0]_n4; MSR0000_0208
 _ccd[1:0]_lthree0_core[7:0]_n5; MSR0000_020A
 _ccd[1:0]_lthree0_core[7:0]_n6; MSR0000_020C
 _ccd[1:0]_lthree0_core[7:0]_n7; MSR0000_020E

Bits	Description
63:48	Reserved.
47:12	PhyBase: base address. Read-write. Reset: X_XXXX_XXXXh. Physical base address.
11:3	Reserved.
2:0	MemType: memory type. Read-write. Reset: XXXb. Address range from 00000h to 0FFFFh.
ValidValues:	
Value	Description
0h	UC or uncacheable.
1h	WC or write combining.
3h-2h	Reserved.
4h	WT or write through.
5h	WP or write protect.
6h	WB or write back.
7h	Reserved.

MSR0000_020[1...F] [Variable-Size MTRRs Mask] (Core::X86::Msrr::MtrrVarMask)

_ccd[1:0]_lthree0_core[7:0]_n0; MSR0000_0201
 _ccd[1:0]_lthree0_core[7:0]_n1; MSR0000_0203
 _ccd[1:0]_lthree0_core[7:0]_n2; MSR0000_0205
 _ccd[1:0]_lthree0_core[7:0]_n3; MSR0000_0207
 _ccd[1:0]_lthree0_core[7:0]_n4; MSR0000_0209
 _ccd[1:0]_lthree0_core[7:0]_n5; MSR0000_020B
 _ccd[1:0]_lthree0_core[7:0]_n6; MSR0000_020D
 _ccd[1:0]_lthree0_core[7:0]_n7; MSR0000_020F

Bits	Description
63:48	Reserved.
47:12	PhyMask: address mask. Read-write. Reset: X_XXXX_XXXXh. Physical address mask.
11	Valid: valid. Read-write. Reset: X. 1=The variable-size MTRR pair is enabled.
10:0	Reserved.

MSR0000_0250 [Fixed-Size MTRRs] (Core::X86::Msrr::MtrrFix_64K)

See Core::X86::Msrr::MtrrVarBase for general MTRR information. Fixed MTRRs are enabled through Core::X86::Msrr::MTRRdefType[MtrrDefTypeFixEn,MtrrDefTypeEn]. For addresses below 1MB, the appropriate Fixed MTRRs override the default access destination. Each fixed MTRR includes two bits, RdDram and WrDram, that determine the destination based on the access type. Writing reserved MemType values causes an error-on-write. If Core::X86::Msrr::SYS_CFG[SecureNestedPagingEn] is set to 1, this register will be read-only and attempts to write to this register will result in #GP(0).

_ccd[1:0]_lthree0_core[7:0]_nSIZE64K; MSR0000_0250

Bits	Description																
63:61	Reserved.																
60	RdDram_64K_70000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
59	WrDram_64K_70000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
58:56	MemType_64K_70000: memory type. Read-write. Reset: XXXb. ValidValues: <table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>UC or uncacheable.</td></tr> <tr> <td>1h</td><td>WC or write combining.</td></tr> <tr> <td>3h-2h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>WT or write through.</td></tr> <tr> <td>5h</td><td>WP or write protect.</td></tr> <tr> <td>6h</td><td>WB or write back.</td></tr> <tr> <td>7h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
Value	Description																
0h	UC or uncacheable.																
1h	WC or write combining.																
3h-2h	Reserved.																
4h	WT or write through.																
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																
55:53	Reserved.																
52	RdDram_64K_60000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
51	WrDram_64K_60000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
50:48	MemType_64K_60000: memory type. Read-write. Reset: XXXb. ValidValues: <table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>UC or uncacheable.</td></tr> <tr> <td>1h</td><td>WC or write combining.</td></tr> <tr> <td>3h-2h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>WT or write through.</td></tr> <tr> <td>5h</td><td>WP or write protect.</td></tr> <tr> <td>6h</td><td>WB or write back.</td></tr> <tr> <td>7h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
Value	Description																
0h	UC or uncacheable.																
1h	WC or write combining.																
3h-2h	Reserved.																
4h	WT or write through.																
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																
47:45	Reserved.																
44	RdDram_64K_50000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM.																

	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
43	WrDram_64K_50000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
42:40	MemType_64K_50000: memory type. Read-write. Reset: XXXb. ValidValues:																
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>UC or uncacheable.</td></tr> <tr> <td>1h</td><td>WC or write combining.</td></tr> <tr> <td>3h-2h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>WT or write through.</td></tr> <tr> <td>5h</td><td>WP or write protect.</td></tr> <tr> <td>6h</td><td>WB or write back.</td></tr> <tr> <td>7h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
Value	Description																
0h	UC or uncacheable.																
1h	WC or write combining.																
3h-2h	Reserved.																
4h	WT or write through.																
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																
39:37	Reserved.																
36	RdDram_64K_40000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
35	WrDram_64K_40000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
34:32	MemType_64K_40000: memory type. Read-write. Reset: XXXb. ValidValues:																
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>UC or uncacheable.</td></tr> <tr> <td>1h</td><td>WC or write combining.</td></tr> <tr> <td>3h-2h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>WT or write through.</td></tr> <tr> <td>5h</td><td>WP or write protect.</td></tr> <tr> <td>6h</td><td>WB or write back.</td></tr> <tr> <td>7h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
Value	Description																
0h	UC or uncacheable.																
1h	WC or write combining.																
3h-2h	Reserved.																
4h	WT or write through.																
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																
31:29	Reserved.																
28	RdDram_64K_30000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
27	WrDram_64K_30000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
26:24	MemType_64K_30000: memory type. Read-write. Reset: XXXb.																

	ValidValues:	
	Value	Description
	0h	UC or uncacheable.
	1h	WC or write combining.
	3h-2h	Reserved.
	4h	WT or write through.
	5h	WP or write protect.
	6h	WB or write back.
	7h	Reserved.
23:21	Reserved.	
20	RdDram_64K_20000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM.	
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.	
19	WrDram_64K_20000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM.	
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.	
18:16	MemType_64K_20000: memory type. Read-write. Reset: XXXb.	
	ValidValues:	
	Value	Description
	0h	UC or uncacheable.
	1h	WC or write combining.
	3h-2h	Reserved.
	4h	WT or write through.
	5h	WP or write protect.
	6h	WB or write back.
	7h	Reserved.
15:13	Reserved.	
12	RdDram_64K_10000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM.	
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.	
11	WrDram_64K_10000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM.	
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.	
10:8	MemType_64K_10000: memory type. Read-write. Reset: XXXb.	
	ValidValues:	
	Value	Description
	0h	UC or uncacheable.
	1h	WC or write combining.
	3h-2h	Reserved.
	4h	WT or write through.
	5h	WP or write protect.
	6h	WB or write back.
	7h	Reserved.
7:5	Reserved.	

4	RdDram_64K_00000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. Address range from 00000h to 0FFFFh. Core::X86::Msr::SYS_CFG[MtrrFixDramEn,MtrrFixDramModEn] masks reads of the stored value.																
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
3	WrDram_64K_00000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. Address range from 00000h to 0FFFFh. Core::X86::Msr::SYS_CFG[MtrrFixDramEn,MtrrFixDramModEn] masks reads of the stored value.																
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
2:0	MemType_64K_00000: memory type. Read-write. Reset: XXXb. Address range from 00000h to 0FFFFh.																
	ValidValues:																
	<table><tr><th>Value</th><th>Description</th></tr><tr><td>0h</td><td>UC or uncacheable.</td></tr><tr><td>1h</td><td>WC or write combining.</td></tr><tr><td>3h-2h</td><td>Reserved.</td></tr><tr><td>4h</td><td>WT or write through.</td></tr><tr><td>5h</td><td>WP or write protect.</td></tr><tr><td>6h</td><td>WB or write back.</td></tr><tr><td>7h</td><td>Reserved.</td></tr></table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
	Value	Description															
	0h	UC or uncacheable.															
	1h	WC or write combining.															
	3h-2h	Reserved.															
	4h	WT or write through.															
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																

MSR0000_0258 [Fixed-Size MTRRs] (Core::X86::Msrr::MtrrFix_16K_0)

See Core::X86::Msrr::MtrrVarBase for general MTRR information. Fixed MTRRs are enabled through Core::X86::Msrr::MTRRdefType[MtrrDefTypeFixEn,MtrrDefTypeEn]. For addresses below 1MB, the appropriate Fixed MTRRs override the default access destination. Each fixed MTRR includes two bits, RdDram and WrDram, that determine the destination based on the access type. Writing reserved MemType values causes an error-on-write. If Core::X86::Msrr::SYS_CFG[SecureNestedPagingEn] is set to 1, this register will be read-only and attempts to write to this register will result in #GP(0).

_ccd[1:0]_lthree0_core[7:0]_nSIZE16K0; MSR0000_0258

Bits	Description																
63:61	Reserved.																
60	RdDram_16K_9C000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
59	WrDram_16K_9C000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
58:56	MemType_16K_9C000: memory type. Read-write. Reset: XXXb. ValidValues: <table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>UC or uncacheable.</td></tr> <tr> <td>1h</td><td>WC or write combining.</td></tr> <tr> <td>3h-2h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>WT or write through.</td></tr> <tr> <td>5h</td><td>WP or write protect.</td></tr> <tr> <td>6h</td><td>WB or write back.</td></tr> <tr> <td>7h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
Value	Description																
0h	UC or uncacheable.																
1h	WC or write combining.																
3h-2h	Reserved.																
4h	WT or write through.																
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																
55:53	Reserved.																
52	RdDram_16K_98000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
51	WrDram_16K_98000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
50:48	MemType_16K_98000: memory type. Read-write. Reset: XXXb. ValidValues: <table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>UC or uncacheable.</td></tr> <tr> <td>1h</td><td>WC or write combining.</td></tr> <tr> <td>3h-2h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>WT or write through.</td></tr> <tr> <td>5h</td><td>WP or write protect.</td></tr> <tr> <td>6h</td><td>WB or write back.</td></tr> <tr> <td>7h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
Value	Description																
0h	UC or uncacheable.																
1h	WC or write combining.																
3h-2h	Reserved.																
4h	WT or write through.																
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																
47:45	Reserved.																
44	RdDram_16K_94000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM.																

	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
43	WrDram_16K_94000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
42:40	MemType_16K_94000: memory type. Read-write. Reset: XXXb.																
	ValidValues:																
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>UC or uncacheable.</td></tr> <tr> <td>1h</td><td>WC or write combining.</td></tr> <tr> <td>3h-2h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>WT or write through.</td></tr> <tr> <td>5h</td><td>WP or write protect.</td></tr> <tr> <td>6h</td><td>WB or write back.</td></tr> <tr> <td>7h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
Value	Description																
0h	UC or uncacheable.																
1h	WC or write combining.																
3h-2h	Reserved.																
4h	WT or write through.																
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																
39:37	Reserved.																
36	RdDram_16K_90000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
35	WrDram_16K_90000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
34:32	MemType_16K_90000: memory type. Read-write. Reset: XXXb.																
	ValidValues:																
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>UC or uncacheable.</td></tr> <tr> <td>1h</td><td>WC or write combining.</td></tr> <tr> <td>3h-2h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>WT or write through.</td></tr> <tr> <td>5h</td><td>WP or write protect.</td></tr> <tr> <td>6h</td><td>WB or write back.</td></tr> <tr> <td>7h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
Value	Description																
0h	UC or uncacheable.																
1h	WC or write combining.																
3h-2h	Reserved.																
4h	WT or write through.																
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																
31:29	Reserved.																
28	RdDram_16K_8C000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
27	WrDram_16K_8C000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
26:24	MemType_16K_8C000: memory type. Read-write. Reset: XXXb.																

	ValidValues:	
	Value	Description
	0h	UC or uncacheable.
	1h	WC or write combining.
	3h-2h	Reserved.
	4h	WT or write through.
	5h	WP or write protect.
	6h	WB or write back.
	7h	Reserved.
23:21	Reserved.	
20	RdDram_16K_88000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM.	
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.	
19	WrDram_16K_88000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM.	
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.	
18:16	MemType_16K_88000: memory type. Read-write. Reset: XXXb.	
	ValidValues:	
	Value	Description
	0h	UC or uncacheable.
	1h	WC or write combining.
	3h-2h	Reserved.
	4h	WT or write through.
	5h	WP or write protect.
	6h	WB or write back.
	7h	Reserved.
15:13	Reserved.	
12	RdDram_16K_84000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM.	
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.	
11	WrDram_16K_84000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM.	
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.	
10:8	MemType_16K_84000: memory type. Read-write. Reset: XXXb.	
	ValidValues:	
	Value	Description
	0h	UC or uncacheable.
	1h	WC or write combining.
	3h-2h	Reserved.
	4h	WT or write through.
	5h	WP or write protect.
	6h	WB or write back.
	7h	Reserved.
7:5	Reserved.	

4	RdDram_16K_80000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. Address range from 80000h to 83FFFh. Core::X86::Msr::SYS_CFG[MtrrFixDramEn,MtrrFixDramModEn] masks reads of the stored value.																
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
3	WrDram_16K_80000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. Address range from 80000h to 83FFFh. Core::X86::Msr::SYS_CFG[MtrrFixDramEn,MtrrFixDramModEn] masks reads of the stored value.																
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
2:0	MemType_16K_80000: memory type. Read-write. Reset: XXXb. Address range from 80000h to 83FFFh.																
	ValidValues:																
	<table><tr><th>Value</th><th>Description</th></tr><tr><td>0h</td><td>UC or uncacheable.</td></tr><tr><td>1h</td><td>WC or write combining.</td></tr><tr><td>3h-2h</td><td>Reserved.</td></tr><tr><td>4h</td><td>WT or write through.</td></tr><tr><td>5h</td><td>WP or write protect.</td></tr><tr><td>6h</td><td>WB or write back.</td></tr><tr><td>7h</td><td>Reserved.</td></tr></table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
	Value	Description															
	0h	UC or uncacheable.															
	1h	WC or write combining.															
	3h-2h	Reserved.															
	4h	WT or write through.															
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																

MSR0000_0259 [Fixed-Size MTRRs] (Core::X86::Msrr::MtrrFix_16K_1)

See Core::X86::Msrr::MtrrVarBase for general MTRR information. Fixed MTRRs are enabled through Core::X86::Msrr::MTRRdefType[MtrrDefTypeFixEn,MtrrDefTypeEn]. For addresses below 1MB, the appropriate Fixed MTRRs override the default access destination. Each fixed MTRR includes two bits, RdDram and WrDram, that determine the destination based on the access type. Writing reserved MemType values causes an error-on-write. If Core::X86::Msrr::SYS_CFG[SecureNestedPagingEn] is set to 1, this register will be read-only and attempts to write to this register will result in #GP(0).

_ccd[1:0]_lthree0_core[7:0]_nSIZE16K1; MSR0000_0259

Bits	Description																
63:61	Reserved.																
60	RdDram_16K_BC000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
59	WrDram_16K_BC000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
58:56	MemType_16K_BC000: memory type. Read-write. Reset: XXXb. ValidValues: <table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>UC or uncacheable.</td></tr> <tr> <td>1h</td><td>WC or write combining.</td></tr> <tr> <td>3h-2h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>WT or write through.</td></tr> <tr> <td>5h</td><td>WP or write protect.</td></tr> <tr> <td>6h</td><td>WB or write back.</td></tr> <tr> <td>7h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
Value	Description																
0h	UC or uncacheable.																
1h	WC or write combining.																
3h-2h	Reserved.																
4h	WT or write through.																
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																
55:53	Reserved.																
52	RdDram_16K_B8000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
51	WrDram_16K_B8000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
50:48	MemType_16K_B8000: memory type. Read-write. Reset: XXXb. ValidValues: <table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>UC or uncacheable.</td></tr> <tr> <td>1h</td><td>WC or write combining.</td></tr> <tr> <td>3h-2h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>WT or write through.</td></tr> <tr> <td>5h</td><td>WP or write protect.</td></tr> <tr> <td>6h</td><td>WB or write back.</td></tr> <tr> <td>7h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
Value	Description																
0h	UC or uncacheable.																
1h	WC or write combining.																
3h-2h	Reserved.																
4h	WT or write through.																
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																
47:45	Reserved.																
44	RdDram_16K_B4000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM.																

	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
43	WrDram_16K_B4000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
42:40	MemType_16K_B4000: memory type. Read-write. Reset: XXXb. ValidValues:																
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>UC or uncacheable.</td></tr> <tr> <td>1h</td><td>WC or write combining.</td></tr> <tr> <td>3h-2h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>WT or write through.</td></tr> <tr> <td>5h</td><td>WP or write protect.</td></tr> <tr> <td>6h</td><td>WB or write back.</td></tr> <tr> <td>7h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
Value	Description																
0h	UC or uncacheable.																
1h	WC or write combining.																
3h-2h	Reserved.																
4h	WT or write through.																
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																
39:37	Reserved.																
36	RdDram_16K_B0000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
35	WrDram_16K_B0000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
34:32	MemType_16K_B0000: memory type. Read-write. Reset: XXXb. ValidValues:																
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>UC or uncacheable.</td></tr> <tr> <td>1h</td><td>WC or write combining.</td></tr> <tr> <td>3h-2h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>WT or write through.</td></tr> <tr> <td>5h</td><td>WP or write protect.</td></tr> <tr> <td>6h</td><td>WB or write back.</td></tr> <tr> <td>7h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
Value	Description																
0h	UC or uncacheable.																
1h	WC or write combining.																
3h-2h	Reserved.																
4h	WT or write through.																
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																
31:29	Reserved.																
28	RdDram_16K_AC000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
27	WrDram_16K_AC000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
26:24	MemType_16K_AC000: memory type. Read-write. Reset: XXXb.																

	ValidValues:	
	Value	Description
	0h	UC or uncacheable.
	1h	WC or write combining.
	3h-2h	Reserved.
	4h	WT or write through.
	5h	WP or write protect.
	6h	WB or write back.
	7h	Reserved.
23:21	Reserved.	
20	RdDram_16K_A8000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM.	
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.	
19	WrDram_16K_A8000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM.	
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.	
18:16	MemType_16K_A8000: memory type. Read-write. Reset: XXXb.	
	ValidValues:	
	Value	Description
	0h	UC or uncacheable.
	1h	WC or write combining.
	3h-2h	Reserved.
	4h	WT or write through.
	5h	WP or write protect.
	6h	WB or write back.
	7h	Reserved.
15:13	Reserved.	
12	RdDram_16K_A4000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM.	
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.	
11	WrDram_16K_A4000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM.	
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.	
10:8	MemType_16K_A4000: memory type. Read-write. Reset: XXXb.	
	ValidValues:	
	Value	Description
	0h	UC or uncacheable.
	1h	WC or write combining.
	3h-2h	Reserved.
	4h	WT or write through.
	5h	WP or write protect.
	6h	WB or write back.
	7h	Reserved.
7:5	Reserved.	

4	RdDram_16K_A0000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. Address range from A0000h to A3FFFh. Core::X86::Msr::SYS_CFG[MtrrFixDramEn,MtrrFixDramModEn] masks Reads of the stored value.																
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
3	WrDram_16K_A0000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. Address range from A0000h to A3FFFh. Core::X86::Msr::SYS_CFG[MtrrFixDramEn,MtrrFixDramModEn] masks Reads of the stored value.																
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
2:0	MemType_16K_A0000: memory type. Read-write. Reset: XXXb. Address range from A0000h to A3FFFh.																
	ValidValues:																
	<table><tr><th>Value</th><th>Description</th></tr><tr><td>0h</td><td>UC or uncacheable.</td></tr><tr><td>1h</td><td>WC or write combining.</td></tr><tr><td>3h-2h</td><td>Reserved.</td></tr><tr><td>4h</td><td>WT or write through.</td></tr><tr><td>5h</td><td>WP or write protect.</td></tr><tr><td>6h</td><td>WB or write back.</td></tr><tr><td>7h</td><td>Reserved.</td></tr></table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
	Value	Description															
	0h	UC or uncacheable.															
	1h	WC or write combining.															
	3h-2h	Reserved.															
	4h	WT or write through.															
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																

MSR0000_0268 [Fixed-Size MTRRs] (Core::X86::Msrr::MtrrFix_4K_0)

See Core::X86::Msrr::MtrrVarBase for general MTRR information. Fixed MTRRs are enabled through Core::X86::Msrr::MTRRdefType[MtrrDefTypeFixEn,MtrrDefTypeEn]. For addresses below 1MB, the appropriate Fixed MTRRs override the default access destination. Each fixed MTRR includes two bits, RdDram and WrDram, that determine the destination based on the access type. Writing Reserved MemType values causes an error-on-write. If Core::X86::Msrr::SYS_CFG[SecureNestedPagingEn] is set to 1, this register will be read-only and attempts to write to this register will result in #GP(0).

_ccd[1:0]_lthree0_core[7:0]_nSIZE4K0; MSR0000_0268

Bits	Description																
63:61	Reserved.																
60	RdDram_4K_C7000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
59	WrDram_4K_C7000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
58:56	MemType_4K_C7000: memory type. Read-write. Reset: XXXb. ValidValues: <table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>UC or uncacheable.</td></tr> <tr> <td>1h</td><td>WC or write combining.</td></tr> <tr> <td>3h-2h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>WT or write through.</td></tr> <tr> <td>5h</td><td>WP or write protect.</td></tr> <tr> <td>6h</td><td>WB or write back.</td></tr> <tr> <td>7h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
Value	Description																
0h	UC or uncacheable.																
1h	WC or write combining.																
3h-2h	Reserved.																
4h	WT or write through.																
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																
55:53	Reserved.																
52	RdDram_4K_C6000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
51	WrDram_4K_C6000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
50:48	MemType_4K_C6000: memory type. Read-write. Reset: XXXb. ValidValues: <table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>UC or uncacheable.</td></tr> <tr> <td>1h</td><td>WC or write combining.</td></tr> <tr> <td>3h-2h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>WT or write through.</td></tr> <tr> <td>5h</td><td>WP or write protect.</td></tr> <tr> <td>6h</td><td>WB or write back.</td></tr> <tr> <td>7h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
Value	Description																
0h	UC or uncacheable.																
1h	WC or write combining.																
3h-2h	Reserved.																
4h	WT or write through.																
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																
47:45	Reserved.																
44	RdDram_4K_C5000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM.																

	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
43	WrDram_4K_C5000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
42:40	MemType_4K_C5000: memory type. Read-write. Reset: XXXb. ValidValues:																
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>UC or uncacheable.</td></tr> <tr> <td>1h</td><td>WC or write combining.</td></tr> <tr> <td>3h-2h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>WT or write through.</td></tr> <tr> <td>5h</td><td>WP or write protect.</td></tr> <tr> <td>6h</td><td>WB or write back.</td></tr> <tr> <td>7h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
Value	Description																
0h	UC or uncacheable.																
1h	WC or write combining.																
3h-2h	Reserved.																
4h	WT or write through.																
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																
39:37	Reserved.																
36	RdDram_4K_C4000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
35	WrDram_4K_C4000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
34:32	MemType_4K_C4000: memory type. Read-write. Reset: XXXb. ValidValues:																
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>UC or uncacheable.</td></tr> <tr> <td>1h</td><td>WC or write combining.</td></tr> <tr> <td>3h-2h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>WT or write through.</td></tr> <tr> <td>5h</td><td>WP or write protect.</td></tr> <tr> <td>6h</td><td>WB or write back.</td></tr> <tr> <td>7h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
Value	Description																
0h	UC or uncacheable.																
1h	WC or write combining.																
3h-2h	Reserved.																
4h	WT or write through.																
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																
31:29	Reserved.																
28	RdDram_4K_C3000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
27	WrDram_4K_C3000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
26:24	MemType_4K_C3000: memory type. Read-write. Reset: XXXb.																

	ValidValues:	
	Value	Description
	0h	UC or uncacheable.
	1h	WC or write combining.
	3h-2h	Reserved.
	4h	WT or write through.
	5h	WP or write protect.
	6h	WB or write back.
	7h	Reserved.
23:21	Reserved.	
20	RdDram_4K_C2000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM.	
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.	
19	WrDram_4K_C2000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM.	
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.	
18:16	MemType_4K_C2000: memory type. Read-write. Reset: XXXb.	
	ValidValues:	
	Value	Description
	0h	UC or uncacheable.
	1h	WC or write combining.
	3h-2h	Reserved.
	4h	WT or write through.
	5h	WP or write protect.
	6h	WB or write back.
	7h	Reserved.
15:13	Reserved.	
12	RdDram_4K_C1000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM.	
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.	
11	WrDram_4K_C1000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM.	
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.	
10:8	MemType_4K_C1000: memory type. Read-write. Reset: XXXb.	
	ValidValues:	
	Value	Description
	0h	UC or uncacheable.
	1h	WC or write combining.
	3h-2h	Reserved.
	4h	WT or write through.
	5h	WP or write protect.
	6h	WB or write back.
	7h	Reserved.
7:5	Reserved.	

4	RdDram_4K_C0000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. Address range from C0000h to C0FFFh. Core::X86::Msr::SYS_CFG[MtrrFixDramEn,MtrrFixDramModEn] masks Reads of the stored value.																
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
3	WrDram_4K_C0000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. Address range from C0000h to C0FFFh. Core::X86::Msr::SYS_CFG[MtrrFixDramEn,MtrrFixDramModEn] masks Reads of the stored value.																
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
2:0	MemType_4K_C0000: memory type. Read-write. Reset: XXXb. Address range from C0000h to C0FFFh.																
	ValidValues:																
	<table><tr><th>Value</th><th>Description</th></tr><tr><td>0h</td><td>UC or uncacheable.</td></tr><tr><td>1h</td><td>WC or write combining.</td></tr><tr><td>3h-2h</td><td>Reserved.</td></tr><tr><td>4h</td><td>WT or write through.</td></tr><tr><td>5h</td><td>WP or write protect.</td></tr><tr><td>6h</td><td>WB or write back.</td></tr><tr><td>7h</td><td>Reserved.</td></tr></table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
	Value	Description															
	0h	UC or uncacheable.															
	1h	WC or write combining.															
	3h-2h	Reserved.															
	4h	WT or write through.															
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																

MSR0000_0269 [Fixed-Size MTRRs] (Core::X86::Msrr::MtrrFix_4K_1)

See Core::X86::Msrr::MtrrVarBase for general MTRR information. Fixed MTRRs are enabled through Core::X86::Msrr::MTRRdefType[MtrrDefTypeFixEn,MtrrDefTypeEn]. For addresses below 1MB, the appropriate Fixed MTRRs override the default access destination. Each fixed MTRR includes two bits, RdDram and WrDram, that determine the destination based on the access type. Writing Reserved MemType values causes an error-on-write. If Core::X86::Msrr::SYS_CFG[SecureNestedPagingEn] is set to 1, this register will be read-only and attempts to write to this register will result in #GP(0).

_ccd[1:0]_lthree0_core[7:0]_nSIZE4K1; MSR0000_0269

Bits	Description																
63:61	Reserved.																
60	RdDram_4K_CF000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
59	WrDram_4K_CF000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
58:56	MemType_4K_CF000: memory type. Read-write. Reset: XXXb. ValidValues: <table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>UC or uncacheable.</td></tr> <tr> <td>1h</td><td>WC or write combining.</td></tr> <tr> <td>3h-2h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>WT or write through.</td></tr> <tr> <td>5h</td><td>WP or write protect.</td></tr> <tr> <td>6h</td><td>WB or write back.</td></tr> <tr> <td>7h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
Value	Description																
0h	UC or uncacheable.																
1h	WC or write combining.																
3h-2h	Reserved.																
4h	WT or write through.																
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																
55:53	Reserved.																
52	RdDram_4K_CE000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
51	WrDram_4K_CE000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
50:48	MemType_4K_CE000: memory type. Read-write. Reset: XXXb. ValidValues: <table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>UC or uncacheable.</td></tr> <tr> <td>1h</td><td>WC or write combining.</td></tr> <tr> <td>3h-2h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>WT or write through.</td></tr> <tr> <td>5h</td><td>WP or write protect.</td></tr> <tr> <td>6h</td><td>WB or write back.</td></tr> <tr> <td>7h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
Value	Description																
0h	UC or uncacheable.																
1h	WC or write combining.																
3h-2h	Reserved.																
4h	WT or write through.																
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																
47:45	Reserved.																
44	RdDram_4K_CD000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM.																

	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
43	WrDram_4K_CD000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
42:40	MemType_4K_CD000: memory type. Read-write. Reset: XXXb. ValidValues:																
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>UC or uncacheable.</td></tr> <tr> <td>1h</td><td>WC or write combining.</td></tr> <tr> <td>3h-2h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>WT or write through.</td></tr> <tr> <td>5h</td><td>WP or write protect.</td></tr> <tr> <td>6h</td><td>WB or write back.</td></tr> <tr> <td>7h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
Value	Description																
0h	UC or uncacheable.																
1h	WC or write combining.																
3h-2h	Reserved.																
4h	WT or write through.																
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																
39:37	Reserved.																
36	RdDram_4K_CC000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
35	WrDram_4K_CC000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
34:32	MemType_4K_CC000: memory type. Read-write. Reset: XXXb. ValidValues:																
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>UC or uncacheable.</td></tr> <tr> <td>1h</td><td>WC or write combining.</td></tr> <tr> <td>3h-2h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>WT or write through.</td></tr> <tr> <td>5h</td><td>WP or write protect.</td></tr> <tr> <td>6h</td><td>WB or write back.</td></tr> <tr> <td>7h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
Value	Description																
0h	UC or uncacheable.																
1h	WC or write combining.																
3h-2h	Reserved.																
4h	WT or write through.																
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																
31:29	Reserved.																
28	RdDram_4K_CB000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
27	WrDram_4K_CB000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
26:24	MemType_4K_CB000: memory type. Read-write. Reset: XXXb.																

	ValidValues:	
	Value	Description
	0h	UC or uncacheable.
	1h	WC or write combining.
	3h-2h	Reserved.
	4h	WT or write through.
	5h	WP or write protect.
	6h	WB or write back.
	7h	Reserved.
23:21	Reserved.	
20	RdDram_4K_CA000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM.	
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.	
19	WrDram_4K_CA000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM.	
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.	
18:16	MemType_4K_CA000: memory type. Read-write. Reset: XXXb.	
	ValidValues:	
	Value	Description
	0h	UC or uncacheable.
	1h	WC or write combining.
	3h-2h	Reserved.
	4h	WT or write through.
	5h	WP or write protect.
	6h	WB or write back.
	7h	Reserved.
15:13	Reserved.	
12	RdDram_4K_C9000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM.	
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.	
11	WrDram_4K_C9000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM.	
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.	
10:8	MemType_4K_C9000: memory type. Read-write. Reset: XXXb.	
	ValidValues:	
	Value	Description
	0h	UC or uncacheable.
	1h	WC or write combining.
	3h-2h	Reserved.
	4h	WT or write through.
	5h	WP or write protect.
	6h	WB or write back.
	7h	Reserved.
7:5	Reserved.	

4	RdDram_4K_C8000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. Address range from C8000 to C8FFF. Core::X86::Msr::SYS_CFG[MtrrFixDramEn,MtrrFixDramModEn] masks Reads of the stored value.																
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
3	WrDram_4K_C8000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. Address range from C8000 to C8FFF. Core::X86::Msr::SYS_CFG[MtrrFixDramEn,MtrrFixDramModEn] masks Reads of the stored value.																
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
2:0	MemType_4K_C8000: memory type. Read-write. Reset: XXXb. Address range from C8000 to C8FFF.																
	ValidValues:																
	<table><tr><th>Value</th><th>Description</th></tr><tr><td>0h</td><td>UC or uncacheable.</td></tr><tr><td>1h</td><td>WC or write combining.</td></tr><tr><td>3h-2h</td><td>Reserved.</td></tr><tr><td>4h</td><td>WT or write through.</td></tr><tr><td>5h</td><td>WP or write protect.</td></tr><tr><td>6h</td><td>WB or write back.</td></tr><tr><td>7h</td><td>Reserved.</td></tr></table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
	Value	Description															
	0h	UC or uncacheable.															
	1h	WC or write combining.															
	3h-2h	Reserved.															
	4h	WT or write through.															
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																

MSR0000_026A [Fixed-Size MTRRs] (Core::X86::Msrr::MtrrFix_4K_2)

See Core::X86::Msrr::MtrrVarBase for general MTRR information. Fixed MTRRs are enabled through Core::X86::Msrr::MTRRdefType[MtrrDefTypeFixEn,MtrrDefTypeEn]. For addresses below 1MB, the appropriate Fixed MTRRs override the default access destination. Each fixed MTRR includes two bits, RdDram and WrDram, that determine the destination based on the access type. Writing Reserved MemType values causes an error-on-write. If Core::X86::Msrr::SYS_CFG[SecureNestedPagingEn] is set to 1, this register will be read-only and attempts to write to this register will result in #GP(0).

_ccd[1:0]_lthree0_core[7:0]_nSIZE4K2; MSR0000_026A

Bits	Description																
63:61	Reserved.																
60	RdDram_4K_D7000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
59	WrDram_4K_D7000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
58:56	MemType_4K_D7000: memory type. Read-write. Reset: XXXb. ValidValues: <table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>UC or uncacheable.</td></tr> <tr> <td>1h</td><td>WC or write combining.</td></tr> <tr> <td>3h-2h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>WT or write through.</td></tr> <tr> <td>5h</td><td>WP or write protect.</td></tr> <tr> <td>6h</td><td>WB or write back.</td></tr> <tr> <td>7h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
Value	Description																
0h	UC or uncacheable.																
1h	WC or write combining.																
3h-2h	Reserved.																
4h	WT or write through.																
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																
55:53	Reserved.																
52	RdDram_4K_D6000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
51	WrDram_4K_D6000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
50:48	MemType_4K_D6000: memory type. Read-write. Reset: XXXb. ValidValues: <table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>UC or uncacheable.</td></tr> <tr> <td>1h</td><td>WC or write combining.</td></tr> <tr> <td>3h-2h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>WT or write through.</td></tr> <tr> <td>5h</td><td>WP or write protect.</td></tr> <tr> <td>6h</td><td>WB or write back.</td></tr> <tr> <td>7h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
Value	Description																
0h	UC or uncacheable.																
1h	WC or write combining.																
3h-2h	Reserved.																
4h	WT or write through.																
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																
47:45	Reserved.																
44	RdDram_4K_D5000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM.																

	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
43	WrDram_4K_D5000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
42:40	MemType_4K_D5000: memory type. Read-write. Reset: XXXb. ValidValues:																
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>UC or uncacheable.</td></tr> <tr> <td>1h</td><td>WC or write combining.</td></tr> <tr> <td>3h-2h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>WT or write through.</td></tr> <tr> <td>5h</td><td>WP or write protect.</td></tr> <tr> <td>6h</td><td>WB or write back.</td></tr> <tr> <td>7h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
Value	Description																
0h	UC or uncacheable.																
1h	WC or write combining.																
3h-2h	Reserved.																
4h	WT or write through.																
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																
39:37	Reserved.																
36	RdDram_4K_D4000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
35	WrDram_4K_D4000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
34:32	MemType_4K_D4000: memory type. Read-write. Reset: XXXb. ValidValues:																
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>UC or uncacheable.</td></tr> <tr> <td>1h</td><td>WC or write combining.</td></tr> <tr> <td>3h-2h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>WT or write through.</td></tr> <tr> <td>5h</td><td>WP or write protect.</td></tr> <tr> <td>6h</td><td>WB or write back.</td></tr> <tr> <td>7h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
Value	Description																
0h	UC or uncacheable.																
1h	WC or write combining.																
3h-2h	Reserved.																
4h	WT or write through.																
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																
31:29	Reserved.																
28	RdDram_4K_D3000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
27	WrDram_4K_D3000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
26:24	MemType_4K_D3000: memory type. Read-write. Reset: XXXb.																

	ValidValues:	
	Value	Description
	0h	UC or uncacheable.
	1h	WC or write combining.
	3h-2h	Reserved.
	4h	WT or write through.
	5h	WP or write protect.
	6h	WB or write back.
	7h	Reserved.
23:21	Reserved.	
20	RdDram_4K_D2000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM.	
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.	
19	WrDram_4K_D2000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM.	
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.	
18:16	MemType_4K_D2000: memory type. Read-write. Reset: XXXb.	
	ValidValues:	
	Value	Description
	0h	UC or uncacheable.
	1h	WC or write combining.
	3h-2h	Reserved.
	4h	WT or write through.
	5h	WP or write protect.
	6h	WB or write back.
	7h	Reserved.
15:13	Reserved.	
12	RdDram_4K_D1000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM.	
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.	
11	WrDram_4K_D1000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM.	
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.	
10:8	MemType_4K_D1000: memory type. Read-write. Reset: XXXb.	
	ValidValues:	
	Value	Description
	0h	UC or uncacheable.
	1h	WC or write combining.
	3h-2h	Reserved.
	4h	WT or write through.
	5h	WP or write protect.
	6h	WB or write back.
	7h	Reserved.
7:5	Reserved.	

4	RdDram_4K_D0000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. Address range from D0000h to D0FFFh. Core::X86::Msr::SYS_CFG[MtrrFixDramEn,MtrrFixDramModEn] masks Reads of the stored value.																
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
3	WrDram_4K_D0000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. Address range from D0000h to D0FFFh. Core::X86::Msr::SYS_CFG[MtrrFixDramEn,MtrrFixDramModEn] masks reads of the stored value.																
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
2:0	MemType_4K_D0000: memory type. Read-write. Reset: XXXb. Address range from D0000h to D0FFFh.																
	ValidValues:																
	<table><tr><th>Value</th><th>Description</th></tr><tr><td>0h</td><td>UC or uncacheable.</td></tr><tr><td>1h</td><td>WC or write combining.</td></tr><tr><td>3h-2h</td><td>Reserved.</td></tr><tr><td>4h</td><td>WT or write through.</td></tr><tr><td>5h</td><td>WP or write protect.</td></tr><tr><td>6h</td><td>WB or write back.</td></tr><tr><td>7h</td><td>Reserved.</td></tr></table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
	Value	Description															
	0h	UC or uncacheable.															
	1h	WC or write combining.															
	3h-2h	Reserved.															
	4h	WT or write through.															
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																

MSR0000_026B [Fixed-Size MTRRs] (Core::X86::Msrr::MtrrFix_4K_3)

See Core::X86::Msrr::MtrrVarBase for general MTRR information. Fixed MTRRs are enabled through Core::X86::Msrr::MTRRdefType[MtrrDefTypeFixEn,MtrrDefTypeEn]. For addresses below 1MB, the appropriate Fixed MTRRs override the default access destination. Each fixed MTRR includes two bits, RdDram and WrDram, that determine the destination based on the access type. Writing Reserved MemType values causes an error-on-write. If Core::X86::Msrr::SYS_CFG[SecureNestedPagingEn] is set to 1, this register will be read-only and attempts to write to this register will result in #GP(0).

_ccd[1:0]_lthree0_core[7:0]_nSIZE4K3; MSR0000_026B

Bits	Description																
63:61	Reserved.																
60	RdDram_4K_DF000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
59	WrDram_4K_DF000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
58:56	MemType_4K_DF000: memory type. Read-write. Reset: XXXb. ValidValues: <table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>UC or uncacheable.</td></tr> <tr> <td>1h</td><td>WC or write combining.</td></tr> <tr> <td>3h-2h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>WT or write through.</td></tr> <tr> <td>5h</td><td>WP or write protect.</td></tr> <tr> <td>6h</td><td>WB or write back.</td></tr> <tr> <td>7h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
Value	Description																
0h	UC or uncacheable.																
1h	WC or write combining.																
3h-2h	Reserved.																
4h	WT or write through.																
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																
55:53	Reserved.																
52	RdDram_4K_DE000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
51	WrDram_4K_DE000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
50:48	MemType_4K_DE000: memory type. Read-write. Reset: XXXb. ValidValues: <table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>UC or uncacheable.</td></tr> <tr> <td>1h</td><td>WC or write combining.</td></tr> <tr> <td>3h-2h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>WT or write through.</td></tr> <tr> <td>5h</td><td>WP or write protect.</td></tr> <tr> <td>6h</td><td>WB or write back.</td></tr> <tr> <td>7h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
Value	Description																
0h	UC or uncacheable.																
1h	WC or write combining.																
3h-2h	Reserved.																
4h	WT or write through.																
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																
47:45	Reserved.																
44	RdDram_4K_DD000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM.																

	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
43	WrDram_4K_DD000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
42:40	MemType_4K_DD000: memory type. Read-write. Reset: XXXb. ValidValues:																
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>UC or uncacheable.</td></tr> <tr> <td>1h</td><td>WC or write combining.</td></tr> <tr> <td>3h-2h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>WT or write through.</td></tr> <tr> <td>5h</td><td>WP or write protect.</td></tr> <tr> <td>6h</td><td>WB or write back.</td></tr> <tr> <td>7h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
Value	Description																
0h	UC or uncacheable.																
1h	WC or write combining.																
3h-2h	Reserved.																
4h	WT or write through.																
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																
39:37	Reserved.																
36	RdDram_4K_DC000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
35	WrDram_4K_DC000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
34:32	MemType_4K_DC000: memory type. Read-write. Reset: XXXb. ValidValues:																
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>UC or uncacheable.</td></tr> <tr> <td>1h</td><td>WC or write combining.</td></tr> <tr> <td>3h-2h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>WT or write through.</td></tr> <tr> <td>5h</td><td>WP or write protect.</td></tr> <tr> <td>6h</td><td>WB or write back.</td></tr> <tr> <td>7h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
Value	Description																
0h	UC or uncacheable.																
1h	WC or write combining.																
3h-2h	Reserved.																
4h	WT or write through.																
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																
31:29	Reserved.																
28	RdDram_4K_DB000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
27	WrDram_4K_DB000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
26:24	MemType_4K_DB000: memory type. Read-write. Reset: XXXb.																

	ValidValues:	
	Value	Description
	0h	UC or uncacheable.
	1h	WC or write combining.
	3h-2h	Reserved.
	4h	WT or write through.
	5h	WP or write protect.
	6h	WB or write back.
	7h	Reserved.
23:21	Reserved.	
20	RdDram_4K_DA000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM.	
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.	
19	WrDram_4K_DA000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM.	
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.	
18:16	MemType_4K_DA000: memory type. Read-write. Reset: XXXb.	
	ValidValues:	
	Value	Description
	0h	UC or uncacheable.
	1h	WC or write combining.
	3h-2h	Reserved.
	4h	WT or write through.
	5h	WP or write protect.
	6h	WB or write back.
	7h	Reserved.
15:13	Reserved.	
12	RdDram_4K_D9000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM.	
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.	
11	WrDram_4K_D9000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM.	
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.	
10:8	MemType_4K_D9000: memory type. Read-write. Reset: XXXb.	
	ValidValues:	
	Value	Description
	0h	UC or uncacheable.
	1h	WC or write combining.
	3h-2h	Reserved.
	4h	WT or write through.
	5h	WP or write protect.
	6h	WB or write back.
	7h	Reserved.
7:5	Reserved.	

4	RdDram_4K_D8000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. Address range from D8000h to D8FFFh. Core::X86::Msr::SYS_CFG[MtrrFixDramEn,MtrrFixDramModEn] masks Reads of the stored value.																
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
3	WrDram_4K_D8000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. Address range from D8000h to D8FFFh. Core::X86::Msr::SYS_CFG[MtrrFixDramEn,MtrrFixDramModEn] masks Reads of the stored value.																
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
2:0	MemType_4K_D8000: memory type. Read-write. Reset: XXXb. Address range from D8000h to D8FFFh.																
	ValidValues:																
	<table><tr><th>Value</th><th>Description</th></tr><tr><td>0h</td><td>UC or uncacheable.</td></tr><tr><td>1h</td><td>WC or write combining.</td></tr><tr><td>3h-2h</td><td>Reserved.</td></tr><tr><td>4h</td><td>WT or write through.</td></tr><tr><td>5h</td><td>WP or write protect.</td></tr><tr><td>6h</td><td>WB or write back.</td></tr><tr><td>7h</td><td>Reserved.</td></tr></table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
	Value	Description															
	0h	UC or uncacheable.															
	1h	WC or write combining.															
	3h-2h	Reserved.															
	4h	WT or write through.															
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																

MSR0000_026C [Fixed-Size MTRRs] (Core::X86::Msrr::MtrrFix_4K_4)

See Core::X86::Msrr::MtrrVarBase for general MTRR information. Fixed MTRRs are enabled through Core::X86::Msrr::MTRRdefType[MtrrDefTypeFixEn,MtrrDefTypeEn]. For addresses below 1MB, the appropriate Fixed MTRRs override the default access destination. Each fixed MTRR includes two bits, RdDram and WrDram, that determine the destination based on the access type. Writing reserved MemType values causes an error-on-write. If Core::X86::Msrr::SYS_CFG[SecureNestedPagingEn] is set to 1, this register will be read-only and attempts to write to this register will result in #GP(0).

_ccd[1:0]_lthree0_core[7:0]_nSIZE4K4; MSR0000_026C

Bits	Description																
63:61	Reserved.																
60	RdDram_4K_E7000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
59	WrDram_4K_E7000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
58:56	MemType_4K_E7000: memory type. Read-write. Reset: XXXb. ValidValues: <table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>UC or uncacheable.</td></tr> <tr> <td>1h</td><td>WC or write combining.</td></tr> <tr> <td>3h-2h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>WT or write through.</td></tr> <tr> <td>5h</td><td>WP or write protect.</td></tr> <tr> <td>6h</td><td>WB or write back.</td></tr> <tr> <td>7h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
Value	Description																
0h	UC or uncacheable.																
1h	WC or write combining.																
3h-2h	Reserved.																
4h	WT or write through.																
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																
55:53	Reserved.																
52	RdDram_4K_E6000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
51	WrDram_4K_E6000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
50:48	MemType_4K_E6000: memory type. Read-write. Reset: XXXb. ValidValues: <table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>UC or uncacheable.</td></tr> <tr> <td>1h</td><td>WC or write combining.</td></tr> <tr> <td>3h-2h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>WT or write through.</td></tr> <tr> <td>5h</td><td>WP or write protect.</td></tr> <tr> <td>6h</td><td>WB or write back.</td></tr> <tr> <td>7h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
Value	Description																
0h	UC or uncacheable.																
1h	WC or write combining.																
3h-2h	Reserved.																
4h	WT or write through.																
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																
47:45	Reserved.																
44	RdDram_4K_E5000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM.																

	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
43	WrDram_4K_E5000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
42:40	MemType_4K_E5000: memory type. Read-write. Reset: XXXb. ValidValues:																
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>UC or uncacheable.</td></tr> <tr> <td>1h</td><td>WC or write combining.</td></tr> <tr> <td>3h-2h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>WT or write through.</td></tr> <tr> <td>5h</td><td>WP or write protect.</td></tr> <tr> <td>6h</td><td>WB or write back.</td></tr> <tr> <td>7h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
Value	Description																
0h	UC or uncacheable.																
1h	WC or write combining.																
3h-2h	Reserved.																
4h	WT or write through.																
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																
39:37	Reserved.																
36	RdDram_4K_E4000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
35	WrDram_4K_E4000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
34:32	MemType_4K_E4000: memory type. Read-write. Reset: XXXb. ValidValues:																
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>UC or uncacheable.</td></tr> <tr> <td>1h</td><td>WC or write combining.</td></tr> <tr> <td>3h-2h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>WT or write through.</td></tr> <tr> <td>5h</td><td>WP or write protect.</td></tr> <tr> <td>6h</td><td>WB or write back.</td></tr> <tr> <td>7h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
Value	Description																
0h	UC or uncacheable.																
1h	WC or write combining.																
3h-2h	Reserved.																
4h	WT or write through.																
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																
31:29	Reserved.																
28	RdDram_4K_E3000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
27	WrDram_4K_E3000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
26:24	MemType_4K_E3000: memory type. Read-write. Reset: XXXb.																

	ValidValues:	
	Value	Description
	0h	UC or uncacheable.
	1h	WC or write combining.
	3h-2h	Reserved.
	4h	WT or write through.
	5h	WP or write protect.
	6h	WB or write back.
	7h	Reserved.
23:21	Reserved.	
20	RdDram_4K_E2000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM.	
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.	
19	WrDram_4K_E2000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM.	
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.	
18:16	MemType_4K_E2000: memory type. Read-write. Reset: XXXb.	
	ValidValues:	
	Value	Description
	0h	UC or uncacheable.
	1h	WC or write combining.
	3h-2h	Reserved.
	4h	WT or write through.
	5h	WP or write protect.
	6h	WB or write back.
	7h	Reserved.
15:13	Reserved.	
12	RdDram_4K_E1000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM.	
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.	
11	WrDram_4K_E1000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM.	
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.	
10:8	MemType_4K_E1000: memory type. Read-write. Reset: XXXb.	
	ValidValues:	
	Value	Description
	0h	UC or uncacheable.
	1h	WC or write combining.
	3h-2h	Reserved.
	4h	WT or write through.
	5h	WP or write protect.
	6h	WB or write back.
	7h	Reserved.
7:5	Reserved.	

4	RdDram_4K_E0000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. Address range from E0000h to E0FFFh. Core::X86::Msr::SYS_CFG[MtrrFixDramEn,MtrrFixDramModEn] masks Reads of the stored value.																
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
3	WrDram_4K_E0000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. Address range from E0000h to E0FFFh. Core::X86::Msr::SYS_CFG[MtrrFixDramEn,MtrrFixDramModEn] masks Reads of the stored value.																
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
2:0	MemType_4K_E0000: memory type. Read-write. Reset: XXXb. Address range from E0000h to E0FFFh.																
	ValidValues:																
	<table><tr><th>Value</th><th>Description</th></tr><tr><td>0h</td><td>UC or uncacheable.</td></tr><tr><td>1h</td><td>WC or write combining.</td></tr><tr><td>3h-2h</td><td>Reserved.</td></tr><tr><td>4h</td><td>WT or write through.</td></tr><tr><td>5h</td><td>WP or write protect.</td></tr><tr><td>6h</td><td>WB or write back.</td></tr><tr><td>7h</td><td>Reserved.</td></tr></table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
	Value	Description															
	0h	UC or uncacheable.															
	1h	WC or write combining.															
	3h-2h	Reserved.															
	4h	WT or write through.															
	5h	WP or write protect.															
6h	WB or write back.																
7h	Reserved.																

MSR0000_026D [Fixed-Size MTRRs] (Core::X86::Msrr::MtrrFix_4K_5)

See Core::X86::Msrr::MtrrVarBase for general MTRR information. Fixed MTRRs are enabled through Core::X86::Msrr::MTRRdefType[MtrrDefTypeFixEn,MtrrDefTypeEn]. For addresses below 1MB, the appropriate Fixed MTRRs override the default access destination. Each fixed MTRR includes two bits, RdDram and WrDram, that determine the destination based on the access type. Writing Reserved MemType values causes an error-on-write. If Core::X86::Msrr::SYS_CFG[SecureNestedPagingEn] is set to 1, this register will be read-only and attempts to write to this register will result in #GP(0).

_ccd[1:0]_lthree0_core[7:0]_nSIZE4K5; MSR0000_026D

Bits	Description																
63:61	Reserved.																
60	RdDram_4K_EF000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
59	WrDram_4K_EF000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
58:56	MemType_4K_EF000: memory type. Read-write. Reset: XXXb. ValidValues: <table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>UC or uncacheable.</td></tr> <tr> <td>1h</td><td>WC or write combining.</td></tr> <tr> <td>3h-2h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>WT or write through.</td></tr> <tr> <td>5h</td><td>WP or write protect.</td></tr> <tr> <td>6h</td><td>WB or write back.</td></tr> <tr> <td>7h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
Value	Description																
0h	UC or uncacheable.																
1h	WC or write combining.																
3h-2h	Reserved.																
4h	WT or write through.																
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																
55:53	Reserved.																
52	RdDram_4K_EE000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
51	WrDram_4K_EE000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
50:48	MemType_4K_EE000: memory type. Read-write. Reset: XXXb. ValidValues: <table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>UC or uncacheable.</td></tr> <tr> <td>1h</td><td>WC or write combining.</td></tr> <tr> <td>3h-2h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>WT or write through.</td></tr> <tr> <td>5h</td><td>WP or write protect.</td></tr> <tr> <td>6h</td><td>WB or write back.</td></tr> <tr> <td>7h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
Value	Description																
0h	UC or uncacheable.																
1h	WC or write combining.																
3h-2h	Reserved.																
4h	WT or write through.																
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																
47:45	Reserved.																
44	RdDram_4K_ED000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM.																

	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
43	WrDram_4K_ED000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
42:40	MemType_4K_ED000: memory type. Read-write. Reset: XXXb. ValidValues:																
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>UC or uncacheable.</td></tr> <tr> <td>1h</td><td>WC or write combining.</td></tr> <tr> <td>3h-2h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>WT or write through.</td></tr> <tr> <td>5h</td><td>WP or write protect.</td></tr> <tr> <td>6h</td><td>WB or write back.</td></tr> <tr> <td>7h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
Value	Description																
0h	UC or uncacheable.																
1h	WC or write combining.																
3h-2h	Reserved.																
4h	WT or write through.																
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																
39:37	Reserved.																
36	RdDram_4K_EC000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
35	WrDram_4K_EC000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
34:32	MemType_4K_EC000: memory type. Read-write. Reset: XXXb. ValidValues:																
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>UC or uncacheable.</td></tr> <tr> <td>1h</td><td>WC or write combining.</td></tr> <tr> <td>3h-2h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>WT or write through.</td></tr> <tr> <td>5h</td><td>WP or write protect.</td></tr> <tr> <td>6h</td><td>WB or write back.</td></tr> <tr> <td>7h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
Value	Description																
0h	UC or uncacheable.																
1h	WC or write combining.																
3h-2h	Reserved.																
4h	WT or write through.																
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																
31:29	Reserved.																
28	RdDram_4K_EB000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
27	WrDram_4K_EB000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
26:24	MemType_4K_EB000: memory type. Read-write. Reset: XXXb.																

	ValidValues:	
	Value	Description
	0h	UC or uncacheable.
	1h	WC or write combining.
	3h-2h	Reserved.
	4h	WT or write through.
	5h	WP or write protect.
	6h	WB or write back.
	7h	Reserved.
23:21	Reserved.	
20	RdDram_4K_EA000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM.	
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.	
19	WrDram_4K_EA000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM.	
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.	
18:16	MemType_4K_EA000: memory type. Read-write. Reset: XXXb.	
	ValidValues:	
	Value	Description
	0h	UC or uncacheable.
	1h	WC or write combining.
	3h-2h	Reserved.
	4h	WT or write through.
	5h	WP or write protect.
	6h	WB or write back.
	7h	Reserved.
15:13	Reserved.	
12	RdDram_4K_E9000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM.	
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.	
11	WrDram_4K_E9000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM.	
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.	
10:8	MemType_4K_E9000: memory type. Read-write. Reset: XXXb.	
	ValidValues:	
	Value	Description
	0h	UC or uncacheable.
	1h	WC or write combining.
	3h-2h	Reserved.
	4h	WT or write through.
	5h	WP or write protect.
	6h	WB or write back.
	7h	Reserved.
7:5	Reserved.	

4	RdDram_4K_E8000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. Address range from E8000h to E8FFFh. Core::X86::Msr::SYS_CFG[MtrrFixDramEn,MtrrFixDramModEn] masks Reads of the stored value.																
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
3	WrDram_4K_E8000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. Address range from E8000h to E8FFFh. Core::X86::Msr::SYS_CFG[MtrrFixDramEn,MtrrFixDramModEn] masks Reads of the stored value.																
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
2:0	MemType_4K_E8000: memory type. Read-write. Reset: XXXb. Address range from E8000h to E8FFFh.																
	ValidValues:																
	<table><tr><th>Value</th><th>Description</th></tr><tr><td>0h</td><td>UC or uncacheable.</td></tr><tr><td>1h</td><td>WC or write combining.</td></tr><tr><td>3h-2h</td><td>Reserved.</td></tr><tr><td>4h</td><td>WT or write through.</td></tr><tr><td>5h</td><td>WP or write protect.</td></tr><tr><td>6h</td><td>WB or write back.</td></tr><tr><td>7h</td><td>Reserved.</td></tr></table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
	Value	Description															
	0h	UC or uncacheable.															
	1h	WC or write combining.															
	3h-2h	Reserved.															
	4h	WT or write through.															
	5h	WP or write protect.															
6h	WB or write back.																
7h	Reserved.																

MSR0000_026E [Fixed-Size MTRRs] (Core::X86::Msrr::MtrrFix_4K_6)

See Core::X86::Msrr::MtrrVarBase for general MTRR information. Fixed MTRRs are enabled through Core::X86::Msrr::MTRRdefType[MtrrDefTypeFixEn,MtrrDefTypeEn]. For addresses below 1MB, the appropriate Fixed MTRRs override the default access destination. Each fixed MTRR includes two bits, RdDram and WrDram, that determine the destination based on the access type. Writing Reserved MemType values causes an error-on-write. If Core::X86::Msrr::SYS_CFG[SecureNestedPagingEn] is set to 1, this register will be read-only and attempts to write to this register will result in #GP(0).

_ccd[1:0]_lthree0_core[7:0]_nSIZE4K6; MSR0000_026E

Bits	Description																
63:61	Reserved.																
60	RdDram_4K_F7000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
59	WrDram_4K_F7000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
58:56	MemType_4K_F7000: memory type. Read-write. Reset: XXXb. ValidValues: <table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>UC or uncacheable.</td></tr> <tr> <td>1h</td><td>WC or write combining.</td></tr> <tr> <td>3h-2h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>WT or write through.</td></tr> <tr> <td>5h</td><td>WP or write protect.</td></tr> <tr> <td>6h</td><td>WB or write back.</td></tr> <tr> <td>7h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
Value	Description																
0h	UC or uncacheable.																
1h	WC or write combining.																
3h-2h	Reserved.																
4h	WT or write through.																
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																
55:53	Reserved.																
52	RdDram_4K_F6000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
51	WrDram_4K_F6000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
50:48	MemType_4K_F6000: memory type. Read-write. Reset: XXXb. ValidValues: <table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>UC or uncacheable.</td></tr> <tr> <td>1h</td><td>WC or write combining.</td></tr> <tr> <td>3h-2h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>WT or write through.</td></tr> <tr> <td>5h</td><td>WP or write protect.</td></tr> <tr> <td>6h</td><td>WB or write back.</td></tr> <tr> <td>7h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
Value	Description																
0h	UC or uncacheable.																
1h	WC or write combining.																
3h-2h	Reserved.																
4h	WT or write through.																
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																
47:45	Reserved.																
44	RdDram_4K_F5000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM.																

	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
43	WrDram_4K_F5000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
42:40	MemType_4K_F5000: memory type. Read-write. Reset: XXXb. ValidValues:																
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>UC or uncacheable.</td></tr> <tr> <td>1h</td><td>WC or write combining.</td></tr> <tr> <td>3h-2h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>WT or write through.</td></tr> <tr> <td>5h</td><td>WP or write protect.</td></tr> <tr> <td>6h</td><td>WB or write back.</td></tr> <tr> <td>7h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
Value	Description																
0h	UC or uncacheable.																
1h	WC or write combining.																
3h-2h	Reserved.																
4h	WT or write through.																
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																
39:37	Reserved.																
36	RdDram_4K_F4000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
35	WrDram_4K_F4000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
34:32	MemType_4K_F4000: memory type. Read-write. Reset: XXXb. ValidValues:																
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>UC or uncacheable.</td></tr> <tr> <td>1h</td><td>WC or write combining.</td></tr> <tr> <td>3h-2h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>WT or write through.</td></tr> <tr> <td>5h</td><td>WP or write protect.</td></tr> <tr> <td>6h</td><td>WB or write back.</td></tr> <tr> <td>7h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
Value	Description																
0h	UC or uncacheable.																
1h	WC or write combining.																
3h-2h	Reserved.																
4h	WT or write through.																
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																
31:29	Reserved.																
28	RdDram_4K_F3000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
27	WrDram_4K_F3000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
26:24	MemType_4K_F3000: memory type. Read-write. Reset: XXXb.																

	ValidValues:	
	Value	Description
	0h	UC or uncacheable.
	1h	WC or write combining.
	3h-2h	Reserved.
	4h	WT or write through.
	5h	WP or write protect.
	6h	WB or write back.
	7h	Reserved.
23:21	Reserved.	
20	RdDram_4K_F2000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM.	
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.	
19	WrDram_4K_F2000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM.	
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.	
18:16	MemType_4K_F2000: memory type. Read-write. Reset: XXXb.	
	ValidValues:	
	Value	Description
	0h	UC or uncacheable.
	1h	WC or write combining.
	3h-2h	Reserved.
	4h	WT or write through.
	5h	WP or write protect.
	6h	WB or write back.
	7h	Reserved.
15:13	Reserved.	
12	RdDram_4K_F1000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM.	
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.	
11	WrDram_4K_F1000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM.	
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.	
10:8	MemType_4K_F1000: memory type. Read-write. Reset: XXXb.	
	ValidValues:	
	Value	Description
	0h	UC or uncacheable.
	1h	WC or write combining.
	3h-2h	Reserved.
	4h	WT or write through.
	5h	WP or write protect.
	6h	WB or write back.
	7h	Reserved.
7:5	Reserved.	

4	RdDram_4K_F0000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. Address range from F0000h to F0FFF. Core::X86::Msr::SYS_CFG[MtrrFixDramEn,MtrrFixDramModEn] masks Reads of the stored value.																
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
3	WrDram_4K_F0000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. Address range from F0000h to F0FFF. Core::X86::Msr::SYS_CFG[MtrrFixDramEn,MtrrFixDramModEn] masks Reads of the stored value.																
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
2:0	MemType_4K_F0000: memory type. Read-write. Reset: XXXb. Address range from F0000h to F0FFFh.																
	ValidValues:																
	<table><tr><th>Value</th><th>Description</th></tr><tr><td>0h</td><td>UC or uncacheable.</td></tr><tr><td>1h</td><td>WC or write combining.</td></tr><tr><td>3h-2h</td><td>Reserved.</td></tr><tr><td>4h</td><td>WT or write through.</td></tr><tr><td>5h</td><td>WP or write protect.</td></tr><tr><td>6h</td><td>WB or write back.</td></tr><tr><td>7h</td><td>Reserved.</td></tr></table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
	Value	Description															
	0h	UC or uncacheable.															
	1h	WC or write combining.															
	3h-2h	Reserved.															
	4h	WT or write through.															
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																

MSR0000_026F [Fixed-Size MTRRs] (Core::X86::Msrr::MtrrFix_4K_7)

See Core::X86::Msrr::MtrrVarBase for general MTRR information. Fixed MTRRs are enabled through Core::X86::Msrr::MTRRdefType[MtrrDefTypeFixEn,MtrrDefTypeEn]. For addresses below 1MB, the appropriate Fixed MTRRs override the default access destination. Each fixed MTRR includes two bits, RdDram and WrDram, that determine the destination based on the access type. Writing Reserved MemType values causes an error-on-write. If Core::X86::Msrr::SYS_CFG[SecureNestedPagingEn] is set to 1, this register will be read-only and attempts to write to this register will result in #GP(0).

_ccd[1:0]_lthree0_core[7:0]_nSIZE4K7; MSR0000_026F

Bits	Description																
63:61	Reserved.																
60	RdDram_4K_FF000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
59	WrDram_4K_FF000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
58:56	MemType_4K_FF000: memory type. Read-write. Reset: XXXb. ValidValues: <table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>UC or uncacheable.</td></tr> <tr> <td>1h</td><td>WC or write combining.</td></tr> <tr> <td>3h-2h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>WT or write through.</td></tr> <tr> <td>5h</td><td>WP or write protect.</td></tr> <tr> <td>6h</td><td>WB or write back.</td></tr> <tr> <td>7h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
Value	Description																
0h	UC or uncacheable.																
1h	WC or write combining.																
3h-2h	Reserved.																
4h	WT or write through.																
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																
55:53	Reserved.																
52	RdDram_4K_FE000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
51	WrDram_4K_FE000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msrr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
50:48	MemType_4K_FE000: memory type. Read-write. Reset: XXXb. ValidValues: <table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>UC or uncacheable.</td></tr> <tr> <td>1h</td><td>WC or write combining.</td></tr> <tr> <td>3h-2h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>WT or write through.</td></tr> <tr> <td>5h</td><td>WP or write protect.</td></tr> <tr> <td>6h</td><td>WB or write back.</td></tr> <tr> <td>7h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
Value	Description																
0h	UC or uncacheable.																
1h	WC or write combining.																
3h-2h	Reserved.																
4h	WT or write through.																
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																
47:45	Reserved.																
44	RdDram_4K_FD000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM.																

	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
43	WrDram_4K_FD000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
42:40	MemType_4K_FD000: memory type. Read-write. Reset: XXXb. ValidValues:																
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>UC or uncacheable.</td></tr> <tr> <td>1h</td><td>WC or write combining.</td></tr> <tr> <td>3h-2h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>WT or write through.</td></tr> <tr> <td>5h</td><td>WP or write protect.</td></tr> <tr> <td>6h</td><td>WB or write back.</td></tr> <tr> <td>7h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
Value	Description																
0h	UC or uncacheable.																
1h	WC or write combining.																
3h-2h	Reserved.																
4h	WT or write through.																
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																
39:37	Reserved.																
36	RdDram_4K_FC000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
35	WrDram_4K_FC000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
34:32	MemType_4K_FC000: memory type. Read-write. Reset: XXXb. ValidValues:																
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>UC or uncacheable.</td></tr> <tr> <td>1h</td><td>WC or write combining.</td></tr> <tr> <td>3h-2h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>WT or write through.</td></tr> <tr> <td>5h</td><td>WP or write protect.</td></tr> <tr> <td>6h</td><td>WB or write back.</td></tr> <tr> <td>7h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
Value	Description																
0h	UC or uncacheable.																
1h	WC or write combining.																
3h-2h	Reserved.																
4h	WT or write through.																
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																
31:29	Reserved.																
28	RdDram_4K_FB000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
27	WrDram_4K_FB000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
26:24	MemType_4K_FB000: memory type. Read-write. Reset: XXXb.																

	ValidValues:	
	Value	Description
	0h	UC or uncacheable.
	1h	WC or write combining.
	3h-2h	Reserved.
	4h	WT or write through.
	5h	WP or write protect.
	6h	WB or write back.
	7h	Reserved.
23:21	Reserved.	
20	RdDram_4K_FA000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM.	
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.	
19	WrDram_4K_FA000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM.	
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.	
18:16	MemType_4K_FA000: memory type. Read-write. Reset: XXXb.	
	ValidValues:	
	Value	Description
	0h	UC or uncacheable.
	1h	WC or write combining.
	3h-2h	Reserved.
	4h	WT or write through.
	5h	WP or write protect.
	6h	WB or write back.
	7h	Reserved.
15:13	Reserved.	
12	RdDram_4K_F9000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM.	
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.	
11	WrDram_4K_F9000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM.	
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.	
10:8	MemType_4K_F9000: memory type. Read-write. Reset: XXXb.	
	ValidValues:	
	Value	Description
	0h	UC or uncacheable.
	1h	WC or write combining.
	3h-2h	Reserved.
	4h	WT or write through.
	5h	WP or write protect.
	6h	WB or write back.
	7h	Reserved.
7:5	Reserved.	

4	RdDram_4K_F8000: read DRAM. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. Address range from F8000h to F8FFFh. Core::X86::Msr::SYS_CFG[MtrrFixDramEn,MtrrFixDramModEn] masks Reads of the stored value.																
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
3	WrDram_4K_F8000: write DRAM. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. Address range from F8000h to F8FFFh. Core::X86::Msr::SYS_CFG[MtrrFixDramEn,MtrrFixDramModEn] masks Reads of the stored value.																
	AccessType: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? Read-write : Read,Error-on-write-1. Reset: Core::X86::Msr::SYS_CFG[MtrrFixDramModEn] ? X : Fixed,0.																
2:0	MemType_4K_F8000: memory type. Read-write. Reset: XXXb. Address range from F8000h to F8FFFh.																
	ValidValues:																
	<table><tr><th>Value</th><th>Description</th></tr><tr><td>0h</td><td>UC or uncacheable.</td></tr><tr><td>1h</td><td>WC or write combining.</td></tr><tr><td>3h-2h</td><td>Reserved.</td></tr><tr><td>4h</td><td>WT or write through.</td></tr><tr><td>5h</td><td>WP or write protect.</td></tr><tr><td>6h</td><td>WB or write back.</td></tr><tr><td>7h</td><td>Reserved.</td></tr></table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
	Value	Description															
	0h	UC or uncacheable.															
	1h	WC or write combining.															
	3h-2h	Reserved.															
	4h	WT or write through.															
	5h	WP or write protect.															
6h	WB or write back.																
7h	Reserved.																

MSR0000_0277 [Page Attribute Table] (Core::X86::Msr::PAT)

This register specifies the memory type based on the PAT, PCD, and PWT bits in the virtual address page tables.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSR0000_0277

Bits	Description
63:59	Reserved.
58:56	PA7MemType. Read-write. Reset: 0h. Default UC. MemType for {PAT, PCD, PWT} = 7h.
ValidValues:	
Value	Description
0h	UC or uncacheable.
1h	WC or write combining.
3h-2h	Reserved.
4h	WT or write through.
5h	WP or write protect.
6h	WB or write back.
7h	Reserved.
55:51	Reserved.
50:48	PA6MemType. Read-write. Reset: 7h. Default UC. MemType for {PAT, PCD, PWT} = 6h.
ValidValues:	
Value	Description
0h	UC or uncacheable.
1h	WC or write combining.
3h-2h	Reserved.
4h	WT or write through.
5h	WP or write protect.
6h	WB or write back.
7h	Reserved.
47:43	Reserved.
42:40	PA5MemType. Read-write. Reset: 4h. Default WT. MemType for {PAT, PCD, PWT} = 5h.
ValidValues:	
Value	Description
0h	UC or uncacheable.
1h	WC or write combining.
3h-2h	Reserved.
4h	WT or write through.
5h	WP or write protect.
6h	WB or write back.
7h	Reserved.
39:35	Reserved.
34:32	PA4MemType. Read-write. Reset: 6h. Default WB. MemType for {PAT, PCD, PWT} = 4h.
ValidValues:	
Value	Description
0h	UC or uncacheable.
1h	WC or write combining.
3h-2h	Reserved.
4h	WT or write through.
5h	WP or write protect.
6h	WB or write back.
7h	Reserved.

31:27	Reserved.																
26:24	PA3MemType. Read-write. Reset: 0h. Default UC. MemType for {PAT, PCD, PWT} = 3h.																
	ValidValues:																
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>UC or uncacheable.</td></tr> <tr> <td>1h</td><td>WC or write combining.</td></tr> <tr> <td>3h-2h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>WT or write through.</td></tr> <tr> <td>5h</td><td>WP or write protect.</td></tr> <tr> <td>6h</td><td>WB or write back.</td></tr> <tr> <td>7h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
Value	Description																
0h	UC or uncacheable.																
1h	WC or write combining.																
3h-2h	Reserved.																
4h	WT or write through.																
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																
23:19	Reserved.																
18:16	PA2MemType. Read-write. Reset: 7h. Default UC. MemType for {PAT, PCD, PWT} = 2h.																
	ValidValues:																
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>UC or uncacheable.</td></tr> <tr> <td>1h</td><td>WC or write combining.</td></tr> <tr> <td>3h-2h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>WT or write through.</td></tr> <tr> <td>5h</td><td>WP or write protect.</td></tr> <tr> <td>6h</td><td>WB or write back.</td></tr> <tr> <td>7h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
Value	Description																
0h	UC or uncacheable.																
1h	WC or write combining.																
3h-2h	Reserved.																
4h	WT or write through.																
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																
15:11	Reserved.																
10:8	PA1MemType. Read-write. Reset: 4h. Default WT. MemType for {PAT, PCD, PWT} = 1h.																
	ValidValues:																
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>UC or uncacheable.</td></tr> <tr> <td>1h</td><td>WC or write combining.</td></tr> <tr> <td>3h-2h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>WT or write through.</td></tr> <tr> <td>5h</td><td>WP or write protect.</td></tr> <tr> <td>6h</td><td>WB or write back.</td></tr> <tr> <td>7h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
Value	Description																
0h	UC or uncacheable.																
1h	WC or write combining.																
3h-2h	Reserved.																
4h	WT or write through.																
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																
7:3	Reserved.																
2:0	PA0MemType. Read-write. Reset: 6h. MemType for {PAT, PCD, PWT} = 0h.																
	ValidValues:																
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>UC or uncacheable.</td></tr> <tr> <td>1h</td><td>WC or write combining.</td></tr> <tr> <td>3h-2h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>WT or write through.</td></tr> <tr> <td>5h</td><td>WP or write protect.</td></tr> <tr> <td>6h</td><td>WB or write back.</td></tr> <tr> <td>7h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
Value	Description																
0h	UC or uncacheable.																
1h	WC or write combining.																
3h-2h	Reserved.																
4h	WT or write through.																
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																

MSR0000_02FF [MTRR Default Memory Type] (Core::X86::Msrr::MTRRdefType)

See Core::X86::Msrr::MtrrVarBase for general MTRR information.

_ccd[1:0]_lthree0_core[7:0]; MSR0000_02FF

Bits	Description
63:12	Reserved.
11	MtrrDefTypeEn: variable and fixed MTRR enable. Read-write. Reset: 0. 0=Fixed and variable MTRRs are not enabled. 1=Core::X86::Msrr::MtrrVarBase, and Core::X86::Msrr::MtrrFix_64K through Core::X86::Msrr::MtrrFix_4K_7 are enabled.
10	MtrrDefTypeFixEn: fixed MTRR enable. Read-write. Reset: 0. 0=Core::X86::Msrr::MtrrFix_64K through Core::X86::Msrr::MtrrFix_4K_7 are not enabled. 1=Core::X86::Msrr::MtrrFix_64K through Core::X86::Msrr::MtrrFix_4K_7 are enabled. This field is ignored (and the fixed MTRRs are not enabled) if Core::X86::Msrr::MTRRdefType[MtrrDefTypeEn] == 0.
9:8	Reserved.
7:0	MemType: memory type. Read-write. Reset: 00h. Description: If MtrrDefTypeEn == 1 then MemType specifies the memory type for memory space that is not specified by either the fixed or variable range MTRRs. If MtrrDefTypeEn == 0 then the default memory type for all of memory is UC. Valid encodings are {00000b, Core::X86::Msrr::MtrrFix_64K through Core::X86::Msrr::MtrrFix_4K_7[2:0]}. Other Write values cause a GP(0).

MSR0000_06A0 [User CET] (Core::X86::Msrr::U_CET)

Read-write. Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSR0000_06A0

Bits	Description
63:2	Reserved.
1	WRSHSTKEN. Read-write. Reset: 0. Enables the WRSS instruction in User Mode.
0	SHSTKEN. Read-write. Reset: 0. When Set Shadow stack is enabled in User mode.

MSR0000_06A2 [Supervisor CET] (Core::X86::Msrr::S_CET)

Read-write. Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSR0000_06A2

Bits	Description
63:2	Reserved.
1	WRSHSTKEN. Read-write. Reset: 0. Enables the WRSS instruction in Supervisor Mode.
0	SHSTKEN. Read-write. Reset: 0. When Set Shadow stack is enabled in Supervisor mode.

MSR0000_06A4 [PL0 Shadow Stack Pointer] (Core::X86::Msrr::PL0Ssp)

Read-write. Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSR0000_06A4

Bits	Description
63:2	UserLinAddress: PL0 user top of SSP. Read-write. Reset: 0000_0000_0000_0000h. UserLinAddress[63:32] must be zero in 32-bit mode.
1:0	Reserved.

MSR0000_06A5 [PL1 Shadow Stack Pointer] (Core::X86::Msr::PL1Ssp)

Read-write. Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSR0000_06A5

Bits	Description
63:2	UserLinAddress: PL1 user top of SSP. Read-write. Reset: 0000_0000_0000_0000h. UserLinAddress[63:32] must be zero in 32-bit mode.
1:0	Reserved.

MSR0000_06A6 [PL2 Shadow Stack Pointer] (Core::X86::Msr::PL2Ssp)

Read-write. Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSR0000_06A6

Bits	Description
63:2	UserLinAddress: PL2 user top of SSP. Read-write. Reset: 0000_0000_0000_0000h. UserLinAddress[63:32] must be zero in 32-bit mode.
1:0	Reserved.

MSR0000_06A7 [PL3 Shadow Stack Pointer] (Core::X86::Msr::PL3Ssp)

Read-write. Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSR0000_06A7

Bits	Description
63:2	UserLinAddress: PL3 user top of SSP. Read-write. Reset: 0000_0000_0000_0000h. UserLinAddress[63:32] must be zero in 32-bit mode.
1:0	Reserved.

MSR0000_06A8 [Interrupt SSP Table Address] (Core::X86::Msr::IstSspAddr)

Read-write. Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSR0000_06A8

Bits	Description
63:0	IntrLinTableAddress. Read-write. Reset: 0000_0000_0000_0000h. Shadow Stack Pointer interrupt table.

MSR0000_0802 [APIC ID] (Core::X86::Msr::APIC_ID)

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSR0000_0802

Bits	Description
63:32	Reserved.
31:0	ApicId[31:0]: APIC ID[31:0]. Reset: XXXX_XXXXh. Local x2APIC ID register. AccessType: X2APICEN ? Read-only,Error-on-write : Error-on-read,Error-on-write.

MSR0000_0803 [APIC Version] (Core::X86::Msr::ApicVersion)

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSR0000_0803	
Bits	Description
63:32	Reserved.
31	ExtApicSpace: extended APIC register space present. Reset: 1. 1=Indicates the presence of extended APIC register space starting at Core::X86::Msr::ExtendedApicFeature. AccessType: X2APICEN ? Read-only,Error-on-write : Error-on-read,Error-on-write.
30:25	Reserved.
24	DirectedEoiSupport: directed EOI support. Reset: 1. 0=Directed EOI capability not supported. 1=Directed EOI capability supported. AccessType: X2APICEN ? Read-only,Error-on-write : Error-on-read,Error-on-write.
23:16	MaxLvtEntry. Reset: XXh. Specifies the number of entries in the local vector table minus one. AccessType: X2APICEN ? Read-only,Error-on-write : Error-on-read,Error-on-write.
15:8	Reserved.
7:0	Version. Reset: 10h. Indicates the version number of this APIC implementation. AccessType: X2APICEN ? Read-only,Error-on-write : Error-on-read,Error-on-write.

MSR0000_0808 [Task Priority] (Core::X86::Msr::TPR)

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSR0000_0808	
Bits	Description
63:8	Reserved.
7:0	Priority. Reset: 00h. This field is assigned by software to set a threshold priority at which the core is interrupted. AccessType: X2APICEN ? Read-write,Volatile : Error-on-read,Error-on-write.

MSR0000_0809 [Arbitration Priority] (Core::X86::Msr::ArbitrationPriority)

Reset: 0000_0000_0000_0000h.	
_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSR0000_0809	
Bits	Description
63:8	Reserved.
7:0	Priority. Reset: 00h. Indicates the current priority for a pending interrupt, or a task or interrupt being serviced by the core. The priority is used to arbitrate between cores to determine which accepts a lowest-priority interrupt request. AccessType: X2APICEN ? Read-only,Error-on-write,Volatile : Error-on-read,Error-on-write.

MSR0000_080A [Processor Priority] (Core::X86::Msr::ProcessorPriority)

Reset: 0000_0000_0000_0000h.	
_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSR0000_080A	
Bits	Description
63:8	Reserved.
7:0	Priority. Reset: 00h. Indicates the core's current priority servicing a task or interrupt, and is used to determine if any pending interrupts should be serviced. It is the higher value of the task priority value and the current highest in-service interrupt. AccessType: X2APICEN ? Read-only,Error-on-write,Volatile : Error-on-read,Error-on-write.

MSR0000_080B [End Of Interrupt] (Core::X86::Msr::EOI)

Reset: 0000_0000_0000_0000h.	
_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSR0000_080B	
Bits	Description
63:0	EOI. Reset: 0000_0000_0000_0000h. A Write zero to this field indicates the end of interrupt processing the currently in service interrupt. AccessType: X2APICEN ? Write-0-only,Error-on-read,Error-on-write-1 : Error-on-read,Error-on-write.

MSR0000_080D [Logical Destination Register] (Core::X86::Msr::LDR)

Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSR0000_080D

Bits	Description																																		
63:32	Reserved.																																		
31:16	ClusterDestination. Reset: 0000h. Specifies cluster's destination identification. AccessType: X2APICEN ? Read-only,Error-on-write : Error-on-read,Error-on-write.																																		
15:0	LogicalDestination. Reset: 0000h. Specifies one of up to sixteen x2APICs within the cluster specified by ClusterDestination. AccessType: X2APICEN ? Read-only,Error-on-write : Error-on-read,Error-on-write. ValidValues:																																		
	<table> <tr> <th>Bit</th><th>Description</th></tr> <tr><td>[0]</td><td>x2APIC 0</td></tr> <tr><td>[1]</td><td>x2APIC 1</td></tr> <tr><td>[2]</td><td>x2APIC 2</td></tr> <tr><td>[3]</td><td>x2APIC 3</td></tr> <tr><td>[4]</td><td>x2APIC 4</td></tr> <tr><td>[5]</td><td>x2APIC 5</td></tr> <tr><td>[6]</td><td>x2APIC 6</td></tr> <tr><td>[7]</td><td>x2APIC 7</td></tr> <tr><td>[8]</td><td>x2APIC 8</td></tr> <tr><td>[9]</td><td>x2APIC 9</td></tr> <tr><td>[10]</td><td>x2APIC 10</td></tr> <tr><td>[11]</td><td>x2APIC 11</td></tr> <tr><td>[12]</td><td>x2APIC 12</td></tr> <tr><td>[13]</td><td>x2APIC 13</td></tr> <tr><td>[14]</td><td>x2APIC 14</td></tr> <tr><td>[15]</td><td>x2APIC 15</td></tr> </table>	Bit	Description	[0]	x2APIC 0	[1]	x2APIC 1	[2]	x2APIC 2	[3]	x2APIC 3	[4]	x2APIC 4	[5]	x2APIC 5	[6]	x2APIC 6	[7]	x2APIC 7	[8]	x2APIC 8	[9]	x2APIC 9	[10]	x2APIC 10	[11]	x2APIC 11	[12]	x2APIC 12	[13]	x2APIC 13	[14]	x2APIC 14	[15]	x2APIC 15
Bit	Description																																		
[0]	x2APIC 0																																		
[1]	x2APIC 1																																		
[2]	x2APIC 2																																		
[3]	x2APIC 3																																		
[4]	x2APIC 4																																		
[5]	x2APIC 5																																		
[6]	x2APIC 6																																		
[7]	x2APIC 7																																		
[8]	x2APIC 8																																		
[9]	x2APIC 9																																		
[10]	x2APIC 10																																		
[11]	x2APIC 11																																		
[12]	x2APIC 12																																		
[13]	x2APIC 13																																		
[14]	x2APIC 14																																		
[15]	x2APIC 15																																		

MSR0000_080F [Spurious Interrupt Vector] (Core::X86::Msr::SVR)

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSR0000_080F

Bits	Description
63:10	Reserved.
9	FocusDisable. Reset: 0. 1=Disable focus core checking during lowest-priority arbitrated interrupts. AccessType: X2APICEN ? Read-write : Error-on-read,Error-on-write.
8	APICSWEn: APIC software enable. Reset: 0. All LVT entry mask bits are set and cannot be cleared. AccessType: X2APICEN ? Read-write : Error-on-read,Error-on-write.
7:0	Vector. Reset: FFh. The vector that is sent to the core in the event of a spurious interrupt. AccessType: X2APICEN ? Read-write : Error-on-read,Error-on-write.

MSR0000_081[0...7] [In Service Register] (Core::X86::Msr::ISR)

Reset: 0000_0000_0000_0000h.

Interrupt In Service status bits [255:0] accessible through 8 ISR registers.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_nISR0_aliasMSR; MSR0000_0810

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_nISR1_aliasMSR; MSR0000_0811

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_nISR2_aliasMSR; MSR0000_0812

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_nISR3_aliasMSR; MSR0000_0813

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_nISR4_aliasMSR; MSR0000_0814

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_nISR5_aliasMSR; MSR0000_0815

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_nISR6_aliasMSR; MSR0000_0816

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_nISR7_aliasMSR; MSR0000_0817

Bits	Description
63:32	Reserved.
31:0	InServiceBits. Reset: 0000_0000h. These bits are set when the corresponding interrupt is being serviced by the core. AccessType: X2APICEN ? Read-only,Error-on-write,Volatile : Error-on-read,Error-on-write.

MSR0000_081[8...F] [Trigger Mode Register] (Core::X86::Msr::TMR)

Reset: 0000_0000_0000_0000h.

Trigger Mode status bits [255:0] accessible through 8 TMR registers.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_nTMR0_aliasMSR; MSR0000_0818

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_nTMR1_aliasMSR; MSR0000_0819

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_nTMR2_aliasMSR; MSR0000_081A

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_nTMR3_aliasMSR; MSR0000_081B

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_nTMR4_aliasMSR; MSR0000_081C

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_nTMR5_aliasMSR; MSR0000_081D

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_nTMR6_aliasMSR; MSR0000_081E

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_nTMR7_aliasMSR; MSR0000_081F

Bits	Description						
63:32	Reserved.						
31:0	TriggerModeBits. Reset: 0000_0000h. The corresponding trigger mode bit is updated when an interrupt is accepted. AccessType: X2APICEN ? Read-only,Error-on-write,Volatile : Error-on-read,Error-on-write. ValidValues:						
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0</td><td>Edge-triggered interrupt</td></tr> <tr> <td>1</td><td>Level-triggered interrupt</td></tr> </table>	Value	Description	0	Edge-triggered interrupt	1	Level-triggered interrupt
Value	Description						
0	Edge-triggered interrupt						
1	Level-triggered interrupt						

MSR0000_082[0...7] [Interrupt Request Register] (Core::X86::Msr::IRR)

Reset: 0000_0000_0000_0000h.

Interrupt Request status bits [255:0] accessible through 8 IRR registers.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_nIRR0_aliasMSR; MSR0000_0820

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_nIRR1_aliasMSR; MSR0000_0821

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_nIRR2_aliasMSR; MSR0000_0822

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_nIRR3_aliasMSR; MSR0000_0823

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_nIRR4_aliasMSR; MSR0000_0824

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_nIRR5_aliasMSR; MSR0000_0825

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_nIRR6_aliasMSR; MSR0000_0826

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_nIRR7_aliasMSR; MSR0000_0827

Bits	Description
63:32	Reserved.
31:0	RequestBits. Reset: 0000_0000h. The corresponding request bit is set when the an interrupt is accepted by the x2APIC. AccessType: X2APICEN ? Read-only,Error-on-write,Volatile : Error-on-read,Error-on-write.

MSR0000_0828 [Error Status Register] (Core::X86::Msr::ESR)

Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSR0000_0828

Bits	Description
63:8	Reserved.
7	IllegalRegAddr: illegal register address. Reset: 0. This bit indicates that an access to a nonexistent register location within this APIC was attempted. Can only be set in xAPIC mode. AccessType: X2APICEN ? Read,Write-0-only,Error-on-write-1,Volatile : Error-on-read,Error-on-write.
6	RcvdIllegalVector: received illegal vector. Reset: 0. This bit indicates that this APIC has received a message with an illegal vector (00h to 0Fh for fixed and lowest priority interrupts). AccessType: X2APICEN ? Read,Write-0-only,Error-on-write-1,Volatile : Error-on-read,Error-on-write.
5	SentIllegalVector. Reset: 0. This bit indicates that this x2APIC attempted to send a message with an illegal vector (00h to 0Fh for fixed and lowest priority interrupts). AccessType: X2APICEN ? Read,Write-0-only,Error-on-write-1,Volatile : Error-on-read,Error-on-write.
4	Reserved.
3	RcvAcceptError: receive accept error. Reset: 0. This bit indicates that a message received by this APIC was not accepted by this or any other x2APIC. AccessType: X2APICEN ? Read,Write-0-only,Error-on-write-1,Volatile : Error-on-read,Error-on-write.
2	SendAcceptError. Reset: 0. This bit indicates that a message sent by this APIC was not accepted by any x2APIC. AccessType: X2APICEN ? Read,Write-0-only,Error-on-write-1,Volatile : Error-on-read,Error-on-write.
1:0	Reserved.

MSR0000_0830 [Interrupt Command] (Core::X86::Msr::InterruptCommand)

Reset: 0000_0000_0000_0000h.																			
_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSR0000_0830																			
Bits	Description																		
63:32	DestinationField. Reset: 0000_0000h. The destination encoding used when Core::X86::Msr::InterruptCommand[DestShrthnd] is 00b. AccessType: X2APICEN ? Read-write : Error-on-read,Error-on-write.																		
31:20	Reserved.																		
19:18	DestShrthnd: destination shorthand. Reset: 0h. Provides a quick way to specify a destination for a message. If all including self or all excluding self is used, then destination mode is ignored and physical is automatically used. AccessType: X2APICEN ? Read-write : Error-on-read,Error-on-write. ValidValues: <table border="1"> <thead> <tr> <th>Value</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>No shorthand (Destination field).</td></tr> <tr> <td>1h</td><td>Self.</td></tr> <tr> <td>2h</td><td>All including self.</td></tr> <tr> <td>3h</td><td>All excluding self. (This sends a message with a destination encoding of all 1s, so if lowest priority is used the message could end up being reflected back to this APIC.)</td></tr> </tbody> </table>	Value	Description	0h	No shorthand (Destination field).	1h	Self.	2h	All including self.	3h	All excluding self. (This sends a message with a destination encoding of all 1s, so if lowest priority is used the message could end up being reflected back to this APIC.)								
Value	Description																		
0h	No shorthand (Destination field).																		
1h	Self.																		
2h	All including self.																		
3h	All excluding self. (This sends a message with a destination encoding of all 1s, so if lowest priority is used the message could end up being reflected back to this APIC.)																		
17:16	Reserved.																		
15	TM: trigger mode. Reset: 0. 0=Edge triggered. 1=Level triggered. Indicates how this interrupt is triggered. AccessType: X2APICEN ? Read-write : Error-on-read,Error-on-write.																		
14	Level. Reset: 0. 0=Deasserted. 1=Asserted. AccessType: X2APICEN ? Read-write : Error-on-read,Error-on-write.																		
13:12	Reserved.																		
11	DM: destination mode. Reset: 0. 0=Physical. 1=Logical. AccessType: X2APICEN ? Read-write : Error-on-read,Error-on-write.																		
10:8	MsgType. Reset: 0h. The message types are encoded as follows: AccessType: X2APICEN ? Read-write : Error-on-read,Error-on-write. ValidValues: <table border="1"> <thead> <tr> <th>Value</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>Fixed</td></tr> <tr> <td>1h</td><td>Lowest Priority.</td></tr> <tr> <td>2h</td><td>SMI</td></tr> <tr> <td>3h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>NMI</td></tr> <tr> <td>5h</td><td>INIT</td></tr> <tr> <td>6h</td><td>Startup</td></tr> <tr> <td>7h</td><td>External interrupt.</td></tr> </tbody> </table>	Value	Description	0h	Fixed	1h	Lowest Priority.	2h	SMI	3h	Reserved.	4h	NMI	5h	INIT	6h	Startup	7h	External interrupt.
Value	Description																		
0h	Fixed																		
1h	Lowest Priority.																		
2h	SMI																		
3h	Reserved.																		
4h	NMI																		
5h	INIT																		
6h	Startup																		
7h	External interrupt.																		
7:0	Vector. Reset: 00h. The vector that is sent for this interrupt source. AccessType: X2APICEN ? Read-write : Error-on-read,Error-on-write.																		

MSR0000_0832 [LVT Timer] (Core::X86::Msr::TimerLvtEntry)

Reset: 0000_0000_0001_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSR0000_0832

Bits	Description
63:18	Reserved.
17	Mode. Reset: 0. 0=One-shot. 1=Periodic. AccessType: X2APICEN ? Read-write : Error-on-read,Error-on-write.
16	Mask. Reset: 1. 0=Not masked. 1=Masked. AccessType: X2APICEN ? Read-write : Error-on-read,Error-on-write.
15:13	Reserved.
12	DS: interrupt delivery status. Reset: 0. 0=Idle. 1=Send pending. (Indicates that the interrupt has not yet been accepted by the core.) AccessType: X2APICEN ? Read-only,Volatile : Error-on-read,Error-on-write.
11:8	Reserved.
7:0	Vector. Reset: 00h. Interrupt vector number. AccessType: X2APICEN ? Read-write : Error-on-read,Error-on-write.

MSR0000_0833 [LVT Thermal Sensor] (Core::X86::Msr::ThermalLvtEntry)

Reset: 0000_0000_0001_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSR0000_0833

Bits	Description
63:17	Reserved.
16	Mask. Reset: 1. 0=Not masked. 1=Masked. AccessType: X2APICEN ? Read-write : Error-on-read,Error-on-write.
15:13	Reserved.
12	DS: interrupt delivery status. Reset: 0. 0=Idle. 1=Send pending. (Indicates that the interrupt has not yet been accepted by the core.) AccessType: X2APICEN ? Read-only,Volatile : Error-on-read,Error-on-write.
11	Reserved.
10:8	MsgType: message type. Reset: 0h. See 2.1.10.2.1.14 [Generalized Local Vector Table]. AccessType: X2APICEN ? Read-write : Error-on-read,Error-on-write.
7:0	Vector. Reset: 00h. Interrupt vector number. AccessType: X2APICEN ? Read-write : Error-on-read,Error-on-write.

MSR0000_0834 [LVT Performance Monitor] (Core::X86::Msr::PerformanceCounterLvtEntry)

Reset: 0000_0000_0001_0000h.

Interrupts for this local vector table are caused by overflows of:

- Core::X86::Msr::PERF_LEGACY_CTL0..3(Performance Event Select [3:0]).
- Core::X86::Msr::PERF_CTL0..5(Performance Event Select [5:0]).

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSR0000_0834

Bits	Description
63:17	Reserved.
16	Mask. Reset: 1. 0=Not masked. 1=Masked. AccessType: X2APICEN ? Read-write : Error-on-read,Error-on-write.
15:13	Reserved.
12	DS: interrupt delivery status. Reset: 0. 0=Idle. 1=Send pending. Indicates that the interrupt has not yet been accepted by the core. AccessType: X2APICEN ? Read-only, Volatile : Error-on-read,Error-on-write.
11	Reserved.
10:8	MsgType: message type. Reset: 0h. See 2.1.10.2.1.14 [Generalized Local Vector Table]. AccessType: X2APICEN ? Read-write : Error-on-read,Error-on-write.
7:0	Vector. Reset: 00h. Interrupt vector number. AccessType: X2APICEN ? Read-write : Error-on-read,Error-on-write.

MSR0000_083[5...6] [LVT LINT[1:0]] (Core::X86::Msr::LVTLINT)

Reset: 0000_0000_0001_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_nLVTLINT0_aliasMSR; MSR0000_0835

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_nLVTLINT1_aliasMSR; MSR0000_0836

Bits	Description
63:17	Reserved.
16	Mask. Reset: 1. 0=Not masked. 1=Masked. AccessType: X2APICEN ? Read-write : Error-on-read,Error-on-write.
15	TM: trigger mode. Reset: 0. 0=Edge. 1=Level. AccessType: X2APICEN ? Read-write : Error-on-read,Error-on-write.
14	RmtIRR. Reset: 0. If trigger mode is level, remote Core::X86::Msr::IRR is set when the interrupt has begun service. Remote Core::X86::Msr::IRR is cleared when the end of interrupt has occurred. AccessType: X2APICEN ? Read-only, Volatile : Error-on-read,Error-on-write.
13	Reserved.
12	DS: interrupt delivery status. Reset: 0. 0=Idle. 1=Send pending. (Indicates that the interrupt has not yet been accepted by the core.) AccessType: X2APICEN ? Read-only, Volatile : Error-on-read,Error-on-write.
11	Reserved.
10:8	MsgType: message type. Reset: 0h. See 2.1.10.2.1.14 [Generalized Local Vector Table]. AccessType: X2APICEN ? Read-write : Error-on-read,Error-on-write.
7:0	Vector. Reset: 00h. Interrupt vector number. AccessType: X2APICEN ? Read-write : Error-on-read,Error-on-write.

MSR0000_0837 [LVT Error] (Core::X86::Msr::ErrorLvtEntry)

Reset: 0000_0000_0001_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSR0000_0837

Bits	Description
63:17	Reserved.
16	Mask. Reset: 1. 0=Not masked. 1=Masked. AccessType: X2APICEN ? Read-write : Error-on-read,Error-on-write.
15:13	Reserved.
12	DS: interrupt delivery status. Reset: 0. 0=Idle. 1=Send pending. (Indicates that the interrupt has not yet been accepted by the core.) AccessType: X2APICEN ? Read-only,Volatile : Error-on-read,Error-on-write.
11	Reserved.
10:8	MsgType: message type. Reset: 0h. See 2.1.10.2.1.14 [Generalized Local Vector Table]. AccessType: X2APICEN ? Read-write : Error-on-read,Error-on-write.
7:0	Vector. Reset: 00h. Interrupt vector number. AccessType: X2APICEN ? Read-write : Error-on-read,Error-on-write.

MSR0000_0838 [Timer Initial Count] (Core::X86::Msr::TimerInitialCount)

Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSR0000_0838

Bits	Description
63:32	Reserved.
31:0	Count. Reset: 0000_0000h. The value copied into the current count register when the timer is loaded or reloaded. AccessType: X2APICEN ? Read-write : Error-on-read,Error-on-write.

MSR0000_0839 [Timer Current Count] (Core::X86::Msr::TimerCurrentCount)

Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSR0000_0839

Bits	Description
63:32	Reserved.
31:0	Count. Reset: 0000_0000h. The current value of the counter. AccessType: X2APICEN ? Read,Error-on-write,Volatile : Error-on-read,Error-on-write.

MSR0000_083E [Timer Divide Configuration] (Core::X86::Msr::TimerDivideConfiguration)

Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSR0000_083E

Bits	Description
63:4	Reserved.
3:0	Div[3:0] . Reset: 0h. Div[2] is unused. AccessType: X2APICEN ? Read-write : Error-on-read,Error-on-write.
ValidValues:	
Value	Description
0h	Divide by 2.
1h	Divide by 4.
2h	Divide by 8.
3h	Divide by 16.
7h-4h	Reserved.
8h	Divide by 32.
9h	Divide by 64.
Ah	Divide by 128.
Bh	Divide by 1.
Fh-Ch	Reserved.

MSR0000_083F [Self IPI] (Core::X86::Msr::SelfIPI)

Reset: 0000_0000_0000_0000h.

The self IPI register provides a performance optimized path for sending self IPI's. A self IPI is semantically identical to an inter-processor interrupt sent via the ICR, with a Destination Shorthand of Self, Trigger Mode equal to Edge, and a Delivery Mode equal to Fixed.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSR0000_083F

Bits	Description
63:8	Reserved.
7:0	Vector . Reset: 00h. Interrupt vector number. AccessType: X2APICEN ? Write-only,Error-on-read : Error-on-read,Error-on-write.

MSR0000_0840 [Extended APIC Feature] (Core::X86::Msr::ExtendedApicFeature)

Reset: 0000_0000_0004_0007h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSR0000_0840

Bits	Description
63:24	Reserved.
23:16	ExtLvtCount: extended local vector table count . Reset: 04h. This specifies the number of extended LVT registers (Core::X86::Msr::ExtendedInterruptLvtEntries) in the local APIC. AccessType: X2APICEN ? Read-only,Error-on-write : Error-on-read,Error-on-write.
15:3	Reserved.
2	ExtApicIdCap: extended APIC ID capable . Reset: 1. 1=The processor is capable of supporting an 8-bit APIC ID, as controlled by Core::X86::Msr::ExtendedApicControl[ExtApicIdEn]. AccessType: X2APICEN ? Read-only,Error-on-write : Error-on-read,Error-on-write.
1	SeoiCap: specific end of interrupt capable . Reset: 1. 1=The Core::X86::Msr::SpecificEndOfInterrupt is present. AccessType: X2APICEN ? Read-only,Error-on-write : Error-on-read,Error-on-write.
0	IerCap: interrupt enable register capable . Reset: 1. This bit indicates that the Core::X86::Msr::InterruptEnable0 - 7 are present. See 2.1.10.2.1.8 [Interrupt Masking]. AccessType: X2APICEN ? Read-only,Error-on-write : Error-on-read,Error-on-write.

MSR0000_0841 [Extended APIC Control] (Core::X86::Msr::ExtendedApicControl)

Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSR0000_0841

Bits	Description
63:3	Reserved.
2	ExtApicIdEn: extended APIC ID enable. Reset: 0. 1=Enable 8-bit APIC ID; Core::X86::Msr::APIC_ID[ApicId[31:0]] supports an 8-bit value; an interrupt broadcast in physical destination mode requires that the (IntDest[7:0] = 1111_1111b) (instead of XXXX_1111b); a match in physical destination mode occurs when (IntDest[7:0] == ApicId[7:0]) instead of (IntDest[3:0] == ApicId[3:0]).
	AccessType: X2APICEN ? Read-write : Error-on-read,Error-on-write.
1	SeoiEn. Reset: 0. 1=Enable SEOI generation when a write to Core::X86::Msr::SpecificEndOfInterrupt is received.
	AccessType: X2APICEN ? Read-write : Error-on-read,Error-on-write.
0	IerEn. Reset: 0. 1=Enable writes to the interrupt enable registers.
	AccessType: X2APICEN ? Read-write : Error-on-read,Error-on-write.

MSR0000_0842 [Specific End Of Interrupt] (Core::X86::Msr::SpecificEndOfInterrupt)

Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSR0000_0842

Bits	Description
63:8	Reserved.
7:0	EoiVec: end of interrupt vector. Reset: 00h. A write to this field causes an end of interrupt cycle to be performed for the vector specified in this field. The behavior is undefined if no interrupt is pending for the specified interrupt vector.
	AccessType: X2APICEN ? Read-write : Error-on-read,Error-on-write.

MSR0000_0848 [Interrupt Enable 0] (Core::X86::Msr::InterruptEnable0)

Reset: 0000_0000_FFFF_FFFFh.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n0_aliasMSR; MSR0000_0848

Bits	Description
63:32	Reserved.
31:16	InterruptEnableBits. Reset: FFFFh. The interrupt enable bits can be used to enable each of the 256 interrupts.
	AccessType: X2APICEN ? Read-write : Error-on-read,Error-on-write.
15:0	Reserved.

MSR0000_084[9...F] [Interrupt Enable 7..1] (Core::X86::Msr::InterruptEnable71)

Reset: 0000_0000_FFFF_FFFFh.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n1_aliasMSR; MSR0000_0849

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n2_aliasMSR; MSR0000_084A

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n3_aliasMSR; MSR0000_084B

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n4_aliasMSR; MSR0000_084C

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n5_aliasMSR; MSR0000_084D

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n6_aliasMSR; MSR0000_084E

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n7_aliasMSR; MSR0000_084F

Bits	Description
63:32	Reserved.
31:0	InterruptEnableBits. Reset: FFFF_FFFFh. The interrupt enable bits can be used to enable each of the 256 interrupts.
	AccessType: X2APICEN ? Read-write : Error-on-read,Error-on-write.

MSR0000_085[0...3] [Extended Interrupt Local Vector Table] (Core::X86::Msr::ExtendedInterruptLvtEntries)

Reset: 0000_0000_0001_0000h.	
_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n0_aliasMSR; MSR0000_0850	
_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n1_aliasMSR; MSR0000_0851	
_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n2_aliasMSR; MSR0000_0852	
_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n3_aliasMSR; MSR0000_0853	
Bits	Description
63:17	Reserved.
16	Mask. Reset: 1. 0=Not masked. 1=Masked. Interrupt Mask. AccessType: X2APICEN ? Read-write : Error-on-read,Error-on-write.
15:13	Reserved.
12	DS: interrupt delivery status. Reset: 0. 0=Idle. 1=Send pending. Indicates that the interrupt has not yet been accepted by the core. AccessType: X2APICEN ? Read-write, Volatile : Error-on-read,Error-on-write.
11	Reserved.
10:8	MsgType: message type. Reset: 0h. See 2.1.10.2.1.14 [Generalized Local Vector Table]. AccessType: X2APICEN ? Read-write : Error-on-read,Error-on-write.
7:0	Vector. Reset: 00h. Interrupt vector number. AccessType: X2APICEN ? Read-write : Error-on-read,Error-on-write.

MSR0000_0C8D [Monitoring Event Select] (Core::X86::Msr::QM_EVTSEL)

_ccd[1:0]_lthree0; MSR0000_0C8D	
Bits	Description
63:40	Reserved.
39:32	RMID. Read-write. Reset: 00h. Resource Monitoring Identifier.
31:8	Reserved.
7:0	EventId. Read-write. Reset: 00h. Monitored Event ID.

MSR0000_0C8E [QOS L3 Counter] (Core::X86::Msr::QM_CTR)

Read,Error-on-write. Reset: 8000_0000_0000_0000h.	
_ccd[1:0]_lthree0; MSR0000_0C8E	
Bits	Description
63	Error. Read,Error-on-write. Reset: 1. Unsupported RMID or event type was written to Core::X86::Msr::QM_EVTSEL.
62	Unavailable. Read,Error-on-write. Reset: 0. Data for this RMID is not available or not monitored for this resource or RMID.
61:0	RmData. Read,Error-on-write. Reset: 0000_0000_0000_0000h. Resource Monitored Data.

MSR0000_0C8F (Core::X86::Msr::PQR_ASSOC)

Reset: 0000_0000_0000_0000h.	
QOS L2 RMID. The behavior of this register is defined in the AMD64 Technology Platform Quality of Service Extensions specification.	
_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSR0000_0C8F	
Bits	Description
63:36	Reserved.
35:32	Clos. Read-write. Reset: 0h. Class of Service.
31:8	Reserved.
7:0	Rmid. Read-write. Reset: 00h. Resource Monitor Identifier.

MSR0000_0DA0 [Extended Supervisor State] (Core::X86::Msr::XSS)

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSR0000_0DA0	
Bits	Description
63:13	Reserved.
12	CET_S . Read-write. Reset: 0. System Control-flow Enforcement Technology.
11	CET_U . Read-write. Reset: 0. User Control-flow Enforcement Technology.
10:0	Reserved.

2.1.12.2 MSRs – MSRC000_xxxx**MSRC000_0080 [Extended Feature Enable] (Core::X86::Msr::EFER)**

SKINIT Execution: 0000_0000_0000_0000h.	
_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC000_0080	
Bits	Description
63:22	Reserved.
21	AutomaticIBRSEn: Automatic IBRS Enable . Read-write. Reset: 0. 0=IBRS protection is not enabled unless (SPEC_CTRL[IBRS] == 1). 1=IBRS protection is enabled for any process running at (CPL < 3) or ((ASID == 0) && SEV-SNP).
20	UAIE: Upper Address Ignore Enable . Read-write. Reset: 0. Upper Address Ignore suppresses canonical faults for most data access virtual addresses, which allows software to use the upper bits of a virtual address as tags.
19	Reserved.
18	IntWbinvdEn . Read-write. Reset: 0. Interruptible wbinvd, wbinvd enable.
17:16	Reserved.
15	TCE: translation cache extension enable . Read-write. Reset: 0. 1=Translation cache extension is enabled. PDC entries related to the linear address of the INVLPG instruction are invalidated. If this bit is 0 all PDC entries are invalidated by the INVLPG instruction.
14	FFXSE: fast FXSAVE/FRSTOR enable . Read-write. Reset: 0. 1=Enables the fast FXSAVE/FRSTOR mechanism. A 64-bit operating system may enable the fast FXSAVE/FRSTOR mechanism if (Core::X86::CpuId::FeatureExtIdEdx[FFXSR] == 1). This bit is set once by the operating system and its value is not changed afterwards.
13	LMSLE: long mode segment limit enable . Read-only, Error-on-write-1. Reset: Fixed, 0. 1=Enables the long mode segment limit check mechanism.
12	SVME: secure virtual machine (SVM) enable . Reset: Fixed, 0. 1=SVM features are enabled. AccessType: Core::X86::Msr::VM_CR[SvmeDisable] ? Read-only, Error-on-write-1 : Read-write.
11	NXE: no-execute page enable . Read-write. Reset: 0. 1=The no-execute page protection feature is enabled.
10	LMA: long mode active . Read-only. Reset: 0. 1=Indicates that long mode is active. When writing the EFER register the value of this bit must be preserved. Software must read the EFER register to determine the value of LMA, change any other bits as required and then write the EFER register. An attempt to write a value that differs from the state determined by hardware results in a #GP fault.
9	Reserved.
8	LME: long mode enable . Read-write. Reset: 0. 1=Long mode is enabled.
7:1	Reserved.
0	SYSCALL: system call extension enable . Read-write. Reset: 0. 1=SYSCALL and SYSRET instructions are enabled. This adds the SYSCALL and SYSRET instructions which can be used in flat addressed operating systems as low latency system calls and returns.

MSRC000_0081 [SYSCALL Target Address] (Core::X86::Msr::STAR)

Read-write. Reset: 0000_0000_0000_0000h.

This register holds the target address used by the SYSCALL instruction and the code and stack segment selector bases used by the SYSCALL and SYSRET instructions.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC000_0081

Bits	Description
63:48	SysRetSel. Read-write. Reset: 0000h. SYSRET CS and SS.
47:32	SysCallSel. Read-write. Reset: 0000h. SYSCALL CS and SS.
31:0	Target. Read-write. Reset: 0000_0000h. SYSCALL target address.

MSRC000_0082 [Long Mode SYSCALL Target Address] (Core::X86::Msr::STAR64)

Read-write. Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC000_0082

Bits	Description
63:0	LSTAR: long mode target address. Read-write. Reset: 0000_0000_0000_0000h. Target address for 64-bit mode calling programs. The address stored in this register must be in canonical form (if not canonical, a #GP fault occurs).

MSRC000_0083 [Compatibility Mode SYSCALL Target Address] (Core::X86::Msr::STARCOMPAT)

Read-write. Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC000_0083

Bits	Description
63:0	CSTAR: compatibility mode target address. Read-write. Reset: 0000_0000_0000_0000h. Target address for compatibility mode. The address stored in this register must be in canonical form (if not canonical, a #GP fault occurs).

MSRC000_0084 [SYSCALL Flag Mask] (Core::X86::Msr::SYSCALL_FLAG_MASK)

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC000_0084

Bits	Description
63:32	Reserved.
31:0	Mask: SYSCALL flag mask. Read-write. Reset: 0000_0000h. This register holds the EFLAGS mask used by the SYSCALL instruction. 1=Clear the corresponding EFLAGS bit when executing the SYSCALL instruction.

MSRC000_00E7 [Read-Only Max Performance Frequency Clock Count] (Core::X86::Msr::MPerfReadOnly)

Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC000_00E7

Bits	Description
63:0	MPerfReadOnly: read-only maximum core clocks counter. Reset: 0000_0000_0000_0000h. Incremented by hardware at the P0 frequency while the core is in C0. In combination with Core::X86::Msr::APerfReadOnly, this is used to determine the effective frequency of the core. A read of this MSR in guest mode is affected by Core::X86::Msr::TscRateMsr. This field uses software P-state numbering. See Core::X86::Msr::HWCR[EffFreqCntMwait], 2.1.3 [Effective Frequency]. This register is not affected by writes to Core::X86::Msr::MPERF. AccessType: Core::X86::Msr::HWCR[EffFreqReadOnlyLock] ? Read,Error-on-write,Volatile : Read-write,Volatile.

MSRC000_00E8 [Read-Only Actual Performance Frequency Clock Count] (Core::X86::Msr::APerfReadOnly)

Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC000_00E8

Bits	Description
63:0	APerfReadOnly: read-only actual core clocks counter. Reset: 0000_0000_0000_0000h. This register increments in proportion to the actual number of core clocks cycles while the core is in C0. See Core::X86::Msr::MPerfReadOnly. This register is not affected by writes to Core::X86::Msr::APERF. AccessType: Core::X86::Msr::HWCR[EffFreqReadOnlyLock] ? Read,Error-on-write,Volatile : Read-write,Volatile.

MSRC000_00E9 [Instructions Retired Performance Count] (Core::X86::Msr::IRPerfCount)

Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC000_00E9

Bits	Description
63:48	Reserved.
47:0	IRPerfCount: instructions retired counter. Reset: 0000_0000_0000_0000h. Dedicated Instructions Retired register increments on once for every instruction retired. See Core::X86::Msr::HWCR[IRPerfEn]. AccessType: Core::X86::Msr::HWCR[EffFreqReadOnlyLock] ? Read,Error-on-write,Volatile : Read-write,Volatile.

MSRC000_0100 [FS Base] (Core::X86::Msr::FS_BASE)

Read-write. Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC000_0100

Bits	Description
63:0	FSBase: expanded FS segment base. Read-write. Reset: 0000_0000_0000_0000h. This register provides access to the expanded 64-bit FS segment base. The address stored in this register must be in canonical form (if not canonical, a #GP fault fill occurs).

MSRC000_0101 [GS Base] (Core::X86::Msr::GS_BASE)

Read-write. Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC000_0101

Bits	Description
63:0	GSBase: expanded GS segment base. Read-write. Reset: 0000_0000_0000_0000h. This register provides access to the expanded 64-bit GS segment base. The address stored in this register must be in canonical form (if not canonical, a #GP fault fill occurs).

MSRC000_0102 [Kernel GS Base] (Core::X86::Msr::KernelGSbase)

Read-write. Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC000_0102

Bits	Description
63:0	KernelGSBase: kernel data structure pointer. Read-write. Reset: 0000_0000_0000_0000h. This register holds the kernel data structure pointer which can be swapped with the GS_BASE register using the SwapGS instruction. The address stored in this register must be in canonical form (if not canonical, a #GP fault occurs).

MSRC000_0103 [Auxiliary Time Stamp Counter] (Core::X86::Msr::TSC_AUX)

Read-write,Volatile. Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC000_0103

Bits	Description
63:32	Reserved.
31:0	TscAux: auxiliary time stamp counter data. Read-write,Volatile. Reset: 0000_0000h. It is expected that this is initialized by privileged software to a meaningful value, such as a processor ID. This value is returned in the RDTSCP instruction.

MSRC000_0104 [Time Stamp Counter Ratio] (Core::X86::Msr::TscRateMsr)

Core::X86::Msr::TscRateMsr allows the hypervisor to control the guest's view of the Time Stamp Counter. It provides a multiplier that scales the value returned when Core::X86::Msr::TSC[TSC], Core::X86::Msr::MPERF[MPERF], and Core::X86::Msr::MPerfReadOnly[MPerfReadOnly] are read by a guest running under virtualization. This allows the hypervisor to provide a consistent TSC, MPERF, and MPerfReadOnly rate for a guest process when moving that process between cores that have a differing P0 rate. The TSC Ratio MSR does not affect the value read from the TSC, MPERF, and MPerfReadOnly MSRs when read when in host mode or when virtualization is not being used or when accessed by code executed in system management mode (SMM) unless the SMM code is executed within a guest container. The TSC Ratio value does not affect the rate of the underlying TSC, MPERF, and MPerfReadOnly counters, or the value that gets written to the TSC, MPERF, and MPerfReadOnly MSRs counters on a Write by either the host or the guest. The TSC Ratio MSR contains a fixed-point number in 8.32 format, which is 8 bits of integer and 32 bits of fraction. This number is the ratio of the desired P0 frequency to the P0 frequency of the core. The reset value of the TSC Ratio MSR is 1.0, which results when a guest frequency matches the core P0 frequency.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC000_0104

Bits	Description
63:40	Reserved.
39:32	TscRateMsrInt: time stamp counter rate integer. Read-write. Reset: 01h. Specifies the integer part of the MSR TSC ratio value.
31:0	TscRateMsrFrac: time stamp counter rate fraction. Read-write. Reset: 0000_0000h. Specifies the fractional part of the MSR TSC ratio value.

MSRC000_0108 [Prefetch Control] (Core::X86::Msr::PrefetchControl)

Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]; MSRC000_0108

Bits	Description
63:6	Reserved.
5	UpDown. Read-write. Reset: 0. Disable prefetcher that uses memory access history to determine whether to fetch the next or previous line into L2 cache for all memory accesses.
4	Reserved.
3	L2Stream. Read-write. Reset: 0. Disable prefetcher that uses history of memory access patterns to fetch additional sequential lines into L2 cache.
2	L1Region. Read-write. Reset: 0. Disable prefetcher that uses memory access history to fetch additional lines into L1 cache when the data access for a given instruction tends to be followed by a consistent pattern of other accesses within a localized region.
1	L1Stride. Read-write. Reset: 0. Disable stride prefetcher that uses memory access history of individual instructions to fetch additional lines into L1 cache when each access is a constant distance from the previous.
0	L1Stream. Read-write. Reset: 0. Disable stream prefetcher that uses history of memory access patterns to fetch additional sequential lines into L1 cache.

MSRC000_010E [LBR V2 Branch Select] (Core::X86::Msr::LbrSelect)

Read-write. Reset: 0000_0000_0000_0000h.

This MSR allows LBR V2 recording to be suppressed based on branch type and privilege level.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC000_010E

Bits	Description
63:9	Reserved.
8	FarBranch. Read-write. Reset: 0. When set far branches are not recorded.
7	JmpNearRel. Read-write. Reset: 0. When set, near relative jumps, excluding near relative calls, are not recorded.
6	JmpNearInd. Read-write. Reset: 0. When set, near indirect jumps, excluding near indirect calls and near returns, are not recorded.
5	RetNear. Read-write. Reset: 0. When set, near returns are not recorded.
4	CallNearInd. Read-write. Reset: 0. When set, near indirect calls are not recorded.
3	CallNearRel. Read-write. Reset: 0. When set, near relative calls are not recorded.
2	Jcc. Read-write. Reset: 0. When set conditional branches are not recorded.
1	CplGe0. Read-write. Reset: 0. When set, no branches ending in CPL > 0 are recorded.
0	CplEq0. Read-write. Reset: 0. When set, no branches ending in CPL = 0 are recorded.

MSRC000_010F [Debug Extension Configuration] (Core::X86::Msr::DbgExtnCfg)

Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC000_010F

Bits	Description
63:7	Reserved.
6	LBRV2EN. Read-write. Reset: 0. When enabled the last 16 branch targets and from addresses are recorded in LBR_TO_V2_[0..15] and LBR_FROM_V2_[0..15]. Core::X86::Msr::DbgExtnCfg[LBRV2EN] is cleared upon #DB entry.
5:0	Reserved.

MSRC000_0300 [Performance Counter Global Status] (Core::X86::Msr::PerfCntGlobalStatus)

Read-only. Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC000_0300

Bits	Description
63:60	Reserved.
59	PmcFreeze: Performance Counter Freeze. Read-only. Reset: 0. When set, the performance monitor counters have been frozen due an interrupt signaled for the overflow of at least one counter. This feature is enabled via Core::X86::Msr::DBG_CTL_MSR[FPMCI].
58	LbrFreeze: LBR Stack Freeze. Read-only. Reset: 0. When set, LBR stack has been frozen due to an interrupt signaled for the overflow of at least one counter. This feature is enabled via Core::X86::Msr::DBG_CTL_MSR[FLBRI]. LBR Freeze does not affect the legacy LBR registers.
57:6	Reserved.
5:0	PerfCntOvfl: Performance Counter Overflow Bits. Read-only. Reset: 00h. For each available core Performance Counter there is one overflow bit starting at bit position 0 for counter 0 (PerfCnt0). The bit is set when the corresponding counter overflows and remains set until cleared by software via Core::X86::Msr::PerfCntGlobalStatusClr. The bits can also be set directly by software via Core::X86::Msr::PerfCntGlobalStatusSet. Note that the overflow bit is set even when the Performance Counter was not configured to signal an interrupt.

MSRC000_0301 [Performance Counter Global Control] (Core::X86::Msr::PerfCntGlobalCtl)

Read-write. Reset: 0000_0000_0000_003Fh.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC000_0301

Bits	Description
63:6	Reserved.
5:0	PerfCntEn: Global Performance Counter Enable. Read-write. Reset: 3Fh. For each available performance counter there is one enable bit in this field. Bit position 0 corresponds to counter 0 (PerfCnt0), bit position 1 corresponds to counter 1 (PerfCnt1) and so forth. A Performance counter is enabled to count when both its Core::X86::Msr::PerfCntGlobalCtl[PerfCntEn] bit and its Core::X86::Msr::PERF_CTL0..5[En] bit are set.

MSRC000_0302 [Performance Counter Global Status Clear] (Core::X86::Msr::PerfCntGlobalStatusClr)

Write-only. Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC000_0302

Bits	Description
63:60	Reserved.
59	PmcFreezeClr: PMC Freeze Clear. Write-only. Reset: 0. When written as 1, Core::X86::Msr::PerfCntGlobalStatus[PmcFreeze] is cleared and the Performance Monitor Counter Freeze is cleared and counters that are enabled to count continue to count. Software should use this feature to restart counters after it serviced overflow conditions in a Performance Monitor interrupt handler.
58	LbrFreezeClr: LBR Freeze Clear. Write-only. Reset: 0. When written as 1, Core::X86::Msr::PerfCntGlobalStatus[LbrFreeze] is cleared, the LBR stack freeze is lifted and continues to record branches as configured. Software should use this feature to restart LBR after it serviced overflow conditions in a Performance Monitor interrupt handler.
57:6	Reserved.
5:0	PerfCntOvflClr: Performance Counter Overflow Bits Clear. Write-only. Reset: 00h. Description: These bits allow software to clear PerfCntOvfl bits in Core::X86::Msr::PerfCntGlobalStatus. To clear a bit software needs to write a 1 to the corresponding bit. Software should clear the Performance Counter Overflow bits when: <ul style="list-style-type: none"> - Handling a performance counter overflow interrupt - Disabling a performance counter - Resetting a performance counter

MSRC000_0303 [Performance Counter Global Status Set] (Core::X86::Msr::PerfCntGlobalStatusSet)

Write-only. Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC000_0303

Bits	Description
63:60	Reserved.
59	PmcFreezeSet: PMC Freeze Set. Write-only. Reset: 0. When written as 1, Core::X86::Msr::PerfCntGlobalStatus[PmcFreeze] is set and the Performance Monitor Counters are frozen. In normal operation it is not expected that software would need to set these bits. It is the hardware that sets this bit when Core::X86::Msr::DBG_CTL_MSR[FPMCI] is set and a PMC overflow signals an interrupt.
58	LbrFreezeSet: LBR Freeze Set. Write-only. Reset: 0. When written as 1, Core::X86::Msr::PerfCntGlobalStatus[LbrFreeze] is set, the LBR stack is frozen and no longer records branches. In normal operation it is not expected that software would need to set these bits. It is the hardware that sets this bit when Core::X86::Msr::DBG_CTL_MSR[FLBRI] is set and a PMC overflow signals an interrupt.
57:6	Reserved.
5:0	PerfCntOvflSet: Performance Counter Overflow Bits Set. Write-only. Reset: 00h. These bits allow software to set PerfCntOvfl bits PerfCntGlobalStatus. Setting an overflow bit in PerfCntGlobalStatus does not result in the generation of an interrupt, freeze of performance counters, freeze of LBR or other actions that may be taken when a performance counter overflows.

MSRC000_0410 [MCA Interrupt Configuration] (Core::X86::Msr::McaIntrCfg)

Read-write. Reset: 0000_0000_0000_0000h.

MSRC000_0410

Bits	Description
63:16	Reserved.
15:12	ThresholdLvtOffset. Read-write. Reset: 0h. For error thresholding interrupts, specifies the address of the LVT entry in the APIC registers as follows: LVT address = (LvtOffset shifted left 4 bits) + 500h (see Core::X86::Apic::ExtendedInterruptLvtEntries).
11:8	Reserved.
7:4	DeferredLvtOffset. Read-write. Reset: 0h. For deferred error interrupts, specifies the address of the LVT entry in the APIC registers as follows: LVT address = (LvtOffset shifted left 4 bits) + 500h (see APIC[530:500]).
3:0	Reserved.

2.1.12.3 MSRs - MSRC001_0xxx

MSRC001_0000 [Performance Event Select 0] (Core::X86::Msr::PERF_LEGACY_CTL0)

Read-write. Reset: 0000_0000_0000_0000h.

The legacy alias of Core::X86::Msr::PERF_CTL0. See Core::X86::Msr::PERF_CTL0.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC001_0000

Bits	Description										
63:42	Reserved.										
41:40	HostGuestOnly: count only host/guest events. Read-write. Reset: 0h.										
	ValidValues:										
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>Count all events, irrespective of guest/host.</td></tr> <tr> <td>1h</td><td>Count guest events if [SVME] == 1.</td></tr> <tr> <td>2h</td><td>Count host events if [SVME] == 1.</td></tr> <tr> <td>3h</td><td>Count all guest and host events if [SVME] == 1.</td></tr> </table>	Value	Description	0h	Count all events, irrespective of guest/host.	1h	Count guest events if [SVME] == 1.	2h	Count host events if [SVME] == 1.	3h	Count all guest and host events if [SVME] == 1.
Value	Description										
0h	Count all events, irrespective of guest/host.										
1h	Count guest events if [SVME] == 1.										
2h	Count host events if [SVME] == 1.										
3h	Count all guest and host events if [SVME] == 1.										
39:36	Reserved.										
35:32	EventSelect[11:8]. Read-write. Reset: 0h. Performance event select[11:8].										
31:24	CntMask: counter mask. Read-write. Reset: 00h. Controls the number of events counted per clock cycle.										
	ValidValues:										
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>00h</td><td>The corresponding PERF_CTR[5:0] register increments by the number of events occurring in a clock cycle. See 2.1.13.3 [Large Increment per Cycle Events] for events that can increment greater than 15 per cycle.</td></tr> <tr> <td>7Fh-01h</td><td>When Inv == 0, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is greater than or equal to the CntMask value. When Inv == 1, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is less than CntMask value.</td></tr> <tr> <td>FFh-80h</td><td>Reserved.</td></tr> </table>	Value	Description	00h	The corresponding PERF_CTR[5:0] register increments by the number of events occurring in a clock cycle. See 2.1.13.3 [Large Increment per Cycle Events] for events that can increment greater than 15 per cycle.	7Fh-01h	When Inv == 0, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is greater than or equal to the CntMask value. When Inv == 1, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is less than CntMask value.	FFh-80h	Reserved.		
Value	Description										
00h	The corresponding PERF_CTR[5:0] register increments by the number of events occurring in a clock cycle. See 2.1.13.3 [Large Increment per Cycle Events] for events that can increment greater than 15 per cycle.										
7Fh-01h	When Inv == 0, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is greater than or equal to the CntMask value. When Inv == 1, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is less than CntMask value.										
FFh-80h	Reserved.										
23	Inv: invert counter mask. Read-write. Reset: 0. See CntMask.										
22	En: enable performance counter. Read-write. Reset: 0. 1=Performance event counter is enabled. Performance counter enable.										
21	Reserved.										
20	Int: enable APIC interrupt. Read-write. Reset: 0. 1=APIC performance counter LVT interrupt is enabled to generate an interrupt via Core::X86::Apic::PerformanceCounterLvtEntry when the performance counter overflows. APIC Interrupt enable.										
19	Reserved.										
18	Edge: edge detect. Read-write. Reset: 0. 0=Level detect. 1=Zero-to-one Edge detect. The edge count mode increments the counter when a transition happens on the monitored event. If the event selected is changed without disabling the counter, an extra edge is falsely detected when the first event is a static 0 and the second event is a static one. To avoid this false edge detection, disable the counter when changing the event and then enable the counter with a second MSR write.										
17:16	OsUserMode: OS and user mode. Read-write. Reset: 0h. Event counter for OS and user mode.										
	ValidValues:										
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>Count no events.</td></tr> <tr> <td>1h</td><td>Count user events (CPL>0).</td></tr> <tr> <td>2h</td><td>Count OS events (CPL=0).</td></tr> <tr> <td>3h</td><td>Count all events, irrespective of the CPL.</td></tr> </table>	Value	Description	0h	Count no events.	1h	Count user events (CPL>0).	2h	Count OS events (CPL=0).	3h	Count all events, irrespective of the CPL.
Value	Description										
0h	Count no events.										
1h	Count user events (CPL>0).										
2h	Count OS events (CPL=0).										
3h	Count all events, irrespective of the CPL.										

15:8	UnitMask: event qualification. Read-write. Reset: 00h. Each UnitMask bit further specifies or qualifies the event specified by EventSelect. All events selected by UnitMask are simultaneously monitored. Unless otherwise stated, the UnitMask values shown may be combined (logically ORed) to select any desired combination of the sub-events for a given event. In some cases, certain combinations can result in misleading counts, or the UnitMask value is an ordinal rather than a bit mask. These situations are described where applicable, or should be obvious from the event descriptions. For events where no UnitMask table is shown, the UnitMask is Unused.
7:0	EventSelect[7:0]: event select. Read-write. Reset: 00h. EventSelect[11:0] = {EventSelect[11:8], EventSelect[7:0]}. EventSelect specifies the event or event duration in a processor unit to be counted by the corresponding PERF_CTR[5:0] register. The events are specified in 2.1.13.4 [Core Performance Monitor Counters]. Some events are Reserved; when a Reserved event is selected, the results are undefined.

MSRC001_0001 [Performance Event Select 1] (Core::X86::Msr::PERF_LEGACY_CTL1)

Read-write. Reset: 0000_0000_0000_0000h.

The legacy alias of Core::X86::Msr::PERF_CTL1. See Core::X86::Msr::PERF_CTL1.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC001_0001

Bits	Description										
63:42	Reserved.										
41:40	HostGuestOnly: count only host/guest events. Read-write. Reset: 0h. Host/Guest event counter.										
	ValidValues:										
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>Count all events, irrespective of guest/host.</td></tr> <tr> <td>1h</td><td>Count guest events if [SVME] == 1.</td></tr> <tr> <td>2h</td><td>Count host events if [SVME] == 1.</td></tr> <tr> <td>3h</td><td>Count all guest and host events if [SVME] == 1.</td></tr> </table>	Value	Description	0h	Count all events, irrespective of guest/host.	1h	Count guest events if [SVME] == 1.	2h	Count host events if [SVME] == 1.	3h	Count all guest and host events if [SVME] == 1.
Value	Description										
0h	Count all events, irrespective of guest/host.										
1h	Count guest events if [SVME] == 1.										
2h	Count host events if [SVME] == 1.										
3h	Count all guest and host events if [SVME] == 1.										
39:36	Reserved.										
35:32	EventSelect[11:8]. Read-write. Reset: 0h. Performance event select[11:8].										
31:24	CntMask: counter mask. Read-write. Reset: 00h. Controls the number of events counted per clock cycle.										
	ValidValues:										
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>00h</td><td>The corresponding PERF_CTR[5:0] register increments by the number of events occurring in a clock cycle. See 2.1.13.3 [Large Increment per Cycle Events] for events that can increment greater than 15 per cycle.</td></tr> <tr> <td>7Fh-01h</td><td>When Inv == 0, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is greater than or equal to the CntMask value. When Inv == 1, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is less than CntMask value.</td></tr> <tr> <td>FFh-80h</td><td>Reserved.</td></tr> </table>	Value	Description	00h	The corresponding PERF_CTR[5:0] register increments by the number of events occurring in a clock cycle. See 2.1.13.3 [Large Increment per Cycle Events] for events that can increment greater than 15 per cycle.	7Fh-01h	When Inv == 0, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is greater than or equal to the CntMask value. When Inv == 1, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is less than CntMask value.	FFh-80h	Reserved.		
Value	Description										
00h	The corresponding PERF_CTR[5:0] register increments by the number of events occurring in a clock cycle. See 2.1.13.3 [Large Increment per Cycle Events] for events that can increment greater than 15 per cycle.										
7Fh-01h	When Inv == 0, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is greater than or equal to the CntMask value. When Inv == 1, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is less than CntMask value.										
FFh-80h	Reserved.										
23	Inv: invert counter mask. Read-write. Reset: 0. See CntMask.										
22	En: enable performance counter. Read-write. Reset: 0. 1=Performance event counter is enabled. Performance counter enable.										
21	Reserved.										
20	Int: enable APIC interrupt. Read-write. Reset: 0. 1=APIC performance counter LVT interrupt is enabled to generate an interrupt via Core::X86::Apic::PerformanceCounterLvtEntry when the performance counter overflows. APIC interrupt enable.										
19	Reserved.										
18	Edge: edge detect. Read-write. Reset: 0. 0=Level detect. 1=Zero-to-one Edge detect. The edge count mode increments the counter when a transition happens on the monitored event. If the event selected is changed without disabling the counter, an extra edge is falsely detected when the first event is a static 0 and the second event is a static one. To avoid this false edge detection, disable the counter when changing the event and then enable the counter with a second MSR write.										
17:16	OsUserMode: OS and user mode. Read-write. Reset: 0h. OS and user mode counter events.										
	ValidValues:										
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>Count no events.</td></tr> <tr> <td>1h</td><td>Count user events (CPL>0).</td></tr> <tr> <td>2h</td><td>Count OS events (CPL=0).</td></tr> <tr> <td>3h</td><td>Count all events, irrespective of the CPL.</td></tr> </table>	Value	Description	0h	Count no events.	1h	Count user events (CPL>0).	2h	Count OS events (CPL=0).	3h	Count all events, irrespective of the CPL.
Value	Description										
0h	Count no events.										
1h	Count user events (CPL>0).										
2h	Count OS events (CPL=0).										
3h	Count all events, irrespective of the CPL.										

15:8	UnitMask: event qualification. Read-write. Reset: 00h. Each UnitMask bit further specifies or qualifies the event specified by EventSelect. All events selected by UnitMask are simultaneously monitored. Unless otherwise stated, the UnitMask values shown may be combined (logically ORed) to select any desired combination of the sub-events for a given event. In some cases, certain combinations can result in misleading counts, or the UnitMask value is an ordinal rather than a bit mask. These situations are described where applicable, or should be obvious from the event descriptions. For events where no UnitMask table is shown, the UnitMask is Unused.
7:0	EventSelect[7:0]: event select. Read-write. Reset: 00h. EventSelect[11:0] = {EventSelect[11:8], EventSelect[7:0]}. EventSelect specifies the event or event duration in a processor unit to be counted by the corresponding PERF_CTR[5:0] register. The events are specified in 2.1.13.4 [Core Performance Monitor Counters]. Some events are Reserved; when a Reserved event is selected, the results are undefined.

MSRC001_0002 [Performance Event Select 2] (Core::X86::Msr::PERF_LEGACY_CTL2)

Read-write. Reset: 0000_0000_0000_0000h.

The legacy alias of Core::X86::Msr::PERF_CTL2. See Core::X86::Msr::PERF_CTL2.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC001_0002

Bits	Description										
63:42	Reserved.										
41:40	HostGuestOnly: count only host/guest events. Read-write. Reset: 0h. Host/Guest event counter.										
	ValidValues:										
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>Count all events, irrespective of guest/host.</td></tr> <tr> <td>1h</td><td>Count guest events if [SVME] == 1.</td></tr> <tr> <td>2h</td><td>Count host events if [SVME] == 1.</td></tr> <tr> <td>3h</td><td>Count all guest and host events if [SVME] == 1.</td></tr> </table>	Value	Description	0h	Count all events, irrespective of guest/host.	1h	Count guest events if [SVME] == 1.	2h	Count host events if [SVME] == 1.	3h	Count all guest and host events if [SVME] == 1.
Value	Description										
0h	Count all events, irrespective of guest/host.										
1h	Count guest events if [SVME] == 1.										
2h	Count host events if [SVME] == 1.										
3h	Count all guest and host events if [SVME] == 1.										
39:36	Reserved.										
35:32	EventSelect[11:8]. Read-write. Reset: 0h. Performance event select[11:8].										
31:24	CntMask: counter mask. Read-write. Reset: 00h. Controls the number of events counted per clock cycle.										
	ValidValues:										
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>00h</td><td>The corresponding PERF_CTR[5:0] register increments by the number of events occurring in a clock cycle. See 2.1.13.3 [Large Increment per Cycle Events] for events that can increment greater than 15 per cycle.</td></tr> <tr> <td>7Fh-01h</td><td>When Inv == 0, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is greater than or equal to the CntMask value. When Inv == 1, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is less than CntMask value.</td></tr> <tr> <td>FFh-80h</td><td>Reserved.</td></tr> </table>	Value	Description	00h	The corresponding PERF_CTR[5:0] register increments by the number of events occurring in a clock cycle. See 2.1.13.3 [Large Increment per Cycle Events] for events that can increment greater than 15 per cycle.	7Fh-01h	When Inv == 0, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is greater than or equal to the CntMask value. When Inv == 1, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is less than CntMask value.	FFh-80h	Reserved.		
Value	Description										
00h	The corresponding PERF_CTR[5:0] register increments by the number of events occurring in a clock cycle. See 2.1.13.3 [Large Increment per Cycle Events] for events that can increment greater than 15 per cycle.										
7Fh-01h	When Inv == 0, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is greater than or equal to the CntMask value. When Inv == 1, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is less than CntMask value.										
FFh-80h	Reserved.										
23	Inv: invert counter mask. Read-write. Reset: 0. See CntMask.										
22	En: enable performance counter. Read-write. Reset: 0. 1=Performance event counter is enabled. Performance counter enable.										
21	Reserved.										
20	Int: enable APIC interrupt. Read-write. Reset: 0. 1=APIC performance counter LVT interrupt is enabled to generate an interrupt via Core::X86::Apic::PerformanceCounterLvtEntry when the performance counter overflows. APIC interrupt enable.										
19	Reserved.										
18	Edge: edge detect. Read-write. Reset: 0. 0=Level detect. 1=Zero-to-one Edge detect. The edge count mode increments the counter when a transition happens on the monitored event. If the event selected is changed without disabling the counter, an extra edge is falsely detected when the first event is a static 0 and the second event is a static one. To avoid this false edge detection, disable the counter when changing the event and then enable the counter with a second MSR write.										
17:16	OsUserMode: OS and user mode. Read-write. Reset: 0h. OS and user mode.										
	ValidValues:										
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>Count no events.</td></tr> <tr> <td>1h</td><td>Count user events (CPL>0).</td></tr> <tr> <td>2h</td><td>Count OS events (CPL=0).</td></tr> <tr> <td>3h</td><td>Count all events, irrespective of the CPL.</td></tr> </table>	Value	Description	0h	Count no events.	1h	Count user events (CPL>0).	2h	Count OS events (CPL=0).	3h	Count all events, irrespective of the CPL.
Value	Description										
0h	Count no events.										
1h	Count user events (CPL>0).										
2h	Count OS events (CPL=0).										
3h	Count all events, irrespective of the CPL.										

15:8	UnitMask: event qualification. Read-write. Reset: 00h. Each UnitMask bit further specifies or qualifies the event specified by EventSelect. All events selected by UnitMask are simultaneously monitored. Unless otherwise stated, the UnitMask values shown may be combined (logically ORed) to select any desired combination of the sub-events for a given event. In some cases, certain combinations can result in misleading counts, or the UnitMask value is an ordinal rather than a bit mask. These situations are described where applicable, or should be obvious from the event descriptions. For events where no UnitMask table is shown, the UnitMask is Unused.
7:0	EventSelect[7:0]: event select. Read-write. Reset: 00h. EventSelect[11:0] = {EventSelect[11:8], EventSelect[7:0]}. EventSelect specifies the event or event duration in a processor unit to be counted by the corresponding PERF_CTR[5:0] register. The events are specified in 2.1.13.4 [Core Performance Monitor Counters]. Some events are Reserved; when a Reserved event is selected, the results are undefined.

MSRC001_0003 [Performance Event Select 3] (Core::X86::Msr::PERF_LEGACY_CTL3)

Read-write. Reset: 0000_0000_0000_0000h.

The legacy alias of Core::X86::Msr::PERF_CTL3. See Core::X86::Msr::PERF_CTL3.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC001_0003

Bits	Description										
63:42	Reserved.										
41:40	HostGuestOnly: count only host/guest events. Read-write. Reset: 0h. Host/guest event counter.										
	ValidValues:										
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>Count all events, irrespective of guest/host.</td></tr> <tr> <td>1h</td><td>Count guest events if [SVME] == 1.</td></tr> <tr> <td>2h</td><td>Count host events if [SVME] == 1.</td></tr> <tr> <td>3h</td><td>Count all guest and host events if [SVME] == 1.</td></tr> </table>	Value	Description	0h	Count all events, irrespective of guest/host.	1h	Count guest events if [SVME] == 1.	2h	Count host events if [SVME] == 1.	3h	Count all guest and host events if [SVME] == 1.
Value	Description										
0h	Count all events, irrespective of guest/host.										
1h	Count guest events if [SVME] == 1.										
2h	Count host events if [SVME] == 1.										
3h	Count all guest and host events if [SVME] == 1.										
39:36	Reserved.										
35:32	EventSelect[11:8]. Read-write. Reset: 0h. Performance event select[11:8].										
31:24	CntMask: counter mask. Read-write. Reset: 00h. Controls the number of events counted per clock cycle.										
	ValidValues:										
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>00h</td><td>The corresponding PERF_CTR[5:0] register increments by the number of events occurring in a clock cycle. See 2.1.13.3 [Large Increment per Cycle Events] for events that can increment greater than 15 per cycle.</td></tr> <tr> <td>7Fh-01h</td><td>When Inv == 0, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is greater than or equal to the CntMask value. When Inv == 1, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is less than CntMask value.</td></tr> <tr> <td>FFh-80h</td><td>Reserved.</td></tr> </table>	Value	Description	00h	The corresponding PERF_CTR[5:0] register increments by the number of events occurring in a clock cycle. See 2.1.13.3 [Large Increment per Cycle Events] for events that can increment greater than 15 per cycle.	7Fh-01h	When Inv == 0, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is greater than or equal to the CntMask value. When Inv == 1, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is less than CntMask value.	FFh-80h	Reserved.		
Value	Description										
00h	The corresponding PERF_CTR[5:0] register increments by the number of events occurring in a clock cycle. See 2.1.13.3 [Large Increment per Cycle Events] for events that can increment greater than 15 per cycle.										
7Fh-01h	When Inv == 0, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is greater than or equal to the CntMask value. When Inv == 1, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is less than CntMask value.										
FFh-80h	Reserved.										
23	Inv: invert counter mask. Read-write. Reset: 0. See CntMask.										
22	En: enable performance counter. Read-write. Reset: 0. 1=Performance event counter is enabled. Performance counter enable.										
21	Reserved.										
20	Int: enable APIC interrupt. Read-write. Reset: 0. 1=APIC performance counter LVT interrupt is enabled to generate an interrupt via Core::X86::Apic::PerformanceCounterLvtEntry when the performance counter overflows. APIC interrupt enable.										
19	Reserved.										
18	Edge: edge detect. Read-write. Reset: 0. 0=Level detect. 1=Zero-to-one Edge detect. The edge count mode increments the counter when a transition happens on the monitored event. If the event selected is changed without disabling the counter, an extra edge is falsely detected when the first event is a static 0 and the second event is a static one. To avoid this false edge detection, disable the counter when changing the event and then enable the counter with a second MSR write.										
17:16	OsUserMode: OS and user mode. Read-write. Reset: 0h. OS and user mode counter events.										
	ValidValues:										
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>Count no events.</td></tr> <tr> <td>1h</td><td>Count user events (CPL>0).</td></tr> <tr> <td>2h</td><td>Count OS events (CPL=0).</td></tr> <tr> <td>3h</td><td>Count all events, irrespective of the CPL.</td></tr> </table>	Value	Description	0h	Count no events.	1h	Count user events (CPL>0).	2h	Count OS events (CPL=0).	3h	Count all events, irrespective of the CPL.
Value	Description										
0h	Count no events.										
1h	Count user events (CPL>0).										
2h	Count OS events (CPL=0).										
3h	Count all events, irrespective of the CPL.										

15:8	UnitMask: event qualification. Read-write. Reset: 00h. Each UnitMask bit further specifies or qualifies the event specified by EventSelect. All events selected by UnitMask are simultaneously monitored. Unless otherwise stated, the UnitMask values shown may be combined (logically ORed) to select any desired combination of the sub-events for a given event. In some cases, certain combinations can result in misleading counts, or the UnitMask value is an ordinal rather than a bit mask. These situations are described where applicable, or should be obvious from the event descriptions. For events where no UnitMask table is shown, the UnitMask is Unused.
7:0	EventSelect[7:0]: event select. Read-write. Reset: 00h. EventSelect[11:0] = {EventSelect[11:8], EventSelect[7:0]}. EventSelect specifies the event or event duration in a processor unit to be counted by the corresponding PERF_CTR[5:0] register. The events are specified in 2.1.13.4 [Core Performance Monitor Counters]. Some events are Reserved; when a Reserved event is selected, the results are undefined.

MSRC001_000[4...7] [Performance Event Counter [3:0]] (Core::X86::Msr::PERF_LEGACY_CTR)

Read-write, Volatile. Reset: 0000_0000_0000_0000h.

Note: When counting events that capable of counting greater than 15 events per cycle (MergeEvent) the even and the corresponding odd PERF_LEGACY_CTR must be paired to appear as a single 64-bit counter. See 2.1.13.3 [Large Increment per Cycle Events].

The legacy alias of Core::X86::Msr::PERF_CTR. See Core::X86::Msr::PERF_CTR.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n0; MSRC001_0004

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n1; MSRC001_0005

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n2; MSRC001_0006

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n3; MSRC001_0007

Bits	Description
63:48	Reserved.
47:0	CTR. Read-write, Volatile. Reset: 0000_0000_0000h. Performance counter value.

MSRC001_0010 [System Configuration] (Core::X86::Msrr::SYS_CFG)

Reset: 0000_0000_0000_0000h.

If Core::X86::Msrr::SYS_CFG[SecureNestedPagingEn] is set, writes to this register are ignored.

_ccd[1:0]_lthree0_core[7:0]; MSRC001_0010

Bits	Description															
63:27	Reserved.															
26	HMKEE: Host Multi-Key Encryption Enable. Read,Write-1-only. Reset: 0. Used with SYS_CFG[SMEE] to select secure memory encryption mode. See SYS_CFG[SMEE] for a table listing the available memory encryption modes.															
25	VmplEn. Reset: 0. VM permission levels enable. AccessType: Core::X86::Msrr::SYS_CFG[SecureNestedPagingEn] ? Read-only : Read-write.															
24	SecureNestedPagingEn. Read,Error-on-write-1. Reset: 0. Enable Secure Nested Paging (SNP).															
23	SMEE: Secure Memory Encryption Enable. Read,Write-1-only. Reset: 0. Description: Used with SYS_CFG[HMKEE] to select secure memory encryption mode. See the table below for the available memory encryption modes. <table><tr><th>HMKEE</th><th>SMEE</th><th>Description</th></tr><tr><td>0</td><td>0</td><td>No encryption.</td></tr><tr><td>0</td><td>1</td><td>Enables SME and SEV memory encryption.</td></tr><tr><td>1</td><td>0</td><td>Enables SME-HMK memory encryption.</td></tr><tr><td>1</td><td>1</td><td>Not supported. Results in #GP.</td></tr></table>	HMKEE	SMEE	Description	0	0	No encryption.	0	1	Enables SME and SEV memory encryption.	1	0	Enables SME-HMK memory encryption.	1	1	Not supported. Results in #GP.
HMKEE	SMEE	Description														
0	0	No encryption.														
0	1	Enables SME and SEV memory encryption.														
1	0	Enables SME-HMK memory encryption.														
1	1	Not supported. Results in #GP.														
22	Tom2ForceMemTypeWB: top of memory 2 memory type write back. Read-write. Reset: 0. 1=The default memory type of memory between 4GB and Core::X86::Msrr::TOM2 is write back instead of the memory type defined by Core::X86::Msrr::MTRRdefType[MemType]. For this bit to have any effect, Core::X86::Msrr::MTRRdefType[MtrrDefTypeEn] must be 1. MTRRs and PAT can be used to override this memory type.															
21	MtrrTom2En: MTRR top of memory 2 enable. Read-write. Reset: 0. 0=Core::X86::Msrr::TOM2 is disabled. 1=Core::X86::Msrr::TOM2 is enabled.															
20	MtrrVarDramEn: MTRR variable DRAM enable. Read-write. Reset: 0. Init: BIOS,1. 0=Core::X86::Msrr::TOP_MEM and IORRs are disabled. 1=These registers are enabled.															
19	MtrrFixDramModEn: MTRR fixed RdDram and WrDram modification enable. Read-write. Reset: 0. 0=Core::X86::Msrr::MtrrFix_64K through Core::X86::Msrr::MtrrFix_4K_7 [RdDram,WrDram] read values is masked 00b; writing does not change the hidden value. 1=Core::X86::Msrr::MtrrFix_64K through Core::X86::Msrr::MtrrFix_4K_7 [RdDram,WrDram] access type is Read-write. Not shared between threads. Controls access to Core::X86::Msrr::MtrrFix_64K through Core::X86::Msrr::MtrrFix_4K_7 [RdDram ,WrDram]. This bit should be set to 1 during BIOS initialization of the fixed MTRRs, then cleared to 0 for operation.															
18	MtrrFixDramEn: MTRR fixed RdDram and WrDram attributes enable. Read-write. Reset: 0. Init: BIOS,1. 1=Enables the RdDram and WrDram attributes in Core::X86::Msrr::MtrrFix_64K through Core::X86::Msrr::MtrrFix_4K_7.															
17:0	Reserved.															

MSRC001_0015 [Hardware Configuration] (Core::X86::Msr::HWCR)

Reset: 0000_0000_0100_0010h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC001_0015

Bits	Description
63:36	Reserved.
35	CpuidFltEn . Read-write. Reset: 0. 1=Executing CPUID outside of SMM and with CPL > 0 results in #GP.
34	Reserved.
33	SmmPgCfgLock . Read-write. Reset: 0. 1=SMM page config locked. Error-on-write-1 if not in SMM mode. RSM unconditionally clears Core::X86::Msr::HWCR[SmmPgCfgLock].
32:31	Reserved.
30	IRPerfEn: enable instructions retired counter . Read-write. Reset: 0. 1=Enable Core::X86::Msr::IRPerfCount.
29:28	Reserved.
27	EffFreqReadOnlyLock: read-only effective frequency counter lock . Write-1-only. Reset: 0. Init: BIOS, 1. 1=Core::X86::Msr::MPerfReadOnly, Core::X86::Msr::APerfReadOnly and Core::X86::Msr::IRPerfCount are read-only.
26	EffFreqCntMwait: effective frequency counting during mwait . Read-write. Reset: 0. 0=The registers do not increment. 1=The registers increment. Specifies whether Core::X86::Msr::MPERF and Core::X86::Msr::APERF increment while the core is in the monitor event pending state. See 2.1.3 [Effective Frequency].
25	CpbDis: core performance boost disable . Read-write. Reset: 0. 0=CPB is requested to be enabled. 1=CPB is disabled. Specifies whether core performance boost is requested to be enabled or disabled. If core performance boost is disabled while a core is in a boosted P-state, the core automatically transitions to the highest performance non-boosted P-state.
24	TscFreqSel: TSC frequency select . Read-only. Reset: 1. 1=The TSC increments at the P0 frequency.
23:22	Reserved.
21	LockTscToCurrentP0: lock the TSC to the current P0 frequency . Read-write. Reset: 0. 0=The TSC will count at the P0 frequency. 1=The TSC frequency is locked to the current P0 frequency at the time this bit is set and remains fixed regardless of future changes to the P0 frequency.
20	IoCfgGpFault: IO-space configuration causes a GP fault . Read-write. Reset: 0. 1=IO-space accesses to configuration space cause a GP fault. The fault is triggered if any part of the IO Read/Write address range is between CF8h and CFFh, inclusive. These faults only result from single IO instructions, not to string and REP IO instructions. This fault takes priority over the IO trap mechanism described by Core::X86::Msr::SMI_ON_IO_TRAP_CTL_STS.
19	Reserved.
18	McStatusWrEn: machine check status write enable . Read-write. Reset: 0. 0=MCA_STATUS registers are readable; writing a non-zero pattern to these registers causes a general protection fault. 1=MCA_STATUS registers are Read-write, including Reserved fields; do not cause general protection faults; such writes update all implemented bits in these registers; All fields of all threshold registers are Read-write when accessed from MSR space, including Locked, except BlkPtr which is always Read-only; McStatusWrEn does not change the access type for the thresholding registers accessed via configuration space. Description: McStatusWrEn can be used to debug machine check exception and interrupt handlers. Independent of the value of this bit, the processor may enforce Write-Ignored behavior on MCA_STATUS registers depending on platform settings. See 3.1 [Machine Check Architecture].
17	Wrap32Dis: 32-bit address wrap disable . Read-write. Reset: 0. 1=Disable 32-bit address wrapping. Software can use Wrap32Dis to access physical memory above 4 Gbytes without switching into 64-bit mode. To do so, software should write a greater-than 4 Gbyte address to Core::X86::Msr::FS_BASE and Core::X86::Msr::GS_BASE. Then it would address ± 2 Gbytes from one of those bases using normal memory reference instructions with a FS or GS override prefix. However, the INVLPG, FST, and SSE store instructions generate 32-bit addresses in legacy mode, regardless of the state of Wrap32Dis.
16:15	Reserved.

14	RsmSpCycDis: RSM special bus cycle disable. Reset: 0. Init: BIOS,1. 0=A link special bus cycle, SMIACK, is generated on a resume from SMI. AccessType: Core::X86::Msrr::HWCR[SmmLock] ? Read-only : Read-write.
13	SmiSpCycDis: SMI special bus cycle disable. Reset: 0. Init: BIOS,1. 0=A link special bus cycle, SMIACK, is generated when an SMI interrupt is taken. AccessType: Core::X86::Msrr::HWCR[SmmLock] ? Read-only : Read-write.
12:11	Reserved.
10	MonMwaitUserEn: MONITOR/MWAIT user mode enable. Read-write. Reset: 0. 0=The MONITOR and MWAIT instructions are supported only in privilege level 0; these instructions in privilege levels 1 to 3 cause a #UD exception. 1=The MONITOR and MWAIT instructions are supported in all privilege levels. The state of this bit is ignored if MonMwaitDis is set.
9	MonMwaitDis: MONITOR and MWAIT disable. Read-write. Reset: 0. 1=The MONITOR, MWAIT, MONITORX, and MWAITX opcodes become invalid. This affects what is reported back through Core::X86::Cpuid::FeatureIdEcxC[Monitor] and Core::X86::Cpuid::FeatureExtIdEcxC[MwaitExtended].
8	IgnneEm: IGNNE port emulation enable. Read-write. Reset: 0. 1=Enable emulation of IGNNE port.
7	AllowFERRonNE: allow FERR on NE. Read-write. Reset: 0. 0=Disable FERR signalling when generating an x87 floating point exception (when CR0[NE] is set). 1=FERR is signaled on any x87 floating point exception, regardless of CR0[NE].
6:5	Reserved.
4	INVDWBINVD: INVD to WBINVD conversion. Read,Error-on-write-0. Reset: 1. 1=Convert INVD to WBINVD. Description: This bit is required to be set for normal operation when any of the following are true: <ul style="list-style-type: none"> • An L2 is shared by multiple threads. • An L3 is shared by multiple cores. • CC6 is enabled. • Probe filter is enabled.
3	TlbCacheDis: cacheable memory disable. Read-write. Reset: 0. 1=Disable performance improvement that assumes that the PML4, PDP, PDE and PTE entries are in cacheable WB DRAM. Description: Operating systems that maintain page tables in any other memory type must set the TlbCacheDis bit to insure proper operation. Operating system should do a full TLB flush before and after any changes to this bit value. <ul style="list-style-type: none"> • TlbCacheDis does not override the memory type specified by the SMM ASeg and TSeg memory regions controlled by Core::X86::Msrr::SMMAddr Core::X86::Msrr::SMMMMask.
2:1	Reserved.
0	SmmLock: SMM code lock. Read,Write-1-only. Reset: 0. Init: BIOS,1. 1=SMM code in the ASeg and TSeg range and the SMM registers are Read-only and SMI interrupts are not intercepted in SVM. See 2.1.10.1.10 [Locking SMM].

MSRC001_001[6...8] [IO Range Base] (Core::X86::MsR::IORR_BASE)

Read-write.

Core::X86::MsR::IORR_BASE and Core::X86::MsR::IORR_MASK combine to specify the two sets of base and mask pairs for two IORR ranges. A core access, with address CPUAddr, is determined to be within IORR address range if the following equation is true:

$\text{CPUAddr}[47:12] \& \text{PhyMask}[47:12] == \text{PhyBase}[47:12] \& \text{PhyMask}[47:12]$.

BIOS can use the IORRs to create an IO hole within a range of addresses that would normally be mapped to DRAM. It can also use the IORRs to re-assert a DRAM destination for a range of addresses that fall within a bigger IO hole that overlays DRAM.

If Core::X86::MsR::SYS_CFG[SecureNestedPagingEn] is set to 1, this register will be read-only and attempts to write to this register will result in #GP(0).

_ccd[1:0]_lthree0_core[7:0]_n0; MSRC001_0016

_ccd[1:0]_lthree0_core[7:0]_n1; MSRC001_0018

Bits	Description
63:48	Reserved.
47:12	PhyBase. Read-write. Reset: X_XXXX_XXXXh. Physical base address for IO range.
11:5	Reserved.
4	RdMem: read from memory. Read-write. Reset: X. 0=Read accesses to the range are directed to IO. 1=Read accesses to the range are directed to system memory.
3	WrMem: write to memory. Read-write. Reset: X. 0=Write accesses to the range are directed to IO. 1=Write accesses to the range are directed to system memory.
2:0	Reserved.

MSRC001_001[7...9] [IO Range Mask] (Core::X86::MsR::IORR_MASK)

Read-write. Reset: 0000_0000_0000_0000h.

See Core::X86::MsR::IORR_BASE.

If Core::X86::MsR::SYS_CFG[SecureNestedPagingEn] is set to 1, this register will be read-only and attempts to write to this register will result in #GP(0).

_ccd[1:0]_lthree0_core[7:0]_n0; MSRC001_0017

_ccd[1:0]_lthree0_core[7:0]_n1; MSRC001_0019

Bits	Description
63:48	Reserved.
47:12	PhyMask. Read-write. Reset: 0_0000_0000h. Physical address mask for IO range.
11	Valid. Read-write. Reset: 0. 1=The pair of registers that specifies an IORR range is valid.
10:0	Reserved.

MSRC001_001A [Top Of Memory] (Core::X86::MsR::TOP_MEM)

Read-write.

If Core::X86::MsR::SYS_CFG[SecureNestedPagingEn] is set to 1, this register will be read-only and attempts to write to this register will result in #GP(0).

_ccd[1:0]_lthree0_core[7:0]; MSRC001_001A

Bits	Description
63:48	Reserved.
47:23	TOM[47:23]: top of memory. Read-write. Reset: XXX_XXXXh. Specifies the address that divides between MMIO and DRAM. This value is normally placed below 4G. From TOM to 4G is MMIO; below TOM is DRAM. See 2.1.4.3 [System Address Map].
22:0	Reserved.

MSRC001_001D [Top Of Memory 2] (Core::X86::Msr::TOM2)

Read-write.

If Core::X86::Msr::SYS_CFG[SecureNestedPagingEn] is set to 1, this register will be read-only and attempts to write to this register will result in #GP(0).

_ccd[1:0]_lthree0_core[7:0]; MSRC001_001D

Bits	Description
63:48	Reserved.
47:23	TOM2[47:23]: second top of memory. Read-write. Reset: XXX_XXXXh. Specifies the address divides between MMIO and DRAM. This value is normally placed above 4G. From 4G to TOM2 - 1 is DRAM; TOM2 and above is MMIO. See 2.1.4.3 [System Address Map]. This register is enabled by Core::X86::Msr::SYS_CFG[MtrrTom2En].
22:0	Reserved.

MSRC001_0020 [Patch Loader] (Core::X86::Msr::PATCH_LOADER)

Write-only, Error-on-read.

_ccd[1:0]_lthree0_core[7:0]; MSRC001_0020

Bits	Description
63:0	PatchBase. Write-only, Error-on-read. Reset: XXXX_XXXX_XXXX_XXXXh. Linear address of the Microcode Patch Block. PatchBase[63:32] is ignored when the core is not operating in 64-bit mode.

MSRC001_0022 [Machine Check Exception Redirection] (Core::X86::Msr::McExcepRedir)

Read-write. Reset: 0000_0000_0000_0000h.

This register can be used to redirect machine check exceptions (MCEs) to SMIs or vectored interrupts. If both RedirSmiEn and RedirVecEn are set, then undefined behavior results.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC001_0022

Bits	Description
63:10	Reserved.
9	RedirSmiEn. Read-write. Reset: 0. 1=Redirect MCEs (that are directed to this core) to generate an SMI-trigger IO cycle via Core::X86::Msr::SmiTrigIoCycle. The status is stored in Core::X86::Smm::LocalSmiStatus[MceRedirSts].
8	RedirVecEn. Read-write. Reset: 0. 1=Redirect MCEs (that are directed to this core) to generate a vectored interrupt, using the interrupt vector specified in RedirVector.
7:0	RedirVector. Read-write. Reset: 00h. See RedirVecEn.

MSRC001_003[0...5] [Processor Name String] (Core::X86::Msr::ProcNameString)

Read-write.

These 6 registers hold the CPUID name string in ASCII. The state of these registers are returned by CPUID instructions, Core::X86::Cpuid::ProcNameStr0Eax through Core::X86::Cpuid::ProcNameStr2Edx. BIOS should set these registers to the product name for the processor as provided by AMD. Each register contains a block of 8 ASCII characters; the least byte corresponds to the first ASCII character of the block; the most-significant byte corresponds to the last character of the block. MSRC001_0030 contains the first block of the name string; MSRC001_0035 contains the last block of the name string.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n0; MSRC001_0030

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n1; MSRC001_0031

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n2; MSRC001_0032

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n3; MSRC001_0033

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n4; MSRC001_0034

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n5; MSRC001_0035

Bits	Description
63:56	CpuNameString7 . Read-write. Reset: XXh. CPUID name string in ASCII.
55:48	CpuNameString6 . Read-write. Reset: XXh. CPUID name string in ASCII.
47:40	CpuNameString5 . Read-write. Reset: XXh. CPUID name string in ASCII.
39:32	CpuNameString4 . Read-write. Reset: XXh. CPUID name string in ASCII.
31:24	CpuNameString3 . Read-write. Reset: XXh. CPUID name string in ASCII.
23:16	CpuNameString2 . Read-write. Reset: XXh. CPUID name string in ASCII.
15:8	CpuNameString1 . Read-write. Reset: XXh. CPUID name string in ASCII.
7:0	CpuNameString0 . Read-write. Reset: XXh. CPUID name string in ASCII.

MSRC001_005[0...3] [IO Trap] (Core::X86::Msr::SMI_ON_IO_TRAP)

Read-write. Reset: 0000_0000_0000_0000h.

Core::X86::Msr::SMI_ON_IO_TRAP and Core::X86::Msr::SMI_ON_IO_TRAP_CTL_STS provide a mechanism for executing the SMI handler if an access to one of the specified addresses is detected. Access address and access type checking is performed before IO instruction execution. If the access address and access type match one of the specified IO address and access types, then: (1) the IO instruction is not executed; (2) any breakpoint, other than the single-step breakpoint, set on the IO instruction is not taken (the single-step breakpoint is taken after resuming from SMM); and (3) issue the SMI-trigger IO cycle specified by Core::X86::Msr::SmiTrigIoCycle if enabled. The status is stored in Core::X86::Smm::LocalSmiStatus[IoTrapSts].

IO-space configuration accesses are special IO accesses. An IO access is defined as an IO-space configuration access when IO instruction address bits[31:0] are CFCh, CFDh, CFEh, or CFFh when IO-space configuration is enabled (IO::IoCfgAddr[ConfigEn]). The access address for a configuration space access is the current value of IO::IoCfgAddr[BusNo,Device,Function,RegNo]. The access address for an IO access that is not a configuration access is equivalent to the IO instruction address, bits[31:0].

The access address is compared with SmiAddr, and the instruction access type is compared with the enabled access types defined by ConfigSmi, SmiOnRdEn, and SmiOnWrEn. Access address bits[23:0] can be masked with SmiMask. IO and configuration space trapping to SMI applies only to single IO instructions; it does not apply to string and REP IO instructions. The conditional GP fault described by Core::X86::Msr::HWCR[IoCfgGpFault] takes priority over this trap.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n0; MSRC001_0050

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n1; MSRC001_0051

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n2; MSRC001_0052

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n3; MSRC001_0053

Bits	Description						
63	SmiOnRdEn: enable SMI on IO Read. Read-write. Reset: 0. 1=Enables SMI generation on a Read access.						
62	SmiOnWrEn: enable SMI on IO Write. Read-write. Reset: 0. 1=Enables SMI generation on a Write access.						
61	ConfigSmi: configuration space SMI. Read-write. Reset: 0. 0=IO access (that is not an IO-space configuration access). 1=Configuration access.						
60:56	Reserved.						
55:32	SmiMask[23:0]. Read-write. Reset: 00_0000h. SMI IO trap mask. ValidValues:						
<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0</td><td>Mask address bit</td></tr> <tr> <td>1</td><td>Do not mask address bit</td></tr> </table>		Value	Description	0	Mask address bit	1	Do not mask address bit
Value	Description						
0	Mask address bit						
1	Do not mask address bit						
31:0	SmiAddr[31:0]. Read-write. Reset: 0000_0000h. SMI IO trap address.						

MSRC001_0054 [IO Trap Control] (Core::X86::Msr::SMI_ON_IO_TRAP_CTL_STS)

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC001_0054

Bits	Description
63:16	Reserved.
15	IoTrapEn: IO trap enable. Read-write. Reset: 0. 1=Enable IO and configuration space trapping specified by Core::X86::Msr::SMI_ON_IO_TRAP and Core::X86::Msr::SMI_ON_IO_TRAP_CTL_STS.
14:8	Reserved.
7	SmiEn3. Read-write. Reset: 0. 1=The trap Core::X86::Msr::SMI_ON_IO_TRAP_n[3] is enabled.
6	Reserved.
5	SmiEn2. Read-write. Reset: 0. 1=The trap Core::X86::Msr::SMI_ON_IO_TRAP_n[2] is enabled.
4	Reserved.
3	SmiEn1. Read-write. Reset: 0. 1=The trap Core::X86::Msr::SMI_ON_IO_TRAP_n[1] is enabled.
2	Reserved.
1	SmiEn0. Read-write. Reset: 0. 1=The trap Core::X86::Msr::SMI_ON_IO_TRAP_n[0] is enabled.
0	Reserved.

MSRC001_0055 [Reserved.] (Core::X86::Msr::IntPend)

Read-only. Reset: Fixed, 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]; MSRC001_0055

Bits Description

63:0 Reserved.

MSRC001_0056 [SMI Trigger IO Cycle] (Core::X86::Msr::SmiTrigIoCycle)

Read-write. Reset: 0000_0000_0000_0000h.

See 2.1.10.1.3 [SMI Sources And Delivery]. This register specifies an IO cycle that may be generated when a local SMI trigger event occurs. If IoCycleEn is set and there is a local SMI trigger event, then the IO cycle generated is a byte Read or Write, based on IoRd, to address IoPortAddress. If the cycle is a Write, then IoData contains the data written. If the cycle is a Read, the value read is discarded. If IoCycleEn is clear and a local SMI trigger event occurs, then undefined behavior results.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC001_0056

Bits Description

63:27 Reserved.

26 **IoRd: IO Read.** Read-write. Reset: 0. 0=IO write. 1=IO read.25 **IoCycleEn: IO cycle enable.** Read-write. Reset: 0. 1=The SMI trigger IO cycle is enabled to be generated.

24 Reserved.

23:16 **IoData.** Read-write. Reset: 00h. See 2.1.10.1.3 [SMI Sources And Delivery].15:0 **IoPortAddress.** Read-write. Reset: 0000h. See 2.1.10.1.3 [SMI Sources And Delivery].

MSRC001_0058 [MMIO Configuration Base Address] (Core::X86::Msr::MmioCfgBaseAddr)

See 2.1.5 [Configuration Space] for a description of MMIO configuration space.

_ccd[1:0]_lthree0_core[7:0]; MSRC001_0058

Bits	Description																																		
63:48	Reserved.																																		
47:20	MmioCfgBaseAddr[47:20]: MMIO configuration base address bits[47:20]. Read-write. Reset: XXX_XXXXh. Specifies the base address of the MMIO configuration range.																																		
19:6	Reserved.																																		
5:2	BusRange: bus range identifier. Read-write. Reset: 0h. Specifies the number of buses in the MMIO configuration space range. The size of the MMIO configuration space is 1 MB times the number of buses. ValidValues:																																		
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr><td>0h</td><td>1 bus, 1 segment</td></tr> <tr><td>1h</td><td>2 buses, 1 segment</td></tr> <tr><td>2h</td><td>4 buses, 1 segment</td></tr> <tr><td>3h</td><td>8 buses, 1 segment</td></tr> <tr><td>4h</td><td>16 buses, 1 segment</td></tr> <tr><td>5h</td><td>32 buses, 1 segment</td></tr> <tr><td>6h</td><td>64 buses, 1 segment</td></tr> <tr><td>7h</td><td>128 buses, 1 segment</td></tr> <tr><td>8h</td><td>256 buses, 1 segment</td></tr> <tr><td>9h</td><td>2 segments, 256 buses per segment</td></tr> <tr><td>Ah</td><td>4 segments, 256 buses per segment</td></tr> <tr><td>Bh</td><td>8 segments, 256 buses per segment</td></tr> <tr><td>Ch</td><td>16 segments, 256 buses per segment</td></tr> <tr><td>Dh</td><td>32 segments, 256 buses per segment</td></tr> <tr><td>Eh</td><td>64 segments, 256 buses per segment</td></tr> <tr><td>Fh</td><td>128 segments, 256 buses per segment</td></tr> </table>	Value	Description	0h	1 bus, 1 segment	1h	2 buses, 1 segment	2h	4 buses, 1 segment	3h	8 buses, 1 segment	4h	16 buses, 1 segment	5h	32 buses, 1 segment	6h	64 buses, 1 segment	7h	128 buses, 1 segment	8h	256 buses, 1 segment	9h	2 segments, 256 buses per segment	Ah	4 segments, 256 buses per segment	Bh	8 segments, 256 buses per segment	Ch	16 segments, 256 buses per segment	Dh	32 segments, 256 buses per segment	Eh	64 segments, 256 buses per segment	Fh	128 segments, 256 buses per segment
Value	Description																																		
0h	1 bus, 1 segment																																		
1h	2 buses, 1 segment																																		
2h	4 buses, 1 segment																																		
3h	8 buses, 1 segment																																		
4h	16 buses, 1 segment																																		
5h	32 buses, 1 segment																																		
6h	64 buses, 1 segment																																		
7h	128 buses, 1 segment																																		
8h	256 buses, 1 segment																																		
9h	2 segments, 256 buses per segment																																		
Ah	4 segments, 256 buses per segment																																		
Bh	8 segments, 256 buses per segment																																		
Ch	16 segments, 256 buses per segment																																		
Dh	32 segments, 256 buses per segment																																		
Eh	64 segments, 256 buses per segment																																		
Fh	128 segments, 256 buses per segment																																		
1	Reserved.																																		
0	Enable. Read-write. Reset: 0. 1=MMIO configuration space is enabled.																																		

MSRC001_0061 [P-state Current Limit] (Core::X86::Msr::PStateCurLim)

_ccd[1:0]_lthree0_core[7:0]; MSRC001_0061

Bits	Description
63:7	Reserved.
6:4	PstateMaxVal: P-state maximum value. Read,Error-on-write,Volatile. Reset: XXXb. Specifies the lowest-performance non-boosted P-state (highest non-boosted value) allowed. Attempts to change Core::X86::Msr::PStateCtl[PstateCmd] to a lower-performance P-state (higher value) are clipped to the value of this field.
3	Reserved.
2:0	CurPstateLimit: current P-state limit. Read,Error-on-write,Volatile. Reset: XXXb. Specifies the highest-performance P-state (lowest value) allowed. CurPstateLimit is always bounded by Core::X86::Msr::PStateCurLim[PstateMaxVal]. Attempts to change the CurPstateLimit to a value greater (lower performance) than Core::X86::Msr::PStateCurLim[PstateMaxVal] leaves CurPstateLimit unchanged.

MSRC001_0062 [P-state Control] (Core::X86::Msrr::PStateCtl)

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC001_0062

Bits	Description
63:3	Reserved.
2:0	PstateCmd: P-state change command. Read-write. Reset: XXXb. Cold reset value varies by product; after a warm reset, value initializes to the P-state the core was in prior to the reset. Writes to this field cause the core to change to the indicated non-boosted P-state number, specified by Core::X86::Msrr::PStateDef. 0=P0, 1=P1, etc. P-state limits are applied to any P-state requests made through this register. Reads from this field return the last written value, regardless of whether any limits are applied.

MSRC001_0063 [P-state Status] (Core::X86::Msrr::PStateStat)

Read,Error-on-write,Volatile.

_ccd[1:0]_lthree0_core[7:0]; MSRC001_0063

Bits	Description
63:3	Reserved.
2:0	CurPstate: current P-state. Read,Error-on-write,Volatile. Reset: XXXb. This field provides the frequency component of the current non-boosted P-state of the core (regardless of the source of the P-state change, including Core::X86::Msrr::PStateCtl[PstateCmd]). 0=P0, 1=P1, etc.). The value of this field is updated when the COF transitions to a new value associated with a P-state.

MSRC001_006[4...B] [P-state [7:0]] (Core::X86::Msrr::PStateDef)

Read-write.

Each of these registers specify the frequency and voltage associated with each of the core P-states.

The CpuVid field in these registers is required to be programmed to the same value in all cores of a processor, but are allowed to be different between processors in a multi-processor system. All other fields in these registers are required to be programmed to the same value in each core of the coherent fabric.

_n0_aliasMSR; MSRC001_0064

_n1_aliasMSR; MSRC001_0065

_n2_aliasMSR; MSRC001_0066

_n3_aliasMSR; MSRC001_0067

_n4_aliasMSR; MSRC001_0068

_n5_aliasMSR; MSRC001_0069

_n6_aliasMSR; MSRC001_006A

_n7_aliasMSR; MSRC001_006B

Bits	Description
63	PstateEn. Read-write. Reset: X. 0=The P-state specified by this MSR is not valid. 1=The P-state specified by this MSR is valid. The purpose of this register is to indicate if the rest of the P-state information in the register is valid after a reset; it controls no hardware.
62:33	Reserved.
32	CpuVid[8]: core VID[8]. Read-write. Reset: X.
31:30	IddDiv: current divisor. Read-write. Reset: XXb. See IddValue.
29:22	IddValue: current value. Read-write. Reset: XXXXXXXXb. After a reset, IddDiv and IddValue combine to specify the expected maximum current dissipation of a single core that is in the P-state corresponding to the MSR number. These values are intended to be used to create ACPI-defined _PSS objects. The values are expressed in amps; they are not intended to convey final product power levels; they may not match the power levels specified in the Power and Thermal Datasheets.
21:14	CpuVid[7:0]: core VID[7:0]. Read-write. Reset: XXXXXXXXb.
13:8	CpuDfsId: core divisor ID. Read-write. Reset: XXXXXXXb. Specifies the core frequency divisor; see CpuFid. For values [1Ah:08h], 1/8th integer divide steps supported down to VCO/3.25 (Note, L3/L2 fifo logic related to 4-cycle data heads-up requires core to be 1/3 of L3 frequency or higher). For values [30h:1Ch], 1/4th integer divide steps supported down to VCO/6 (DID[0] should zero if DID[5:0]>1Ah). (Note, core and L3 frequencies below 400MHz are not supported by the architecture). Core supports DID up to 30h, but L3 must be 2Ch (VCO/5.5) or less.

	ValidValues:	
	Value	Description
	00h	Off
	07h-01h	Reserved.
	08h	VCO/1
	09h	VCO/1.125
	1Ah-0Ah	VCO/<Value/8>
	1Bh	Reserved.
	1Ch	VCO/<Value/8>
	1Dh	Reserved.
	1Eh	VCO/<Value/8>
	1Fh	Reserved.
	20h	VCO/<Value/8>
	21h	Reserved.
	22h	VCO/<Value/8>
	23h	Reserved.
	24h	VCO/<Value/8>
	25h	Reserved.
	26h	VCO/<Value/8>
	27h	Reserved.
	28h	VCO/<Value/8>
	29h	Reserved.
	2Ah	VCO/<Value/8>
	2Bh	Reserved.
	2Ch	VCO/<Value/8>
	3Fh-2Dh	Reserved.
7:0	CpuFid[7:0]: core frequency ID. Read-write. Reset: XXh. Specifies the core frequency multiplier. The core COF is defined as CpuFid * 5MHz.	
	ValidValues:	
	Value	Description
	0Fh-00h	Reserved.
	FFh-10h	<Value>*25

MSRC001_0073 [C-state Base Address] (Core::X86::Msr::CStateBaseAddr)

Read-write. Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC001_0073

Bits	Description
63:16	Reserved.
15:0	CstateAddr: C-state address. Read-write. Reset: 0000h. Specifies the IO addresses trapped by the core for C-state entry requests. A value of 0 in this field specifies that the core does not trap any IO addresses for C-state entry. Writing values greater than FFF8h into this field result in undefined behavior. All other values cause the core to trap IO addresses CstateAddr through CstateAddr + 7.

MSRC001_0111 [SMM Base Address] (Core::X86::Msrr::SMM_BASE)

Reset: 0000_0000_0003_0000h.

This holds the base of the SMM memory region. The value of this register is stored in the save state on entry into SMM (see 2.1.10.1.5 [SMM Save State]) and it is restored on returning from SMM. The 16-bit CS (code segment) selector is loaded with SmmBase[19:4] on entering SMM. SmmBase[3:0] is required to be 0. The SMM base address can be changed in two ways:

- The SMM base address, at offset FF00h in the SMM state save area, may be changed by the SMI handler. The RSM instruction updates SmmBase with the new value.
- Normal WRMSR access to this register.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC001_0111

Bits	Description
63:32	Reserved.
31:0	SmmBase. Reset: 0003_0000h. Base address of the SMM memory region. AccessType: Core::X86::Msrr::HWCR[SmmLock] ? Read-only : Read-write.

MSRC001_0112 [SMM TSeg Base Address] (Core::X86::Msrr::SMMAddr)

Configurable. Reset: 0000_0000_0000_0000h.

See 2.1.10.1 [System Management Mode (SMM)] and 2.1.4.3.1 [Memory Access to the Physical Address Space]. See Core::X86::Msrr::SMMMask for more information about the ASeg and TSeg address ranges.

Each CPU access, directed at CPUAddr, is determined to be in the TSeg range if the following is true:

$\text{CPUAddr}[47:17] \& \text{TSegMask}[47:17] == \text{TSegBase}[47:17] \& \text{TSegMask}[47:17]$.

For example, if TSeg spans 256 KB and starts at the 1 MB address. The Core::X86::Msrr::SMMAddr[TSegBase[47:17]] would be set to 0010_0000h and the Core::X86::Msrr::SMMMask[TSegMask[47:17]] to FFFC_0000h (with zeros filling in for bits[16:0]). This results in a TSeg range from 0010_0000 to 0013_FFFFh.

_ccd[1:0]_lthree0_core[7:0]; MSRC001_0112

Bits	Description
63:48	Reserved.
47:17	TSegBase[47:17]: TSeg address range base. Configurable. Reset: 0000_0000h. AccessType: (Core::X86::Msrr::HWCR[SmmLock]) ? Read-only : Read-write.
16:0	Reserved.

MSRC001_0113 [SMM TSeg Mask] (Core::X86::Msr::SMMMask)

Configurable. Reset: 0000_0000_0000_0000h.

See 2.1.10.1 [System Management Mode (SMM)].

The ASeg address range is located at a fixed address from A0000h–BFFFFh. The TSeg range is located at a variable base (specified by Core::X86::Msr::SMMAddr[TSegBase[47:17]]) with a variable size (specified by Core::X86::Msr::SMMMask[TSegMask[47:17]]). These ranges provide a safe location for SMM code and data that is not readily accessible by non-SMM applications. The SMI handler can be located in one of these two ranges, or it can be located outside these ranges. These ranges must never overlap each other.

This register specifies how accesses to the ASeg and TSeg address ranges are controlled as follows:

- If [A,T]Valid == 1, then:
 - If in SMM, then:
 - If [A,T]Close == 0, then the accesses are directed to DRAM with memory type as specified in [A,T]MTypeDram.
 - If [A,T]Close == 1, then instruction accesses are directed to DRAM with memory type as specified in [A,T]MTypeDram and data accesses are directed at MMIO space and with attributes based on [A,T]MTypeIoWc.
 - If not in SMM, then the accesses are directed at MMIO space with attributes based on [A,T]MTypeIoWc.
- See 2.1.4.3.1.1 [Determining Memory Type].

_ccd[1:0]_lthree0_core[7:0]; MSRC001_0113

Bits	Description																
63:48	Reserved.																
47:17	TSegMask[47:17]: TSeg address range mask. Configurable. Reset: 0000_0000h. See Core::X86::Msr::SMMAddr. AccessType: (Core::X86::Msr::HWCR[SmmLock]) ? Read-only : Read-write.																
16:15	Reserved.																
14:12	TMTypeDram: TSeg address range memory type. Configurable. Reset: 0h. Specifies the memory type for SMM accesses to the TSeg range that are directed to DRAM. AccessType: (Core::X86::Msr::HWCR[SmmLock]) ? Read-only : Read-write. ValidValues:																
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>UC or uncacheable.</td></tr> <tr> <td>1h</td><td>WC or write combining.</td></tr> <tr> <td>3h-2h</td><td>Reserved.</td></tr> <tr> <td>4h</td><td>WT or write through.</td></tr> <tr> <td>5h</td><td>WP or write protect.</td></tr> <tr> <td>6h</td><td>WB or write back.</td></tr> <tr> <td>7h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	UC or uncacheable.	1h	WC or write combining.	3h-2h	Reserved.	4h	WT or write through.	5h	WP or write protect.	6h	WB or write back.	7h	Reserved.
Value	Description																
0h	UC or uncacheable.																
1h	WC or write combining.																
3h-2h	Reserved.																
4h	WT or write through.																
5h	WP or write protect.																
6h	WB or write back.																
7h	Reserved.																
11	Reserved.																
10:8	AMTypeDram: ASeg Range Memory Type. Configurable. Reset: 0h. Specifies the memory type for SMM accesses to the ASeg range that are directed to DRAM. AccessType: (Core::X86::Msr::HWCR[SmmLock]) ? Read-only : Read-write.																

ValidValues:	
Value	Description
0h	UC or uncacheable.
1h	WC or write combining.
3h-2h	Reserved.
4h	WT or write through.
5h	WP or write protect.
6h	WB or write back.
7h	Reserved.
7:6	Reserved.
5	TMTypeIoWc: non-SMM TSeg address range memory type. Configurable. Reset: 0. 0=UC (uncacheable). 1=WC (write combining). Specifies the attribute of TSeg accesses that are directed to MMIO space. AccessType: (Core::X86::Msr::HWCR[SmmLock]) ? Read-only : Read-write.
4	AMTypeIoWc: non-SMM ASeg address range memory type. Configurable. Reset: 0. 0=UC (uncacheable). 1=WC (write combining). Specifies the attribute of ASeg accesses that are directed to MMIO space. AccessType: (Core::X86::Msr::HWCR[SmmLock]) ? Read-only : Read-write.
3	TClose: send TSeg address range data accesses to MMIO. Configurable. Reset: 0. 1=When in SMM, direct data accesses in the TSeg address range to MMIO space. See AClose. AccessType: (Core::X86::Msr::HWCR[SmmLock]) ? Read-only : Read-write.
2	AClose: send ASeg address range data accesses to MMIO. Configurable. Reset: 0. 1=When in SMM, direct data accesses in the ASeg address range to MMIO space. [A,T]Close allows the SMI handler to access the MMIO space located in the same address region as the [A,T]Seg. When the SMI handler is finished accessing the MMIO space, it must clear the bit. Failure to do so before resuming from SMM causes the CPU to erroneously read the save state from MMIO space. AccessType: (Core::X86::Msr::HWCR[SmmLock]) ? Read-only : Read-write.
1	TValid: enable TSeg SMM address range. Configurable. Reset: 0. 1=The TSeg address range SMM enabled. AccessType: (Core::X86::Msr::HWCR[SmmLock]) ? Read-only : Read-write.
0	AValid: enable ASeg SMM address range. Configurable. Reset: 0. 1=The ASeg address range SMM enabled. AccessType: (Core::X86::Msr::HWCR[SmmLock]) ? Read-only : Read-write.

MSRC001_0114 [Virtual Machine Control] (Core::X86::Msr::VM_CR)

Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC001_0114

Bits	Description
63:5	Reserved.
4	SvmeDisable: SVM disable. Configurable. Reset: 0. 0=Core::X86::Msr::EFER[SVME] is Read-write. 1=Core::X86::Msr::EFER[SVME] is Read-only, Error-on-write-1. See Lock for the access type of this field. Attempting to set this field when (Core::X86::Msr::EFER[SVME] == 1) causes a #GP fault, regardless of the state of Lock. See the docAPM2 section titled "Enabling SVM" for software use of this field.
3	Lock: SVM lock. Read-only, Volatile. Reset: 0. 0=SvmeDisable is Read-write. 1=SvmeDisable is Read-only. See Core::X86::Msr::SvmLockKey[SvmLockKey] for the condition that causes hardware to clear this field.
2	Reserved.
1	InterceptInit: intercept INIT. Read-write, Volatile. Reset: 0. 0=INIT delivered normally. 1=INIT translated into a SX interrupt. This bit controls how INIT is delivered in host mode. This bit is set by hardware when the SKINIT instruction is executed.
0	Reserved.

MSRC001_0115 [IGNNE] (Core::X86::Msr::IGNNE)

Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC001_0115

Bits	Description
63:1	Reserved.
0	IGNNE: current IGNNE state. Read-write. Reset: 0. This bit controls the current state of the processor internal IGNNE signal.

MSRC001_0117 [Virtual Machine Host Save Physical Address] (Core::X86::Msr::VM_HSAVE_PA)

Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC001_0117

Bits	Description
63:48	Reserved.
47:12	VM_HSAVE_PA: physical address of host save area. Read-write. Reset: 0_0000_0000h. This register contains the physical address of a 4-KB region where VMRUN saves host state and where vm-exit restores host state from. Writing this register causes a #GP if (FFFF_FFFF_Fh >= VM_HSAVE_PA >= FFFD_0000_0h) or if either the TSEG or ASEG regions overlap with the range defined by this register.
11:0	Reserved.

MSRC001_0118 [SVM Lock Key] (Core::X86::Msr::SvmLockKey)

Read-write. Reset: Fixed,0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC001_0118

Bits	Description
63:0	SvmLockKey: SVM lock key. Read-write. Reset: Fixed,0000_0000_0000_0000h. Writes to this register when (Core::X86::Msr::VM_CR[Lock] == 0) modify SvmLockKey. If ((Core::X86::Msr::VM_CR[Lock] == 1) && (SvmLockKey!=0) && (The write value == The value stored in SvmLockKey)) for a write to this register, then hardware updates Core::X86::Msr::VM_CR[Lock] = 0. Reads of this register always return zero.

MSRC001_011B [AVIC Doorbell] (Core::X86::Msr::AvicDoorbell)

Write-only,Error-on-read. Reset: 0000_0000_0000_0000h.

The ApicId is a physical APIC Id; not valid for logical APIC ID.

Enable: (Core::X86::Cpuid::SvmRevFeatIdEdx[AVIC] == 1).

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC001_011B

Bits	Description
63:32	Reserved.
31:0	ApicId: APIC ID [31:0]. Write-only,Error-on-read. Reset: 0000_0000h. The value written must be a valid physical APID_ID.

MSRC001_011E [VM Page Flush] (Core::X86::Msr::VMPAGE_FLUSH)

Write-only,Error-on-read.

Writes to this MSR cause 4KB of encrypted, guest-tagged data to be flushed from caches if present. This MSR is Write-only, and can only be written from ASID=0 code and only if Core::X86::Msr::SYS_CFG[SME] == 1.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC001_011E

Bits	Description
63:12	GuestPhysicalAddr. Write-only,Error-on-read. Reset: X_XXXX_XXXX_XXXXh. Guest physical address of page to flush.
11:0	ASID. Write-only,Error-on-read. Reset: XXXh. ASID to use for flush. This value must be within the legal ASID range indicated by CPUID_Fn8000001F_ECX (Core::X86::Cpuid::SecureEncryptionEcx), and cannot be zero.

MSRC001_0135 [Virtual TOM] (Core::X86::Msr::VIRTUAL_TOM)

Configurable. Reset: 0000_0000_0000_0000h.

Access of Core::X86::Msr::VIRTUAL_TOM in hypervisor mode causes #GP.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC001_0135

Bits	Description
63:52	Reserved.
51:21	VIRTUAL_TOM . Configurable. Reset: 0000_0000h. Guest physical addresses below VIRTUAL_TOM are considered private (C=1) when VIRTUAL_TOM is enabled. Access is AccessType: (SEV_FEATURES[VirtualTom] AND SEV_FEATURES[SNPActive]) ? Read-write : Error-on-read, Error-on-write.
20:0	Reserved.

MSRC001_0140 [OS Visible Work-around Length] (Core::X86::Msr::OSVW_ID_Length)

Read-write. Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC001_0140

Bits	Description
63:16	Reserved.
15:0	OSVWIdLength: OS visible work-around ID length . Read-write. Reset: 0000h. Init: BIOS,0005h. See the Revision Guide for the definition of this field; see 1.2 [Reference Documents].

MSRC001_0141 [OS Visible Work-around Status] (Core::X86::Msr::OSVW_Status)

Read-write. Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC001_0141

Bits	Description
63:0	OsvwStatusBits: OS visible work-around status bits . Read-write. Reset: 0000_0000_0000_0000h. See the Revision Guide for the definition of this field; see 1.2 [Reference Documents].

MSRC001_0200 [Performance Event Select 0] (Core::X86::Msr::PERF_CTL0)

Read-write. Reset: 0000_0000_0000_0000h.

See 2.1.13 [Performance Monitor Counters]. Core::X86::Msr::PERF_LEGACY_CTL0 is an alias of this register.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC001_0200

Bits	Description										
63:42	Reserved.										
41:40	HostGuestOnly: count only host/guest events. Read-write. Reset: 0h. Host/Guest event counter.										
	ValidValues:										
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>Count all events, irrespective of guest/host.</td></tr> <tr> <td>1h</td><td>Count guest events if [SVME] == 1.</td></tr> <tr> <td>2h</td><td>Count host events if [SVME] == 1.</td></tr> <tr> <td>3h</td><td>Count all guest and host events if [SVME] == 1.</td></tr> </table>	Value	Description	0h	Count all events, irrespective of guest/host.	1h	Count guest events if [SVME] == 1.	2h	Count host events if [SVME] == 1.	3h	Count all guest and host events if [SVME] == 1.
Value	Description										
0h	Count all events, irrespective of guest/host.										
1h	Count guest events if [SVME] == 1.										
2h	Count host events if [SVME] == 1.										
3h	Count all guest and host events if [SVME] == 1.										
39:36	Reserved.										
35:32	EventSelect[11:8]. Read-write. Reset: 0h. Performance event select[11:8].										
31:24	CntMask: counter mask. Read-write. Reset: 00h. Controls the number of events counted per clock cycle.										
	ValidValues:										
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>00h</td><td>The corresponding PERF_CTR[5:0] register increments by the number of events occurring in a clock cycle. See 2.1.13.3 [Large Increment per Cycle Events] for events that can increment greater than 15 per cycle.</td></tr> <tr> <td>7Fh-01h</td><td>When Inv == 0, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is greater than or equal to the CntMask value. When Inv == 1, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is less than CntMask value.</td></tr> <tr> <td>FFh-80h</td><td>Reserved.</td></tr> </table>	Value	Description	00h	The corresponding PERF_CTR[5:0] register increments by the number of events occurring in a clock cycle. See 2.1.13.3 [Large Increment per Cycle Events] for events that can increment greater than 15 per cycle.	7Fh-01h	When Inv == 0, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is greater than or equal to the CntMask value. When Inv == 1, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is less than CntMask value.	FFh-80h	Reserved.		
Value	Description										
00h	The corresponding PERF_CTR[5:0] register increments by the number of events occurring in a clock cycle. See 2.1.13.3 [Large Increment per Cycle Events] for events that can increment greater than 15 per cycle.										
7Fh-01h	When Inv == 0, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is greater than or equal to the CntMask value. When Inv == 1, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is less than CntMask value.										
FFh-80h	Reserved.										
23	Inv: invert counter mask. Read-write. Reset: 0. See CntMask.										
22	En: enable performance counter. Read-write. Reset: 0. 1=Performance event counter is enabled. Performance counter enable.										
21	Reserved.										
20	Int: enable APIC interrupt. Read-write. Reset: 0. 1=APIC performance counter LVT interrupt is enabled to generate an interrupt via Core::X86::Apic::PerformanceCounterLvtEntry when the performance counter overflows. APIC interrupt enable.										
19	Reserved.										
18	Edge: edge detect. Read-write. Reset: 0. 0=Level detect. 1=Zero-to-one Edge detect. The edge count mode increments the counter when a transition happens on the monitored event. If the event selected is changed without disabling the counter, an extra edge is falsely detected when the first event is a static 0 and the second event is a static one. To avoid this false edge detection, disable the counter when changing the event and then enable the counter with a second MSR write.										
17:16	OsUserMode: OS and user mode. Read-write. Reset: 0h. OS and user mode counter events.										
	ValidValues:										
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>Count no events.</td></tr> <tr> <td>1h</td><td>Count user events (CPL>0).</td></tr> <tr> <td>2h</td><td>Count OS events (CPL=0).</td></tr> <tr> <td>3h</td><td>Count all events, irrespective of the CPL.</td></tr> </table>	Value	Description	0h	Count no events.	1h	Count user events (CPL>0).	2h	Count OS events (CPL=0).	3h	Count all events, irrespective of the CPL.
Value	Description										
0h	Count no events.										
1h	Count user events (CPL>0).										
2h	Count OS events (CPL=0).										
3h	Count all events, irrespective of the CPL.										

15:8	UnitMask: event qualification. Read-write. Reset: 00h. Each UnitMask bit further specifies or qualifies the event specified by EventSelect. All events selected by UnitMask are simultaneously monitored. Unless otherwise stated, the UnitMask values shown may be combined (logically ORed) to select any desired combination of the sub-events for a given event. In some cases, certain combinations can result in misleading counts, or the UnitMask value is an ordinal rather than a bit mask. These situations are described where applicable, or should be obvious from the event descriptions. For events where no UnitMask table is shown, the UnitMask is Unused.
7:0	EventSelect[7:0]: event select. Read-write. Reset: 00h. EventSelect[11:0] = {EventSelect[11:8], EventSelect[7:0]}. EventSelect specifies the event or event duration in a processor unit to be counted by the corresponding PERF_CTR[5:0] register. The events are specified in 2.1.13.4 [Core Performance Monitor Counters]. Some events are Reserved; when a Reserved event is selected, the results are undefined.

MSRC001_020[1...B] [Performance Event Counter [5:0]] (Core::X86::Msr::PERF_CTR)

Note: When counting events that capable of counting greater than 15 events per cycle (MergeEvent) the even and the corresponding odd PERF_CTR must be paired to appear as a single 64-bit counter. See 2.1.13.3 [Large Increment per Cycle Events].

See Core::X86::Msr::PERF_CTL0..5. Core::X86::Msr::PERF_LEGACY_CTR is an alias of MSRC001_020[7,5,3,1]. Also can be read via x86 instructions RDPMC ECX=[05:00].

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n0; MSRC001_0201

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n1; MSRC001_0203

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n2; MSRC001_0205

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n3; MSRC001_0207

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n4; MSRC001_0209

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n5; MSRC001_020B

Bits	Description
63:48	Reserved.
47:0	CTR. Read-write, Volatile. Reset: 0000_0000_0000h. Performance counter value.

MSRC001_0202 [Performance Event Select 1] (Core::X86::Msr::PERF_CTL1)

Read-write. Reset: 0000_0000_0000_0000h.

See 2.1.13 [Performance Monitor Counters]. Core::X86::Msr::PERF_LEGACY_CTL1 is an alias of this register.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC001_0202

Bits	Description										
63:42	Reserved.										
41:40	HostGuestOnly: count only host/guest events. Read-write. Reset: 0h. Host/Guest event counter.										
	ValidValues:										
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>Count all events, irrespective of guest/host.</td></tr> <tr> <td>1h</td><td>Count guest events if [SVME] == 1.</td></tr> <tr> <td>2h</td><td>Count host events if [SVME] == 1.</td></tr> <tr> <td>3h</td><td>Count all guest and host events if [SVME] == 1.</td></tr> </table>	Value	Description	0h	Count all events, irrespective of guest/host.	1h	Count guest events if [SVME] == 1.	2h	Count host events if [SVME] == 1.	3h	Count all guest and host events if [SVME] == 1.
Value	Description										
0h	Count all events, irrespective of guest/host.										
1h	Count guest events if [SVME] == 1.										
2h	Count host events if [SVME] == 1.										
3h	Count all guest and host events if [SVME] == 1.										
39:36	Reserved.										
35:32	EventSelect[11:8]. Read-write. Reset: 0h. Performance event select[11:8].										
31:24	CntMask: counter mask. Read-write. Reset: 00h. Controls the number of events counted per clock cycle.										
	ValidValues:										
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>00h</td><td>The corresponding PERF_CTR[5:0] register increments by the number of events occurring in a clock cycle. See 2.1.13.3 [Large Increment per Cycle Events] for events that can increment greater than 15 per cycle.</td></tr> <tr> <td>7Fh-01h</td><td>When Inv == 0, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is greater than or equal to the CntMask value. When Inv == 1, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is less than CntMask value.</td></tr> <tr> <td>FFh-80h</td><td>Reserved.</td></tr> </table>	Value	Description	00h	The corresponding PERF_CTR[5:0] register increments by the number of events occurring in a clock cycle. See 2.1.13.3 [Large Increment per Cycle Events] for events that can increment greater than 15 per cycle.	7Fh-01h	When Inv == 0, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is greater than or equal to the CntMask value. When Inv == 1, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is less than CntMask value.	FFh-80h	Reserved.		
Value	Description										
00h	The corresponding PERF_CTR[5:0] register increments by the number of events occurring in a clock cycle. See 2.1.13.3 [Large Increment per Cycle Events] for events that can increment greater than 15 per cycle.										
7Fh-01h	When Inv == 0, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is greater than or equal to the CntMask value. When Inv == 1, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is less than CntMask value.										
FFh-80h	Reserved.										
23	Inv: invert counter mask. Read-write. Reset: 0. See CntMask.										
22	En: enable performance counter. Read-write. Reset: 0. 1=Performance event counter is enabled. Performance counter enable.										
21	Reserved.										
20	Int: enable APIC interrupt. Read-write. Reset: 0. 1=APIC performance counter LVT interrupt is enabled to generate an interrupt via Core::X86::Apic::PerformanceCounterLvtEntry when the performance counter overflows. APIC interrupt enable.										
19	Reserved.										
18	Edge: edge detect. Read-write. Reset: 0. 0=Level detect. 1=Zero-to-one Edge detect. The edge count mode increments the counter when a transition happens on the monitored event. If the event selected is changed without disabling the counter, an extra edge is falsely detected when the first event is a static 0 and the second event is a static one. To avoid this false edge detection, disable the counter when changing the event and then enable the counter with a second MSR write.										
17:16	OsUserMode: OS and user mode. Read-write. Reset: 0h. OS and user mode counter events.										
	ValidValues:										
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>Count no events.</td></tr> <tr> <td>1h</td><td>Count user events (CPL>0).</td></tr> <tr> <td>2h</td><td>Count OS events (CPL=0).</td></tr> <tr> <td>3h</td><td>Count all events, irrespective of the CPL.</td></tr> </table>	Value	Description	0h	Count no events.	1h	Count user events (CPL>0).	2h	Count OS events (CPL=0).	3h	Count all events, irrespective of the CPL.
Value	Description										
0h	Count no events.										
1h	Count user events (CPL>0).										
2h	Count OS events (CPL=0).										
3h	Count all events, irrespective of the CPL.										

15:8	UnitMask: event qualification. Read-write. Reset: 00h. Each UnitMask bit further specifies or qualifies the event specified by EventSelect. All events selected by UnitMask are simultaneously monitored. Unless otherwise stated, the UnitMask values shown may be combined (logically ORed) to select any desired combination of the sub-events for a given event. In some cases, certain combinations can result in misleading counts, or the UnitMask value is an ordinal rather than a bit mask. These situations are described where applicable, or should be obvious from the event descriptions. For events where no UnitMask table is shown, the UnitMask is Unused.
7:0	EventSelect[7:0]: event select. Read-write. Reset: 00h. EventSelect[11:0] = {EventSelect[11:8], EventSelect[7:0]}. EventSelect specifies the event or event duration in a processor unit to be counted by the corresponding PERF_CTR[5:0] register. The events are specified in 2.1.13.4 [Core Performance Monitor Counters]. Some events are Reserved; when a Reserved event is selected, the results are undefined.

MSRC001_0204 [Performance Event Select 2] (Core::X86::Msr::PERF_CTL2)

Read-write. Reset: 0000_0000_0000_0000h.

See 2.1.13 [Performance Monitor Counters]. Core::X86::Msr::PERF_LEGACY_CTL2 is an alias of this register.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC001_0204

Bits	Description										
63:42	Reserved.										
41:40	HostGuestOnly: count only host/guest events. Read-write. Reset: 0h. Host/Guest event counter.										
	ValidValues:										
	<table><tr><th>Value</th><th>Description</th></tr><tr><td>0h</td><td>Count all events, irrespective of guest/host.</td></tr><tr><td>1h</td><td>Count guest events if [SVME] == 1.</td></tr><tr><td>2h</td><td>Count host events if [SVME] == 1.</td></tr><tr><td>3h</td><td>Count all guest and host events if [SVME] == 1.</td></tr></table>	Value	Description	0h	Count all events, irrespective of guest/host.	1h	Count guest events if [SVME] == 1.	2h	Count host events if [SVME] == 1.	3h	Count all guest and host events if [SVME] == 1.
	Value	Description									
	0h	Count all events, irrespective of guest/host.									
	1h	Count guest events if [SVME] == 1.									
2h	Count host events if [SVME] == 1.										
3h	Count all guest and host events if [SVME] == 1.										
39:36	Reserved.										
35:32	EventSelect[11:8]. Read-write. Reset: 0h. Performance event select[11:8].										
31:24	CntMask: counter mask. Read-write. Reset: 00h. Controls the number of events counted per clock cycle.										
	ValidValues:										
	<table><tr><th>Value</th><th>Description</th></tr><tr><td>00h</td><td>The corresponding PERF_CTR[5:0] register increments by the number of events occurring in a clock cycle. See 2.1.13.3 [Large Increment per Cycle Events] for events that can increment greater than 15 per cycle.</td></tr><tr><td>7Fh-01h</td><td>When Inv == 0, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is greater than or equal to the CntMask value. When Inv == 1, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is less than CntMask value.</td></tr><tr><td>FFh-80h</td><td>Reserved.</td></tr></table>	Value	Description	00h	The corresponding PERF_CTR[5:0] register increments by the number of events occurring in a clock cycle. See 2.1.13.3 [Large Increment per Cycle Events] for events that can increment greater than 15 per cycle.	7Fh-01h	When Inv == 0, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is greater than or equal to the CntMask value. When Inv == 1, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is less than CntMask value.	FFh-80h	Reserved.		
	Value	Description									
	00h	The corresponding PERF_CTR[5:0] register increments by the number of events occurring in a clock cycle. See 2.1.13.3 [Large Increment per Cycle Events] for events that can increment greater than 15 per cycle.									
7Fh-01h	When Inv == 0, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is greater than or equal to the CntMask value. When Inv == 1, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is less than CntMask value.										
FFh-80h	Reserved.										
23	Inv: invert counter mask. Read-write. Reset: 0. See CntMask.										
22	En: enable performance counter. Read-write. Reset: 0. 1=Performance event counter is enabled. Performance counter enable.										
21	Reserved.										
20	Int: enable APIC interrupt. Read-write. Reset: 0. 1=APIC performance counter LVT interrupt is enabled to generate an interrupt via Core::X86::Apic::PerformanceCounterLvtEntry when the performance counter overflows. APIC interrupt enable.										
19	Reserved.										
18	Edge: edge detect. Read-write. Reset: 0. 0=Level detect. 1=Zero-to-one Edge detect. The edge count mode increments the counter when a transition happens on the monitored event. If the event selected is changed without disabling the counter, an extra edge is falsely detected when the first event is a static 0 and the second event is a static one. To avoid this false edge detection, disable the counter when changing the event and then enable the counter with a second MSR write.										
17:16	OsUserMode: OS and user mode. Read-write. Reset: 0h. OS and user mode counter events.										
	ValidValues:										
	<table><tr><th>Value</th><th>Description</th></tr><tr><td>0h</td><td>Count no events.</td></tr><tr><td>1h</td><td>Count user events (CPL>0).</td></tr><tr><td>2h</td><td>Count OS events (CPL=0).</td></tr><tr><td>3h</td><td>Count all events, irrespective of the CPL.</td></tr></table>	Value	Description	0h	Count no events.	1h	Count user events (CPL>0).	2h	Count OS events (CPL=0).	3h	Count all events, irrespective of the CPL.
	Value	Description									
	0h	Count no events.									
	1h	Count user events (CPL>0).									
2h	Count OS events (CPL=0).										
3h	Count all events, irrespective of the CPL.										

15:8	UnitMask: event qualification. Read-write. Reset: 00h. Each UnitMask bit further specifies or qualifies the event specified by EventSelect. All events selected by UnitMask are simultaneously monitored. Unless otherwise stated, the UnitMask values shown may be combined (logically ORed) to select any desired combination of the sub-events for a given event. In some cases, certain combinations can result in misleading counts, or the UnitMask value is an ordinal rather than a bit mask. These situations are described where applicable, or should be obvious from the event descriptions. For events where no UnitMask table is shown, the UnitMask is Unused.
7:0	EventSelect[7:0]: event select. Read-write. Reset: 00h. EventSelect[11:0] = {EventSelect[11:8], EventSelect[7:0]}. EventSelect specifies the event or event duration in a processor unit to be counted by the corresponding PERF_CTR[5:0] register. The events are specified in 2.1.13.4 [Core Performance Monitor Counters]. Some events are Reserved; when a Reserved event is selected, the results are undefined.

MSRC001_0206 [Performance Event Select 3] (Core::X86::Msr::PERF_CTL3)

Read-write. Reset: 0000_0000_0000_0000h.

See 2.1.13 [Performance Monitor Counters]. Core::X86::Msr::PERF_LEGACY_CTL3 is an alias of this register.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC001_0206

Bits	Description
63:42	Reserved.
41:40	HostGuestOnly: count only host/guest events. Read-write. Reset: 0h. Host/Guest event counter.
ValidValues:	
Value	Description
0h	Count all events, irrespective of guest/host.
1h	Count guest events if [SVME] == 1.
2h	Count host events if [SVME] == 1.
3h	Count all guest and host events if [SVME] == 1.
39:36	Reserved.
35:32	EventSelect[11:8]. Read-write. Reset: 0h. Performance event select[11:8].
31:24	CntMask: counter mask. Read-write. Reset: 00h. Controls the number of events counted per clock cycle.
ValidValues:	
Value	Description
00h	The corresponding PERF_CTR[5:0] register increments by the number of events occurring in a clock cycle. See 2.1.13.3 [Large Increment per Cycle Events] for events that can increment greater than 15 per cycle.
7Fh-01h	When Inv == 0, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is greater than or equal to the CntMask value. When Inv == 1, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is less than CntMask value.
FFh-80h	Reserved.
23	Inv: invert counter mask. Read-write. Reset: 0. See CntMask.
22	En: enable performance counter. Read-write. Reset: 0. 1=Performance event counter is enabled. Performance counter enable.
21	Reserved.
20	Int: enable APIC interrupt. Read-write. Reset: 0. 1=APIC performance counter LVT interrupt is enabled to generate an interrupt via Core::X86::Apic::PerformanceCounterLvtEntry when the performance counter overflows. APIC interrupt enable.
19	Reserved.
18	Edge: edge detect. Read-write. Reset: 0. 0=Level detect. 1=Zero-to-one Edge detect. The edge count mode increments the counter when a transition happens on the monitored event. If the event selected is changed without disabling the counter, an extra edge is falsely detected when the first event is a static 0 and the second event is a static one. To avoid this false edge detection, disable the counter when changing the event and then enable the counter with a second MSR write.
17:16	OsUserMode: OS and user mode. Read-write. Reset: 0h. OS and user mode counter events.
ValidValues:	
Value	Description
0h	Count no events.
1h	Count user events (CPL>0).
2h	Count OS events (CPL=0).
3h	Count all events, irrespective of the CPL.

15:8	UnitMask: event qualification. Read-write. Reset: 00h. Each UnitMask bit further specifies or qualifies the event specified by EventSelect. All events selected by UnitMask are simultaneously monitored. Unless otherwise stated, the UnitMask values shown may be combined (logically ORed) to select any desired combination of the sub-events for a given event. In some cases, certain combinations can result in misleading counts, or the UnitMask value is an ordinal rather than a bit mask. These situations are described where applicable, or should be obvious from the event descriptions. For events where no UnitMask table is shown, the UnitMask is Unused.
7:0	EventSelect[7:0]: event select. Read-write. Reset: 00h. EventSelect[11:0] = {EventSelect[11:8], EventSelect[7:0]}. EventSelect specifies the event or event duration in a processor unit to be counted by the corresponding PERF_CTR[5:0] register. The events are specified in 2.1.13.4 [Core Performance Monitor Counters]. Some events are Reserved; when a Reserved event is selected, the results are undefined.

MSRC001_0208 [Performance Event Select 4] (Core::X86::Msr::PERF_CTL4)

Read-write. Reset: 0000_0000_0000_0000h.

See 2.1.13 [Performance Monitor Counters].

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC001_0208

Bits	Description										
63:42	Reserved.										
41:40	HostGuestOnly: count only host/guest events. Read-write. Reset: 0h. Host/Guest event counters.										
	ValidValues:										
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>Count all events, irrespective of guest/host.</td></tr> <tr> <td>1h</td><td>Count guest events if [SVME] == 1.</td></tr> <tr> <td>2h</td><td>Count host events if [SVME] == 1.</td></tr> <tr> <td>3h</td><td>Count all guest and host events if [SVME] == 1.</td></tr> </table>	Value	Description	0h	Count all events, irrespective of guest/host.	1h	Count guest events if [SVME] == 1.	2h	Count host events if [SVME] == 1.	3h	Count all guest and host events if [SVME] == 1.
Value	Description										
0h	Count all events, irrespective of guest/host.										
1h	Count guest events if [SVME] == 1.										
2h	Count host events if [SVME] == 1.										
3h	Count all guest and host events if [SVME] == 1.										
39:36	Reserved.										
35:32	EventSelect[11:8]. Read-write. Reset: 0h. Performance event select[11:8].										
31:24	CntMask: counter mask. Read-write. Reset: 00h. Controls the number of events counted per clock cycle.										
	ValidValues:										
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>00h</td><td>The corresponding PERF_CTR[5:0] register increments by the number of events occurring in a clock cycle. See 2.1.13.3 [Large Increment per Cycle Events] for events that can increment greater than 15 per cycle.</td></tr> <tr> <td>7Fh-01h</td><td>When Inv == 0, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is greater than or equal to the CntMask value. When Inv == 1, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is less than CntMask value.</td></tr> <tr> <td>FFh-80h</td><td>Reserved.</td></tr> </table>	Value	Description	00h	The corresponding PERF_CTR[5:0] register increments by the number of events occurring in a clock cycle. See 2.1.13.3 [Large Increment per Cycle Events] for events that can increment greater than 15 per cycle.	7Fh-01h	When Inv == 0, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is greater than or equal to the CntMask value. When Inv == 1, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is less than CntMask value.	FFh-80h	Reserved.		
Value	Description										
00h	The corresponding PERF_CTR[5:0] register increments by the number of events occurring in a clock cycle. See 2.1.13.3 [Large Increment per Cycle Events] for events that can increment greater than 15 per cycle.										
7Fh-01h	When Inv == 0, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is greater than or equal to the CntMask value. When Inv == 1, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is less than CntMask value.										
FFh-80h	Reserved.										
23	Inv: invert counter mask. Read-write. Reset: 0. See CntMask.										
22	En: enable performance counter. Read-write. Reset: 0. 1=Performance event counter is enabled. Performance counter enable.										
21	Reserved.										
20	Int: enable APIC interrupt. Read-write. Reset: 0. 1=APIC performance counter LVT interrupt is enabled to generate an interrupt via Core::X86::Apic::PerformanceCounterLvtEntry when the performance counter overflows. APIC interrupt enable.										
19	Reserved.										
18	Edge: edge detect. Read-write. Reset: 0. 0=Level detect. 1=Zero-to-one Edge detect. The edge count mode increments the counter when a transition happens on the monitored event. If the event selected is changed without disabling the counter, an extra edge is falsely detected when the first event is a static 0 and the second event is a static one. To avoid this false edge detection, disable the counter when changing the event and then enable the counter with a second MSR write.										
17:16	OsUserMode: OS and user mode. Read-write. Reset: 0h. OS and user mode counter events.										
	ValidValues:										
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>Count no events.</td></tr> <tr> <td>1h</td><td>Count user events (CPL>0).</td></tr> <tr> <td>2h</td><td>Count OS events (CPL=0).</td></tr> <tr> <td>3h</td><td>Count all events, irrespective of the CPL.</td></tr> </table>	Value	Description	0h	Count no events.	1h	Count user events (CPL>0).	2h	Count OS events (CPL=0).	3h	Count all events, irrespective of the CPL.
Value	Description										
0h	Count no events.										
1h	Count user events (CPL>0).										
2h	Count OS events (CPL=0).										
3h	Count all events, irrespective of the CPL.										

15:8	UnitMask: event qualification. Read-write. Reset: 00h. Each UnitMask bit further specifies or qualifies the event specified by EventSelect. All events selected by UnitMask are simultaneously monitored. Unless otherwise stated, the UnitMask values shown may be combined (logically ORed) to select any desired combination of the sub-events for a given event. In some cases, certain combinations can result in misleading counts, or the UnitMask value is an ordinal rather than a bit mask. These situations are described where applicable, or should be obvious from the event descriptions. For events where no UnitMask table is shown, the UnitMask is Unused.
7:0	EventSelect[7:0]: event select. Read-write. Reset: 00h. EventSelect[11:0] = {EventSelect[11:8], EventSelect[7:0]}. EventSelect specifies the event or event duration in a processor unit to be counted by the corresponding PERF_CTR[5:0] register. The events are specified in 2.1.13.4 [Core Performance Monitor Counters]. Some events are Reserved; when a Reserved event is selected, the results are undefined.

MSRC001_020A [Performance Event Select 5] (Core::X86::Msr::PERF_CTL5)

Read-write. Reset: 0000_0000_0000_0000h.

See 2.1.13 [Performance Monitor Counters].

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC001_020A

Bits	Description										
63:42	Reserved.										
41:40	HostGuestOnly: count only host/guest events. Read-write. Reset: 0h. Host/Guest event counter.										
	ValidValues:										
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>Count all events, irrespective of guest/host.</td></tr> <tr> <td>1h</td><td>Count guest events if [SVME] == 1.</td></tr> <tr> <td>2h</td><td>Count host events if [SVME] == 1.</td></tr> <tr> <td>3h</td><td>Count all guest and host events if [SVME] == 1.</td></tr> </table>	Value	Description	0h	Count all events, irrespective of guest/host.	1h	Count guest events if [SVME] == 1.	2h	Count host events if [SVME] == 1.	3h	Count all guest and host events if [SVME] == 1.
Value	Description										
0h	Count all events, irrespective of guest/host.										
1h	Count guest events if [SVME] == 1.										
2h	Count host events if [SVME] == 1.										
3h	Count all guest and host events if [SVME] == 1.										
39:36	Reserved.										
35:32	EventSelect[11:8]. Read-write. Reset: 0h. Performance event select[11:8].										
31:24	CntMask: counter mask. Read-write. Reset: 00h. Controls the number of events counted per clock cycle.										
	ValidValues:										
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>00h</td><td>The corresponding PERF_CTR[5:0] register increments by the number of events occurring in a clock cycle. See 2.1.13.3 [Large Increment per Cycle Events] for events that can increment greater than 15 per cycle.</td></tr> <tr> <td>7Fh-01h</td><td>When Inv == 0, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is greater than or equal to the CntMask value. When Inv == 1, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is less than CntMask value.</td></tr> <tr> <td>FFh-80h</td><td>Reserved.</td></tr> </table>	Value	Description	00h	The corresponding PERF_CTR[5:0] register increments by the number of events occurring in a clock cycle. See 2.1.13.3 [Large Increment per Cycle Events] for events that can increment greater than 15 per cycle.	7Fh-01h	When Inv == 0, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is greater than or equal to the CntMask value. When Inv == 1, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is less than CntMask value.	FFh-80h	Reserved.		
Value	Description										
00h	The corresponding PERF_CTR[5:0] register increments by the number of events occurring in a clock cycle. See 2.1.13.3 [Large Increment per Cycle Events] for events that can increment greater than 15 per cycle.										
7Fh-01h	When Inv == 0, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is greater than or equal to the CntMask value. When Inv == 1, the corresponding PERF_CTR[5:0] register increments by 1, if the number of events occurring in a clock cycle is less than CntMask value.										
FFh-80h	Reserved.										
23	Inv: invert counter mask. Read-write. Reset: 0. See CntMask.										
22	En: enable performance counter. Read-write. Reset: 0. 1=Performance event counter is enabled. Performance counter enable.										
21	Reserved.										
20	Int: enable APIC interrupt. Read-write. Reset: 0. 1=APIC performance counter LVT interrupt is enabled to generate an interrupt via Core::X86::Apic::PerformanceCounterLvtEntry when the performance counter overflows. APIC interrupt enable.										
19	Reserved.										
18	Edge: edge detect. Read-write. Reset: 0. 0=Level detect. 1=Zero-to-one Edge detect. The edge count mode increments the counter when a transition happens on the monitored event. If the event selected is changed without disabling the counter, an extra edge is falsely detected when the first event is a static 0 and the second event is a static one. To avoid this false edge detection, disable the counter when changing the event and then enable the counter with a second MSR write.										
17:16	OsUserMode: OS and user mode. Read-write. Reset: 0h. OS and user mode counter events.										
	ValidValues:										
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>Count no events.</td></tr> <tr> <td>1h</td><td>Count user events (CPL>0).</td></tr> <tr> <td>2h</td><td>Count OS events (CPL=0).</td></tr> <tr> <td>3h</td><td>Count all events, irrespective of the CPL.</td></tr> </table>	Value	Description	0h	Count no events.	1h	Count user events (CPL>0).	2h	Count OS events (CPL=0).	3h	Count all events, irrespective of the CPL.
Value	Description										
0h	Count no events.										
1h	Count user events (CPL>0).										
2h	Count OS events (CPL=0).										
3h	Count all events, irrespective of the CPL.										

15:8	UnitMask: event qualification. Read-write. Reset: 00h. Each UnitMask bit further specifies or qualifies the event specified by EventSelect. All events selected by UnitMask are simultaneously monitored. Unless otherwise stated, the UnitMask values shown may be combined (logically ORed) to select any desired combination of the sub-events for a given event. In some cases, certain combinations can result in misleading counts, or the UnitMask value is an ordinal rather than a bit mask. These situations are described where applicable, or should be obvious from the event descriptions. For events where no UnitMask table is shown, the UnitMask is Unused.
7:0	EventSelect[7:0]: event select. Read-write. Reset: 00h. EventSelect[11:0] = {EventSelect[11:8], EventSelect[7:0]}. EventSelect specifies the event or event duration in a processor unit to be counted by the corresponding PERF_CTR[5:0] register. The events are specified in 2.1.13.4 [Core Performance Monitor Counters]. Some events are Reserved; when a Reserved event is selected, the results are undefined.

MSRC001_023[0...A] [L3 Performance Event Select [5:0]] (Core::X86::Msr::ChL3PmcCfg)

Read-write. Reset: 0000_0000_0000_0000h.

See 2.1.13.5 [L3 Cache Performance Monitor Counters]

_ccd[1:0]_lthree0_n0; MSRC001_0230

_ccd[1:0]_lthree0_n1; MSRC001_0232

_ccd[1:0]_lthree0_n2; MSRC001_0234

_ccd[1:0]_lthree0_n3; MSRC001_0236

_ccd[1:0]_lthree0_n4; MSRC001_0238

_ccd[1:0]_lthree0_n5; MSRC001_023A

Bits	Description								
63:60	Reserved.								
59:56	ThreadMask. Read-write. Reset: 0h. Controls which of the 2 threads in the selected core are being counted. In non-SMT mode, thread 0 must be selected. One or more threads must be selected unless otherwise specified by the specific L3PMC event. ValidValues: <table> <tr> <th>Bit</th><th>Description</th></tr> <tr> <td>[0]</td><td>Thread 0.</td></tr> <tr> <td>[1]</td><td>Thread 1.</td></tr> <tr> <td>[3:2]</td><td>Reserved.</td></tr> </table>	Bit	Description	[0]	Thread 0.	[1]	Thread 1.	[3:2]	Reserved.
Bit	Description								
[0]	Thread 0.								
[1]	Thread 1.								
[3:2]	Reserved.								
55:51	Reserved.								
50:48	SliceId. Read-write. Reset: 0h. Controls the L3 slice for which events are counted. Unless otherwise noted by the specific L3PMC event, use Core::X86::Msr::ChL3PmcCfg[SliceId] to select an individual slice or Core::X86::Msr::ChL3PmcCfg[EnAllSlices] to select all slices. ValidValues: <table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>7h-0h</td><td><Value> Slice.</td></tr> </table>	Value	Description	7h-0h	<Value> Slice.				
Value	Description								
7h-0h	<Value> Slice.								
47	EnAllCores. Read-write. Reset: 0. 1=Enable counting L3 events for all cores simultaneously.								
46	EnAllSlices. Read-write. Reset: 0. 1=Enable counting L3 events for all 8 L3 slices simultaneously.								
45	Reserved.								
44:42	CoreId. Read-write. Reset: 0h. Controls core for which events are to be counted. See Core::X86::Msr::ChL3PmcCfg[EnAllCores] to count all cores simultaneously. ValidValues: <table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>7h-0h</td><td><Value> CoreId.</td></tr> </table>	Value	Description	7h-0h	<Value> CoreId.				
Value	Description								
7h-0h	<Value> CoreId.								
41:23	Reserved.								
22	Enable: Enable L3 performance counter. Read-write. Reset: 0. 1=Enable.								
21:16	Reserved.								
15:8	UnitMask: event qualification. Read-write. Reset: 00h. Each UnitMask bit further specifies or qualifies the event specified by EventSelect. All events selected by UnitMask are simultaneously monitored. Unless otherwise stated, the UnitMask values shown may be combined (logically ORed) to select any desired combination of the sub-events for a given event. In some cases, certain combinations can result in misleading counts, or the UnitMask value is an ordinal rather than a bit mask. These situations are described where applicable, or should be obvious from the event descriptions. For events where no UnitMask table is shown, the UnitMask is Unused. When selecting an event for which not all UnitMask bits are defined, the undefined UnitMask bits should be set to zero.								
7:0	EventSel. Read-write. Reset: 00h. L3 Event select.								

MSRC001_02[40...5E] [Data Fabric Performance Event Select [3:0]] (Core::X86::Msr::DF_PERF_CTL)

Read-write. Reset: 0000_0000_0000_0000h.

See 2.1.13 [Performance Monitor Counters].

The DF Performance Monitors are shared by all cores/threads in the node. See 2.1.8 [Register Sharing].

_n0; MSRC001_0240

_n1; MSRC001_0242

_n2; MSRC001_0244

_n3; MSRC001_0246

_n4; MSRC001_0248

_n5; MSRC001_024A

_n6; MSRC001_024C

_n7; MSRC001_024E

_n8; MSRC001_0250

_n9; MSRC001_0252

_n10; MSRC001_0254

_n11; MSRC001_0256

_n12; MSRC001_0258

_n13; MSRC001_025A

_n14; MSRC001_025C

_n15; MSRC001_025E

Bits	Description
63:38	Reserved.
37:32	EventSelect[13:8]: performance event select. Read-write. Reset: 00h. Performance event select [13:0]. See EventSelect[7:0].
31:28	Reserved.
27:24	UnitMask[11:8]: event qualification. Read-write. Reset: 0h. Uppper 4 bits of UnitMask. See UnitMask[7:0].
23	Reserved.
22	En: enable performance counter. Read-write. Reset: 0. 1=Performance event counter is enabled.
21:16	Reserved.
15:8	UnitMask[7:0]: event qualification. Read-write. Reset: 00h. Each UnitMask bit further specifies or qualifies the event specified by EventSelect. All events selected by UnitMask are simultaneously monitored.
7:0	EventSelect[7:0]: event select. Read-write. Reset: 00h. This field, along with EventSelect[13:12] and EventSelect[11:8] above, combine to form the 14-bit event select field, EventSelect[13:0]. EventSelect specifies the event or event duration in a processor unit to be counted by the corresponding DF_PERF_CTR[3:0] register. Some events are Reserved; when a Reserved event is selected, the results are undefined.

MSRC001_02[41...5F] [Data Fabric Performance Event Counter [3:0]] (Core::X86::Msr::DF_PERF_CTR)

See Core::X86::Msr::DF_PERF_CTL. Also can be read via x86 instructions RDPMC ECX=[09:06].
The DF Performance Monitors are shared by all cores/threads in the socket.

_n0; MSRC001_0241	
_n1; MSRC001_0243	
_n2; MSRC001_0245	
_n3; MSRC001_0247	
_n4; MSRC001_0249	
_n5; MSRC001_024B	
_n6; MSRC001_024D	
_n7; MSRC001_024F	
_n8; MSRC001_0251	
_n9; MSRC001_0253	
_n10; MSRC001_0255	
_n11; MSRC001_0257	
_n12; MSRC001_0259	
_n13; MSRC001_025B	
_n14; MSRC001_025D	
_n15; MSRC001_025F	
Bits	Description
63:48	Reserved.
47:0	CTR[47:0]: performance counter value[47:0]. Read-write, Volatile. Reset: 0000_0000_0000h. The current value of the event counter.

MSRC001_029A [Core Energy Status] (Core::X86::Msr::CORE_ENERGY_STAT)

Read-only, Volatile. Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]; MSRC001_029A

Bits	Description
63:0	TotalEnergyConsumed. Read-only, Volatile. Reset: 0000_0000_0000_0000h.

MSRC001_02B0 [CPPC Capability 1] (Core::X86::Msr::CpccCapability1)

Collaborative Processor Performance Control Capability 1.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC001_02B0

Bits	Description
63:32	Reserved.
31:24	HighestPerf: Highest Performance. Read-only, Error-on-write, Volatile. Reset: 00h. Value for the maximum non-ensured performance level.
23:16	NominalPerf: Nominal Performance. Read-only, Error-on-write, Volatile. Reset: 00h. Value for the maximum sustained performance level assuming ideal operating conditions.
15:8	LowNonLinPerf: Lowest Nonlinear Performance. Read-only, Error-on-write, Volatile. Reset: 00h. Value for the lowest nonlinear performance level.
7:0	LowestPerf: Lowest Performance. Read-only, Error-on-write, Volatile. Reset: 00h. Value for the lowest performance level that software can program to MSR_CPPC_REQUEST.

MSRC001_02B1 [CPPC Enable] (Core::X86::Msr::CpccEnable)

Collaborative Processor Performance Control Enable.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC001_02B1

Bits	Description
63:1	Reserved.
0	CpccEnable. Read, Write-1-only. Reset: 0. CPPC Enable.

MSRC001_02B3 [CPPC Request] (Core::X86::Msrr::CpccRequest)

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC001_02B3

Bits	Description
63:32	Reserved.
31:24	EnergyPerfPref. Read-write. Reset: 00h. Energy Performance Preference.
23:16	DesPerf. Read-write. Reset: 00h. Desired Performance.
15:8	MinPerf. Read-write. Reset: 00h. Minimum Performance.
7:0	MaxPerf. Read-write. Reset: 00h. Maximum Performance.

MSRC001_02B4 [CPPC Status] (Core::X86::Msrr::CpccStatus)

Reset: 0000_0000_0000_0000h.

Collaborative Processor Performance Control Status.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC001_02B4

Bits	Description
63:2	Reserved.
1	MINEXCURSION. Read-write, Volatile. Reset: 0. 1=Minimum Excursion has occurred.
0	Reserved.

MSRC001_02F0 [Protected Processor Inventory Number Control] (Core::X86::Msrr::PPIN_CTL)

Unpredictable.

MSRC001_02F0

Bits	Description
63:2	Reserved.
1	PPIN_EN. Unpredictable. Reset: X. 0=Reading Core::X86::Msrr::PPIN will cause a #GP. 1=Core::X86::Msrr::PPIN is accessible using RDMSR. Once set, attempting to write 1 to Core::X86::Msrr::PPIN_CTL[Lockout] will cause a #GP.
0	Lockout. Unpredictable. Reset: X. 0=Writes to Core::X86::Msrr::PPIN_CTL are permitted if PPIN_EN=0. 1=Further writes to Core::X86::Msrr::PPIN_CTL are ignored. Description: Writing 1 to Core::X86::Msrr::PPIN_CTL[Lockout] is permitted only if Core::X86::Msrr::PPIN_CTL[PPIN_EN] == 0. BIOS should provide an opt-in menu to enable the user to turn on Core::X86::Msrr::PPIN_CTL[PPIN_EN] for privileged inventory initialization agent to access Core::X86::Msrr::PPIN. After reading Core::X86::Msrr::PPIN, the privileged inventory initialization agent should write 00b followed by 01b to Core::X86::Msrr::PPIN_CTL to disable further access to MSR_PPIN and prevent unauthorized modification to MSR_PPIN_CTL. Once this bit is written with 1, subsequent writes to this register are ignored, and a reset (warm or cold) is required in order to clear it, which gives BIOS the opportunity to set it again at the next boot.

MSRC001_02F1 [Protected Processor Inventory Number] (Core::X86::Msrr::PPIN)

MSRC001_02F1

Bits	Description
63:0	PPIN. Reset: Fixed, XXXX_XXXX_XXXX_XXXXh. Protected Processor Inventory Number. AccessType: ({Core::X86::Msrr::PPIN_CTL[PPIN_EN] , Core::X86::Msrr::PPIN_CTL[Lockout]} == 2h) ? Read, Error-on-write : Error-on-read, Error-on-write.

MSRC001_03[00...1E] [LBR V2 Branch From] (Core::X86::Msr::LBR_FROM_V2)

Reset: 0000_0000_0000_0000h.

These MSRs capture the branch from IP when LBR V2 is enabled (see Core::X86::Msr::DbgExtnCfg[LBRV2EN]). The youngest branch is in LBR_FROM_V2_00 and the oldest branch is in LBR_FROM_V2_15.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n0; MSRC001_0300

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n1; MSRC001_0302

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n2; MSRC001_0304

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n3; MSRC001_0306

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n4; MSRC001_0308

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n5; MSRC001_030A

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n6; MSRC001_030C

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n7; MSRC001_030E

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n8; MSRC001_0310

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n9; MSRC001_0312

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n10; MSRC001_0314

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n11; MSRC001_0316

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n12; MSRC001_0318

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n13; MSRC001_031A

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n14; MSRC001_031C

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n15; MSRC001_031E

Bits	Description
63	Mispredict. Read-write. Reset: 0. Indicates if the recorded branch mispredicted.
62:58	BranchFromIpSignExt. Read-write, Volatile. Reset: 00h. Sign extension of BranchFromIp.
57:0	BranchFromIp. Read-write, Volatile. Reset: 000_0000_0000_0000h. Either the lower 63b of the branch segment offset or the segment offset of an instruction preceding the branch. If the segment offset recorded is not the start of the branch instruction, it is the start of a non-branch instruction up to 16 bytes before the end of the branch instruction. The next branch in the sequential path after this instruction is the branch for this LBR Stack entry. Not recording the segment offset of the branch is the result of instruction fusion. If it is desired that BranchFromIp always records the address of branches Instruction Fusion needs to be disabled by also enabling Legacy LBR via Core::X86::Msr::DBG_CTL_MSR[LBR].

MSRC001_03[01...1F] [LBR V2 Branch To] (Core::X86::Msr::LBR_TO_V2)

Reset: 0000_0000_0000_0000h.

These MSRs capture the branch to IP and additional information when LBR V2 is enabled (see Core::X86::Msr::DbgExtnCfg[LBRV2EN]). The youngest branch is in LBR_TO_V2_00 and the oldest branch is in LBR_TO_V2_15.

The following table shows the types of branch records based on the Valid and Spec bits:

Valid	Spec	Description
1	0	Normal recorded branch.
1	1	Branch was recorded when speculative performance feature was active.
0	1	Branch was recorded but speculative feature was not successful.
0	0	No branch has yet been logged in this entry since software last cleared this MSR by writing 0.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n0; MSRC001_0301

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n1; MSRC001_0303

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n2; MSRC001_0305

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n3; MSRC001_0307

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n4; MSRC001_0309

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n5; MSRC001_030B

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n6; MSRC001_030D

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n7; MSRC001_030F

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n8; MSRC001_0311

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n9; MSRC001_0313

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n10; MSRC001_0315

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n11; MSRC001_0317

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n12; MSRC001_0319

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n13; MSRC001_031B

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n14; MSRC001_031D

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_n15; MSRC001_031F

Bits	Description
63	Valid. Read-write. Reset: 0. The valid bit is cleared when the branch was speculatively recorded by the hardware but eventually discarded. Valid LastBranchFrom/To entries have this bit set.
62	Spec: Speculative. Read-write. Reset: 0. When set, the entry was written speculatively .
61	Reserved.
60:58	BranchToIpSignExt. Read-write, Volatile. Reset: 0h. Sign extension of BranchToIp.
57:0	BranchToIp. Read-write, Volatile. Reset: 000_0000_0000_0000h. Lower 58b of the branch target code segment offset.

MSRC001_08[00...7E] [UMC Performance Monitor Control] (Core::X86::MsR::UMC_PerfMonCtl)

Read-write. Reset: 0000_0000_0000_0000h.

These MSRs provide access to the UMC Performance Monitor Control registers. Refer to Core::X86::Cpuid::ExtPerfMonAndDbgEbx[NumPerfCtrUmc] and Core::X86::Cpuid::ExtPerfMonAndDbgEcx[ActiveUmcMask] for the number of available UMC PMCs and the number of PMCs per UMC. MSRs belonging to non-existent UMC Performance Monitors return zero when read and ignore writes. Reserved bits must be set to 0 for reliable results.

_n0; MSRC001_0800

_n1; MSRC001_0802

_n2; MSRC001_0804

_n3; MSRC001_0806

_n4; MSRC001_0808

_n5; MSRC001_080A

_n6; MSRC001_080C

_n7; MSRC001_080E

_n8; MSRC001_0810

_n9; MSRC001_0812

_n10; MSRC001_0814

_n11; MSRC001_0816

_n12; MSRC001_0818

_n13; MSRC001_081A

_n14; MSRC001_081C

_n15; MSRC001_081E

_n16; MSRC001_0820

_n17; MSRC001_0822

_n18; MSRC001_0824

_n19; MSRC001_0826

_n20; MSRC001_0828

_n21; MSRC001_082A

_n22; MSRC001_082C

_n23; MSRC001_082E

_n24; MSRC001_0830

_n25; MSRC001_0832

_n26; MSRC001_0834

_n27; MSRC001_0836

_n28; MSRC001_0838

_n29; MSRC001_083A

_n30; MSRC001_083C

_n31; MSRC001_083E

_n32; MSRC001_0840

_n33; MSRC001_0842

_n34; MSRC001_0844

_n35; MSRC001_0846

_n36; MSRC001_0848

_n37; MSRC001_084A

_n38; MSRC001_084C

_n39; MSRC001_084E

_n40; MSRC001_0850

_n41; MSRC001_0852

_n42; MSRC001_0854

_n43; MSRC001_0856

_n44; MSRC001_0858

_n45; MSRC001_085A

_n46; MSRC001_085C

_n47; MSRC001_085E

_n48; MSRC001_0860

_n49; MSRC001_0862

_n50; MSRC001_0864

_n51; MSRC001_0866

_n52; MSRC001_0868

_n53; MSRC001_086A

_n54; MSRC001_086C

_n55; MSRC001_086E

_n56; MSRC001_0870		
_n57; MSRC001_0872		
_n58; MSRC001_0874		
_n59; MSRC001_0876		
_n60; MSRC001_0878		
_n61; MSRC001_087A		
_n62; MSRC001_087C		
_n63; MSRC001_087E		
Bits	Description	
63:32	Reserved.	
31	Enable. Read-write. Reset: 0. 0=Disable. 1=Enable. Counter enable.	
30:10	Reserved.	
9:8	RdWrMask. Read-write. Reset: 0h. Mask transactions based on read or write.	
	ValidValues:	
	Value	Description
	0h	No masking, includes reads and writes.
	1h	Mask writes.
	2h	Mask reads.
	3h	Reserved.
7:0	EventSelect. Read-write. Reset: 00h. Select the performance monitor event.	

MSRC001_08[01...7F] [UMC Performance Monitor Counter] (Core::X86::Msr::UMC_PerfMonCntr)

Read-write. Reset: 0000_0000_0000_0000h.

These MSRs provide access to the UMC Performance Monitor Counter registers. Refer to Core::X86::Cpuid::ExtPerfMonAndDbgEbx[NumPerfCtrUmc] and Core::X86::Cpuid::ExtPerfMonAndDbgEcx[ActiveUmcMask] for the number of available UMC PMCs and the number of PMCs per UMC. MSRs belonging to non-existent UMC Performance Monitors return zero when read and ignore writes.

_n0; MSRC001_0801

_n1; MSRC001_0803

_n2; MSRC001_0805

_n3; MSRC001_0807

_n4; MSRC001_0809

_n5; MSRC001_080B

_n6; MSRC001_080D

_n7; MSRC001_080F

_n8; MSRC001_0811

_n9; MSRC001_0813

_n10; MSRC001_0815

_n11; MSRC001_0817

_n12; MSRC001_0819

_n13; MSRC001_081B

_n14; MSRC001_081D

_n15; MSRC001_081F

_n16; MSRC001_0821

_n17; MSRC001_0823

_n18; MSRC001_0825

_n19; MSRC001_0827

_n20; MSRC001_0829

_n21; MSRC001_082B

_n22; MSRC001_082D

_n23; MSRC001_082F

_n24; MSRC001_0831

_n25; MSRC001_0833

_n26; MSRC001_0835

_n27; MSRC001_0837

_n28; MSRC001_0839

_n29; MSRC001_083B

_n30; MSRC001_083D

_n31; MSRC001_083F

_n32; MSRC001_0841

_n33; MSRC001_0843

_n34; MSRC001_0845

_n35; MSRC001_0847

_n36; MSRC001_0849

_n37; MSRC001_084B

_n38; MSRC001_084D

_n39; MSRC001_084F

_n40; MSRC001_0851

_n41; MSRC001_0853

_n42; MSRC001_0855

_n43; MSRC001_0857

_n44; MSRC001_0859

_n45; MSRC001_085B

_n46; MSRC001_085D

_n47; MSRC001_085F

_n48; MSRC001_0861

_n49; MSRC001_0863

_n50; MSRC001_0865

_n51; MSRC001_0867

_n52; MSRC001_0869

_n53; MSRC001_086B

_n54; MSRC001_086D

_n55; MSRC001_086F

_n56; MSRC001_0871	
_n57; MSRC001_0873	
_n58; MSRC001_0875	
_n59; MSRC001_0877	
_n60; MSRC001_0879	
_n61; MSRC001_087B	
_n62; MSRC001_087D	
_n63; MSRC001_087F	
Bits	Description
63:49	Reserved.
48	Overflow. Read-write. Reset: 0. Performance Counter Overflow bit. Write-0-to-clear.
47:0	Data. Read-write. Reset: 0000_0000_0000h. Performance Counter Value.

2.1.12.4 MSRs - MSRC001_1xxx

MSRC001_1003 [Thermal and Power Management CPUID Features] (Core::X86::Msr::CPUID_PWR_THERM)

Read-write.	
Core::X86::Msr::CPUID_PWR_THERM provides control over values read from Core::X86::CpuId::ThermalPwrMgmtEcx.	
_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC001_1003	
Bits	Description
63:1	Reserved.
0	EffFreq. Read-write. Reset: Core::X86::CpuId::ThermalPwrMgmtEcx[EffFreq]. See Core::X86::CpuId::ThermalPwrMgmtEcx[EffFreq].

MSRC001_1004 [CPUID Features for CPUID Fn00000001_E[C,D]X] (Core::X86::Msr::CPUID_Features)

Read-write.

Core::X86::Msr::CPUID_Features[63:32] provides control over values read from Core::X86::Cpuid::FeatureIdEcX;
Core::X86::Msr::CPUID_Features[31:0] provides control over values read from Core::X86::Cpuid::FeatureIdEdX.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC001_1004

Bits	Description
63	Reserved.
62	RDRAND . Read-write. Reset: Core::X86::Cpuid::FeatureIdEcX[RDRAND]. See Core::X86::Cpuid::FeatureIdEcX[RDRAND].
61	F16C . Read-write. Reset: Core::X86::Cpuid::FeatureIdEcX[F16C]. See Core::X86::Cpuid::FeatureIdEcX[F16C].
60	AVX . Read-write. Reset: Core::X86::Cpuid::FeatureIdEcX[AVX]. See Core::X86::Cpuid::FeatureIdEcX[AVX].
59	OSXSAVE . Read-write. Reset: Core::X86::Cpuid::FeatureIdEcX[OSXSAVE]. Modifies Core::X86::Cpuid::FeatureIdEcX[OSXSAVE] only if CR4[OSXSAVE].
58	XSAVE . Read-write. Reset: Core::X86::Cpuid::FeatureIdEcX[XSAVE]. See Core::X86::Cpuid::FeatureIdEcX[XSAVE].
57	AES . Read-write. Reset: Core::X86::Cpuid::FeatureIdEcX[AES]. Modifies Core::X86::Cpuid::FeatureIdEcX[AES] only if the reset value is 1 .
56	Reserved.
55	POPCNT . Read-write. Reset: Core::X86::Cpuid::FeatureIdEcX[POPCNT]. See Core::X86::Cpuid::FeatureIdEcX[POPCNT].
54	MOVBE . Read-write. Reset: Core::X86::Cpuid::FeatureIdEcX[MOVBE]. See Core::X86::Cpuid::FeatureIdEcX[MOVBE].
53	X2APIC . Read-write. Reset: Core::X86::Cpuid::FeatureIdEcX[X2APIC]. See Core::X86::Cpuid::FeatureIdEcX[X2APIC].
52	SSE42 . Read-write. Reset: Core::X86::Cpuid::FeatureIdEcX[SSE42]. See Core::X86::Cpuid::FeatureIdEcX[SSE42].
51	SSE41 . Read-write. Reset: Core::X86::Cpuid::FeatureIdEcX[SSE41]. See Core::X86::Cpuid::FeatureIdEcX[SSE41].
50	Reserved.
49	PCID . Read-write. Reset: Core::X86::Cpuid::FeatureIdEcX[PCID]. See Core::X86::Cpuid::FeatureIdEcX[PCID].
48:46	Reserved.
45	CMPXCHG16B . Read-write. Reset: Core::X86::Cpuid::FeatureIdEcX[CMPXCHG16B]. See Core::X86::Cpuid::FeatureIdEcX[CMPXCHG16B].
44	FMA . Read-write. Reset: Core::X86::Cpuid::FeatureIdEcX[FMA]. See Core::X86::Cpuid::FeatureIdEcX[FMA].
43:42	Reserved.
41	SSSE3 . Read-write. Reset: Core::X86::Cpuid::FeatureIdEcX[SSSE3]. See Core::X86::Cpuid::FeatureIdEcX[SSSE3].
40:36	Reserved.
35	Monitor . Read-write. Reset: Core::X86::Cpuid::FeatureIdEcX[Monitor]. Modifies Core::X86::Cpuid::FeatureIdEcX[Monitor] only if ~Core::X86::Msr::HWCR[MonMwaitDis].
34	Reserved.
33	PCLMULQDQ . Read-write. Reset: Core::X86::Cpuid::FeatureIdEcX[PCLMULQDQ]. Modifies Core::X86::Cpuid::FeatureIdEcX[PCLMULQDQ] only if the reset value is 1.
32	SSE3 . Read-write. Reset: Core::X86::Cpuid::FeatureIdEcX[SSE3]. See Core::X86::Cpuid::FeatureIdEcX[SSE3].
31:29	Reserved.
28	HTT . Read-write. Reset: Core::X86::Cpuid::FeatureIdEdX[HTT]. See Core::X86::Cpuid::FeatureIdEdX[HTT].
27	Reserved.
26	SSE2 . Read-write. Reset: Core::X86::Cpuid::FeatureIdEdX[SSE2]. See Core::X86::Cpuid::FeatureIdEdX[SSE2].
25	SSE . Read-write. Reset: Core::X86::Cpuid::FeatureIdEdX[SSE]. See Core::X86::Cpuid::FeatureIdEdX[SSE].

24	FXSR . Read-write. Reset: Core::X86::Cpuid::FeatureIdEdx[FXSR]. See Core::X86::Cpuid::FeatureIdEdx[FXSR].
23	MMX: MMX instructions . Read-write. Reset: Core::X86::Cpuid::FeatureIdEdx[MMX]. See Core::X86::Cpuid::FeatureIdEdx[MMX].
22:20	Reserved.
19	CLFSH . Read-write. Reset: Core::X86::Cpuid::FeatureIdEdx[CLFSH]. See Core::X86::Cpuid::FeatureIdEdx[CLFSH].
18	Reserved.
17	PSE36 . Read-write. Reset: Core::X86::Cpuid::FeatureIdEdx[PSE36]. See Core::X86::Cpuid::FeatureIdEdx[PSE36].
16	PAT . Read-write. Reset: Core::X86::Cpuid::FeatureIdEdx[PAT]. See Core::X86::Cpuid::FeatureIdEdx[PAT].
15	CMOV . Read-write. Reset: Core::X86::Cpuid::FeatureIdEdx[CMOV]. See Core::X86::Cpuid::FeatureIdEdx[CMOV].
14	MCA . Read-write. Reset: Core::X86::Cpuid::FeatureIdEdx[MCA]. See Core::X86::Cpuid::FeatureIdEdx[MCA].
13	PGE . Read-write. Reset: Core::X86::Cpuid::FeatureIdEdx[PGE]. See Core::X86::Cpuid::FeatureIdEdx[PGE].
12	MTRR . Read-write. Reset: Core::X86::Cpuid::FeatureIdEdx[MTRR]. See Core::X86::Cpuid::FeatureIdEdx[MTRR].
11	SysEnterSysExit . Read-write. Reset: Core::X86::Cpuid::FeatureIdEdx[SysEnterSysExit]. See Core::X86::Cpuid::FeatureIdEdx[SysEnterSysExit].
10	Reserved.
9	APIC . Read-write. Reset: Core::X86::Cpuid::FeatureIdEdx[APIC]. Modifies Core::X86::Cpuid::FeatureIdEdx[APIC] only if Core::X86::Msr::APIC_BAR[ApicEn].
8	CMPXCHG8B . Read-write. Reset: Core::X86::Cpuid::FeatureIdEdx[CMXCHG8B]. See Core::X86::Cpuid::FeatureIdEdx[CMXCHG8B].
7	MCE . Read-write. Reset: Core::X86::Cpuid::FeatureIdEdx[MCE]. See Core::X86::Cpuid::FeatureIdEdx[MCE].
6	PAE . Read-write. Reset: Core::X86::Cpuid::FeatureIdEdx[PAE]. See Core::X86::Cpuid::FeatureIdEdx[PAE].
5	MSR . Read-write. Reset: Core::X86::Cpuid::FeatureIdEdx[MSR]. See Core::X86::Cpuid::FeatureIdEdx[MSR].
4	TSC . Read-write. Reset: Core::X86::Cpuid::FeatureIdEdx[TSC]. See Core::X86::Cpuid::FeatureIdEdx[TSC].
3	PSE . Read-write. Reset: Core::X86::Cpuid::FeatureIdEdx[PSE]. See Core::X86::Cpuid::FeatureIdEdx[PSE].
2	DE . Read-write. Reset: Core::X86::Cpuid::FeatureIdEdx[DE]. See Core::X86::Cpuid::FeatureIdEdx[DE].
1	VME . Read-write. Reset: Core::X86::Cpuid::FeatureIdEdx[VME]. See Core::X86::Cpuid::FeatureIdEdx[VME].
0	FPU . Read-write. Reset: Core::X86::Cpuid::FeatureIdEdx[FPU]. See Core::X86::Cpuid::FeatureIdEdx[FPU].

MSRC001_1005 [CPUID Features for CPUID Fn80000001_E[C,D]X] (Core::X86::Msr::CPUID_ExtFeatures)

Read-write.

Core::X86::Msr::CPUID_ExtFeatures[63:32] provides control over values read from

Core::X86::Cpuid::FeatureExtIdEcX; Core::X86::Msr::CPUID_ExtFeatures[31:0] provides control over values read from Core::X86::Cpuid::FeatureExtIdEdX.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC001_1005

Bits	Description
63	Reserved.
62	AdMskExtn . Read-write. Reset: Core::X86::Cpuid::FeatureExtIdEcX[AdMskExtn]. See Core::X86::Cpuid::FeatureExtIdEcX[AdMskExtn].
61	MwaitExtended . Read-write. Reset: Core::X86::Cpuid::FeatureExtIdEcX[MwaitExtended]. See Core::X86::Cpuid::FeatureExtIdEcX[MwaitExtended].
60	PerfCtrExtLLC . Read-write. Reset: Core::X86::Cpuid::FeatureExtIdEcX[PerfCtrExtLLC]. See Core::X86::Cpuid::FeatureExtIdEcX[PerfCtrExtLLC].
59	PerfTsc . Read-write. Reset: Core::X86::Cpuid::FeatureExtIdEcX[PerfTsc]. See Core::X86::Cpuid::FeatureExtIdEcX[PerfTsc].
58	DataBreakpointExtension . Read-write. Reset: Core::X86::Cpuid::FeatureExtIdEcX[DataBreakpointExtension]. See Core::X86::Cpuid::FeatureExtIdEcX[DataBreakpointExtension].
57	Reserved.
56	PerfCtrExtDF . Read-write. Reset: Core::X86::Cpuid::FeatureExtIdEcX[PerfCtrExtDF]. See Core::X86::Cpuid::FeatureExtIdEcX[PerfCtrExtDF].
55	PerfCtrExtCore . Read-write. Reset: Core::X86::Cpuid::FeatureExtIdEcX[PerfCtrExtCore]. See Core::X86::Cpuid::FeatureExtIdEcX[PerfCtrExtCore].
54	TopologyExtensions . Read-write. Reset: Core::X86::Cpuid::FeatureExtIdEcX[TopologyExtensions]. See Core::X86::Cpuid::FeatureExtIdEcX[TopologyExtensions].
53:50	Reserved.
49	TCE . Read-write. Reset: Core::X86::Cpuid::FeatureExtIdEcX[TCE]. See Core::X86::Cpuid::FeatureExtIdEcX[TCE].
48	FMA4 . Read-write. Reset: Core::X86::Cpuid::FeatureExtIdEcX[FMA4]. See Core::X86::Cpuid::FeatureExtIdEcX[FMA4].
47	LWP . Read-write. Reset: Core::X86::Cpuid::FeatureExtIdEcX[LWP]. See Core::X86::Cpuid::FeatureExtIdEcX[LWP].
46	Reserved.
45	WDT . Read-write. Reset: Core::X86::Cpuid::FeatureExtIdEcX[WDT]. See Core::X86::Cpuid::FeatureExtIdEcX[WDT].
44	SKINIT . Read-write. Reset: Core::X86::Cpuid::FeatureExtIdEcX[SKINIT]. See Core::X86::Cpuid::FeatureExtIdEcX[SKINIT].
43	XOP . Read-write. Reset: Core::X86::Cpuid::FeatureExtIdEcX[XOP]. See Core::X86::Cpuid::FeatureExtIdEcX[XOP].
42	IBS . Read-write. Reset: Core::X86::Cpuid::FeatureExtIdEcX[IBS]. See Core::X86::Cpuid::FeatureExtIdEcX[IBS].
41	OSVW . Read-write. Reset: Core::X86::Cpuid::FeatureExtIdEcX[OSVW]. See Core::X86::Cpuid::FeatureExtIdEcX[OSVW].
40	ThreeDNowPrefetch . Read-write. Reset: Core::X86::Cpuid::FeatureExtIdEcX[ThreeDNowPrefetch]. See Core::X86::Cpuid::FeatureExtIdEcX[ThreeDNowPrefetch].
39	MisAlignSse . Read-write. Reset: Core::X86::Cpuid::FeatureExtIdEcX[MisAlignSse]. See Core::X86::Cpuid::FeatureExtIdEcX[MisAlignSse].
38	SSE4A . Read-write. Reset: Core::X86::Cpuid::FeatureExtIdEcX[SSE4A]. See Core::X86::Cpuid::FeatureExtIdEcX[SSE4A].

37	ABM. Read-write. Reset: Core::X86::Cpuid::FeatureExtIdEcxC[ABM]. See Core::X86::Cpuid::FeatureExtIdEcxC[ABM].
36	AltMovCr8. Read-write. Reset: Core::X86::Cpuid::FeatureExtIdEcxC[AltMovCr8]. See Core::X86::Cpuid::FeatureExtIdEcxC[AltMovCr8].
35	ExtApicSpace. Read-write. Reset: Core::X86::Cpuid::FeatureExtIdEcxC[ExtApicSpace]. See Core::X86::Cpuid::FeatureExtIdEcxC[ExtApicSpace].
34	SVM. Read-write. Reset: Core::X86::Cpuid::FeatureExtIdEcxC[SVM]. See Core::X86::Cpuid::FeatureExtIdEcxC[SVM].
33	CmpLegacy. Read-write. Reset: Core::X86::Cpuid::FeatureExtIdEcxC[CmpLegacy]. See Core::X86::Cpuid::FeatureExtIdEcxC[CmpLegacy].
32	LahfSahf. Read-write. Reset: Core::X86::Cpuid::FeatureExtIdEcxC[LahfSahf]. See Core::X86::Cpuid::FeatureExtIdEcxC[LahfSahf].
31	ThreeDNow: 3DNow! instructions. Read-write. Reset: Core::X86::Cpuid::FeatureExtIdEdxC[ThreeDNow]. See Core::X86::Cpuid::FeatureExtIdEdxC[ThreeDNow].
30	ThreeDNowExt. Read-write. Reset: Core::X86::Cpuid::FeatureExtIdEdxC[ThreeDNowExt]. See Core::X86::Cpuid::FeatureExtIdEdxC[ThreeDNowExt].
29	LM. Read-write. Reset: Core::X86::Cpuid::FeatureExtIdEdxC[LM]. See Core::X86::Cpuid::FeatureExtIdEdxC[LM].
28	Reserved.
27	RDTSCP. Read-write. Reset: Core::X86::Cpuid::FeatureExtIdEdxC[RDTSCP]. See Core::X86::Cpuid::FeatureExtIdEdxC[RDTSCP].
26	Page1GB. Read-write. Reset: Core::X86::Cpuid::FeatureExtIdEdxC[Page1GB]. See Core::X86::Cpuid::FeatureExtIdEdxC[Page1GB].
25	FFXSR. Read-write. Reset: Core::X86::Cpuid::FeatureExtIdEdxC[FFXSR]. See Core::X86::Cpuid::FeatureExtIdEdxC[FFXSR].
24	FXSR. Read-write. Reset: Core::X86::Cpuid::FeatureExtIdEdxC[FXSR]. See Core::X86::Cpuid::FeatureExtIdEdxC[FXSR].
23	MMX: MMX instructions. Read-write. Reset: Core::X86::Cpuid::FeatureExtIdEdxC[MMX]. See Core::X86::Cpuid::FeatureExtIdEdxC[MMX].
22	MmxExt. Read-write. Reset: Core::X86::Cpuid::FeatureExtIdEdxC[MmxExt]. See Core::X86::Cpuid::FeatureExtIdEdxC[MmxExt].
21	Reserved.
20	NX. Read-write. Reset: Core::X86::Cpuid::FeatureExtIdEdxC[NX]. See Core::X86::Cpuid::FeatureExtIdEdxC[NX].
19:18	Reserved.
17	PSE36. Read-write. Reset: Core::X86::Cpuid::FeatureExtIdEdxC[PSE36]. See Core::X86::Cpuid::FeatureExtIdEdxC[PSE36].
16	PAT. Read-write. Reset: Core::X86::Cpuid::FeatureExtIdEdxC[PAT]. See Core::X86::Cpuid::FeatureExtIdEdxC[PAT].
15	CMOV. Read-write. Reset: Core::X86::Cpuid::FeatureExtIdEdxC[CMOV]. See Core::X86::Cpuid::FeatureExtIdEdxC[CMOV].
14	MCA. Read-write. Reset: Core::X86::Cpuid::FeatureExtIdEdxC[MCA]. See Core::X86::Cpuid::FeatureExtIdEdxC[MCA].
13	PGE. Read-write. Reset: Core::X86::Cpuid::FeatureExtIdEdxC[PGE]. See Core::X86::Cpuid::FeatureExtIdEdxC[PGE].
12	MTRR. Read-write. Reset: Core::X86::Cpuid::FeatureExtIdEdxC[MTRR]. See Core::X86::Cpuid::FeatureExtIdEdxC[MTRR].
11	SysCallSysRet. Read-write. Reset: Core::X86::Cpuid::FeatureExtIdEdxC[SysCallSysRet]. See Core::X86::Cpuid::FeatureExtIdEdxC[SysCallSysRet].
10	Reserved.

9	APIC . Read-write. Reset: Core::X86::Cpuid::FeatureExtIdEdx[APIC]. See Core::X86::Cpuid::FeatureExtIdEdx[APIC].
8	CMPXCHG8B . Read-write. Reset: Core::X86::Cpuid::FeatureExtIdEdx[CMPXCHG8B]. See Core::X86::Cpuid::FeatureExtIdEdx[CMPXCHG8B].
7	MCE . Read-write. Reset: Core::X86::Cpuid::FeatureExtIdEdx[MCE]. See Core::X86::Cpuid::FeatureExtIdEdx[MCE].
6	PAE . Read-write. Reset: Core::X86::Cpuid::FeatureExtIdEdx[PAE]. See Core::X86::Cpuid::FeatureExtIdEdx[PAE].
5	MSR . Read-write. Reset: Core::X86::Cpuid::FeatureExtIdEdx[MSR]. See Core::X86::Cpuid::FeatureExtIdEdx[MSR].
4	TSC . Read-write. Reset: Core::X86::Cpuid::FeatureExtIdEdx[TSC]. See Core::X86::Cpuid::FeatureExtIdEdx[TSC].
3	PSE . Read-write. Reset: Core::X86::Cpuid::FeatureExtIdEdx[PSE]. See Core::X86::Cpuid::FeatureExtIdEdx[PSE].
2	DE . Read-write. Reset: Core::X86::Cpuid::FeatureExtIdEdx[DE]. See Core::X86::Cpuid::FeatureExtIdEdx[DE].
1	VME . Read-write. Reset: Core::X86::Cpuid::FeatureExtIdEdx[VME]. See Core::X86::Cpuid::FeatureExtIdEdx[VME].
0	FPU . Read-write. Reset: Core::X86::Cpuid::FeatureExtIdEdx[FPU]. See Core::X86::Cpuid::FeatureExtIdEdx[FPU].

MSRC001_1019 [Address Mask For DR1 Breakpoint] (Core::X86::Msr::DR1_ADDR_MASK)

Read-write. Reset: 0000_0000_0000_0000h.

Support indicated by Core::X86::Cpuid::FeatureExtIdEc[DataBreakpointExtension].

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC001_1019

Bits	Description
63:32	Reserved.
31:0	AddrMask: mask for DR linear address data breakpoint DR1 . Read-write. Reset: 0000_0000h. 1=Exclude bit into address compare. 0=Include bit into address compare. See Core::X86::Msr::DR1_ADDR_MASK. AddrMask[11:0] qualifies the DR1 linear address instruction breakpoint, allowing the DR1 instruction breakpoint on a range of addresses in memory.

MSRC001_101A [Address Mask For DR2 Breakpoint] (Core::X86::Msr::DR2_ADDR_MASK)

Read-write. Reset: 0000_0000_0000_0000h.

Support indicated by Core::X86::Cpuid::FeatureExtIdEc[DataBreakpointExtension].

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC001_101A

Bits	Description
63:32	Reserved.
31:0	AddrMask: mask for DR linear address data breakpoint DR2 . Read-write. Reset: 0000_0000h. 1=Exclude bit into address compare. 0=Include bit into address compare. See Core::X86::Msr::DR0_ADDR_MASK. AddrMask[11:0] qualifies the DR2 linear address instruction breakpoint, allowing the DR2 instruction breakpoint on a range of addresses in memory.

MSRC001_101B [Address Mask For DR3 Breakpoint] (Core::X86::Msr::DR3_ADDR_MASK)

Read-write. Reset: 0000_0000_0000_0000h.

Support indicated by Core::X86::Cpuid::FeatureExtIdEc[DataBreakpointExtension].

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC001_101B

Bits	Description
63:32	Reserved.
31:0	AddrMask: mask for DR linear address data breakpoint DR3 . Read-write. Reset: 0000_0000h. 1=Exclude bit into address compare. 0=Include bit into address compare. See Core::X86::Msr::DR0_ADDR_MASK. AddrMask[11:0] qualifies the DR3 linear address instruction breakpoint, allowing the DR3 instruction breakpoint on a range of addresses in memory.

MSRC001_1027 [Address Mask For DR0 Breakpoints] (Core::X86::Msr::DR0_ADDR_MASK)

Read-write. Reset: 0000_0000_0000_0000h.

Support for DR0[31:12] is indicated by Core::X86::Cpuid::FeatureExtIdEcx[DataBreakpointExtension]. See Core::X86::Msr::DR1_ADDR_MASK.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC001_1027

Bits	Description
63:32	Reserved.
31:0	DR0: mask for DR0 linear address data breakpoint. Read-write. Reset: 0000_0000h. 1=Exclude bit into address compare. 0=Include bit into address compare. See Core::X86::Msr::DR1_ADDR_MASK. This field qualifies the DR0 linear address data breakpoint, allowing the DR0 data breakpoint on a range of addresses in memory. AddrMask[11:0] qualifies the DR0 linear address instruction breakpoint, allowing the DR0 instruction breakpoint on a range of addresses in memory. DR0[31:12] is only valid for data breakpoints. The legacy DR0 breakpoint function is provided by DR0[31:0] == 0000_0000h). The mask bits are active high. DR0 is always used, and it can be used in conjunction with any debug function that uses DR0.

MSRC001_1030 [IBS Fetch Control] (Core::X86::Msr::IBS_FETCH_CTL)

Reset: 0000_0000_0000_0000h.

See 2.1.14 [Instruction Based Sampling (IBS)].

The IBS fetch sampling engine is described as follows:

- The periodic fetch counter is an internal 20-bit counter:
 - The periodic fetch counter [19:4] is set to IbsFetchCnt[19:4] and the periodic fetch counter [3:0] is set according to IbsRandEn when IbsFetchEn is changed from 0 to 1.
 - It increments for every fetch cycle that completes when IbsFetchEn == 1 and IbsFetchVal == 0.
 - The periodic fetch counter is undefined when IbsFetchEn == 0 or IbsFetchVal == 1.
 - When IbsFetchCnt[19:4] is read it returns the current value of the periodic fetch counter [19:4].
- When the periodic fetch counter reaches {IbsFetchMaxCnt[19:4], 0h} and the selected instruction fetch completes or is aborted:
 - IbsFetchVal is set to 1.
 - Drivers can't assume that IbsFetchCnt[19:4] is 0 when IbsFetchVal == 1.
- The status of the operation is written to the IBS fetch registers (this register, Core::X86::Msr::IBS_FETCH_LINADDR and Core::X86::Msr::IBS_FETCH_PHYSADDR).
- An interrupt is generated as specified by Core::X86::Msr::IBS_CTL. The interrupt service routine associated with this interrupt is responsible for saving the performance information stored in IBS execution registers.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC001_1030

Bits	Description										
63:62	Reserved.										
61	IbsFetchL3Miss: L3 cache miss for the sampled fetch. Read-write, Volatile. Reset: 0. 1=The instruction fetch missed in the L3 Cache on the same CCX.										
60	IbsFetchOcMiss: Op cache miss for the sampled fetch. Read-write, Volatile. Reset: 0. 1=The Op Cache was not able to supply all bytes for the tagged fetch.										
59	IbsL3MissOnly: Only L3 miss samples are reported. Read-write, Volatile. Reset: 0. 1=An IBS interrupt is only created for fetch samples that had an L3 miss; Fetch samples without an L3 miss are discarded and the internal periodic fetch counter is reset to a pseudo random value between 0 and 15. Allows for filtering of Fetch IBS samples based on their L3Miss status.										
58	IbsFetchL2Miss: L2 cache miss for the sampled fetch. Read-write, Volatile. Reset: 0. 1=The instruction fetch missed in the L2 Cache. Qualified by (IbsFetchComp == 1).										
57	IbsRandEn: random instruction fetch tagging enable. Read-write. Reset: 0. 0=Bits[3:0] of the fetch counter are set to 0h when IbsFetchEn is set to start the fetch counter. 1=Bits[3:0] of the fetch counter are randomized when IbsFetchEn is set to start the fetch counter.										
56	IbsL2TlbMiss: instruction cache L2TLB miss. Read-write, Volatile. Reset: 0. 1=The instruction fetch missed in the L2 TLB.										
55	IbsL1TlbMiss: instruction cache L1TLB miss. Read-write, Volatile. Reset: 0. 1=The instruction fetch missed in the L1 TLB.										
54:53	IbsL1TlbPgSz: instruction cache L1TLB page size. Read-write, Volatile. Reset: 0h. Indicates the page size of the translation in the L1 TLB. This field is only valid if IbsPhyAddrValid == 1.										
Valid Values:											
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>4 KB</td></tr> <tr> <td>1h</td><td>2 MB</td></tr> <tr> <td>2h</td><td>1 GB</td></tr> <tr> <td>3h</td><td>16 KB (Coalesced 4 KB pages)</td></tr> </table>	Value	Description	0h	4 KB	1h	2 MB	2h	1 GB	3h	16 KB (Coalesced 4 KB pages)
Value	Description										
0h	4 KB										
1h	2 MB										
2h	1 GB										
3h	16 KB (Coalesced 4 KB pages)										
52	IbsPhyAddrValid: instruction fetch physical address valid. Read-write, Volatile. Reset: 0. 1=The physical address in Core::X86::Msr::IBS_FETCH_PHYSADDR and the IbsL1TlbPgSz field are valid for the instruction fetch.										
51	IbsIcMiss: instruction cache miss. Read-write, Volatile. Reset: 0. 1=The instruction fetch missed in either the instruction cache or the Op Cache.										

50	IbsFetchComp: instruction fetch complete. Read-write, Volatile. Reset: 0. 1=The instruction fetch completed and the data is available for use by the instruction decoder.
49	IbsFetchVal: instruction fetch valid. Read-write, Volatile. Reset: 0. 1=New instruction fetch data available. When this bit is set, the fetch counter stops counting and an interrupt is generated as specified by Core::X86::Msrr::IBS_CTL. This bit must be cleared for the fetch counter to start counting. When clearing this bit, software can write 0000h to IbsFetchCnt[19:4] to start the fetch counter at IbsFetchMaxCnt[19:4].
48	IbsFetchEn: instruction fetch enable. Read-write. Reset: 0. 1=Instruction fetch sampling is enabled.
47:32	IbsFetchLat: instruction fetch latency. Read-write, Volatile. Reset: 0000h. Indicates the number of clock cycles from when the instruction fetch was initiated to when the data was delivered to the core. If the instruction fetch is abandoned before the fetch completes, this field returns the number of clock cycles from when the instruction fetch was initiated to when the fetch was abandoned.
31:16	IbsFetchCnt[19:4]. Read-write, Volatile. Reset: 0000h. Provides Read/Write access to bits[19:4] of the periodic fetch counter. Programming this field to a value greater than or equal to IbsFetchMaxCnt[19:4] results in undefined behavior.
15:0	IbsFetchMaxCnt[19:4]. Read-write. Reset: 0000h. Specifies bits[19:4] of the maximum count value of the periodic fetch counter. Programming this field to 0000h and setting IbsFetchEn results in undefined behavior. Bits[3:0] of the maximum count are always 0000b.

MSRC001_1031 [IBS Fetch Linear Address] (Core::X86::Msrr::IBS_FETCH_LINADDR)

Read-write, Volatile. Reset: 0000_0000_0000_0000h.

Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC001_1031

Bits	Description
63:0	IbsFetchLinAd: instruction fetch linear address. Read-write, Volatile. Reset: 0000_0000_0000_0000h. Provides the linear address in canonical form for the tagged instruction fetch.

MSRC001_1032 [IBS Fetch Physical Address] (Core::X86::Msrr::IBS_FETCH_PHYSADDR)

Read-write, Volatile. Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC001_1032

Bits	Description
63:48	Reserved.
47:0	IbsFetchPhysAd: instruction fetch physical address. Read-write, Volatile. Reset: 0000_0000_0000h. Provides the physical address for the tagged instruction fetch. The lower 12 bits are not modified by address translation, so they are always the same as the linear address. This field contains valid data only if Core::X86::Msrr::IBS_FETCH_CTL[IbsPhyAddrValid] is asserted. When nested paging is active, the reported physical address is the system physical address. This register reads zero for a guest with active IBS Virtualization.

MSRC001_1033 [IBS Execution Control] (Core::X86::Msr::IBS_OP_CTL)

Reset: 0000_0000_0000_0000h.

See 2.1.14 [Instruction Based Sampling (IBS)].

The IBS execution sampling engine is described as follows for IbsOpCntCtl == 1. If IbsOpCntCtl == 1n then references to "periodic op counter" mean "periodic cycle counter".

- The periodic op counter is an internal 27-bit counter:
 - It is set to IbsOpCurCnt[26:0] when IbsOpEn is changed from 0 to 1.
 - It increments every dispatched macro-op when IbsOpEn == 1 and IbsOpVal == 0.
 - The periodic op counter is undefined when IbsOpEn == 0 or IbsOpVal == 1.
 - When IbsOpCurCnt[26:0] is read then it returns the current value of the periodic op counter [26:0].
- When the periodic op counter reaches IbsOpMaxCnt:
 - The next dispatched op is tagged if IbsOpCntCtl == 1. A valid op in the next dispatched line is tagged if IbsOpCntCtl == 0. See IbsOpCntCtl.
 - The periodic op counter [26:7]=0; [6:0] is randomized by hardware.
- The periodic op counter is not modified when a tagged op is flushed.
- When a tagged op is retired and all sample data has been collected:
 - IbsOpVal is set to 1.
 - Drivers can't assume that IbsOpCurCnt is 0 when IbsOpVal == 1.
- The status of the operation is written to the IBS execution registers (this register, Core::X86::Msr::IBS_OP_RIP, Core::X86::Msr::IBS_OP_DATA, Core::X86::Msr::IBS_OP_DATA2, Core::X86::Msr::IBS_OP_DATA3, Core::X86::Msr::IBS_DC_LINADDR and Core::X86::Msr::IBS_DC_PHYSADDR).
- An interrupt is generated as specified by Core::X86::Msr::IBS_CTL. The interrupt service routine associated with this interrupt is responsible for saving the performance information stored in IBS execution registers.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC001_1033

Bits	Description						
63:59	Reserved.						
58:32	IbsOpCurCnt[26:0]: periodic op counter current count. Read-write, Volatile. Reset: 000_0000h. Returns the current value of the periodic op counter.						
31:27	Reserved.						
26:20	IbsOpMaxCnt[26:20]: periodic op counter maximum count. Read-write. Reset: 00h. See IbsOpMaxCnt[19:4].						
19	IbsOpCntCtl: periodic op counter count control. Read-write. Reset: 0. 0=Count clock cycles; a 1-of-4 round-robin counter selects an op in the next dispatch line; if the op pointed to by the round-robin counter is invalid, then the next younger valid op is selected. 1=Count dispatched ops; when a roll-over occurs, the counter is preloaded with a pseudorandom 7 bit value between 1 and 127.						
18	IbsOpVal: op sample valid. Read-write, Volatile. Reset: 0. 1=New instruction execution data available; the periodic op counter is disabled from counting. An interrupt may be generated when this bit is set as specified by Core::X86::Msr::IBS_CTL[LvtOffset].						
17	IbsOpEn: op sampling enable. Read-write. Reset: 0. 1=Instruction execution sampling enabled.						
16	IbsOpL3MissOnly. Read-write. Reset: 0. 1=An IBS interrupt is only created for op samples that had an L3 miss. L3 miss in this context means the data came outside this core's CCX. A hit in another CCX's L3 is considered an L3 miss. Op samples that do not have an L3 miss are dropped and IbsOpCurCnt is reset to a pseudo random value between 0 and 127.						
15:0	IbsOpMaxCnt[19:4]: periodic op counter maximum count. Read-write. Reset: 0000h. IbsOpMaxCnt[26:0] = {IbsOpMaxCnt[26:20], IbsOpMaxCnt[19:4], 0000b}. Specifies maximum count value of the periodic op counter. Bits[3:0] of the maximum count are always 0000b. Valid Values:						
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0008h-0000h</td><td>Reserved.</td></tr> <tr> <td>FFFFh-0009h</td><td><Value> *16 Ops.</td></tr> </table>	Value	Description	0008h-0000h	Reserved.	FFFFh-0009h	<Value> *16 Ops.
Value	Description						
0008h-0000h	Reserved.						
FFFFh-0009h	<Value> *16 Ops.						

MSRC001_1034 [IBS Op RIP] (Core::X86::Msr::IBS_OP_RIP)

Read-write, Volatile. Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC001_1034

Bits	Description
63:0	IbsOpRip . Read-write, Volatile. Reset: 0000_0000_0000_0000h. 64 bit Segment offset (RIP) of the instruction that contains the tagged op.

MSRC001_1035 [IBS Op Data] (Core::X86::Msr::IBS_OP_DATA)

Read-write, Volatile. Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC001_1035

Bits	Description
63:41	Reserved.
40	IbsOpMicrocode . Read-write, Volatile. Reset: 0. 1=Tagged operation from microcode.
39	IbsOpFuse: fused instruction op . Read-write, Volatile. Reset: 0. 1=Tagged operation was part of a fused instruction pair; IBS_OP_RIP reports the RIP of the older instruction within that pair. Support indicated by Core::X86::Cpuid::IbsIdEax[OpFuse].
38	IbsRipInvalid: RIP is invalid . Read-write, Volatile. Reset: 0. 1=Tagged operation RIP is invalid. Support indicated by Core::X86::Cpuid::IbsIdEax[RipInvalidChk].
37	IbsOpBrnRet: branch op retired . Read-write, Volatile. Reset: 0. 1=Tagged operation was a branch op that retired.
36	IbsOpBrnMisp: mispredicted branch op . Read-write, Volatile. Reset: 0. 1=Tagged operation was a branch op that was mispredicted. Qualified by IbsOpBrnRet == 1.
35	IbsOpBrnTaken: taken branch op . Read-write, Volatile. Reset: 0. 1=Tagged operation was a branch op that was taken. Qualified by IbsOpBrnRet == 1.
34	IbsOpReturn: return op . Read-write, Volatile. Reset: 0. 1=Tagged operation was return op. Qualified by (IbsOpBrnRet == 1).
33:32	Reserved.
31:16	IbsTagToRetCtr: op tag to retire count . Read-write, Volatile. Reset: 0000h. This field returns the number of cycles from when the op was tagged to when the op was retired. This field is equal to IbsCompToRetCtr when the tagged op has zero-cycle latency.
15:0	IbsCompToRetCtr: op completion to retire count . Read-write, Volatile. Reset: 0000h. This field returns the number of cycles from when the op was completed to when the op was retired.

MSRC001_1036 [IBS Op Data 2] (Core::X86::Msr::IBS_OP_DATA2)

Reset: 0000_0000_0000_0000h.

Data is only valid for load operations that miss both the L1 data cache and the L2 cache. If a load or store operation crosses a 64B boundary, the data returned in this register may be for either one of the two cache lines that are accessed. This register is not expected to be updated for store operations to non-cacheable memory.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC001_1036

Bits	Description
63:8	Reserved.
7:6	DataSrc[4:3]: northbridge IBS request data source high bits. Read-write, Volatile. Reset: 0h. High order bits for the DataSrc field. See DataSrcLo for a description of the valid values.
5	CacheHitSt: IBS cache hit state. Read-write, Volatile. Reset: 0. 0=M State. 1=O State. Valid when the data source type is a cache.
4	RmtNode: IBS request destination node. Read-write, Volatile. Reset: 0. 0=The request is serviced by the NB in the same node as the core. 1=The request is serviced by the NB in a different node than the core. Valid when DataSrc is non-zero.
3	Reserved.
2:0	DataSrc[2:0]: northbridge IBS request data source low bits. Read-write. Reset: 0h.
Description: Valid Values for {DataSrc[4:3],DataSrc[2:0]:	
Values	Description
0h	No valid status.
1h	Local L3 or other L1/L2 in CCX.
2h	Another CCX cache in the same NUMA node.
3h	DRAM.
4h	Reserved.
5h	Another CCX cache in a different NUMA node.
6h	Long-latency DIMM.
7h	MMIO/Config/PCI/APIC.
8h	Extension Memory.
9h-Bh	Reserved.
Ch	Coherent Memory of a different processor type.
Dh-1Fh	Reserved.

MSRC001_1037 [IBS Op Data 3] (Core::X86::Msr::IBS_OP_DATA3)

Read-write, Volatile. Reset: 0000_0000_0000_0000h.

Data in this register is only valid when either Core::X86::Msr::IBS_OP_DATA3[IbsStOp] or Core::X86::Msr::IBS_OP_DATA3[IbsLdOp] are set. If a load or store operation crosses a 64B boundary, the data returned in this register may be for either one of the two cache lines that are accessed.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC001_1037

Bits	Description																				
63:48	IbsTlbRefillLat: L1 DTLB refill latency. Read-write, Volatile. Reset: 0000h. The number of cycles from when a L1 DTLB refill is triggered by a tagged op to when the L1 DTLB fill has been completed.																				
47:32	IbsDcMissLat: data cache miss latency. Read-write, Volatile. Reset: 0000h. Indicates the number of clock cycles from when a miss is detected in the data cache to when the data was delivered to the core. The value returned by this counter is not valid for data cache Writes or prefetch instructions.																				
31:26	IbsOpDcMissOpenMemReqs: outstanding memory requests on DC fill. Read-write, Volatile. Reset: 00h. The number of allocated, valid DC MABs when the MAB corresponding to a tagged DC miss op is deallocated. Includes the MAB allocated by the sampled op. 00000b=No information provided.																				
25:22	IbsOpMemWidth: load/store size in bytes. Read-write, Volatile. Reset: 0h. Report the number of bytes the load or store is attempting to access. Valid Values:																				
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>No information provided.</td></tr> <tr> <td>1h</td><td>Byte.</td></tr> <tr> <td>2h</td><td>Word.</td></tr> <tr> <td>3h</td><td>DW (4 Bytes).</td></tr> <tr> <td>4h</td><td>QW (8 Bytes).</td></tr> <tr> <td>5h</td><td>OW (16 Bytes).</td></tr> <tr> <td>6h</td><td>32 Bytes.</td></tr> <tr> <td>7h</td><td>64 Bytes.</td></tr> <tr> <td>Fh-8h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	No information provided.	1h	Byte.	2h	Word.	3h	DW (4 Bytes).	4h	QW (8 Bytes).	5h	OW (16 Bytes).	6h	32 Bytes.	7h	64 Bytes.	Fh-8h	Reserved.
Value	Description																				
0h	No information provided.																				
1h	Byte.																				
2h	Word.																				
3h	DW (4 Bytes).																				
4h	QW (8 Bytes).																				
5h	OW (16 Bytes).																				
6h	32 Bytes.																				
7h	64 Bytes.																				
Fh-8h	Reserved.																				
21	IbsSwPf: software prefetch. Read-write, Volatile. Reset: 0. 1=The op is a software prefetch.																				
20	IbsL2Miss: L2 cache miss for the sampled operation. Read-write, Volatile. Reset: 0. 1=The operation missed in the L2, regardless of whether the op initiated the request to the L2. This is not expected to be set for store operations to non-cacheable memory.																				
19	IbsDcL2TlbHit1G: data cache L2TLB hit in 1G page. Read-write, Volatile. Reset: 0. 1=The physical address for the tagged load or store operation was present in a 1G page table entry in the data cache L2TLB.																				
18	IbsDcPhyAddrValid: data cache physical address valid. Read-write, Volatile. Reset: 0. 1=The physical address in Core::X86::Msr::IBS_DC_PHYSADDR is valid for the load or store operation.																				
17	IbsDcLinAddrValid: data cache linear address valid. Read-write, Volatile. Reset: 0. 1=The linear address in Core::X86::Msr::IBS_DC_LINADDR is valid for the load or store operation.																				
16	DcMissNoMabAlloc: DC miss with no MAB allocated. Read-write, Volatile. Reset: 0. 1=The tagged load or store operation hit on an already allocated MAB.																				
15	IbsDcLockedOp: locked operation. Read-write, Volatile. Reset: 0. 1=Tagged load or store operation is a locked operation.																				
14	IbsDcUcMemAcc: UC memory access. Read-write, Volatile. Reset: 0. 1=Tagged load or store operation accessed uncachable memory.																				
13	IbsDcWcMemAcc: WC memory access. Read-write, Volatile. Reset: 0. 1=Tagged load or store operation accessed write combining memory.																				
12:9	Reserved.																				
8	IbsDcMisAcc: misaligned access. Read-write, Volatile. Reset: 0. 1=The tagged load or store operation crosses a 64 byte address boundary.																				

7	IbsDcMiss: data cache miss. Read-write, Volatile. Reset: 0. 1=The cache line used by the tagged load or store was not present in the data cache. This is not expected to be set for store operations to non-cacheable memory.
6	IbsDcL2tlbHit2M: data cache L2TLB hit in 2M page. Read-write, Volatile. Reset: 0. 1=The physical address for the tagged load or store operation was present in a 2M page table entry in the data cache L2TLB.
5	IbsDcL1TlbHit1G: data cache L1TLB hit in 1G page. Read-write, Volatile. Reset: 0. 1=The physical address for the tagged load or store operation was present in a 1G page table entry in the data cache L1TLB.
4	IbsDcL1TlbHit2M: data cache L1TLB hit in 2M page. Read-write, Volatile. Reset: 0. 1=The physical address for the tagged load or store operation was present in a 2M page table entry in the data cache L1TLB.
3	IbsDcL2TlbMiss: data cache L2TLB miss. Read-write, Volatile. Reset: 0. 1=The physical address for the tagged load or store operation was not present in the data cache L2TLB.
2	IbsDcL1tlbMiss: data cache L1TLB miss. Read-write, Volatile. Reset: 0. 1=The physical address for the tagged load or store operation was not present in the data cache L1TLB.
1	IbsStOp: store op. Read-write, Volatile. Reset: 0. 1=Tagged operation is a store operation.
0	IbsLdOp: load op. Read-write, Volatile. Reset: 0. 1=Tagged operation is a load operation.

MSRC001_1038 [IBS DC Linear Address] (Core::X86::Msr::IBS_DC_LINADDR)

Read-write, Volatile. Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC001_1038

Bits	Description
63:0	IbsDcLinAd. Read-write, Volatile. Reset: 0000_0000_0000_0000h. Provides the linear address in canonical form for the tagged load or store operation. This field contains valid data only if Core::X86::Msr::IBS_OP_DATA3[IbsDcLinAddrValid] is asserted.

MSRC001_1039 [IBS DC Physical Address] (Core::X86::Msr::IBS_DC_PHYSADDR)

Read-write, Volatile. Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC001_1039

Bits	Description
63:48	Reserved.
47:0	IbsDcPhysAd: load or store physical address. Read-write, Volatile. Reset: 0000_0000_0000_0000h. Provides the physical address for the tagged load or store operation. The lower 12 bits are not modified by address translation, so they are always the same as the linear address. For memory accesses, that cross a 64B boundary (Core::X86::Msr::IBS_OP_DATA3[IbsDcMisAcc] is set), this field always points to the first cache line for the access. Cache miss related information in Core::X86::Msr::IBS_OP_DATA3 or Core::X86::Msr::IBS_OP_DATA2 will be for one of the two cache lines accessed by the load or store operation. This field contains valid data only if Core::X86::Msr::IBS_OP_DATA3[IbsDcPhyAddrValid] is asserted. When nested paging is active, the reported physical address is the system physical address. This register reads zero for a guest with active IBS Virtualization.

MSRC001_103A [IBS Control] (Core::X86::Msr::IBS_CTL)

Read, Error-on-write.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC001_103A

Bits	Description
63:9	Reserved.
8	LvtOffsetVal: local vector table offset valid. Read, Error-on-write. Reset: X.
7:4	Reserved.
3:0	LvtOffset: local vector table offset. Read, Error-on-write. Reset: Xh.

MSRC001_103B [IBS Branch Target Address] (Core::X86::Msr::BP_IBSTGT_RIP)	
Read-write, Volatile. Reset: 0000_0000_0000_0000h.	
Support for this register indicated by Core::X86::Cpuid::IbsIdEax[BrnTrgt].	
_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC001_103B	
Bits	Description
63:0	IbsBrTarget. Read-write, Volatile. Reset: 0000_0000_0000_0000h. The logical address in canonical form for the branch target. It only contains a valid value for branch instructions (Core::X86::Msr::IBS_OP_DATA[IbsOpBrnRet] == 1).
MSRC001_103C [IBS Fetch Control Extended] (Core::X86::Msr::IC_IBS_EXTD_CTL)	
Read-write, Volatile. Reset: 0000_0000_0000_0000h.	
Support for this register indicated by Core::X86::Cpuid::IbsIdEax[IbsFetchCtlExtd].	
_ccd[1:0]_lthree0_core[7:0]_thread[1:0]; MSRC001_103C	
Bits	Description
63:16	Reserved.
15:0	IbsItlbRefillLat: ITLB Refill Latency for the sampled fetch, if there is a reload. Read-write, Volatile. Reset: 0000h. The number of cycles when the fetch engine is stalled for an ITLB reload for the sampled fetch. If there is no reload, the latency is 0.

2.1.12.5 L3 MSRs - MSRC001_1xxx

See 2.2.1 [L3 MSR Registers].

2.1.13 Performance Monitor Counters

2.1.13.1 RDPMC Assignments

There are six core performance event counters per thread, six performance events counters per L3 complex and sixteen Data Fabric performance events counters mapped to the RDPMC instruction as follows:

- The RDPMC[5:0] instruction accesses core events. See 2.1.13.4 [Core Performance Monitor Counters].
- The RDPMC[9:6, 1B:10] instruction accesses data fabric events.
- The RDPMC[F:A] instruction accesses L3 cache events. See 2.1.13.5 [L3 Cache Performance Monitor Counters].

2.1.13.2 Performance Measurement

This section contains AMD's recommended method for collecting microarchitecture performance common to software optimization. This may require combining multiple performance event selections. Table 18 [Guidance for Common Performance Statistics with Complex Event Selects] lists formulas for collecting common performance statistics.

- The term Event is the full value written to Core::X86::Msr::PERF_CTL0..5.
 - Core PMC select bits [63:36, 31:16] are at the user's discretion, (i.e., they are not part of the event selection).
- The term L3Event is the full value written to Core::X86::Msr::ChL3PmcCfg.
- The term DFEvent is the full value written to Core::X86::Msr::DF_PERF_CTL.

Some UnitMask fields are not disclosed, but may be used by 2.1.13.2 [Performance Measurement].

Table 18: Guidance for Common Performance Statistics with Complex Event Selects

Description	Equation
-------------	----------

Branch Prediction	
Execution-Time Branch Misprediction Ratio (Non-Speculative).	Event[0x4300C3] / Event[0x4300C2]
Basic Caching	
All Data Cache Accesses	Event[0x430729]
All L2 Cache Accesses	Event[0x43F960] + Event[0x431F70] + Event[0x431F71] + Event[0x431F72]
L2 Cache Access from L1 Instruction Cache Miss (including prefetch)	Event[0x431060]
L2 Cache Access from L1 Data Cache Miss (including Prefetch)	Event[0x43E860]
L2 Cache Access from L2 Cache HWPF	Event[0x431F70] + Event[0x431F71] + Event[0x431F72]
All L2 Cache Misses	Event[0x430964] + Event[0x431F71] + Event[0x431F72]
L2 Cache Miss from L1 Instruction Cache Miss	Event[0x430164]
L2 Cache Miss from L1 Data Cache Miss	Event[0x430864]
L2 Cache Miss from L2 Cache HWPF	Event[0x431F71] + Event[0x431F72]
All L2 Cache Hits	Event[0x43f664] + Event[0x431f70]
L2 Cache Hit from L1 Instruction Cache Miss	Event[0x430664]
L2 Cache Hit from L1 Data Cache Miss	Event[0x43F064]
L2 Cache Hit from L2 Cache HWPF	Event[0x431F70]
L3 Cache Accesses	L3Event[0x0300C0000040FF04]
L3 Miss (includes cacheline state change requests)	L3Event[0x0300C00000400104]
Average L3 Cache Read Miss Latency (in core clocks)	L3Event[0x0303C00000403FAC]*10/ L3Event[0x0303C00000403FAD]
Op Cache (64B) Fetch Miss Ratio	Event[0x20043048F] / Event[0x20043078F]
Instruction Cache (32B) Fetch Miss Ratio	Event[0x10043188E] / Event[0x100431F8E]
Advanced Caching	
L1 Data Cache Fills from DRAM or IO in any NUMA node	Event[0x434844]
L1 Data Cache Fills from a different NUMA node	Event[0x435044]
L1 Data Cache Fills from within the same CCX	Event[0x430344]
L1 Data Cache Fills from another CCX cache in any NUMA node	Event[0x431444]
L1 Data Cache Fills All	Event[0x435F44]
Demand L1 Data Cache Fills from local L2	Event[0x430143]
Demand L1 Data Cache Fills from local L3 or different L2 in same CCX	Event[0x430243]
Demand L1 Data Cache Fills from another CCX cache in the same NUMA node	Event[0x430443]
Demand L1 Data Cache Fills from DRAM or MMIO in the same NUMA node	Event[0x430843]
Demand L1 Data Cache Fills from another CCX cache in a different NUMA node	Event[0x431043]
Demand L1 Data Cache Fills from Remote Memory or IO	Event[0x434043]
64B lines written per WCB close	Event[0x431043] / Event[0x432063]
TLBs	
L1 ITLB Misses	Event[0x430084] + Event[0x430785]

L2 ITLB Misses & Instruction page walk	Event[0x430785]
L1 DTLB Misses	Event[0x43FF45]
L2 DTLB Misses & Data page walk	Event[0x43F045]
All TLBs Flushed	Event[0x43FF78]
Stalls	
Macro-ops Dispatched	Event[0x4307AA]
Mixed SSE/AVX Stalls	Event[0x430E0E]
Macro-ops Retired	Event[0x4300C1]
Data Fabric	
DRAM read data bytes for local processor	(DfEvent[0x000000000740FE1F] + DfEvent[0x000000000740FE5F] + DfEvent[0x000000000740FE9F] + DfEvent[0x000000000740FEDF] + DfEvent[0x000000010740FE1F] + DfEvent[0x000000010740FE5F] + DfEvent[0x000000010740FE9F] + DfEvent[0x000000010740FEDF] + DfEvent[0x000000020740FE1F] + DfEvent[0x000000020740FE5F] + DfEvent[0x000000020740FE9F] + DfEvent[0x000000020740FEDF]) * 64B
DRAM write data bytes for local processor	(DfEvent[0x000000000740FF1F] + DfEvent[0x000000000740FF5F] + DfEvent[0x000000000740FF9F] + DfEvent[0x000000000740FFDF] + DfEvent[0x000000010740FF1F] + DfEvent[0x000000010740FF5F] + DfEvent[0x000000010740FF9F] + DfEvent[0x000000010740FFDF] + DfEvent[0x000000020740FF1F] + DfEvent[0x000000020740FF5F] + DfEvent[0x000000020740FF9F] + DfEvent[0x000000020740FFDF]) * 64B
DRAM read data bytes for remote processor	(DfEvent[0x000000000B40FE1F] + DfEvent[0x000000000B40FE5F] + DfEvent[0x000000000B40FE9F] + DfEvent[0x000000000B40FEDF] + DfEvent[0x000000010B40FE1F] + DfEvent[0x000000010B40FE5F] + DfEvent[0x000000010B40FE9F] + DfEvent[0x000000010B40FEDF] + DfEvent[0x000000020B40FE1F] + DfEvent[0x000000020B40FE5F] + DfEvent[0x000000020B40FE9F] + DfEvent[0x000000020B40FEDF]) * 64B
DRAM write data bytes for remote processor	(DfEvent[0x000000000B40FF1F] + DfEvent[0x000000000B40FF5F] + DfEvent[0x000000000B40FF9F] + DfEvent[0x000000000B40FFDF] + DfEvent[0x000000010B40FF1F] + DfEvent[0x000000010B40FF5F] + DfEvent[0x000000010B40FF9F] + DfEvent[0x000000010B40FFDF])

	DfEvent[0x000000010B40FFDF] + DfEvent[0x000000020B40FF1F] + DfEvent[0x000000020B40FF5F] + DfEvent[0x000000020B40FF9F] + DfEvent[0x000000020B40FFDF]) * 64B
Local upstream DMA read data bytes	(DfEvent[0x000000080740FE1F] + DfEvent[0x000000080740FE5F] + DfEvent[0x000000080740FE9F] + DfEvent[0x000000080740FEDF]) * 64B
Local upstream DMA write data bytes	(DfEvent[0x000000080740FF1F] + DfEvent[0x000000080740FF5F] + DfEvent[0x000000080740FF9F] + DfEvent[0x000000080740FFDF]) * 64B
Remote socket upstream DMA read data bytes	(DfEvent[0x000000080B40FE1F] + DfEvent[0x000000080B40FE5F] + DfEvent[0x000000080B40FE9F] + DfEvent[0x000000080B40FEDF]) * 64B
Remote socket upstream DMA write data bytes	(DfEvent[0x000000080B40FF1F] + DfEvent[0x000000080B40FF5F] + DfEvent[0x000000080B40FF9F] + DfEvent[0x000000080B40FFDF]) * 64B
Local inbound data bytes to the CPU (e.g. read data)	(DfEvent[0x000000040740FE1E] + DfEvent[0x000000040740FE1F] + DfEvent[0x000000040740FE5E] + DfEvent[0x000000040740FE5F] + DfEvent[0x000000040740FE9E] + DfEvent[0x000000040740FE9F] + DfEvent[0x000000040740FEDE] + DfEvent[0x000000040740FEDF] + DfEvent[0x000000050740FE1E] + DfEvent[0x000000050740FE1F] + DfEvent[0x000000050740FE5E] + DfEvent[0x000000050740FE5F] + DfEvent[0x000000050740FE9E] + DfEvent[0x000000050740FE9F] + DfEvent[0x000000050740FEDE] + DfEvent[0x000000050740FEDF]) * 32B
Local outbound data bytes from the CPU (e.g. write data)	(DfEvent[0x000000040740FF1E] + DfEvent[0x000000040740FF1F] + DfEvent[0x000000040740FF5E] + DfEvent[0x000000040740FF5F] + DfEvent[0x000000040740FF9E] + DfEvent[0x000000040740FF9F] + DfEvent[0x000000040740FFDE] + DfEvent[0x000000040740FFDF] + DfEvent[0x000000050740FF1E] + DfEvent[0x000000050740FF1F] + DfEvent[0x000000050740FF5E] + DfEvent[0x000000050740FF5F] + DfEvent[0x000000050740FF9E] + DfEvent[0x000000050740FF9F] + DfEvent[0x000000050740FFDE] +

	DfEvent[0x000000050740FFDF]) * 64
Remote socket inbound data bytes to the CPU (e.g. read data)	(DfEvent[0x000000040B40FE1E] + DfEvent[0x000000040B40FE1F] + DfEvent[0x000000040B40FE5E] + DfEvent[0x000000040B40FE5F] + DfEvent[0x000000040B40FE9E] + DfEvent[0x000000040B40FE9F] + DfEvent[0x000000040B40FEDE] + DfEvent[0x000000040B40FEDF] + DfEvent[0x000000050B40FE1E] + DfEvent[0x000000050B40FE1F] + DfEvent[0x000000050B40FE5E] + DfEvent[0x000000050B40FE5F] + DfEvent[0x000000050B40FE9E] + DfEvent[0x000000050B40FE9F] + DfEvent[0x000000050B40FEDE] + DfEvent[0x000000050B40FEDF]) * 32B
Remote socket outbound data bytes from the CPU (e.g. write data)	(DfEvent[0x000000040B40FF1E] + DfEvent[0x000000040B40FF1F] + DfEvent[0x000000040B40FF5E] + DfEvent[0x000000040B40FF5F] + DfEvent[0x000000040B40FF9E] + DfEvent[0x000000040B40FF9F] + DfEvent[0x000000040B40FFDE] + DfEvent[0x000000040B40FFDF] + DfEvent[0x000000050B40FF1E] + DfEvent[0x000000050B40FF1F] + DfEvent[0x000000050B40FF5E] + DfEvent[0x000000050B40FF5F] + DfEvent[0x000000050B40FF9E] + DfEvent[0x000000050B40FF9F] + DfEvent[0x000000050B40FFDE] + DfEvent[0x000000050B40FFDF]) * 64B
Outbound data bytes from all links (local socket)	(DfEvent[0x0000000B0F403E5F] + DfEvent[0x0000000B0F403E9F] + DfEvent[0x0000000B0F403EDF] + DfEvent[0x0000000C0F403E1F] + DfEvent[0x0000000C0F403E5F] + DfEvent[0x0000000C0F403E9F] + DfEvent[0x0000000C0F403EDF] + DfEvent[0x0000000D0F403E1F]) * 64B

Table 19: Guidance for Pipeline Utilization Analysis Statistics

Name	Description	Equation
	Level 1	
Total Dispatch Slots	Up to 6 instructions can be dispatched in one cycle.	6 * Event[430076]
Frontend Bound	Fraction of dispatch slots that remained unused because the frontend did not supply enough instructions/ops.	Event[1004301A0] / Total Dispatch Slots
Bad Speculation	Fraction of dispatched ops that did not retire.	(Event[4307AA] – Event[4300C1]) / Total Dispatch Slots

Backend Bound	Fraction of dispatch slots that remained unused because of backend stalls.	Event[100431EA0] / Total Dispatch Slots
SMT contention	Fraction of unused dispatch slots because the other thread was selected.	Event[1004360A0] / Total Dispatch Slots
Retiring	Fraction of dispatch slots used by ops that retired.	Event[4300C1] / Total Dispatch Slots
Level 2		
Frontend Bound - Latency	Fraction of dispatch slots that remained unused because of a latency bottleneck in the frontend, such as Instruction Cache or ITLB misses.	6 * Event[1064301A0] / Total Dispatch Slots
Frontend Bound - BW	Fraction of dispatch slots that remained unused because of a bandwidth bottleneck in the frontend, such as decode bandwidth or Op Cache fetch bandwidth.	(Event[1004301A0] – (6 * Event[1064301A0])) / Total Dispatch Slots
Bad Speculation – Mispredicts	Fraction of dispatched ops that were flushed due to branch mispredicts.	Bad Speculation * Event[4300C3] / (Event[4300C3] + Event[430096])
Bad Speculation - Pipeline Restarts	Fraction of dispatched ops that were flushed due to pipeline restarts (resyncs).	Bad Speculation * Event[430096] / (Event[4300C3] + Event[430096])
Backend Bound - Memory	Fraction of dispatched slots that remained unused because of stalls due to the memory subsystem.	Backend Bound * (Event[43A2D6] / Event[4302D6])
Backend Bound – CPU	Fraction of dispatched slots that remained unused because of stalls not related to the memory subsystem.	Backend Bound * (1 - (Event[43A2D6] / Event[4302D6]))
Retiring - Fastpath	Fraction of dispatch slots used by fastpath ops that retired.	Retiring * (Event[4300C1] – Event[1004300C2]) / Event[4300C1]
Retiring - Microcode	Fraction of dispatch slots used by microcode ops that retired.	Retiring * Event[1004300C2] / Event[4300C1]

2.1.13.3 Large Increment per Cycle Events

Table 20: PMC_Definitions

Term	Description
MergeEvent	A PMC event that is capable of counter increments greater than 15, thus requiring merging a pair of even/odd performance monitors.

The maximum increment for a regular performance event is 15 (i.e., a 4-bit event). However some event types can have a larger increments every cycle (example: Core::X86::Pmc::Core::FpRetSseAvxOps).

An option is provided for merging a pair of even/odd performance monitors to acquire an accurate count. First the odd numbered Core::X86::Msrr::PERF_CTL0..5 is programmed with the event Core::X86::Pmc::Core::Merge (PMCxFFF) with the enable bit (En) turned on and with the remaining bits off. Then the corresponding even numbered Core::X86::Msrr::PERF_CTL0..5 is programmed with the desired PMC event. Both the odd and even numbered counter need to be enabled in Core::X86::Msrr::PerfCntrGlobalCtl for the merged counter to count. The performance monitor

combines the count value to an 8-bit increment event and extends the counter to a 64-bit counter.

Software wanting to preload a value to a merged counter pair writes the high-order 16-bit value to the low-order 16 bits of the odd counter and then writes the low-order 48-bit value to the even counter. Reading the even counter of the merged counter pair returns the full 64-bit value.

If an even performance monitor is programmed with the event `Core::X86::Pmc::Core::Merge` the Read results are undetermined. If an even performance monitor is programmed with a non-merge-able event (i.e., a 4-bit event) while the corresponding odd performance monitor is programmed as `Merge`, the Read results are undetermined. When discontinuing use of a merged counter pair, clear the `Merge` event from the odd performance monitor.

PMCxFFF [Merge] (Core::X86::Pmc::Core::Merge)

See 2.1.13.3 [Large Increment per Cycle Events].

PMCxFFF

Bits	Description
7:0	Reserved.

2.1.13.4 Core Performance Monitor Counters

This section provides the core performance counter events that may be selected through `Core::X86::Msr::PERF_CTL0[EventSelect[11:8],EventSelect[7:0],UnitMask]`. See `Core::X86::Msr::PERF_CTR`. See `Core::X86::Msr::PERF_LEGACY_CTL0..3` and `Core::X86::Msr::PERF_LEGACY_CTR`.

2.1.13.4.1 Floating-Point (FP) Events

PMCx002 [Retired x87 FP Ops] (Core::X86::Pmc::Core::FpRetx87FpOps)

Read-write. Reset: 00h.

The number of x87 floating-point Ops that have retired.

PMCx002

Bits	Description
7:3	Reserved.
2	DivSqrROps: Divide and square root Ops. Read-write. Reset: 0.
1	MulOps: Multiply Ops. Read-write. Reset: 0.
0	AddSubOps: Add/subtract Ops. Read-write. Reset: 0.

PMCx003 [Retired SSE/AVX FLOPs] (Core::X86::Pmc::Core::FpRetSseAvxOps)

Read-write. Reset: 00h.

This is a retire-based event. The number of retired SSE/AVX FLOPs. The number of events logged per cycle can vary from 0 to 64. This event requires the use of the `MergeEvent` since it can count above 15 events per cycle. See 2.1.13.3 [Large Increment per Cycle Events]. It does not provide a useful count without the use of the `MergeEvent`.

PMCx003

Bits	Description
7:5	Reserved.
4	BfloatMacFLOPs: bfloat Multiply-Accumulate FLOPs. Read-write. Reset: 0. Each bfloat MAC operation is counted as 2 FLOPs.
3	MacFLOPs: Multiply-Accumulate FLOPs. Read-write. Reset: 0. Each MAC operation is counted as 2 FLOPs. This event does not include bfloat MAC operations.
2	DivFLOPs: Divide/square root FLOPs. Read-write. Reset: 0.
1	MultFLOPs: Multiply FLOPs. Read-write. Reset: 0.
0	AddSubFLOPs: Add/subtract FLOPs. Read-write. Reset: 0.

PMCx005 [Retired Serializing Ops] (Core::X86::Pmc::Core::FpRetiredSerOps)

Read-write. Reset: 00h.

The number of serializing Ops retired.

PMCx005

Bits	Description
7:4	Reserved.
3	SseBotRet. Read-write. Reset: 0. SSE/AVX bottom-executing ops retired.
2	SseCtrlRet. Read-write. Reset: 0. SSE/AVX control word mispredict traps.
1	X87BotRet. Read-write. Reset: 0. x87 bottom-executing ops retired.
0	X87CtrlRet. Read-write. Reset: 0. x87 control word mispredict traps due to mispredictions in RC or PC, or changes in Exception Mask bits.

PMCx008 [Retired FP Ops By Width] (Core::X86::Pmc::Core::FpOpsRetiredByWidth)

Read-write. Reset: 00h.

PMCx008

Bits	Description
7:6	Reserved.
5	Pack512uOpsRetired. Read-write. Reset: 0. Number of packed 512-bit ops retired.
4	Pack256uOpsRetired. Read-write. Reset: 0. Number of packed 256-bit ops retired.
3	Pack128uOpsRetired. Read-write. Reset: 0. Number of packed 128-bit ops retired.
2	ScalaruOpsRetired. Read-write. Reset: 0. Number of scalar ops retired.
1	MMXuOpsRetired. Read-write. Reset: 0. Number of MMX ops retired.
0	x87uOpsRetired. Read-write. Reset: 0. Number of x87 ops retired.

PMCx00A [Retired FP Ops By Type] (Core::X86::Pmc::Core::FpOpsRetiredByType)

Read-write. Reset: 00h.

Note: Shuffle op counts may count for instructions that are not necessarily thought of as including shuffles. For example, Horizontal Add, Dot Product, and certain MOV instructions may include or use only shuffle type ops.

PMCx00A

Bits	Description																																		
7:4	VectorFpOpType. Read-write. Reset: 0h. ValidValues: <table> <tr> <th>Value</th><th>Description</th></tr> <tr><td>0h</td><td>None</td></tr> <tr><td>1h</td><td>Add</td></tr> <tr><td>2h</td><td>Sub</td></tr> <tr><td>3h</td><td>Mul</td></tr> <tr><td>4h</td><td>Mac</td></tr> <tr><td>5h</td><td>Div</td></tr> <tr><td>6h</td><td>Sqrt</td></tr> <tr><td>7h</td><td>Cmp</td></tr> <tr><td>8h</td><td>Cvt</td></tr> <tr><td>9h</td><td>Blend</td></tr> <tr><td>Ah</td><td>Reserved.</td></tr> <tr><td>Bh</td><td>Shuffle</td></tr> <tr><td>Ch</td><td>Reserved.</td></tr> <tr><td>Dh</td><td>Logical</td></tr> <tr><td>Eh</td><td>Other</td></tr> <tr><td>Fh</td><td>All</td></tr> </table>	Value	Description	0h	None	1h	Add	2h	Sub	3h	Mul	4h	Mac	5h	Div	6h	Sqrt	7h	Cmp	8h	Cvt	9h	Blend	Ah	Reserved.	Bh	Shuffle	Ch	Reserved.	Dh	Logical	Eh	Other	Fh	All
Value	Description																																		
0h	None																																		
1h	Add																																		
2h	Sub																																		
3h	Mul																																		
4h	Mac																																		
5h	Div																																		
6h	Sqrt																																		
7h	Cmp																																		
8h	Cvt																																		
9h	Blend																																		
Ah	Reserved.																																		
Bh	Shuffle																																		
Ch	Reserved.																																		
Dh	Logical																																		
Eh	Other																																		
Fh	All																																		
3:0	ScalarFpOpType. Read-write. Reset: 0h. ValidValues: <table> <tr> <th>Value</th><th>Description</th></tr> <tr><td>0h</td><td>None</td></tr> <tr><td>1h</td><td>Add</td></tr> <tr><td>2h</td><td>Sub</td></tr> <tr><td>3h</td><td>Mul</td></tr> <tr><td>4h</td><td>Mac</td></tr> <tr><td>5h</td><td>Div</td></tr> <tr><td>6h</td><td>Sqrt</td></tr> <tr><td>7h</td><td>Cmp</td></tr> <tr><td>8h</td><td>Cvt</td></tr> <tr><td>9h</td><td>Blend</td></tr> <tr><td>Dh-Ah</td><td>Reserved.</td></tr> <tr><td>Eh</td><td>Other</td></tr> <tr><td>Fh</td><td>All</td></tr> </table>	Value	Description	0h	None	1h	Add	2h	Sub	3h	Mul	4h	Mac	5h	Div	6h	Sqrt	7h	Cmp	8h	Cvt	9h	Blend	Dh-Ah	Reserved.	Eh	Other	Fh	All						
Value	Description																																		
0h	None																																		
1h	Add																																		
2h	Sub																																		
3h	Mul																																		
4h	Mac																																		
5h	Div																																		
6h	Sqrt																																		
7h	Cmp																																		
8h	Cvt																																		
9h	Blend																																		
Dh-Ah	Reserved.																																		
Eh	Other																																		
Fh	All																																		

PMCx00B [INT Ops Retired] (Core::X86::Pmc::Core::SseAvxOpsRetired)

Read-write. Reset: 00h.

Note: Shuffle op counts may count for instructions that are not necessarily thought of as including shuffles. For example, Horizontal Add, Dot Product, and certain MOV instructions may include or use only shuffle type ops.

PMCx00B

Bits	Description																																		
7:4	SseAvxOpType. Read-write. Reset: 0h. ValidValues: <table> <tr> <th>Value</th><th>Description</th></tr> <tr><td>0h</td><td>None</td></tr> <tr><td>1h</td><td>Add</td></tr> <tr><td>2h</td><td>Sub</td></tr> <tr><td>3h</td><td>Mul</td></tr> <tr><td>4h</td><td>Mac</td></tr> <tr><td>5h</td><td>AES</td></tr> <tr><td>6h</td><td>SHA</td></tr> <tr><td>7h</td><td>Cmp</td></tr> <tr><td>8h</td><td>CLM</td></tr> <tr><td>9h</td><td>Shift</td></tr> <tr><td>Ah</td><td>Mov</td></tr> <tr><td>Bh</td><td>Shuffle</td></tr> <tr><td>Ch</td><td>Pack</td></tr> <tr><td>Dh</td><td>Logical</td></tr> <tr><td>Eh</td><td>Other</td></tr> <tr><td>Fh</td><td>All</td></tr> </table>	Value	Description	0h	None	1h	Add	2h	Sub	3h	Mul	4h	Mac	5h	AES	6h	SHA	7h	Cmp	8h	CLM	9h	Shift	Ah	Mov	Bh	Shuffle	Ch	Pack	Dh	Logical	Eh	Other	Fh	All
Value	Description																																		
0h	None																																		
1h	Add																																		
2h	Sub																																		
3h	Mul																																		
4h	Mac																																		
5h	AES																																		
6h	SHA																																		
7h	Cmp																																		
8h	CLM																																		
9h	Shift																																		
Ah	Mov																																		
Bh	Shuffle																																		
Ch	Pack																																		
Dh	Logical																																		
Eh	Other																																		
Fh	All																																		
3:0	MmxOpType. Read-write. Reset: 0h. ValidValues: <table> <tr> <th>Value</th><th>Description</th></tr> <tr><td>0h</td><td>None</td></tr> <tr><td>1h</td><td>Add</td></tr> <tr><td>2h</td><td>Sub</td></tr> <tr><td>3h</td><td>Mul</td></tr> <tr><td>4h</td><td>Mac</td></tr> <tr><td>6h-5h</td><td>Reserved.</td></tr> <tr><td>7h</td><td>Cmp</td></tr> <tr><td>8h</td><td>Reserved.</td></tr> <tr><td>9h</td><td>Shift</td></tr> <tr><td>Ah</td><td>Mov</td></tr> <tr><td>Bh</td><td>Shuffle</td></tr> <tr><td>Ch</td><td>Pack</td></tr> <tr><td>Dh</td><td>Logical</td></tr> <tr><td>Eh</td><td>Other</td></tr> <tr><td>Fh</td><td>All</td></tr> </table>	Value	Description	0h	None	1h	Add	2h	Sub	3h	Mul	4h	Mac	6h-5h	Reserved.	7h	Cmp	8h	Reserved.	9h	Shift	Ah	Mov	Bh	Shuffle	Ch	Pack	Dh	Logical	Eh	Other	Fh	All		
Value	Description																																		
0h	None																																		
1h	Add																																		
2h	Sub																																		
3h	Mul																																		
4h	Mac																																		
6h-5h	Reserved.																																		
7h	Cmp																																		
8h	Reserved.																																		
9h	Shift																																		
Ah	Mov																																		
Bh	Shuffle																																		
Ch	Pack																																		
Dh	Logical																																		
Eh	Other																																		
Fh	All																																		

PMCx00C [Packed FP Ops Retired] (Core::X86::Pmc::Core::FpPackOpsRetired)

Read-write. Reset: 00h.

Note: Shuffle op counts may count for instructions that are not necessarily thought of as including shuffles. For example, Horizontal Add, Dot Product, and certain MOV instructions may include or use only shuffle type ops.

PMCx00C

Bits	Description																																		
7:4	Fp256OpType. Read-write. Reset: 0h. ValidValues: <table> <tr> <th>Value</th><th>Description</th></tr> <tr><td>0h</td><td>None</td></tr> <tr><td>1h</td><td>Add</td></tr> <tr><td>2h</td><td>Sub</td></tr> <tr><td>3h</td><td>Mul</td></tr> <tr><td>4h</td><td>Mac</td></tr> <tr><td>5h</td><td>Div</td></tr> <tr><td>6h</td><td>Sqrt</td></tr> <tr><td>7h</td><td>Cmp</td></tr> <tr><td>8h</td><td>Cvt</td></tr> <tr><td>9h</td><td>Blend</td></tr> <tr><td>Ah</td><td>Reserved.</td></tr> <tr><td>Bh</td><td>Shuffle</td></tr> <tr><td>Ch</td><td>Reserved.</td></tr> <tr><td>Dh</td><td>Logical</td></tr> <tr><td>Eh</td><td>Other</td></tr> <tr><td>Fh</td><td>All</td></tr> </table>	Value	Description	0h	None	1h	Add	2h	Sub	3h	Mul	4h	Mac	5h	Div	6h	Sqrt	7h	Cmp	8h	Cvt	9h	Blend	Ah	Reserved.	Bh	Shuffle	Ch	Reserved.	Dh	Logical	Eh	Other	Fh	All
Value	Description																																		
0h	None																																		
1h	Add																																		
2h	Sub																																		
3h	Mul																																		
4h	Mac																																		
5h	Div																																		
6h	Sqrt																																		
7h	Cmp																																		
8h	Cvt																																		
9h	Blend																																		
Ah	Reserved.																																		
Bh	Shuffle																																		
Ch	Reserved.																																		
Dh	Logical																																		
Eh	Other																																		
Fh	All																																		
3:0	Fp128OpType. Read-write. Reset: 0h. ValidValues: <table> <tr> <th>Value</th><th>Description</th></tr> <tr><td>0h</td><td>None</td></tr> <tr><td>1h</td><td>Add</td></tr> <tr><td>2h</td><td>Sub</td></tr> <tr><td>3h</td><td>Mul</td></tr> <tr><td>4h</td><td>Mac</td></tr> <tr><td>5h</td><td>Div</td></tr> <tr><td>6h</td><td>Sqrt</td></tr> <tr><td>7h</td><td>Cmp</td></tr> <tr><td>8h</td><td>Cvt</td></tr> <tr><td>9h</td><td>Blend</td></tr> <tr><td>Ah</td><td>Reserved.</td></tr> <tr><td>Bh</td><td>Shuffle</td></tr> <tr><td>Ch</td><td>Reserved.</td></tr> <tr><td>Dh</td><td>Logical</td></tr> <tr><td>Eh</td><td>Other</td></tr> <tr><td>Fh</td><td>All</td></tr> </table>	Value	Description	0h	None	1h	Add	2h	Sub	3h	Mul	4h	Mac	5h	Div	6h	Sqrt	7h	Cmp	8h	Cvt	9h	Blend	Ah	Reserved.	Bh	Shuffle	Ch	Reserved.	Dh	Logical	Eh	Other	Fh	All
Value	Description																																		
0h	None																																		
1h	Add																																		
2h	Sub																																		
3h	Mul																																		
4h	Mac																																		
5h	Div																																		
6h	Sqrt																																		
7h	Cmp																																		
8h	Cvt																																		
9h	Blend																																		
Ah	Reserved.																																		
Bh	Shuffle																																		
Ch	Reserved.																																		
Dh	Logical																																		
Eh	Other																																		
Fh	All																																		

PMCx00D [Packed INT Ops Retired] (Core::X86::Pmc::Core::PackedIntOpType)

Read-write. Reset: 00h.

Note: Shuffle op counts may count for instructions that are not necessarily thought of as including shuffles. For example, Horizontal Add, Dot Product, and certain MOV instructions may include or use only shuffle type ops.

PMCx00D

Bits	Description																																		
7:4	Int256OpType. Read-write. Reset: 0h. This event also counts FP data type packed and scalar MOV and shuffle operations. ValidValues: <table> <tr> <th>Value</th><th>Description</th></tr> <tr><td>0h</td><td>None</td></tr> <tr><td>1h</td><td>Add</td></tr> <tr><td>2h</td><td>Sub</td></tr> <tr><td>3h</td><td>Mul</td></tr> <tr><td>4h</td><td>Mac</td></tr> <tr><td>6h-5h</td><td>Reserved.</td></tr> <tr><td>7h</td><td>Cmp</td></tr> <tr><td>8h</td><td>Reserved.</td></tr> <tr><td>9h</td><td>Shift</td></tr> <tr><td>Ah</td><td>Mov</td></tr> <tr><td>Bh</td><td>Shuffle</td></tr> <tr><td>Ch</td><td>Pack</td></tr> <tr><td>Dh</td><td>Logical</td></tr> <tr><td>Eh</td><td>Other</td></tr> <tr><td>Fh</td><td>All</td></tr> </table>	Value	Description	0h	None	1h	Add	2h	Sub	3h	Mul	4h	Mac	6h-5h	Reserved.	7h	Cmp	8h	Reserved.	9h	Shift	Ah	Mov	Bh	Shuffle	Ch	Pack	Dh	Logical	Eh	Other	Fh	All		
Value	Description																																		
0h	None																																		
1h	Add																																		
2h	Sub																																		
3h	Mul																																		
4h	Mac																																		
6h-5h	Reserved.																																		
7h	Cmp																																		
8h	Reserved.																																		
9h	Shift																																		
Ah	Mov																																		
Bh	Shuffle																																		
Ch	Pack																																		
Dh	Logical																																		
Eh	Other																																		
Fh	All																																		
3:0	Int128OpType. Read-write. Reset: 0h. This event also counts FP data type packed and scalar MOV and shuffle operations. ValidValues: <table> <tr> <th>Value</th><th>Description</th></tr> <tr><td>0h</td><td>None</td></tr> <tr><td>1h</td><td>Add</td></tr> <tr><td>2h</td><td>Sub</td></tr> <tr><td>3h</td><td>Mul</td></tr> <tr><td>4h</td><td>Mac</td></tr> <tr><td>5h</td><td>AES</td></tr> <tr><td>6h</td><td>SHA</td></tr> <tr><td>7h</td><td>Cmp</td></tr> <tr><td>8h</td><td>CLM</td></tr> <tr><td>9h</td><td>Shift</td></tr> <tr><td>Ah</td><td>Mov</td></tr> <tr><td>Bh</td><td>Shuffle</td></tr> <tr><td>Ch</td><td>Pack</td></tr> <tr><td>Dh</td><td>Logical</td></tr> <tr><td>Eh</td><td>Other</td></tr> <tr><td>Fh</td><td>All</td></tr> </table>	Value	Description	0h	None	1h	Add	2h	Sub	3h	Mul	4h	Mac	5h	AES	6h	SHA	7h	Cmp	8h	CLM	9h	Shift	Ah	Mov	Bh	Shuffle	Ch	Pack	Dh	Logical	Eh	Other	Fh	All
Value	Description																																		
0h	None																																		
1h	Add																																		
2h	Sub																																		
3h	Mul																																		
4h	Mac																																		
5h	AES																																		
6h	SHA																																		
7h	Cmp																																		
8h	CLM																																		
9h	Shift																																		
Ah	Mov																																		
Bh	Shuffle																																		
Ch	Pack																																		
Dh	Logical																																		
Eh	Other																																		
Fh	All																																		

PMCx00E [FP Dispatch Faults] (Core::X86::Pmc::Core::FpDispFaults)

Read-write. Reset: 00h.

Floating-point Dispatch Faults.

PMCx00E

Bits	Description
7:4	Reserved.
3	YmmSpillFault: YMM Spill fault. Read-write. Reset: 0.
2	YmmFillFault: YMM Fill fault. Read-write. Reset: 0.
1	XmmFillFault: XMM Fill fault. Read-write. Reset: 0.
0	x87FillFault: x87 Fill fault. Read-write. Reset: 0.

2.1.13.4.2 Load/Store (LS) Events**PMCx024 [Bad Status 2] (Core::X86::Pmc::Core::LsBadStatus2)**

Read-write. Reset: 00h.

PMCx024

Bits	Description
7:2	Reserved.
1	StliOther. Read-write. Reset: 0. Store-to-load conflicts: A load was unable to complete due to a non-forwardable conflict with an older store. Most commonly, a load's address range partially but not completely overlaps with an uncompleted older store. Software can avoid this problem by using same-size and same-alignment loads and stores when accessing the same data. Vector/SIMD code is particularly susceptible to this problem; software should construct wide vector stores by manipulating vector elements in registers using shuffle/blend/swap instructions prior to storing to memory, instead of using narrow element-by-element stores.
0	Reserved.

PMCx025 [Retired Lock Instructions] (Core::X86::Pmc::Core::LsLocks)

Read-write. Reset: 00h.

PMCx025

Bits	Description
7:1	Reserved.
0	BusLock. Read-write. Reset: 0. Comparable to legacy bus lock.

PMCx026 [Retired CLFLUSH Instructions] (Core::X86::Pmc::Core::LsRetClflush)

The number of retired CLFLUSH instructions. This is a non-speculative event.

PMCx026

Bits	Description
7:0	Reserved.

PMCx027 [Retired CPUID Instructions] (Core::X86::Pmc::Core::LsRetCpuid)

The number of CPUID instructions retired.

PMCx027

Bits	Description
7:0	Reserved.

PMCx029 [LS Dispatch] (Core::X86::Pmc::Core::LsDispatch)

Read-write. Reset: 00h.

Counts the number of operations dispatched to the LS unit. Unit Masks events are ADDED.

PMCx029

Bits	Description
7:3	Reserved.
2	LdStDispatch: Load-op-Store Dispatch. Read-write. Reset: 0. Dispatch of an op that performs a load from and store to the same memory address.
1	StoreDispatch. Read-write. Reset: 0. Dispatch of an op that performs a memory store.
0	LdDispatch. Read-write. Reset: 0. Dispatch of an op that performs a memory load.

PMCx02B [SMIs Received] (Core::X86::Pmc::Core::LsSmiRx)

Reset: 00h.

Counts the number of SMIs received.

PMCx02B

Bits	Description
7:0	Reserved.

PMCx02C [Interrupts Taken] (Core::X86::Pmc::Core::LsIntTaken)

Read-write. Reset: 00h.

Counts the number of interrupts taken.

PMCx02C

Bits	Description
7:1	Reserved.
0	IntTaken. Read-write. Reset: 0. Number of Interrupts taken. This event is also counted when UnitMask[7:0]=0.

PMCx035 [Store to Load Forward] (Core::X86::Pmc::Core::LsSTLF)

Number of STLF hits.

PMCx035

Bits	Description
7:0	Reserved.

PMCx037 [Store Commit Cancels 2] (Core::X86::Pmc::Core::LsStCommitCancel2)

Read-write. Reset: 00h.

PMCx037

Bits	Description
7:1	Reserved.
0	StCommitCancelWcbFull. Read-write. Reset: 0. A non-cacheable store and the non-cacheable commit buffer is full.

PMCx041 [LS MAB Allocates by Type] (Core::X86::Pmc::Core::LsMabAlloc)

Read-write. Reset: 00h.

Counts when a LS pipe allocates a MAB entry.

PMCx041

Bits	Description												
7	Reserved.												
6:0	LsMabAllocation. Read-write. Reset: 00h.												
	ValidValues:												
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>3Eh-00h</td><td>Reserved.</td></tr> <tr> <td>3Fh</td><td>Load Store Allocations.</td></tr> <tr> <td>40h</td><td>Hardware Prefetcher Allocations.</td></tr> <tr> <td>7Eh-41h</td><td>Reserved.</td></tr> <tr> <td>7Fh</td><td>All Allocations.</td></tr> </table>	Value	Description	3Eh-00h	Reserved.	3Fh	Load Store Allocations.	40h	Hardware Prefetcher Allocations.	7Eh-41h	Reserved.	7Fh	All Allocations.
Value	Description												
3Eh-00h	Reserved.												
3Fh	Load Store Allocations.												
40h	Hardware Prefetcher Allocations.												
7Eh-41h	Reserved.												
7Fh	All Allocations.												

PMCx043 [Demand Data Cache Fills by Data Source] (Core::X86::Pmc::Core::LsDmndFillsFromSys)

Read-write. Reset: 00h.

Demand Data Cache Fills by Data Source.

PMCx043

Bits	Description
7	AlternateMemories_NearFar. Read-write. Reset: 0. Requests that return from Extension Memory.
6	DramIO_Far. Read-write. Reset: 0. Requests that target another NUMA node and return from DRAM or MMIO.
5	Reserved.
4	NearFarCache_Far. Read-write. Reset: 0. Requests that target another NUMA node and return from another CCX's cache.
3	DramIO_Near. Read-write. Reset: 0. Requests that target another NUMA node and return from DRAM or MMIO.
2	NearFarCache_Near. Read-write. Reset: 0. Requests that target the same NUMA node and return from another CCX's cache.
1	LocalCcx. Read-write. Reset: 0. Data returned from L3 or different L2 in the same CCX.
0	LocalL2. Read-write. Reset: 0. Data returned from local L2.

PMCx044 [Any Data Cache Fills by Data Source] (Core::X86::Pmc::Core::LsAnyFillsFromSys)

Read-write. Reset: 00h.

Any Data Cache Fills by Data Source.

PMCx044

Bits	Description
7	AlternateMemories_NearFar. Read-write. Reset: 0. Requests that return from Extension Memory.
6	DramIO_Far. Read-write. Reset: 0. Requests that target another NUMA node and return from DRAM.
5	Reserved.
4	NearFarCache_Far. Read-write. Reset: 0. Requests that target another NUMA node and return from another CCX's cache.
3	DramIO_Near. Read-write. Reset: 0. Requests that target another NUMA node and return from DRAM or MMIO.
2	NearFarCache_Near. Read-write. Reset: 0. Requests that target the same NUMA node and return from another CCX's cache.
1	LocalCcx. Read-write. Reset: 0. Data returned from L3 or different L2 in the same CCX.
0	LocalL2. Read-write. Reset: 0. Data returned from local L2.

PMCx045 [L1 DTLB Misses] (Core::X86::Pmc::Core::LsL1DTlbMiss)

Read-write. Reset: 00h.

PMCx045

Bits	Description
7	TlbReload1GL2Miss. Read-write. Reset: 0. DTLB reload to a 1-G page that also missed in the L2 TLB.
6	TlbReload2ML2Miss. Read-write. Reset: 0. DTLB reload to a 2-M page that also missed in the L2 TLB.
5	TlbReloadCoalescedPageMiss. Read-write. Reset: 0. DTLB reload to a coalesced page that also missed in the L2 TLB.
4	TlbReload4KL2Miss. Read-write. Reset: 0. DTLB reload to a 4-K page that missed the L2 TLB.
3	TlbReload1GL2Hit. Read-write. Reset: 0. DTLB reload to a 1-G page that hit in the L2 TLB.
2	TlbReload2ML2Hit. Read-write. Reset: 0. DTLB reload to a 2-M page that hit in the L2 TLB.
1	TlbReloadCoalescedPageHit. Read-write. Reset: 0. DTLB reload to a coalesced page that hit in the L2 TLB.
0	TlbReload4KL2Hit. Read-write. Reset: 0. DTLB reload to a 4-K page that hit in the L2 TLB.

PMCx047 [Misaligned loads] (Core::X86::Pmc::Core::LsMisalLoads)

Read-write. Reset: 00h.

PMCx047

Bits	Description
7:2	Reserved.
1	MA4K. Read-write. Reset: 0. The number of 4-KB misaligned (i.e., page crossing) loads.
0	MA64. Read-write. Reset: 0. The number of 64-B misaligned (i.e., cacheline crossing) loads.

PMCx04B [Prefetch Instructions Dispatched] (Core::X86::Pmc::Core::LsPrefInstrDisp)

Read-write. Reset: 00h.

Software Prefetch Instructions Dispatched (Speculative).

PMCx04B

Bits	Description
7:3	Reserved.
2	PREFETCHNTA. Read-write. Reset: 0. PrefetchNTA instruction. See docAPM3 PREFETCHlevel.
1	PREFETCHW. Read-write. Reset: 0. PrefetchW instruction. See docAPM3 PREFETCHW.
0	PREFETCH. Read-write. Reset: 0. PrefetchT0, T1 and T2 instructions. See docAPM3 PREFETCHlevel.

PMCx050 [Write Combine Buffer Close Flush] (Core::X86::Pmc::Core::LsWcbCloseFlush)

Read-write. Reset: 00h.

UnitMask events ADDed.

Multiple WCB can report events at the same time.

PMCx050

Bits	Description
7:1	Reserved.
0	FullLine64B. Read-write. Reset: 0. All 64 bytes of the WCB entry have been written.

PMCx052 [Ineffective Software Prefetches] (Core::X86::Pmc::Core::LsInefSwPref)

Read-write. Reset: 00h.

The number of software prefetches that did not fetch data outside of the processor core.

PMCx052

Bits	Description
7:2	Reserved.
1	MabMchCnt. Read-write. Reset: 0. Software PREFETCH instruction saw a match on an already-allocated miss request buffer.
0	DataPipeSwPfdCHit. Read-write. Reset: 0. Software PREFETCH instruction saw a DC hit.

PMCx059 [Software Prefetch Data Cache Fills] (Core::X86::Pmc::Core::LsSwPfdCfills)

Read-write. Reset: 00h.

Software Prefetch Data Cache Fills by Data Source.

PMCx059

Bits	Description
7	AlternateMemories_NearFar . Read-write. Reset: 0. Requests that return from Extension Memory.
6	DramIO_Far . Read-write. Reset: 0. Requests that target another NUMA node and return from DRAM or MMIO.
5	Reserved.
4	NearFarCache_Far . Read-write. Reset: 0. Requests that target another NUMA node and return from another CCX's cache.
3	DramIO_Near . Read-write. Reset: 0. Requests that target another NUMA node and return from DRAM or MMIO.
2	NearFarCache_Near . Read-write. Reset: 0. Requests that target the same NUMA node and return from another CCX's cache.
1	LocalCcx . Read-write. Reset: 0. Data returned from L3 or different L2 in the same CCX.
0	LocalL2 . Read-write. Reset: 0. Data returned from local L2.

PMCx05A [Hardware Prefetch Data Cache Fills] (Core::X86::Pmc::Core::LsHwPfdCfills)

Read-write. Reset: 00h.

Hardware Prefetch Data Cache Fills by Data Source.

PMCx05A

Bits	Description
7	AlternateMemories_NearFar . Read-write. Reset: 0. Requests that return from Extension Memory.
6	DramIO_Far . Read-write. Reset: 0. Requests that target another NUMA node and return from DRAM or MMIO.
5	Reserved.
4	NearFarCache_Far . Read-write. Reset: 0. Requests that target another NUMA node and return from another CCX's cache.
3	DramIO_Near . Read-write. Reset: 0. Requests that target another NUMA node and return from DRAM or MMIO.
2	NearFarCache_Near . Read-write. Reset: 0. Requests that target the same NUMA node and return from another CCX's cache.
1	LocalCcx . Read-write. Reset: 0. Data returned from L3 or different L2 in the same CCX.
0	LocalL2 . Read-write. Reset: 0. Data returned from local L2.

PMCx05F [Count of Allocated Mabs] (Core::X86::Pmc::Core::LsAllocMabCount)

This event counts the in-flight L1 data cache misses (allocated Miss Address Buffers) each cycle.

PMCx05F

Bits	Description
7:0	Reserved.

PMCx076 [Cycles not in Halt] (Core::X86::Pmc::Core::LsNotHaltedCyc)

PMCx076

Bits	Description
7:0	Reserved.

PMCx078 [All TLB Flushes] (Core::X86::Pmc::Core::LsTlbFlush)

Read-write. Reset: 00h.

PMCx078

Bits	Description
7:0	All. Read-write. Reset: 00h.
ValidValues:	
Value	Description
FEh-00h	Reserved.
FFh	All TLB Flushes.

PMCx120 [P0 Freq Cycles not in Halt] (Core::X86::Pmc::Core::LsNotHaltedP0Cyc)

Read-write. Reset: 00h.

PMCx120

Bits	Description
7:1	Reserved.
0	P0FreqCyc. Read-write. Reset: 0. Counts at the P0 frequency (same as Core::X86::Msr::MPERF) when not in Halt.

2.1.13.4.3 Instruction Cache (IC) and Branch Prediction (BP) Events

Note: All instruction cache events are speculative events unless specified otherwise.

PMCx082 [Instruction Cache Refills from L2] (Core::X86::Pmc::Core::IcCacheFillL2)

The number of 64-byte instruction cache lines fulfilled from the L2 cache.

PMCx082

Bits	Description
7:0	Reserved.

PMCx083 [Instruction Cache Refills from System] (Core::X86::Pmc::Core::IcCacheFillSys)

The number of 64-byte instruction cache line fulfilled from system memory or another cache.

PMCx083

Bits	Description
7:0	Reserved.

PMCx084 [L1 ITLB Miss, L2 ITLB Hit] (Core::X86::Pmc::Core::BpL1TlbMissL2TlbHit)

The number of instruction fetches that miss in the L1 ITLB but hit in the L2 ITLB.

PMCx084

Bits	Description
7:0	Reserved.

PMCx085 [ITLB Reload from Page-Table walk] (Core::X86::Pmc::Core::BpL1TlbMissL2TlbMiss)

Read-write. Reset: 00h.

The number of valid fills into the ITLB originating from the LS Page-Table Walker. Tablewalk requests are issued for L1-ITLB and L2-ITLB misses.

PMCx085

Bits	Description
7:4	Reserved.
3	Coalesced4K. Read-write. Reset: 0. Walk for >4-K Coalesced page.
2	IF1G. Read-write. Reset: 0. Walk for 1-G page.
1	IF2M. Read-write. Reset: 0. Walk for 2-M page.
0	IF4K. Read-write. Reset: 0. Walk to 4-K page.

PMCx08B [L2 Branch Prediction Overrides Existing Prediction (speculative)] (Core::X86::Pmc::Core::BpL2BTBCorrect)

PMCx08B

Bits	Description
7:0	Reserved.

PMCx08E [Dynamic Indirect Predictions] (Core::X86::Pmc::Core::BpDynIndPred)

The number of times a branch used the indirect predictor to make a prediction.

PMCx08E

Bits	Description
7:0	Reserved.

PMCx091 [Decode Redirects] (Core::X86::Pmc::Core::BpDeReDirect)

Reset: 00h.

The number of times the instruction decoder overrides the predicted target.

PMCx091

Bits	Description
7:0	Reserved.

PMCx094 [L1 TLB Hits for Instruction Fetch] (Core::X86::Pmc::Core::BpL1TlbFetchHit)

Read-write. Reset: 00h.

The number of instruction fetches that hit in the L1 ITLB.

PMCx094

Bits	Description
7:3	Reserved.
2	IF1G. Read-write. Reset: 0. L1 Instruction TLB hit (1-G page size).
1	IF2M. Read-write. Reset: 0. L1 Instruction TLB hit (2-M page size).
0	IF4K. Read-write. Reset: 0. L1 Instruction TLB hit (4-K or 16-K page size).

PMCx096 [Resyncs] (Core::X86::Pmc::Core::ResyncsOrNcRedirects)

Counts the number of HW resyncs (pipeline restarts) or NC redirects. NC redirects occur when the front-end transitions to fetching from UC (un-cacheable) memory.

PMCx096

Bits	Description
7:0	Reserved.

PMCx18E [IC Tag Hit/Miss Events] (Core::X86::Pmc::Core::IcTagHitMiss)

Read-write. Reset: 00h.

Counts various IC tag related hit and miss events.

PMCx18E

Bits	Description
7:5	Reserved.
4:0	IcAccessTypes. Read-write. Reset: 00h. Instruction Cache accesses.
ValidValues:	
Value	Description
06h-00h	Reserved.
07h	Instruction Cache Hit.
17h-08h	Reserved.
18h	Instruction Cache Miss.
1Eh-19h	Reserved.
1Fh	All Instruction Cache Accesses.

PMCx28F [Op Cache Hit/Miss] (Core::X86::Pmc::Core::OpCacheHitMiss)

Read-write. Reset: 00h.

Counts Op Cache micro-tag hit/miss events.

PMCx28F

Bits	Description
7:3	Reserved.
2:0	OpCacheAccesses. Read-write. Reset: 0h.
ValidValues:	
Value	Description
2h-0h	Reserved.
3h	Op Cache Hit.
4h	Op Cache Miss.
6h-5h	Reserved.
7h	All Op Cache accesses.

2.1.13.4.4 DE Events**PMCx0A9 [Op Queue Empty] (Core::X86::Pmc::Core::DeOpQueueEmpty)**

Reset: 00h.

Cycles where the Op Queue is empty.

PMCx0A9

Bits	Description
7:0	Reserved.

PMCx0AA [Source of Op Dispatched From Decoder] (Core::X86::Pmc::Core::DeSrcOpDisp)

Read-write. Reset: 00h.

Counts the number of ops dispatched from the decoder classified by op source.

PMCx0AA

Bits	Description
7:3	Reserved.
2	LoopBuffer. Read-write. Reset: 0. Count of ops dispatched from Loop Buffer.
1	OpCache. Read-write. Reset: 0. Count of ops fetched from Op Cache and dispatched.
0	Decoder. Read-write. Reset: 0. Count of ops fetched from Instruction Cache and dispatched.

PMCx0AB [Types of Ops Dispatched From Decoder] (Core::X86::Pmc::Core::DeDisOpsFromDecoder)

Read-write. Reset: 00h.

Counts the number of ops dispatched from the decoder classified by op type. The UnitMask value encodes which types of ops are counted.

PMCx0AB

Bits	Description												
7:5	Reserved.												
4:0	DispOpType. Read-write. Reset: 00h. ValidValues:												
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>03h-00h</td><td>Reserved.</td></tr> <tr> <td>04h</td><td>Any FP dispatch.</td></tr> <tr> <td>07h-05h</td><td>Reserved.</td></tr> <tr> <td>08h</td><td>Any Integer dispatch.</td></tr> <tr> <td>1Fh-09h</td><td>Reserved.</td></tr> </table>	Value	Description	03h-00h	Reserved.	04h	Any FP dispatch.	07h-05h	Reserved.	08h	Any Integer dispatch.	1Fh-09h	Reserved.
Value	Description												
03h-00h	Reserved.												
04h	Any FP dispatch.												
07h-05h	Reserved.												
08h	Any Integer dispatch.												
1Fh-09h	Reserved.												

PMCx0AE [Dispatch Resource Stall Cycles 1] (Core::X86::Pmc::Core::DeDisDispatchTokenStalls1)

Read-write. Reset: 00h.

Cycles where a dispatch group is valid but does not get dispatched due to a Token Stall. UnitMask bits select the stall types included in the count.

PMCx0AE

Bits	Description
7	FpFlushRecoveryStall. Read-write. Reset: 0. Counts FP Flush Recovery stall cycles.
6	FPSchRsrcStall: FP scheduler resource stall. Read-write. Reset: 0. Counts FP Scheduler token stall cycles. .
5	FpRegFileRsrcStall: floating-point register file resource stall. Read-write. Reset: 0. Counts FP Register File token stall cycles. This applies to all ops that have an FP or SIMD destination register. .
4	TakenBrnchBufferRsrc: taken branch buffer resource stall. Read-write. Reset: 0. Counts Taken Branch Buffer token stall cycles.
3	Reserved.
2	StoreQueueRsrcStall: Store Queue resource stall. Read-write. Reset: 0. Counts Store Queue token stall cycles.
1	LoadQueueRsrcStall: Load Queue resource stall. Read-write. Reset: 0. Counts Load Queue token stall cycles.
0	IntPhyRegFileRsrcStall: Integer Physical Register File resource stall. Read-write. Reset: 0. Counts Integer PRF token stall cycles. This applies to all ops that have an integer destination register.

PMCx0AF [Dynamic Tokens Dispatch Stall Cycles 2] (Core::X86::Pmc::Core::DeDisDispatchTokenStalls2)

Read-write. Reset: 00h.

Cycles where a dispatch group is valid but does not get dispatched due to a token stall. UnitMask bits select the stall types included in the count.

PMCx0AF

Bits	Description
7:6	Reserved.
5	RetireTokenStall. Read-write. Reset: 0. Counts Retire Queue token stall cycles.
4	Reserved.
3	IntSch3TokenStall. Read-write. Reset: 0. Counts Integer Scheduler Queue 3 token stall cycles.
2	IntSch2TokenStall. Read-write. Reset: 0. Counts Integer Scheduler Queue 2 token stall cycles.
1	IntSch1TokenStall. Read-write. Reset: 0. Counts Integer Scheduler Queue 1 token stall cycles.
0	IntSch0TokenStall. Read-write. Reset: 0. Counts Integer Scheduler Queue 0 token stall cycles.

PMCx1A0 [Dispatch Stalls Per Slot] (Core::X86::Pmc::Core::DeNoDispatchPerSlot)

Read-write. Reset: 00h.

Counts the number of dispatch slots (each cycle) that remained unused for reasons selected by StallReason.

PMCx1A0

Bits	Description																
7:0	StallReason. Read-write. Reset: 00h. ValidValues:																
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>00h</td><td>Reserved.</td></tr> <tr> <td>01h</td><td>Counts dispatch slots left empty because the front-end did not supply ops.</td></tr> <tr> <td>1Dh-02h</td><td>Reserved.</td></tr> <tr> <td>1Eh</td><td>Counts ops unable to dispatch due to back-end stalls.</td></tr> <tr> <td>5Fh-1Fh</td><td>Reserved.</td></tr> <tr> <td>60h</td><td>Counts ops unable to dispatch because the dispatch cycle was granted to the other SMT thread.</td></tr> <tr> <td>FFh-61h</td><td>Reserved.</td></tr> </table>	Value	Description	00h	Reserved.	01h	Counts dispatch slots left empty because the front-end did not supply ops.	1Dh-02h	Reserved.	1Eh	Counts ops unable to dispatch due to back-end stalls.	5Fh-1Fh	Reserved.	60h	Counts ops unable to dispatch because the dispatch cycle was granted to the other SMT thread.	FFh-61h	Reserved.
Value	Description																
00h	Reserved.																
01h	Counts dispatch slots left empty because the front-end did not supply ops.																
1Dh-02h	Reserved.																
1Eh	Counts ops unable to dispatch due to back-end stalls.																
5Fh-1Fh	Reserved.																
60h	Counts ops unable to dispatch because the dispatch cycle was granted to the other SMT thread.																
FFh-61h	Reserved.																

PMCx1A2 [Dispatch Additional Resource Stalls] (Core::X86::Pmc::Core::DeAdditionalResourceStalls)

Read-write. Reset: 00h.

This PMC event counts additional resource stalls that are not captured by Core::X86::Pmc::Core::DeDisDispatchTokenStalls1 or Core::X86::Pmc::Core::DeDisDispatchTokenStalls2.

PMCx1A2

Bits	Description								
7:0	Stall. Read-write. Reset: 00h. ValidValues:								
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>2Fh-00h</td><td>Reserved.</td></tr> <tr> <td>30h</td><td>Counts additional cycles dispatch is stalled due to the lack of dispatch resources</td></tr> <tr> <td>FFh-31h</td><td>Reserved.</td></tr> </table>	Value	Description	2Fh-00h	Reserved.	30h	Counts additional cycles dispatch is stalled due to the lack of dispatch resources	FFh-31h	Reserved.
Value	Description								
2Fh-00h	Reserved.								
30h	Counts additional cycles dispatch is stalled due to the lack of dispatch resources								
FFh-31h	Reserved.								

2.1.13.4.5 EX (SC) Events

PMCx0C0 [Retired Instructions] (Core::X86::Pmc::Core::ExRetInstr)

The number of instructions retired.

PMCx0C0

Bits Description

7:0 Reserved.

PMCx0C1 [Retired Ops] (Core::X86::Pmc::Core::ExRetOps)

The number of macro-ops retired.

PMCx0C1

Bits Description

7:0 Reserved.

PMCx0C2 [Retired Branch Instructions] (Core::X86::Pmc::Core::ExRetBrn)

The number of branch instructions retired. This includes all types of architectural control flow changes, including exceptions and interrupts.

PMCx0C2

Bits Description

7:0 Reserved.

PMCx0C3 [Retired Branch Instructions Mispredicted] (Core::X86::Pmc::Core::ExRetBrnMisp)

The number of retired branch instructions, that were mispredicted.

PMCx0C3

Bits Description

7:0 Reserved.

PMCx0C4 [Retired Taken Branch Instructions] (Core::X86::Pmc::Core::ExRetBrnTkn)

The number of taken branches that were retired. This includes all types of architectural control flow changes, including exceptions and interrupts.

PMCx0C4

Bits Description

7:0 Reserved.

PMCx0C5 [Retired Taken Branch Instructions Mispredicted] (Core::X86::Pmc::Core::ExRetBrnTknMisp)

The number of retired taken branch instructions that were mispredicted.

PMCx0C5

Bits Description

7:0 Reserved.

PMCx0C6 [Retired Far Control Transfers] (Core::X86::Pmc::Core::ExRetBrnFar)

The number of far control transfers retired including far call/jump/return, IRET, SYSCALL and SYSRET, plus exceptions and interrupts. Far control transfers are not subject to branch prediction.

PMCx0C6

Bits Description

7:0 Reserved.

PMCx0C8 [Retired Near Returns] (Core::X86::Pmc::Core::ExRetNearRet)

The number of near return instructions (RET or RET Iw) retired.

PMCx0C8

Bits Description

7:0 Reserved.

PMCx0C9 [Retired Near Returns Mispredicted] (Core::X86::Pmc::Core::ExRetNearRetMispred)

The number of near returns retired that were not correctly predicted by the return address predictor. Each such mispredict incurs the same penalty as a mispredicted conditional branch instruction.

PMCx0C9

Bits	Description
------	-------------

7:0	Reserved.
-----	-----------

PMCx0CA [Retired Indirect Branch Instructions Mispredicted] (Core::X86::Pmc::Core::ExRetBrnIndMisp)

The number of indirect branches retired that were not correctly predicted. Each such mispredict incurs the same penalty as a mispredicted conditional branch instruction. Note that only EX mispredicts are counted.

PMCx0CA

Bits	Description
------	-------------

7:0	Reserved.
-----	-----------

PMCx0CB [Retired MMX/FP Instructions] (Core::X86::Pmc::Core::ExRetMmxFpInstr)

Read-write. Reset: 00h.

The number of MMX, SSE or x87 instructions retired. The UnitMask allows the selection of the individual classes of instructions as given in the table. Each increment represents one complete instruction. Since this event includes non-numeric instructions it is not suitable for measuring MFLOPs.

PMCx0CB

Bits	Description
------	-------------

7:3	Reserved.
-----	-----------

2	SseInstr. Read-write. Reset: 0. SSE instructions (SSE, SSE2, SSE3, SSSE3, SSE4A, SSE41, SSE42, AVX).
---	---

1	MmxInstr. Read-write. Reset: 0. MMX instructions.
---	--

0	X87Instr: x87 instructions. Read-write. Reset: 0.
---	--

PMCx0CC [Retired Indirect Branch Instructions] (Core::X86::Pmc::Core::ExRetIndBrchInstr)

The number of indirect branches retired.

PMCx0CC

Bits	Description
------	-------------

7:0	Reserved.
-----	-----------

PMCx0D1 [Retired Conditional Branch Instructions] (Core::X86::Pmc::Core::ExRetCond)

PMCx0D1

Bits	Description
------	-------------

7:0	Reserved.
-----	-----------

PMCx0D3 [Div Cycles Busy count] (Core::X86::Pmc::Core::ExDivBusy)

PMCx0D3

Bits	Description
------	-------------

7:0	Reserved.
-----	-----------

PMCx0D4 [Div Op Count] (Core::X86::Pmc::Core::ExDivCount)

PMCx0D4

Bits	Description
------	-------------

7:0	Reserved.
-----	-----------

PMCx0D6 [Cycles With No Retire] (Core::X86::Pmc::Core::ExNoRetire)

Read-write. Reset: 00h.

This event counts cycles when the hardware thread does not retire any ops for reasons selected by UnitMask[4:0]. UnitMask events [4:0] are mutually exclusive. If multiple reasons apply for a given cycle, the lowest numbered UnitMask event is counted.

PMCx0D6

Bits	Description										
7:5	CompletionFilter. Read-write. Reset: 0h. ValidValues:										
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0h</td><td>Load and ALU completion is considered for UnitMask[1]:NotComplete events.</td></tr> <tr> <td>4h-1h</td><td>Reserved.</td></tr> <tr> <td>5h</td><td>Only missing load completion is considered for UnitMask[1]:NotComplete events.</td></tr> <tr> <td>7h-6h</td><td>Reserved.</td></tr> </table>	Value	Description	0h	Load and ALU completion is considered for UnitMask[1]:NotComplete events.	4h-1h	Reserved.	5h	Only missing load completion is considered for UnitMask[1]:NotComplete events.	7h-6h	Reserved.
Value	Description										
0h	Load and ALU completion is considered for UnitMask[1]:NotComplete events.										
4h-1h	Reserved.										
5h	Only missing load completion is considered for UnitMask[1]:NotComplete events.										
7h-6h	Reserved.										
4	ThreadNotSelected. Read-write. Reset: 0. The number cycles where ops could have retired (i.e. did not fall into UnitMask events [0]...[3]), but did not retire because thread arbitration did not select the thread for retire.										
3	Other. Read-write. Reset: 0. The number of cycles where ops could have retired (self and older ops are complete), but were stopped from retirement for other reasons: retire breaks, traps, faults, etc.										
2	Reserved.										
1	NotComplete. Read-write. Reset: 0. The number of cycles where the oldest retire slot did not have its completion bits set.										
0	Empty. Read-write. Reset: 0. The number of cycles when there were no valid ops in the retire queue. This may be caused by front-end bottlenecks or pipeline redirects.										

PMCx1C1 [Retired Microcoded Instructions] (Core::X86::Pmc::Core::ExRetUcodeInstr)

Retired Microcoded Instructions.

PMCx1C1

Bits	Description
7:0	Reserved.

PMCx1C2 [Retired Microcode Ops] (Core::X86::Pmc::Core::ExRetUcodeOps)

The number of microcode ops that have retired.

PMCx1C2

Bits	Description
7:0	Reserved.

PMCx1C7 [Retired Mispredicted Branch Instructions due to Direction Mismatch] (Core::X86::Pmc::Core::ExRetMsprdBnrchInstrDirMsmtch)

The number of retired conditional branch instructions that were not correctly predicted because of a branch direction mismatch.

PMCx1C7

Bits	Description
7:0	Reserved.

PMCx1C8 [Retired Unconditional Indirect Branch Instructions Mispredicted] (Core::X86::Pmc::Core::ExRetUncondBrnchInstrMispred)

The number of retired unconditional indirect branch instructions that were mispredicted.

PMCx1C8

Bits	Description
7:0	Reserved.

PMCx1C9 [Retired Unconditional Branch Instructions] (Core::X86::Pmc::Core::ExRetUncondBrnchInstr)

The number of retired unconditional branch instructions.

PMCx1C9

Bits	Description
------	-------------

7:0	Reserved.
-----	-----------

PMCx1CF [Tagged IBS Ops] (Core::X86::Pmc::Core::ExTaggedIbsOps)

Read-write. Reset: 00h.

Counts Op IBS related events.

PMCx1CF

Bits	Description
------	-------------

7:3	Reserved.
-----	-----------

2	IbsCountRollover. Read-write. Reset: 0. Number of times an op could not be tagged by IBS because of a previous tagged op that has not retired.
---	---

1	IbsTaggedOpsRet. Read-write. Reset: 0. Number of Ops tagged by IBS that retired.
---	---

0	IbsTaggedOps. Read-write. Reset: 0. Number of Ops tagged by IBS.
---	---

PMCx1D0 [Retired Fused Instructions] (Core::X86::Pmc::Core::ExRetFusedInstr)

Reset: 00h.

Counts retired fused instructions.

PMCx1D0

Bits	Description
------	-------------

7:0	Reserved.
-----	-----------

2.1.13.4.6 L2 Cache Events**PMCx060 [Requests to L2 Group1] (Core::X86::Pmc::L2::L2RequestG1)**

Read-write.

All L2 Cache Requests (Breakdown 1 - Common)

PMCx060; PMC=0000_0000h

Bits	Description
------	-------------

7	RdBlkL. Read-write. Data Cache Reads (including hardware and software prefetch).
---	---

6	RdBlkX. Read-write. Data Cache Stores
---	--

5	LsRdBlkC_S. Read-write. Data Cache Shared Reads
---	--

4	CacheableIcRead. Read-write. Instruction Cache Reads.
---	--

3	ChangeToX: Data Cache State Change Requests. Read-write. Request change to writable, check L2 for current state.
---	---

2	PrefetchL2Cmd. Read-write.
---	-----------------------------------

1	L2HwPf: L2 Prefetcher. Read-write. All prefetches accepted by L2 pipeline, hit or miss. Types of PF and L2 hit/miss broken out in a separate perfmon event
---	---

0	Group2. Read-write. MiscRequests. Read-write. Various Noncacheable requests. Non-cached Data Reads, Non-cached Instruction Reads, Self-modifying code checks.
---	--

PMCx061 [Requests to L2 Group2] (Core::X86::Pmc::L2::L2RequestG2)

Read-write.

All L2 Cache Requests (Breakdown 2 - Rare).

PMCx061; PMC=0000_0000h

Bits	Description
7	Reserved.
6	LsRdSized . Read-write. LS sized read, coherent non-cacheable.
5	LsRdSizedNC . Read-write. LS sized read, non-coherent, non-cacheable.
4:0	Reserved.

PMCx063 [Write Combining Buffer Requests] (Core::X86::Pmc::L2::L2WcbReq)

Read-write.

Write Combining Buffer operations. For information on Write Combining see docAPM2 sections: Memory System, Memory Types, Buffering and Combining Memory Writes.

PMCx063; PMC=0000_0000h

Bits	Description
7	Reserved.
6	WcbWrite . Read-write. Write Combining Buffer write
5	WcbClose . Read-write. Write Combining Buffer close
4:0	Reserved.

PMCx064 [Core to L2 Cacheable Request Access Status] (Core::X86::Pmc::L2::L2CacheReqStat)

Read-write.

L2 Cache Request Outcomes (not including L2 Prefetch).

PMCx064; PMC=0000_0000h

Bits	Description
7	LsRdBlkCS: Data Cache Shared Read Hit in L2 . Read-write. LsRdBlkCS
6	LsRdBlkLHitX: Data Cache Read Hit in L2 . Read-write. Modifiable
5	LsRdBlkLHitS: Data Cache Read Hit Non-Modifiable Line in L2 . Read-write.
4	LsRdBlkX: Data Cache Store or State Change Hit in L2 . Read-write.
3	LsRdBlkC: Data Cache Req Miss in L2 . Read-write.
2	IcFillHitX: Instruction Cache Hit Modifiable Line in L2 . Read-write. IcFillHitX
1	IcFillHitS: Instruction Cache Hit Non-Modifiable Line in L2 . Read-write.
0	IcFillMiss: Instruction Cache Req Miss in L2 . Read-write. IcFillMiss

PMCx070 [L2 Prefetch Hit in L2] (Core::X86::Pmc::L2::L2PfHitL2)

Read-write.

Counts all L2 prefetches accepted by L2 pipeline which hit in the L2 cache.

PMCx070; PMC=0000_0000h

Bits	Description														
7:0	Prefetches. Read-write.														
	ValidValues:														
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>1Eh-00h</td><td>Reserved.</td></tr> <tr> <td>1Fh</td><td>Counts requests generated from L2 Hardware Prefetchers.</td></tr> <tr> <td>DFh-20h</td><td>Reserved.</td></tr> <tr> <td>E0h</td><td>Counts requests generated from L1 DC Hardware Prefetchers.</td></tr> <tr> <td>FEh-E1h</td><td>Reserved.</td></tr> <tr> <td>FFh</td><td>Counts requests generated from L1 DC and L2 Hardware Prefetchers.</td></tr> </table>	Value	Description	1Eh-00h	Reserved.	1Fh	Counts requests generated from L2 Hardware Prefetchers.	DFh-20h	Reserved.	E0h	Counts requests generated from L1 DC Hardware Prefetchers.	FEh-E1h	Reserved.	FFh	Counts requests generated from L1 DC and L2 Hardware Prefetchers.
Value	Description														
1Eh-00h	Reserved.														
1Fh	Counts requests generated from L2 Hardware Prefetchers.														
DFh-20h	Reserved.														
E0h	Counts requests generated from L1 DC Hardware Prefetchers.														
FEh-E1h	Reserved.														
FFh	Counts requests generated from L1 DC and L2 Hardware Prefetchers.														

PMCx071 [L2 Prefetcher Hits in L3] (Core::X86::Pmc::L2::L2PfMissL2HitL3)

Read-write.

Counts all L2 prefetches accepted by the L2 pipeline which miss the L2 cache and hit the L3.

PMCx071; PMC=0000_0000h

Bits	Description														
7:0	Prefetches. Read-write. L2Stream														
	ValidValues:														
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>1Eh-00h</td><td>Reserved.</td></tr> <tr> <td>1Fh</td><td>Counts requests generated from L2 Hardware Prefetchers.</td></tr> <tr> <td>DFh-20h</td><td>Reserved.</td></tr> <tr> <td>E0h</td><td>Counts requests generated from L1 DC Hardware Prefetchers.</td></tr> <tr> <td>FEh-E1h</td><td>Reserved.</td></tr> <tr> <td>FFh</td><td>Counts requests generated from L1 DC and L2 Hardware Prefetchers.</td></tr> </table>	Value	Description	1Eh-00h	Reserved.	1Fh	Counts requests generated from L2 Hardware Prefetchers.	DFh-20h	Reserved.	E0h	Counts requests generated from L1 DC Hardware Prefetchers.	FEh-E1h	Reserved.	FFh	Counts requests generated from L1 DC and L2 Hardware Prefetchers.
Value	Description														
1Eh-00h	Reserved.														
1Fh	Counts requests generated from L2 Hardware Prefetchers.														
DFh-20h	Reserved.														
E0h	Counts requests generated from L1 DC Hardware Prefetchers.														
FEh-E1h	Reserved.														
FFh	Counts requests generated from L1 DC and L2 Hardware Prefetchers.														

PMCx072 [L2 Prefetcher Misses in L3] (Core::X86::Pmc::L2::L2PfMissL2L3)

Read-write.

Counts all L2 prefetches accepted by the L2 pipeline which miss the L2 and the L3 caches

PMCx072; PMC=0000_0000h

Bits	Description														
7:0	Prefetches. Read-write. L2Stream														
	ValidValues:														
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>1Eh-00h</td><td>Reserved.</td></tr> <tr> <td>1Fh</td><td>Counts requests generated from L2 Hardware Prefetchers.</td></tr> <tr> <td>DFh-20h</td><td>Reserved.</td></tr> <tr> <td>E0h</td><td>Counts requests generated from L1 DC Hardware Prefetchers.</td></tr> <tr> <td>FEh-E1h</td><td>Reserved.</td></tr> <tr> <td>FFh</td><td>Counts requests generated from L1 DC and L2 Hardware Prefetchers.</td></tr> </table>	Value	Description	1Eh-00h	Reserved.	1Fh	Counts requests generated from L2 Hardware Prefetchers.	DFh-20h	Reserved.	E0h	Counts requests generated from L1 DC Hardware Prefetchers.	FEh-E1h	Reserved.	FFh	Counts requests generated from L1 DC and L2 Hardware Prefetchers.
Value	Description														
1Eh-00h	Reserved.														
1Fh	Counts requests generated from L2 Hardware Prefetchers.														
DFh-20h	Reserved.														
E0h	Counts requests generated from L1 DC Hardware Prefetchers.														
FEh-E1h	Reserved.														
FFh	Counts requests generated from L1 DC and L2 Hardware Prefetchers.														

PMCx165 [L2 Fill Response Source] (Core::X86::Pmc::L2::L2FillRspSrc)

Read-write.

Counts fill responses based on their source. Selecting an event mask of 0xfe will count all L3 responses.

This will count all L3 responses to fill requests.

This event is similar to LS PMC 0x44

PMCx165; PMC=0000_0000h

Bits	Description
7	AlternateMemories_NearFar. Read-write. "Requests that return from Extension Memory"
6	DramIO_Far. Read-write. Requests that target another NUMA node and return from either DRAM or MMIO from another NUMA node, either from the same or different NUMA node.
5	Reserved.
4	NearFarCache_Far. Read-write. Requests that target another NUMA node and return from another CCX's cache.
3	DramIO_Near. Read-write. Requests that target the same NUMA node and return from either DRAM or MMIO from the same NUMA node.
2	NearFarCache_Near. Read-write. Requests that target the same NUMA node and return from another CCX's cache.
1	LocalCcx. Read-write. Data returned from L3 or different L2 in the same CCX.
0	Reserved.

2.1.13.5 L3 Cache Performance Monitor Counters

The L3 cache is organized as eight "slices" of L3 shared by eight cores.

This section provides the core performance counter events that may be selected through Core::X86::Msr::ChL3PmcCfg.

- Unless otherwise noted, Family 19h L3 Perfmon events utilize Core::X86::Msr::ChL3PmcCfg[SliceId] to select an individual slice or Core::X86::Msr::ChL3PmcCfg[EnAllSlices] to select all slices.
- Family 19h L3 Perfmon events utilize Core::X86::Msr::ChL3PmcCfg[CoreId] to select an individual core or Core::X86::Msr::ChL3PmcCfg[EnAllCores] to select all cores.
- Unless otherwise noted, L3 PMC's require Core::X86::Msr::ChL3PmcCfg[CoreId] to be set or the PMC count will be zero.
- When in non-SMT mode, thread 0 must be selected for events that don't ignore ThreadMask.

2.1.13.5.1 L3 Cache PMC Events

L3PMCx04 [L3 tag lookup state] (Core::X86::Pmc::L3::L3LookupState)

Read-write.

All L3 Requests.

L3PMCx04; L3PMC=0000_0000h

Bits	Description												
7:0	L3LookupMask. Read-write. L3 Request Types												
	Valid Values:												
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>00h</td><td>Reserved.</td></tr> <tr> <td>01h</td><td>L3 Miss</td></tr> <tr> <td>FDh-02h</td><td>Reserved.</td></tr> <tr> <td>FEh</td><td>L3 Hit</td></tr> <tr> <td>FFh</td><td>All coherent accesses to L3</td></tr> </table>	Value	Description	00h	Reserved.	01h	L3 Miss	FDh-02h	Reserved.	FEh	L3 Hit	FFh	All coherent accesses to L3
Value	Description												
00h	Reserved.												
01h	L3 Miss												
FDh-02h	Reserved.												
FEh	L3 Hit												
FFh	All coherent accesses to L3												

L3PMCxAC [L3 XiSampledLatency] (Core::X86::Pmc::L3::L3_XiSampledLatency)

Read-write.

When used in conjunction with L3_XiSampledLatencyRequests, this PMC Event will measure the average memory latency (excluding MMIO) observed by this CCX.

Configure two PMCs with the L3_XiSampledLatency and L3_XiSampledLatencyRequests events and use the following equation to identify the observed latency.

$$\text{Average Sampled Latency} = \text{L3_XiSampledLatency} / \text{L3_XiSampledLatencyRequests} * 10\text{ns}$$

Some ChL3PmcCfg fields must be programmed as follows to ensure that these events accurately measure latency: ChL3PmcCfg[EnAllSlices]=0x1 and ChL3PmcCfg[SliceId]=0x3.

Other ChL3PmcCfg fields can be used to filter the measured latency based on originating thread (EnAllCores, CoreID) and Data Source (UnitMask).

To measure average latency from all threads to all Data Sources, use the following configuration:

ChL3PmcCfg[EnAllCores]=0x1, ChL3PmcCfg[ThreadMask]=0x3, and ChL3PmcCfg[UnitMask]=0xFF.

L3PMCxAC; L3PMC=0000_0000h

Bits	Description
7:6	Reserved.
5	Ext_Far. Read-write. Requests that target another NUMA node and return from Extension Memory (CXL™)
4	Ext_Near. Read-write. Requests that target the same NUMA node and return from Extension Memory (CXL)
3	NearCache_FarCache_Far. Read-write. Requests that target another NUMA node and return from another CCX's cache.
2	NearCache_FarCache_Near. Read-write. Requests that target the same NUMA node and return from another CCX's cache.
1	Dram_Far. Read-write. Requests that target another NUMA node and return from DRAM
0	Dram_Near. Read-write. Requests that target the same NUMA node and return from DRAM

L3PMCxAD [L3 XiSampledLatencyRequests] (Core::X86::Pmc::L3::L3_XiSampledLatencyRequests)

Read-write.

When used in conjunction with L3_XiSampledLatency, this PMC Event will measure the average memory latency (excluding MMIO) observed by this CCX.

Configure two PMCs with the L3_XiSampledLatency and L3_XiSampledLatencyRequests events and use the following equation to identify the observed latency.

$$\text{Average Sampled Latency} = \text{L3_XiSampledLatency} / \text{L3_XiSampledLatencyRequests} * 10\text{ns}$$

Some ChL3PmcCfg fields must be programmed as follows to ensure that these events accurately measure latency: ChL3PmcCfg[EnAllSlices]=0x1 and ChL3PmcCfg[SliceId]=0x3.

Other ChL3PmcCfg fields can be used to filter the measured latency based on originating thread (EnAllCores, CoreID) and Data Source (UnitMask).

To measure average latency from all threads to all Data Sources, use the following configuration:

ChL3PmcCfg[EnAllCores]=0x1, ChL3PmcCfg[ThreadMask]=0x3, and ChL3PmcCfg[UnitMask]=0xFF.

L3PMCxAD; L3PMC=0000_0000h

Bits	Description
7:6	Reserved.
5	Ext_Far. Read-write. Requests that target another NUMA node and return from Extension Memory (CXL)
4	Ext_Near. Read-write. Requests that target the same NUMA node and return from Extension Memory (CXL)
3	NearCache_FarCache_Far. Read-write. Requests that target another NUMA node and return from another CCX's cache.
2	NearCache_FarCache_Near. Read-write. Requests that target the same NUMA node and return from another CCX's cache.
1	Dram_Far. Read-write. Requests that target another NUMA node and return from DRAM
0	Dram_Near. Read-write. Requests that target the same NUMA node and return from DRAM

2.1.14 Instruction Based Sampling (IBS)

IBS is a code profiling mechanism that enables the processor to select a random instruction fetch or macro-op after a programmed time interval has expired and record specific performance information about the operation. An interrupt is generated when the operation is complete as specified by Core::X86::Msrr::IBS_CTL. An interrupt handler can then read the performance information that was logged for the operation.

The IBS mechanism is split into two parts: instruction fetch performance controlled by Core::X86::Msrr::IBS_FETCH_CTL; and instruction execution performance controlled by Core::X86::Msrr::IBS_OP_CTL. Instruction fetch sampling provides information about instruction TLB and instruction cache behavior for fetched instructions. Instruction execution sampling provides information about op execution behavior. The data collected for instruction fetch performance is independent from the data collected for instruction execution performance. Support for the IBS feature is indicated by the Core::X86::Cpuid::FeatureExtIdEcX[IBS].

Instruction fetch performance is profiled by recording the following performance information for the tagged instruction fetch:

- If the instruction fetch completed or was aborted. See Core::X86::Msrr::IBS_FETCH_CTL.
- The number of clock cycles spent on the instruction fetch. See Core::X86::Msrr::IBS_FETCH_CTL.
- If the instruction fetch hit or missed the IC, hit/missed in the L1 and L2 TLBs, and page size. See Core::X86::Msrr::IBS_FETCH_CTL.
- The linear address, physical address associated with the fetch. See Core::X86::Msrr::IBS_FETCH_LINADDR, Core::X86::Msrr::IBS_FETCH_PHYSADDR.

Instruction execution performance is profiled by tagging one macro-op associated with an instruction. Instructions that decode to more than one macro-op return different performance data depending upon which macro-op associated with the instruction is tagged. These macro-ops are associated with the RIP of the next instruction to retire. The following performance information is returned for the tagged op:

- Branch and execution status. See Core::X86::Msrb::IBS_OP_DATA.
- Branch target address for branch ops. See Core::X86::Msrb::BP_IBSTGT_RIP.
- The logical address associated with the op. See Core::X86::Msrb::IBS_OP_RIP.
- The linear and physical address associated with a load or store op. See Core::X86::Msrb::IBS_DC_LINADDR, Core::X86::Msrb::IBS_DC_PHYSADDR.
- The data cache access status associated with the op: DC hit/miss, DC miss latency, TLB hit/miss, TLB page size. See Core::X86::Msrb::IBS_OP_DATA3.
- The number clocks from when the op was tagged until the op retires. See Core::X86::Msrb::IBS_OP_DATA.
- The number clocks from when the op completes execution until the op retires. See Core::X86::Msrb::IBS_OP_DATA.
- Source information for DRAM and MMIO. See Core::X86::Msrb::IBS_OP_DATA2.

2.2 L3 Cache

The Level-3 cache (L3) forms the third level of cache in the CPU caching hierarchy. The L3 is a shared, unified cache inside a core complex.

2.2.1 L3 MSR Registers

MSR0000_0C81 [L3 QoS Configuration] (L3::L3CRB::L3QosCfg1)	
Reset: 0000_0000_0000_0000h.	
QOS L3 Cache Allocation CDP mode enable (I vs. D). Contents are copied to ChL2QosCfg1 and ChL3QosCfg1_0.	
_ccd[1:0]_lthree0; MSR0000_0C81	
Bits	Description
63:1	Reserved.
0	CDP. Read-write. Reset: 0. Code and Data Prioritization Technology enable
MSR0000_0C90 [L3 QoS Allocation Mask] (L3::L3CRB::L3QosAllocMask0)	
Reset: 0000_0000_0000_FFFFh.	
QOS L3 Allocation Mask for CLOS0	
_ccd[1:0]_lthree0; MSR0000_0C90	
Bits	Description
63:16	Reserved.
15:0	WayMask. Read-write. Reset: FFFFh. L3 way mask used for allocation control.
MSR0000_0C91 [L3 QoS Allocation Mask] (L3::L3CRB::L3QosAllocMask1)	
Reset: 0000_0000_0000_FFFFh.	
QOS L3 Allocation Mask for CLOS1	
_ccd[1:0]_lthree0; MSR0000_0C91	
Bits	Description
63:16	Reserved.
15:0	WayMask. Read-write. Reset: FFFFh. L3 way mask used for allocation control.

MSR0000_0C92 [L3 QoS Allocation Mask] (L3::L3CRB::L3QosAllocMask2)

Reset: 0000_0000_0000_FFFFh.

QOS L3 Allocation Mask for CLOS2

_ccd[1:0]_lthree0; MSR0000_0C92

Bits Description

63:16 Reserved.

15:0 **WayMask.** Read-write. Reset: FFFFh. L3 way mask used for allocation control.**MSR0000_0C93 [L3 QoS Allocation Mask] (L3::L3CRB::L3QosAllocMask3)**

Reset: 0000_0000_0000_FFFFh.

QOS L3 Allocation Mask for CLOS3

_ccd[1:0]_lthree0; MSR0000_0C93

Bits Description

63:16 Reserved.

15:0 **WayMask.** Read-write. Reset: FFFFh. L3 way mask used for allocation control.**MSR0000_0C94 [L3 QoS Allocation Mask] (L3::L3CRB::L3QosAllocMask4)**

Reset: 0000_0000_0000_FFFFh.

QOS L3 Allocation Mask for CLOS4

_ccd[1:0]_lthree0; MSR0000_0C94

Bits Description

63:16 Reserved.

15:0 **WayMask.** Read-write. Reset: FFFFh. L3 way mask used for allocation control.**MSR0000_0C95 [L3 QoS Allocation Mask] (L3::L3CRB::L3QosAllocMask5)**

Reset: 0000_0000_0000_FFFFh.

QOS L3 Allocation Mask for CLOS5

_ccd[1:0]_lthree0; MSR0000_0C95

Bits Description

63:16 Reserved.

15:0 **WayMask.** Read-write. Reset: FFFFh. L3 way mask used for allocation control.**MSR0000_0C96 [L3 QoS Allocation Mask] (L3::L3CRB::L3QosAllocMask6)**

Reset: 0000_0000_0000_FFFFh.

QOS L3 Allocation Mask for CLOS6

_ccd[1:0]_lthree0; MSR0000_0C96

Bits Description

63:16 Reserved.

15:0 **WayMask.** Read-write. Reset: FFFFh. L3 way mask used for allocation control.**MSR0000_0C97 [L3 QoS Allocation Mask] (L3::L3CRB::L3QosAllocMask7)**

Reset: 0000_0000_0000_FFFFh.

QOS L3 Allocation Mask for CLOS7

_ccd[1:0]_lthree0; MSR0000_0C97

Bits Description

63:16 Reserved.

15:0 **WayMask.** Read-write. Reset: FFFFh. L3 way mask used for allocation control.

MSR0000_0C98 [L3 QoS Allocation Mask] (L3::L3CRB::L3QosAllocMask8)

Reset: 0000_0000_0000_FFFFh.

QOS L3 Allocation Mask for CLOS8

_ccd[1:0]_lthree0; MSR0000_0C98

Bits Description

63:16 Reserved.

15:0 **WayMask.** Read-write. Reset: FFFFh. L3 way mask used for allocation control.**MSR0000_0C99 [L3 QoS Allocation Mask] (L3::L3CRB::L3QosAllocMask9)**

Reset: 0000_0000_0000_FFFFh.

QOS L3 Allocation Mask for CLOS9

_ccd[1:0]_lthree0; MSR0000_0C99

Bits Description

63:16 Reserved.

15:0 **WayMask.** Read-write. Reset: FFFFh. L3 way mask used for allocation control.**MSR0000_0C9A [L3 QoS Allocation Mask] (L3::L3CRB::L3QosAllocMask10)**

Reset: 0000_0000_0000_FFFFh.

QOS L3 Allocation Mask for CLOS10

_ccd[1:0]_lthree0; MSR0000_0C9A

Bits Description

63:16 Reserved.

15:0 **WayMask.** Read-write. Reset: FFFFh. L3 way mask used for allocation control.**MSR0000_0C9B [L3 QoS Allocation Mask] (L3::L3CRB::L3QosAllocMask11)**

Reset: 0000_0000_0000_FFFFh.

QOS L3 Allocation Mask for CLOS11

_ccd[1:0]_lthree0; MSR0000_0C9B

Bits Description

63:16 Reserved.

15:0 **WayMask.** Read-write. Reset: FFFFh. L3 way mask used for allocation control.**MSR0000_0C9C [L3 QoS Allocation Mask] (L3::L3CRB::L3QosAllocMask12)**

Reset: 0000_0000_0000_FFFFh.

QOS L3 Allocation Mask for CLOS12

_ccd[1:0]_lthree0; MSR0000_0C9C

Bits Description

63:16 Reserved.

15:0 **WayMask.** Read-write. Reset: FFFFh. L3 way mask used for allocation control.**MSR0000_0C9D [L3 QoS Allocation Mask] (L3::L3CRB::L3QosAllocMask13)**

Reset: 0000_0000_0000_FFFFh.

QOS L3 Allocation Mask for CLOS13

_ccd[1:0]_lthree0; MSR0000_0C9D

Bits Description

63:16 Reserved.

15:0 **WayMask.** Read-write. Reset: FFFFh. L3 way mask used for allocation control.

MSR0000_0C9E [L3 QoS Allocation Mask] (L3::L3CRB::L3QosAllocMask14)

Reset: 0000_0000_0000_FFFFh.

QOS L3 Allocation Mask for CLOS14

_ccd[1:0]_lthree0; MSR0000_0C9E

Bits Description

63:16 Reserved.

15:0 **WayMask.** Read-write. Reset: FFFFh. L3 way mask used for allocation control.**MSR0000_0C9F [L3 QoS Allocation Mask] (L3::L3CRB::L3QosAllocMask15)**

Reset: 0000_0000_0000_FFFFh.

QOS L3 Allocation Mask for CLOS15

_ccd[1:0]_lthree0; MSR0000_0C9F

Bits Description

63:16 Reserved.

15:0 **WayMask.** Read-write. Reset: FFFFh. L3 way mask used for allocation control.**MSRC000_0200 [L3 QoS Bandwidth Control] (L3::L3CRB::L3QosBwControl0)**

Reset: 0000_0000_0000_0800h.

QOS BW Control0

_ccd[1:0]_lthree0; MSRC000_0200

Bits Description

63:12 Reserved.

11:0 **Ceiling.** Read-write. Reset: 800h. QOS BW Control BW ceiling value**MSRC000_0201 [L3 QoS Bandwidth Control] (L3::L3CRB::L3QosBwControl1)**

Reset: 0000_0000_0000_0800h.

QOS BW Control1

_ccd[1:0]_lthree0; MSRC000_0201

Bits Description

63:12 Reserved.

11:0 **Ceiling.** Read-write. Reset: 800h. QOS BW Control BW ceiling value**MSRC000_0202 [L3 QoS Bandwidth Control] (L3::L3CRB::L3QosBwControl2)**

Reset: 0000_0000_0000_0800h.

QOS BW Control2

_ccd[1:0]_lthree0; MSRC000_0202

Bits Description

63:12 Reserved.

11:0 **Ceiling.** Read-write. Reset: 800h. QOS BW Control BW ceiling value**MSRC000_0203 [L3 QoS Bandwidth Control] (L3::L3CRB::L3QosBwControl3)**

Reset: 0000_0000_0000_0800h.

QOS BW Control3

_ccd[1:0]_lthree0; MSRC000_0203

Bits Description

63:12 Reserved.

11:0 **Ceiling.** Read-write. Reset: 800h. QOS BW Control BW ceiling value

MSRC000_0204 [L3 QoS Bandwidth Control] (L3::L3CRB::L3QosBwControl4)

Reset: 0000_0000_0000_0800h.

QOS BW Control4

_ccd[1:0]_lthree0; MSRC000_0204

Bits Description

63:12 Reserved.

11:0 **Ceiling.** Read-write. Reset: 800h. QOS BW Control BW ceiling value**MSRC000_0205 [L3 QoS Bandwidth Control] (L3::L3CRB::L3QosBwControl5)**

Reset: 0000_0000_0000_0800h.

QOS BW Control5

_ccd[1:0]_lthree0; MSRC000_0205

Bits Description

63:12 Reserved.

11:0 **Ceiling.** Read-write. Reset: 800h. QOS BW Control BW ceiling value**MSRC000_0206 [L3 QoS Bandwidth Control] (L3::L3CRB::L3QosBwControl6)**

Reset: 0000_0000_0000_0800h.

QOS BW Control6

_ccd[1:0]_lthree0; MSRC000_0206

Bits Description

63:12 Reserved.

11:0 **Ceiling.** Read-write. Reset: 800h. QOS BW Control BW ceiling value**MSRC000_0207 [L3 QoS Bandwidth Control] (L3::L3CRB::L3QosBwControl7)**

Reset: 0000_0000_0000_0800h.

QOS BW Control7

_ccd[1:0]_lthree0; MSRC000_0207

Bits Description

63:12 Reserved.

11:0 **Ceiling.** Read-write. Reset: 800h. QOS BW Control BW ceiling value**MSRC000_0208 [L3 QoS Bandwidth Control] (L3::L3CRB::L3QosBwControl8)**

Reset: 0000_0000_0000_0800h.

QOS BW Control8

_ccd[1:0]_lthree0; MSRC000_0208

Bits Description

63:12 Reserved.

11:0 **Ceiling.** Read-write. Reset: 800h. QOS BW Control BW ceiling value**MSRC000_0209 [L3 QoS Bandwidth Control] (L3::L3CRB::L3QosBwControl9)**

Reset: 0000_0000_0000_0800h.

QOS BW Control9

_ccd[1:0]_lthree0; MSRC000_0209

Bits Description

63:12 Reserved.

11:0 **Ceiling.** Read-write. Reset: 800h. QOS BW Control BW ceiling value

MSRC000_020A [L3 QoS Bandwidth Control] (L3::L3CRB::L3QosBwControl10)

Reset: 0000_0000_0000_0800h.

QOS BW Control10

_ccd[1:0]_lthree0; MSRC000_020A

Bits Description

63:12 Reserved.

11:0 **Ceiling.** Read-write. Reset: 800h. QOS BW Control BW ceiling value**MSRC000_020B [L3 QoS Bandwidth Control] (L3::L3CRB::L3QosBwControl11)**

Reset: 0000_0000_0000_0800h.

QOS BW Control11

_ccd[1:0]_lthree0; MSRC000_020B

Bits Description

63:12 Reserved.

11:0 **Ceiling.** Read-write. Reset: 800h. QOS BW Control BW ceiling value**MSRC000_020C [L3 QoS Bandwidth Control] (L3::L3CRB::L3QosBwControl12)**

Reset: 0000_0000_0000_0800h.

QOS BW Control12

_ccd[1:0]_lthree0; MSRC000_020C

Bits Description

63:12 Reserved.

11:0 **Ceiling.** Read-write. Reset: 800h. QOS BW Control BW ceiling value**MSRC000_020D [L3 QoS Bandwidth Control] (L3::L3CRB::L3QosBwControl13)**

Reset: 0000_0000_0000_0800h.

QOS BW Control13

_ccd[1:0]_lthree0; MSRC000_020D

Bits Description

63:12 Reserved.

11:0 **Ceiling.** Read-write. Reset: 800h. QOS BW Control BW ceiling value**MSRC000_020E [L3 QoS Bandwidth Control] (L3::L3CRB::L3QosBwControl14)**

Reset: 0000_0000_0000_0800h.

QOS BW Control14

_ccd[1:0]_lthree0; MSRC000_020E

Bits Description

63:12 Reserved.

11:0 **Ceiling.** Read-write. Reset: 800h. QOS BW Control BW ceiling value**MSRC000_020F [L3 QoS Bandwidth Control] (L3::L3CRB::L3QosBwControl15)**

Reset: 0000_0000_0000_0800h.

QOS BW Control15

_ccd[1:0]_lthree0; MSRC000_020F

Bits Description

63:12 Reserved.

11:0 **Ceiling.** Read-write. Reset: 800h. QOS BW Control BW ceiling value

MSRC000_0280 [L3 QoS Slow Memory Bandwidth Control] (L3::L3CRB::L3QOS_SLOWBW_CONTROL_0)

Reset: 0000_0000_0000_0800h.

QOS SM BW Control0

_ccd[1:0]_lthree0; MSRC000_0280

Bits Description

63:12 Reserved.

11:0 **Ceiling.** Read-write. Reset: 800h. QOS BW Control BW ceiling value**MSRC000_0281 [L3 QoS Slow Memory Bandwidth Control] (L3::L3CRB::L3QOS_SLOWBW_CONTROL_1)**

Reset: 0000_0000_0000_0800h.

QOS SM BW Control1

_ccd[1:0]_lthree0; MSRC000_0281

Bits Description

63:12 Reserved.

11:0 **Ceiling.** Read-write. Reset: 800h. QOS BW Control BW ceiling value**MSRC000_0282 [L3 QoS Slow Memory Bandwidth Control] (L3::L3CRB::L3QOS_SLOWBW_CONTROL_2)**

Reset: 0000_0000_0000_0800h.

QOS SM BW Control2

_ccd[1:0]_lthree0; MSRC000_0282

Bits Description

63:12 Reserved.

11:0 **Ceiling.** Read-write. Reset: 800h. QOS BW Control BW ceiling value**MSRC000_0283 [L3 QoS Slow Memory Bandwidth Control] (L3::L3CRB::L3QOS_SLOWBW_CONTROL_3)**

Reset: 0000_0000_0000_0800h.

QOS SM BW Control3

_ccd[1:0]_lthree0; MSRC000_0283

Bits Description

63:12 Reserved.

11:0 **Ceiling.** Read-write. Reset: 800h. QOS BW Control BW ceiling value**MSRC000_0284 [L3 QoS Slow Memory Bandwidth Control] (L3::L3CRB::L3QOS_SLOWBW_CONTROL_4)**

Reset: 0000_0000_0000_0800h.

QOS SM BW Control4

_ccd[1:0]_lthree0; MSRC000_0284

Bits Description

63:12 Reserved.

11:0 **Ceiling.** Read-write. Reset: 800h. QOS BW Control BW ceiling value**MSRC000_0285 [L3 QoS Slow Memory Bandwidth Control] (L3::L3CRB::L3QOS_SLOWBW_CONTROL_5)**

Reset: 0000_0000_0000_0800h.

QOS SM BW Control5

_ccd[1:0]_lthree0; MSRC000_0285

Bits Description

63:12 Reserved.

11:0 **Ceiling.** Read-write. Reset: 800h. QOS BW Control BW ceiling value

MSRC000_0286 [L3 QoS Slow Memory Bandwidth Control] (L3::L3CRB::L3QOS_SLOWBW_CONTROL_6)

Reset: 0000_0000_0000_0800h.

QOS SM BW Control6

_ccd[1:0]_lthree0; MSRC000_0286

Bits Description

63:12 Reserved.

11:0 **Ceiling.** Read-write. Reset: 800h. QOS BW Control BW ceiling value**MSRC000_0287 [L3 QoS Slow Memory Bandwidth Control] (L3::L3CRB::L3QOS_SLOWBW_CONTROL_7)**

Reset: 0000_0000_0000_0800h.

QOS SM BW Control7

_ccd[1:0]_lthree0; MSRC000_0287

Bits Description

63:12 Reserved.

11:0 **Ceiling.** Read-write. Reset: 800h. QOS BW Control BW ceiling value**MSRC000_0288 [L3 QoS Slow Memory Bandwidth Control] (L3::L3CRB::L3QOS_SLOWBW_CONTROL_8)**

Reset: 0000_0000_0000_0800h.

QOS SM BW Control8

_ccd[1:0]_lthree0; MSRC000_0288

Bits Description

63:12 Reserved.

11:0 **Ceiling.** Read-write. Reset: 800h. QOS BW Control BW ceiling value**MSRC000_0289 [L3 QoS Slow Memory Bandwidth Control] (L3::L3CRB::L3QOS_SLOWBW_CONTROL_9)**

Reset: 0000_0000_0000_0800h.

QOS SM BW Control9

_ccd[1:0]_lthree0; MSRC000_0289

Bits Description

63:12 Reserved.

11:0 **Ceiling.** Read-write. Reset: 800h. QOS BW Control BW ceiling value**MSRC000_028A [L3 QoS Slow Memory Bandwidth Control] (L3::L3CRB::L3QOS_SLOWBW_CONTROL_10)**

Reset: 0000_0000_0000_0800h.

QOS SM BW Control10

_ccd[1:0]_lthree0; MSRC000_028A

Bits Description

63:12 Reserved.

11:0 **Ceiling.** Read-write. Reset: 800h. QOS BW Control BW ceiling value**MSRC000_028B [L3 QoS Slow Memory Bandwidth Control] (L3::L3CRB::L3QOS_SLOWBW_CONTROL_11)**

Reset: 0000_0000_0000_0800h.

QOS SM BW Control11

_ccd[1:0]_lthree0; MSRC000_028B

Bits Description

63:12 Reserved.

11:0 **Ceiling.** Read-write. Reset: 800h. QOS BW Control BW ceiling value

MSRC000_028C [L3 QoS Slow Memory Bandwidth Control] (L3::L3CRB::L3QOS_SLOWBW_CONTROL_12)

Reset: 0000_0000_0000_0800h.

QOS SM BW Control12

_ccd[1:0]_lthree0; MSRC000_028C

Bits	Description
63:12	Reserved.
11:0	Ceiling. Read-write. Reset: 800h. QOS BW Control BW ceiling value

MSRC000_028D [L3 QoS Slow Memory Bandwidth Control] (L3::L3CRB::L3QOS_SLOWBW_CONTROL_13)

Reset: 0000_0000_0000_0800h.

QOS SM BW Control13

_ccd[1:0]_lthree0; MSRC000_028D

Bits	Description
63:12	Reserved.
11:0	Ceiling. Read-write. Reset: 800h. QOS BW Control BW ceiling value

MSRC000_028E [L3 QoS Slow Memory Bandwidth Control] (L3::L3CRB::L3QOS_SLOWBW_CONTROL_14)

Reset: 0000_0000_0000_0800h.

QOS SM BW Control14

_ccd[1:0]_lthree0; MSRC000_028E

Bits	Description
63:12	Reserved.
11:0	Ceiling. Read-write. Reset: 800h. QOS BW Control BW ceiling value

MSRC000_028F [L3 QoS Slow Memory Bandwidth Control] (L3::L3CRB::L3QOS_SLOWBW_CONTROL_15)

Reset: 0000_0000_0000_0800h.

QOS SM BW Control15

_ccd[1:0]_lthree0; MSRC000_028F

Bits	Description
63:12	Reserved.
11:0	Ceiling. Read-write. Reset: 800h. QOS BW Control BW ceiling value

MSRC001_023[1...B] [L3 Performance Monitor Counter] (L3::L3CRB::ChL3Pmc)

Read-write, Volatile. Reset: 0000_0000_0000_0000h.

L3 Performance Monitor Counter Register 0

_ccd[1:0]_lthree0_n0; MSRC001_0231

_ccd[1:0]_lthree0_n1; MSRC001_0233

_ccd[1:0]_lthree0_n2; MSRC001_0235

_ccd[1:0]_lthree0_n3; MSRC001_0237

_ccd[1:0]_lthree0_n4; MSRC001_0239

_ccd[1:0]_lthree0_n5; MSRC001_023B

_ccd0_lthree0_n[5:0]_aliasSMN; L3CRB00x0000_04[C8,C0,B8,B0,A8,A0]; L3CRB00=2035_0400h

_ccd1_lthree0_n[5:0]_aliasSMN; L3CRB10x0000_04[C8,C0,B8,B0,A8,A0]; L3CRB10=20B5_0400h

Bits	Description
63:49	Reserved.
48	Overflow. Read-write, Volatile. Reset: 0. Counter overflow bit
47:32	CountHi. Read-write, Volatile. Reset: 0000h. Bits 47:32 of the count
31:0	CountLo. Read-write, Volatile. Reset: 0000_0000h. Bits 31:0 of the count

MSRC001_1095 [L3 Cache Range Reserve Base Address] (L3::L3CRB::L3RangeReserveBaseAddr)

Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0; MSRC001_1095

Bits	Description
63:52	Reserved.
51:12	Addr. Read-write. Reset: 00_0000_0000h. Base physical address bits 51:12 for the locked range.
11:0	Reserved.

MSRC001_1096 [L3 Cache Range Reserve Maximum Address] (L3::L3CRB::L3RangeReserveMaxAddr)

Reset: 0000_0000_0000_0000h.

_ccd[1:0]_lthree0; MSRC001_1096

Bits	Description
63:52	Reserved.
51:12	Addr. Read-write. Reset: 00_0000_0000h. Max physical address bits 51:12 for the locked range.
11:1	Reserved.
0	En. Read-write. Reset: 0. 0=Disable L3 Range Reservation. 1=Enable L3 Range Reservation. Enables the L3 range reservation when set.

MSRC001_109A [L3 Cache Range Reservation Way Mask] (L3::L3CRB::L3RangeReserveWayMask)

Reset: 0000_0000_0000_0000h.

Way mask used to specify which L3 cache ways are used for range reservation

_ccd[1:0]_lthree0; MSRC001_109A

Bits	Description
63:16	Reserved.
15:0	Mask. Read-write. Reset: 0000h. L3 ways used for range reservation.

2.2.2 L3 Clocks and Test (CT) MSR Registers.**MSRC001_0299 (L3::L3CT::L3RAPLPowerUnit0)**

Read-only. Reset: 0000_0000_0000_0000h.

L3 RAPL Power Unit 0

_ccd[1:0]_lthree0; MSRC001_0299

Bits	Description
63:20	Reserved.
19:16	TimeUnits. Read-only. Reset: 0h. Time information (in Seconds) is based on the multiplier, $1/2^{TU}$ where TU is unsigned integer. Default value is 1010b, indicating time unit is in 976 microseconds increment
15:13	Reserved.
12:8	EnergyStatusUnits. Read-only. Reset: 00h. Energy information (in Joules) is based on the multiplier, $1/2^{ESU}$ where ESU is unsigned integer. Default value is 10000b, indicating energy status unit is in 15.3 micro-Joules increment
7:4	Reserved.
3:0	PowerUnits. Read-only. Reset: 0h. Power information (in Watts) is based on the multiplier, $1/2^{PU}$ where PU is an unsigned integer. Default value is 0011b, indicating power unit is in 1/8 Watts increment

MSRC001_029B (L3::L3CT::L3PackageEnergyStatus)

Read-only. Reset: 0000_0000_0000_0000h.

L3 Package Energy Status 0

_ccd[1:0]_lthree0; MSRC001_029B

Bits	Description
63:0	<p>TotalEnergyConsumed. Read-only. Reset: 0000_0000_0000_0000h.</p> <p>Description: Total Energy consumed since the last time the register is cleared. It reports the actual energy use for respective power domain. This MSR is updated every ~1ms. Energy status is free running. Users calculate power for a given domain by calculating dEnergy/dTime for that domain. Users must ensure successive reads contain at least one, but preferably many energy status updates by hardware. Readable/writable field for use by SMU.</p>

3 Reliability, Availability, and Serviceability (RAS) Features

A full implementation of RAS involves capabilities and support from the processor design, board hardware design, BIOS, firmware, and software.

3.1 Machine Check Architecture

Table 21: Machine Check Terms and Acronyms

Term	Description
MCA	Machine Check Architecture.
MCAX	Machine Check Architecture eXtensions.
WRIG	Writes Ignored.

3.1.1 Overview

The processor contains logic and registers to detect, log, and correct errors in the data or control paths. The Machine Check Architecture (MCA) defines facilities by which processor and system hardware errors are logged and reported to system software. This allows system software to perform a strategic role in recovery from and diagnosis of hardware errors.

3.1.1.1 Legacy Machine Check Architecture

The legacy x86 Machine Check Architecture (MCA) refers to the standard x86 facilities for error logging and reporting. Refer to the AMD64 Architecture Programmer's Manual for an architectural overview of the Machine Check Architecture.

Support for the MCA is indicated by Core::X86::Cpuid::FeatureIdEdx[MCA] or Core::X86::Cpuid::FeatureExtIdEdx[MCA].

3.1.1.2 Machine Check Architecture Extensions

Machine Check Architecture Extensions (MCAX) is AMD's x86-64 extension to the Machine Check Architecture.

Goals of MCAX include:

- Accommodate a variety of implementations, where each implementation may have a different assignment of MCA bank to block.
 - For example, one implementation may have 1 memory channel with an MCA bank, and another otherwise identical implementation may have 2 memory channels, each with their own MCA bank. Therefore, MCA bank allocation will appear different between these two implementations. MCAX is designed to require no assumptions about which MCA banks access which blocks.
 - Provide granular information for error logging, to improve error handling and diagnosability.
 - Preserve compatibility with system software which is not MCAX-aware.

Features of the MCA Extensions include:

- Increased MCA Bank Count: Features to support an expansion of the number of MCA banks supported by AMD processors.
- MCA Extension Registers: Expanded information logged in MCA banks to allow for improved error handling, better diagnosability, and future scalability.
- MCA DOER/SEER Roles: Separation of MCA information to take advantage of emerging software roles, namely

Error Management (Dynamic Operational Error Handling, or DOER) for managing running programs, and Fault Management (Symptom Elaboration of Errors, or SEER) for hardware diagnosability and reconfiguration. This clearer separation is accompanied by the assurances of architectural state (vs. implementation dependent state), so that operating systems can rely on the state and exploit new functionality.

Support for Machine Check Architecture Extensions (MCAX) is indicated by Core::X86::Cpuid::RasCap[ScalableMca].

3.1.1.3 Use of MCA Information

The MCA registers contain information that can be used for multiple purposes. Some of this information is architecturally specified, and remains consistent from generation to generation, enabling portable, stable code. Some of this information is implementation specific; it is vital for diagnosis and other software functions, but may change with new implementations. It is important to understand how this information is categorized, and how it should be used. This section describes a framework for that.

There are two fundamental roles to be carried out after an error occurs; Error Management and Fault Management. All information required for Error Management is architectural and stable; some information required for Fault Management is also architectural.

3.1.1.3.1 Error Management

Error Management describes actions necessary by operational software (e.g., the operating system or the hypervisor) to manage running programs that are affected by the error. The list of possible actions for operational error management is generally fairly short: take no action; terminate a single affected process, program, or virtual machine; terminate system operation. The Error Management role is defined as the DOER role (Dynamic Operational Error Handling). The name is intended to indicate an active role in managing running programs. Information used by the DOER is fairly limited and straightforward. It includes only those status fields needed to make decisions about the scope and severity of the error, and to determine what immediate action is to be taken.

3.1.1.3.2 Fault Management

Fault Management describes optional actions for purposes of diagnosis, repair, and reconfiguration of the underlying hardware. The Fault Management role is described as SEER (Symptom Elaboration of Errors) because it peers further into hardware behavior and may try to influence future behavior via Predictive Fault Analysis, reconfiguration, service actions, etc. Because the SEER depends on understanding specifics of hardware configuration, it necessarily requires implementation specific knowledge and may not be portable across implementations.

Fields that are not explicitly specified as DOER are SEER. By separating error handling software into DOER and SEER roles, programmers can create both simpler and more functional code. The terms DOER and SEER appear in other sections of this document as an aid to reasoning about error handling and understanding actions to be taken.

3.1.2 Machine Check Registers

Host software references MCA registers via MSRs. MSRs are accessed through x86 WRMSR and RDMSR instructions. MSR addresses are private to a logical core; a given MSR referenced by two different cores results in references to two different MCA registers.

3.1.2.1 Global Registers

Core::X86::Cpuid::FeatureIdEdx[MCA] or Core::X86::Cpuid::FeatureExtIdEdx[MCA] indicates the presence of the following machine check registers:

- Core::X86::Msr::MCG_CAP
 - Reports how many machine check register banks are supported. This value reflects the number of MCA banks visible to that logical core. Some banks may be RAZ/WRIG either due to the bank being reserved or unused on this processor or because the block's MCA bank is controlled by another logical core.
- Core::X86::Msr::MCG_STAT
 - Provides basic information about processor state after the occurrence of a machine check error.
- Core::X86::Msr::MCG_CTL
 - Used by software to enable or disable the logging and reporting of machine check errors in the error reporting banks. Some bits may be RAZ/WRIG either due to the bank being reserved or unused on this processor or because the block's MCA bank is controlled by another logical core.
- Core::X86::Msr::McaIntrCfg
 - Used by software to configure certain machine check interrupts.

3.1.2.2 Machine Check Banks

A processor contains multiple blocks, and some of them have banks of machine check architecture registers (MCA banks). An MCA bank logs and reports errors to software.

The legacy MCA supports up to 32 MCA banks per logical core. MCAX supports up to 64 MCA banks per logical core.

The processor ensures that non-zero error status in an MCA bank is visible to exactly one logical core in a system, and that error notifications are directed to that logical core. Hardware also makes MCA bank configuration and control registers available to exactly one logical core. Banks associated with a CPU core are controlled by that logical core. Banks associated with other blocks are controlled by an implementation-specific logical core.

3.1.2.2.1 Legacy MCA Registers

Each legacy MCA bank allocates address space for 4 legacy MCA registers.

The legacy MCA registers include:

- MCA_CTL
 - Enables error reporting via machine check exception.
- MCA_STATUS
 - Logs information associated with errors.
- MCA_ADDR
 - Logs address information associated with errors.
- MCA_MISC0
 - Logs miscellaneous information associated with errors.

3.1.2.2.2 Legacy MCA MSRs

The legacy MCA MSRs are MSR0000_04[7F:00]. The legacy MCA MSR space contains 32 banks of 4 registers per bank. The layout of the legacy MCA MSR space is given in Table 22 [Legacy MCA MSR Layout].

Table 22: Legacy MCA MSR Layout

MCA bank (decimal)	MCA_CTL (MSR0000_0xxx)	MCA_STATUS	MCA_ADDR	MCA_MISC0
0	400	401	402	403
1	404	405	406	407
2	408	409	40A	40B
3	40C	40D	40E	40F

4	410	411	412	413
5	414	415	416	417
6	418	419	41A	41B
...				
31	47C	47D	47E	47F

Features and registers associated with the MCA Extensions are not available in this legacy MSR address range. AMD recommends that operating systems use the MCAX MSR address range, rather than rely on the legacy MCA MSR address range.

All unimplemented or unused registers in the legacy MCA MSR address range are RAZ/WRIG. MC4 registers (MSR0000_0410:0000_0413) are RAZ/WRIG.

MSR0000_0000 is aliased to the MCAX MSR address for MC0_ADDR, and MSR0000_0001 is aliased to the MCAX MSR address of MC0_STATUS.

3.1.2.2.3 MCAX Registers

Each MCAX bank allocates address space for 16 MCA registers. All unimplemented registers in the MCA MSR space are RAZ/WRIG. MCAX bank registers include the legacy MCA registers as well as registers associated with the MCA Extensions.

The MCA Extension registers include:

- MCA_CONFIG
 - Provide configuration capabilities for this MCA bank.
- MCA_IPID
 - Provides information on the block associated with this MCA bank.
- MCA_SYND
 - Logs physical location information associated with a logged error.
- MCA_DESTATUS
 - Logs status information associated with a deferred error.
- MCA_DEADDR
 - Logs address information associated with a deferred error.
- MCA_MISC[1:4]
 - Provides additional threshold counters within an MCA bank.
- MCA_SYND1 & MCA_SYND2
 - Log information associated with a logged error, such as FruText.

3.1.2.2.4 MCAX MSRs

MCAX MSRs are present at MSRC000_2[3FF:000]. This MSR address range contains space for 64 banks of 16 registers each. MSRC000_2[FFF:400] are Reserved for future use. The MCAX MSR address range allows access to both legacy MCA registers and MCAX registers in each MCA bank.

The x86 MCAX MSR address format is SSSS_SBBR (hex). S=MCA register space (i.e., MSRC000_2XXX). B=MCA bank. R=Register offset within MCA bank. The layout of the MCAX MSR space is given in Table 23 [MCAX MSR Layout].

Access to unused MCAX MSRs is RAZ/WRIG. MCA Bank 4 is always Read-as-zero (RAZ/WRIG).

Table 23: MCAX MSR Layout

MCA bank	MCAX MSR (MSRC000_2xxx)												
	Legacy MCA Bank registers				MCAX Bank registers								
	CTL	STATUS	ADDR	MISC0	CONFIG	IPID	SYND	Reserved	DESTAT	DEADDR	MISC[4:1]	SYND1	SYND2
0	000	001	002	003	004	005	006	007	008	009	00D:00A	00E	00F
1	010	011	012	013	014	015	016	017	018	019	01D:01A	01E	01F
2	020	021	022	023	024	025	026	027	028	029	02D:02A	02E	02F
...													
63	3F0	3F1	3F2	3F3	3F4	3F5	3F6	3F7	3F8	3F9	3FD:3FA	3FE	3FF

All processors maintain the same mapping of MSR to MCA bank number (MSRC000_2000 for the beginning of MCA Bank 0, MSRC000_2010 for the beginning of MCA Bank 1, etc.), regardless of what block the bank represents (see 3.1.5.5 [Determining Bank Type]).

MCA_CTL_MASK MSRs are present at MSRC001_04[3F:00]. MSRC001_04[FF:40] are Reserved for future use. The layout of these registers is given in Table 24 [MCAX Implementation-Specific Register Layout].

Table 24: MCAX Implementation-Specific Register Layout

MCA bank	MCA_CTL_MASK (MSRC001_04xx)
0	00
1	01
2	02
...	
63	3F

3.1.2.3 Access Permissions

When McStatusWrEn == 0, a Write to an implemented MCA_STATUS register causes a General Protection Fault (#GP) unless the value being written is zero. When McStatusWrEn == 1, a Write to an implemented MCA_STATUS register does not cause a #GP regardless of data value.

Access to legacy MCA_CTL_MASK (MSRC001_00xx) causes a General Protection Fault (#GP).

Access to legacy MC4_MISC1-8 (MSRC000_0408:C000_040F) is RAZ/WRIG.

3.1.3 Machine Check Errors

3.1.3.1 Error Severities

The classes of machine check errors are, in priority order from highest to lowest:

- Uncorrected
- Deferred
- Corrected

Uncorrected errors cannot be corrected by hardware. Uncorrected errors update the status and address registers if not masked from logging in MCA_CTL_MASK. Information in the status and address registers from a previously logged lower priority error is overwritten. Previously logged errors of the same priority are not overwritten. Uncorrected errors that are enabled for reporting in MCA_CTL result in reporting to software via machine check exceptions. If an uncorrected error is masked from logging, the error is ignored by hardware (exceptions are noted in the register definitions). If an uncorrected error is disabled from reporting, containment of the error and logging/reporting of subsequent errors may be affected. Therefore, enable reporting of unmasked uncorrected errors for normal operation. Disable reporting of uncorrected errors only for debug purposes.

Deferred errors are errors that cannot be corrected by hardware, but do not cause an immediate interruption in program flow, loss of data integrity, or corruption of processor state. These errors indicate that data has been corrupted but not consumed; no exception is generated because the data has not been referenced by a core or an IO link. Hardware writes information to the status and address registers in the corresponding bank that identifies the source of the error if deferred errors are enabled for logging. If there is information in the status and address registers from a previously logged lower priority error, it is overwritten. Previously logged errors of the same or higher priority are not overwritten. Deferred errors are not reported via machine check exceptions; they can optionally be reported via LVT or SMI.

Corrected errors are those which have been corrected by hardware and cause no loss of data or corruption of processor state. Hardware writes the status and address registers in the corresponding register bank with information that identifies the source of the error if they are enabled for logging. Corrected errors are not reported via machine check exceptions. Some corrected errors may optionally be reported to software via LVT or SMI if the number of errors exceeds a configurable threshold.

An error to be logged when the status register contains valid data can result in an overflow condition. During error overflow conditions, the new error may not be logged or an error which has already been logged in the status register may be overwritten.

Table 25 [Error Overwrite Priorities] indicates which errors are overwritten in the error status registers.

Table 25: Error Overwrite Priorities

		Older Error		
		Uncorrected	Deferred	Corrected
Newer	Uncorrected	-	Overwrite	Overwrite
	Deferred	-	-	Overwrite

Error	Corrected	-	-	-
-------	-----------	---	---	---

Table 26 [Error Scope Hierarchy] provides a hierarchy of error scopes that determine the potential ability to recover the system based on fields in MCA_STATUS when MCA_STATUS[Val] == 1.

Table 26: Error Scope Hierarchy

PCC	UC	TCC	Deferred	Comments
1	X	X	X	Uncorrected system fatal error. Action required. A hardware-uncorrected error has corrupted system state. The error is fatal to the system and the system processing must be terminated.
0	1	1	X	Uncorrected thread fatal error. Action required. A hardware-uncorrected error has corrupted state for the process thread executing on the interrupted logical core. State for other process threads is unaffected.
0	1	0	X	Uncorrected recoverable error. Action required. A hardware-uncorrected error has not corrupted state of the process thread. Recovery of the process thread is possible if the uncorrected error is corrected by software.
0	0	0	1	Deferred error. Action optional. A hardware-uncorrected error has been discovered but not yet consumed. Error handling software may attempt to correct this error, or prevent access by processes which map the data, or make the physical resource containing the data inaccessible.
0	0	0	0	Corrected error. Action optional. A hardware-corrected error has been corrected. No action is required by error handling software.

3.1.3.2 Exceptions and Interrupts

Some or all errors logged in the MCA may require an interrupt or exception to be signaled.

The processor supports the following x86 interrupt/exception types to be communicated to the x86 core in response to an error:

- Machine Check Exception (MCE)
- System Management Interrupt (SMI)
- APIC based interrupt (LVT)

MCEs can be architecturally precise, context-synchronous, or asynchronous. An MCE that sets Core::X86::Msr::MCG_STAT[RIPV] = 1 and Core::X86::Msr::MCG_STAT[EIPV] = 1 is precise and the program can be restarted reliably. Other interrupts are architecturally asynchronous.

The ability of hardware to generate a machine check exception upon an error is indicated by Core::X86::Cpuid::FeatureIdEdx[MCE] or Core::X86::Cpuid::FeatureExtIdEdx[MCE].

3.1.3.3 Error Codes

The MCA_STATUS[ErrorCode] field contains information used to identify the logged error. This section identifies how to decode the ErrorCode field.

Table 27: Error Code Types

Error Code	Error Code Type	Description
------------	-----------------	-------------

0000 0000 0001 TTLL	TLB	TT = Transaction Type LL = Cache Level
0000 0001 RRRR TTLL	Memory	RRRR = Memory Transaction Type TT = Transaction Type LL = Cache Level
0000 1XXT RRRR XXLL	Bus	XX = Reserved T = Timeout RRRR = Memory Transaction Type LL = Cache Level
0000 01UU 0000 0000	Internal Unclassified	UU = Internal Error Type

Table 28: Error code: transaction type (TT)

TT	Transaction Type
00	Instruction
01	Data
10	Generic
11	Reserved

Table 29: Error codes: cache level (LL)

LL	Cache Level
00	L0: Core
01	L1: Level 1
10	L2: Level 2
11	LG: Generic

Table 30: Error codes: memory transaction type (RRRR)

RRRR	Memory Transaction Type
0000	Generic
0001	Generic Read
0010	Generic Write
0011	Data Read
0100	Data Write
0101	Instruction Fetch
0110	Prefetch
0111	Evict
1000	Snoop (Probe)

Errors can also be identified by the MCA_STATUS[ErrorCodeExt] field. MCA_STATUS[ErrorCodeExt] indicates which bit position in the corresponding MCA_CTL register enables error reporting for the logged error. For instance, MCA_STATUS[ErrorCodeExt] == 0x9 means that the logged error is enabled by MCA_CTL[9], and the description of MCA_CTL[9] contains information on decoding the error log. Specific ErrorCodeExt values are implementation dependent, and should not be used by architectural or portable code.

3.1.3.4 Extended Error Codes

The MCA_STATUS[ErrorCodeExt] field contains additional information used to identify the logged error. Error positions in MCA_CTL and MCA_CTL_MASK and Extended Error Codes are fixed within a given bank type. That is, for an MCA bank with a given MCA_IPID[HwId, McaType] value, the processor ensures that the same error is reported in a given bit

position of of MCA_CTL regardless of the product in which that bank appears. Similarly, for an MCA bank with a given MCA_IPID[HwId, McaType] value, hardware ensures that the mapping of errors to Extended Error Codes is consistent across products.

3.1.3.5 DOER and SEER State

The DOER fields are:

- MCG_STAT
 - Count
 - MCIP
 - RIPV
 - EIPV
- MCA_STATUS
 - Val
 - PCC
 - TCC
 - UC
 - MiscV
 - AddrV

The MCA_STATUS[Deferred] bit is used for SEER functionality but is architectural.

3.1.3.6 MCA Overflow Recovery

MCA Overflow Recovery is a feature allowing recovery of the system when the overflow bit is set. MCA Overflow Recovery is supported when `Core::X86::Cpuid::RasCap[McaOverflowRecov] == 1`.

When MCA Overflow Recovery is supported, software may rely on `MCA_STATUS[PCC] == 1` to indicate all system-fatal conditions. When MCA Overflow Recovery is not supported, an uncorrected error logged with `MCA_STATUS[Overflow] = 1` may indicate the system-fatal condition that an error requiring software intervention was not logged. Therefore, software must terminate system processing whenever an uncorrected error is logged with `MCA_STATUS[Overflow] = 1`.

3.1.3.7 MCA Recovery

MCA Recovery is a feature allowing recovery of the system when the hardware cannot correct an error. MCA Recovery is supported when `Core::X86::Cpuid::RasCap[SUCCOR] == 1`.

When MCA Recovery is supported and an uncorrected error has been detected that the hardware can contain to the task or process to which the machine check has been delivered, it logs a context-synchronous uncorrectable error (`MCA_STATUS[UC] = 1`, `MCA_STATUS[PCC] = 0`). The rest of the system is unaffected and may continue running if supervisory software can terminate only the affected process or VM.

3.1.4 Machine Check Features

3.1.4.1 Error Thresholding

For some types of errors, the hardware maintains counts of the number of errors. When the counter reaches a programmable threshold, an event may optionally be triggered to signal system software. This is known as error

thresholding. The primary purpose of error thresholding is to help software recognize an excessive rate of errors, which may indicate marginal or failing hardware. This information can be used to make decisions about deconfiguring hardware or scheduling service actions. The error count is incremented for corrected, deferred, and uncorrected errors.

The MCA_MISCx registers contain the architectural interface for error thresholding. The registers contain a 12-bit error counter that can be initialized to any value except FFFh, with the option to interrupt when the counter reaches FFFh.

MCA_MISCx[ThresholdIntType] determines the type of interrupt to be generated for threshold overflow errors in that counter. This can be set to None, LVT, or SMI. If this is set to LVT, Core::X86::Msr::McaIntrCfg[ThresholdLvtOffset] specifies the LVT offset that is used. Only one LVT offset is used per socket and the interrupt is routed to the APIC of the logical core from which the MCA bank is visible.

3.1.4.2 Error Simulation

Error simulation involves creating the appearance to software that an error occurred, and can be used to debug machine check interrupt handlers. See Core::X86::Msr::HWCR[McStatusWrEn] for making MCA registers writable for non-zero values. When McStatusWrEn is set, privileged software can write non-zero values to the specified registers without generating exceptions, and then simulate a machine check using the INT18 instruction (INTn instruction with an operand of 18). Setting a reserved bit in these registers does not generate an exception when this mode is enabled. However, setting a reserved bit may result in undefined behavior.

3.1.5 Software Guidelines

3.1.5.1 Recognizing MCAX Support

Software which reads the MCA registers must recognize whether an implementation uses the legacy format or the MCAX format. This is accomplished by starting with CPUID Fn8000_0007_EBX[ScalableMca]. If ScalableMca == 1, then the implementation supports the MCAX indicator (MCA_CONFIG[Mcax]). An MCA bank is an MCAX bank if MCA_CONFIG[Mcax] == 1 in that bank.

3.1.5.2 Communicating MCAX Support

Software which supports MCAX must set MCA_CONFIG[McaxEn] = 1 in each MCA bank.

Software that supports MCAX should use the MCAX MSRs to access both legacy and MCAX registers.

3.1.5.3 Machine Check Initialization

The following initialization sequence must be followed:

- Platform firmware must initialize the MCA_CTL_MASK registers prior to the initialization of the MCA_CTL registers and Core::X86::Msr::MCG_CTL. Platform firmware and the operating system must not clear MCA_CTL_MASK bits that are set to 1. MCA_CTL_MASK registers must be set the same across all cores.
- The operating system must initialize the MCA_CONFIG registers prior to initialization of the MCA_CTL registers.
- The MCA_CTL registers must be initialized prior to enabling the error reporting banks in MCG_CTL.
- The Core::X86::Msr::MCG_CTL register must be programmed identically for all cores in a processor, although the Read-write bits may differ per core.
- CR4.MCE must be set to enable machine check exceptions.

The operating system should configure the MCA_CONFIG registers as follows:

- MCA_CONFIG[McaXEn] = 1 if the operating system has been updated to use the MCA Extension MSR addresses. Otherwise, the operating system should preserve the platform firmware-programmed value of this field.
- MCA_CONFIG[LogDeferredInMcaStat] and MCA_CONFIG[DeferredIntType] to appropriate values based on OS support for deferred errors.

MCA_STATUS MSRs are cleared by hardware after a cold reset. If initializing after a warm reset, then platform firmware should check for valid MCA errors and if present save the status for later diagnostic use.

Platform firmware may initialize the MCA without setting CR4.MCE; this results in a shutdown on any machine check which would have caused a machine check exception (followed by a reboot if configured). Alternatively, platform firmware that wishes to ensure continued operation in the event that a machine check occurs during boot may write MCG_CTL with all ones and write zeros into each MCA_CTL register. With these settings, a machine check error results in MCA_STATUS being written without generating a machine check exception or a shutdown. Platform firmware may then poll MCA_STATUS registers during critical sections of boot to ensure system integrity. Note that the system may be operating with corrupt data before polling MCA_STATUS registers. Before passing control to the operating system, platform firmware should restore the values of those registers to what the operating system is expecting.

After MCA initialization, system software should check the Val bit on each MCA_STATUS register. It is possible that valid error status information has already been logged in the MCA_STATUS registers at the time software is attempting to initialize them. The status can reflect errors logged prior to a warm reset or errors recorded during the system power-up and boot process. Before clearing the MCA_STATUS registers, software should examine their contents and log any errors found.

3.1.5.4 Determining Bank Count

System software should read Core::X86::Msrr::MCG_CAP[Count] to determine the number of machine check banks visible to a logical core. The banks are numbered from 0 to one less than the value found in Core::X86::Msrr::MCG_CAP[Count]. For example, if the Count field indicates five banks are supported, they are numbered MC0 through MC4.

3.1.5.5 Determining Bank Type

To determine which type of block is mapped to an MCA bank, software can query the MCA_IPID register within that bank. This register exists when MCA_CONFIG[McaX] == 1 in a given bank.

MCA_IPID[HardwareID] provides the block type for the block that contains this MCA bank. For blocks that contain multiple MCA bank types (e.g., CPU cores), MCA_IPID[McaType] provides an identifier for the type of MCA bank. MCA_IPID[McaType] values are specific to a given MCA_IPID[HardwareID]. Therefore, an MCA bank type can be identified by the value of {MCA_IPID[Hwid], MCA_IPID[McaType]}. For instance, the CPU core's LS bank is identified by MCA::LS::MCA_IPID_LS[HardwareID] == 176 and MCA::LS::MCA_IPID_LS[McaType] == 0. An MCA_IPID[HardwareID] value of 0 indicates an unpopulated MCA bank that is ensured to be RAZ/WRIG.

MCA_IPID[InstanceId] provides a unique instance number to allow software to differentiate blocks with multiple identical instances within a processor. MCA_IPID[InstanceId] values are processor-specific and are not ensured to be stable across different processor generations.

3.1.5.6 Recognizing Error Type

Software can use the combination of MCA_IPID[Hwid, McaType] and MCA_STATUS[ErrorCodeExt] to recognize a specific error type.

3.1.5.7 Machine Check Error Handling

A machine check handler is invoked to handle an exception for a particular thread. The information needed by the machine check handler is not shared with other threads, so no cross-thread coordination or special handling is required. Specifically, all MCA banks are only visible from a single thread, so software on a single thread can access each bank through MSR space without contention from other threads.

At a minimum, the machine check handler must be capable of logging error information for later examination. The handler should log as much information as is needed to diagnose the error. More thorough exception handler implementations can analyze errors to determine if each error is recoverable by software. If a recoverable error is identified, the exception handler can attempt to correct the error and restart the interrupted program. An error may not be recoverable for the process or virtual machine it directly affects, but may be containable, so that other processes or virtual machines in the system are unaffected and system operation is recovered.

Machine check exception handlers that attempt to recover must be thorough in their analysis and the corrective actions they take. The following guidelines should be used when writing such a handler:

- Data collection:
 - Read Core::X86::Msr::MCG_CAP[Count] to determine the number of status registers visible to the logical core.
 - All status registers in all error reporting banks must be examined to identify the cause of the machine check exception.
 - Check the valid bit in each status register (MCA_STATUS[Val]). The remainder of the status register should be examined only when its valid bit is set.
 - When identifying the error condition and determining how to handle the error, portable exception handlers should examine only DOER fields in machine check registers.
 - Error handlers should collect all available MCA information, but should only interrogate details to the level which affects their actions. Lower level details may be useful for diagnosis and root cause analysis, but not for error handling.
 - Error handlers should save the values in MCA_ADDR, MCA_MISC0, and MCA_SYND even if MCA_STATUS[AddrV], MCA_STATUS[MiscV], and MCA_STATUS[SyndV] are zero. Error handlers should save the values in MCA_MISC[4:1] if the registers exist.
- DOER Error Management:
 - Check MCA_STATUS[PCC].
 - If PCC is set, error recovery is not possible. The handler should log the error information and terminate the system. If PCC is clear, the handler may continue with the following recovery steps.
 - Check MCA_STATUS[UC].
 - If UC is set, the processor did not correct the error. Continue with the following recovery steps.
 - If MCA Overflow Recovery is not supported, and MCA_STATUS[Overflow] == 1, error recovery is not possible; follow the steps for PCC = 1. See 3.1.3.6 [MCA Overflow Recovery].
 - If MCA Recovery is not supported, error recovery is not possible; follow the steps for PCC = 1. See 3.1.3.7 [MCA Recovery].
 - If MCA Recovery is supported:
 - Check MCA_STATUS[TCC].
 - If TCC is set, the context of the process thread executing on the interrupted logical core may be corrupt and the thread cannot be recovered. The rest of the system is unaffected; it is possible to terminate only the affected process thread.
 - If TCC is clear, the context of the process thread executing on the interrupted logical core is not corrupt. Recovery of the process thread may be possible, but only if the uncorrected error condition is first corrected by software. Otherwise, the interrupted process thread must be terminated.

- Legacy exception handlers can check Core::X86::Msr::MCG_STAT[RIPV] and Core::X86::Msr::MCG_STAT[EIPV] in place of MCA_STATUS[TCC]. If RIPV == EIPV == 1, the interrupted program can be restarted reliably. Otherwise, the program cannot be restarted reliably.
- If UC is clear, the processor either corrected or deferred the error and no software action is needed. The handler can log the error information and continue process execution.
- Exit:
 - When an exception handler is able to successfully log an error condition, clear the MCA_STATUS registers prior to exiting the machine check handler.
 - Prior to exiting the machine check handler, clear Core::X86::Msr::MCG_STAT[MCIP]. MCIP indicates that a machine check exception is in progress. If this bit is set when another machine check exception occurs, the processor enters the shutdown state.

3.2 Machine Check Architecture Implementation

3.2.1 Implemented Machine Check Banks

Table 31: Blocks Capable of Supporting MCA Banks

Acronym	Block Function
LS	Load-Store Unit
IF	Instruction Fetch Unit
L2	L2 Cache Unit
DE	Decode Unit
EX	Execution Unit
FP	Floating-Point Unit
L3	L3 Cache Unit
PIE	Power Management, Interrupts, Etc.
CS	Coherent Station
UMC	Unified Memory Controller
NBIO	Northbridge IO Unit

Table 32: Mapping of Blocks to MCA_IPID[HwId] and MCA_IPID[McaType]

Block	Hardware ID	MCA Type
LS	0xb0	0x0
IF	0xb0	0x1
L2	0xb0	0x2
L3	0xb0	0x7
MP5	0x1	0x2
PB	0x5	0x0
PCS_GMI	0x241	0x0
KPX_GMI	0x269	0x0
UMC	0x96	0x1
NBIO	0x18	0x0
PIE	0x2e	0x1
KPX_SERDES	0x259	0x0

CS	0x2e	0x2
EX	0xb0	0x5
FP	0xb0	0x6
DE	0xb0	0x3

3.2.2 Implemented Machine Check Bank Registers

Table 33 [Legacy MCA Registers] provides links to the description of each block's Legacy MCA registers. Table 34 [MCAX Registers] provides links to the description of each block's MCA Extension Registers.

Table 33: Legacy MCA Registers

Block	MCA Register				
	CTL	STATUS	ADDR	MISC	CTL_MASK
LS	MCA::LS::MCA_CTL_LS	MCA::LS::MCA_STATUS_LS	MCA::LS::MCA_ADDR_LS	MCA::LS::MCA_MISC0_LS	MCA::LS::MCA_CTL_MASK_LS
IF	MCA::IF::MCA_CTL_IF	MCA::IF::MCA_STATUS_IF	MCA::IF::MCA_ADDR_IF	MCA::IF::MCA_MISC0_IF	MCA::IF::MCA_CTL_MASK_IF
L2	MCA::L2::MCA_CTL_L2	MCA::L2::MCA_STATUS_L2	MCA::L2::MCA_ADDR_L2	MCA::L2::MCA_MISC0_L2	MCA::L2::MCA_CTL_MASK_L2
DE	MCA::DE::MCA_CTL_DE	MCA::DE::MCA_STATUS_DE	MCA::DE::MCA_ADDR_DE	MCA::DE::MCA_MISC0_DE	MCA::DE::MCA_CTL_MASK_DE
EX	MCA::EX::MCA_CTL_EX	MCA::EX::MCA_STATUS_EX	MCA::EX::MCA_ADDR_EX	MCA::EX::MCA_MISC0_EX	MCA::EX::MCA_CTL_MASK_EX
FP	MCA::FP::MCA_CTL_FP	MCA::FP::MCA_STATUS_FP	MCA::FP::MCA_ADDR_FP	MCA::FP::MCA_MISC0_FP	MCA::FP::MCA_CTL_MASK_FP
L3	MCA::L3::MCA_CTL_L3	MCA::L3::MCA_STATUS_L3	MCA::L3::MCA_ADDR_L3	MCA::L3::MCA_MISC0_L3	MCA::L3::MCA_CTL_MASK_L3
PIE	MCA::PIE::MCA_CTL_PIE	MCA::PIE::MCA_STATUS_PIE	MCA::PIE::MCA_ADDR_PIE	MCA::PIE::MCA_MISC0_PIE	MCA::PIE::MCA_CTL_MASK_PIE
CS	MCA::CS::MCA_CTL_CS	MCA::CS::MCA_STATUS_CS	MCA::CS::MCA_ADDR_CS	MCA::CS::MCA_MISC0_CS	MCA::CS::MCA_CTL_MASK_CS
UMC	MCA::UMC::MCA_CTL_UMC	MCA::UMC::MCA_STATUS_UMC	MCA::UMC::MCA_ADDR_UMC	MCA::UMC::MCA_MISC0_UMC MCA::UMC::MCA_MISC1_UMC	MCA::UMC::MCA_CTL_MASK_UMC
NBIO	MCA::NBIO::MCA_CTL_NBIO	MCA::NBIO::MCA_STATUS_NBIO	MCA::NBIO::MCA_ADDR_NBIO	MCA::NBIO::MCA_MISC0_NBIO	MCA::NBIO::MCA_CTL_MASK_NBIO

Table 34: MCAX Registers

Block	MCA Register				
	CONFIG	IPID	SYND	DESTAT	DEADDR
LS	MCA::LS::MCA_CONFIG_LS	MCA::LS::MCA_IPID_LS	MCA::LS::MCA_SYND_LS	MCA::LS::MCA_DESTAT_LS	MCA::LS::MCA_DEADDR_LS
IF	MCA::IF::MCA_CONFIG_IF	MCA::IF::MCA_IPID_IF	MCA::IF::MCA_SYND_IF	--	--
L2	MCA::L2::MCA_CONFIG_L2	MCA::L2::MCA_IPID_L2	MCA::L2::MCA_SYND_L2	MCA::L2::MCA_DESTAT_L2	MCA::L2::MCA_DEADDR_L2
DE	MCA::DE::MCA_CONFIG_DE	MCA::DE::MCA_IPID_DE	MCA::DE::MCA_SYND_DE	--	--
EX	MCA::EX::MCA_CONFIG_EX	MCA::EX::MCA_IPID_EX	MCA::EX::MCA_SYND_EX	--	--
FP	MCA::FP::MCA_CONFIG_FP	MCA::FP::MCA_IPID_FP	MCA::FP::MCA_SYND_FP	--	--
L3	MCA::L3::MCA_CONFIG_L3	MCA::L3::MCA_IPID_L3	MCA::L3::MCA_SYND_L3	MCA::L3::MCA_DESTAT_L3	MCA::L3::MCA_DEADDR_L3
PIE	MCA::PIE::MCA_CONFIG_PIE	MCA::PIE::MCA_IPID_PIE	MCA::PIE::MCA_SYND_PIE	MCA::PIE::MCA_DESTAT_PIE	MCA::PIE::MCA_DEADDR_PIE
CS	MCA::CS::MCA_CONFIG_CS	MCA::CS::MCA_IPID_CS	MCA::CS::MCA_SYND_CS	MCA::CS::MCA_DESTAT_CS	MCA::CS::MCA_DEADDR_CS

UMC	MCA::UMC::MCA_CONFIG_UMC	MCA::UMC::MCA_IPID_UMC	MCA::UMC::MCA_SYND_UMC	MCA::UMC::MCA_DESTAT_UMC	MCA::UMC::MCA_DEADDR_UMC
NBIO	MCA::NBIO::MCA_CONFIG_NBIO	MCA::NBIO::MCA_IPID_NBIO	MCA::NBIO::MCA_SYND_NBIO	MCA::NBIO::MCA_DESTAT_NBIO	

3.2.3 Mapping of Banks to Blocks

Table 35 [Core MCA Bank to Block Mapping] shows MCA banks that are present in the address space of every logical core.

Table 35: Core MCA Bank to Block Mapping

Bank	Block
0	LS
1	IF
2	L2
3	DE
4	RAZ
5	EX
6	FP

Table 36 [Non-core MCA Bank to Block Mapping] shows MCA banks that are present in the address space of specific logical cores.

Table 36: Non-core MCA Bank to Block Mapping

Bank	Thread 0	Thread 2
0	LS	LS
1	IF	IF
2	L2	L2
3	DE	DE
4	RAZ	RAZ
5	EX	EX
6	FP	FP
7	L3	L3
8	L3	L3
9	L3	L3
10	L3	L3
11	L3	L3
12	L3	L3
13	L3	L3
14	L3	L3
15	MP5	MP5
16	PB	PB
17	PCS_GMI	PCS_GMI
18	PCS_GMI	PCS_GMI
19	KPX_GMI	KPX_GMI
20	KPX_GMI	KPX_GMI
21	UMC	RAZ

22	UMC	RAZ
23	CS	RAZ
24	CS	RAZ
25	NBIO	RAZ
26	RAZ	RAZ
27	RAZ	RAZ
28	PIE	RAZ
29	KPX_SERDES	RAZ
30	KPX_SERDES	RAZ
31	RAZ	RAZ
32	RAZ	RAZ
33	RAZ	RAZ
34	RAZ	RAZ
35	RAZ	RAZ
36	RAZ	RAZ
37	RAZ	RAZ
38	RAZ	RAZ
39	RAZ	RAZ
40	RAZ	RAZ
41	RAZ	RAZ
42	RAZ	RAZ
43	RAZ	RAZ
44	RAZ	RAZ
45	RAZ	RAZ
46	RAZ	RAZ
47	RAZ	RAZ
48	RAZ	RAZ
49	RAZ	RAZ
50	RAZ	RAZ
51	RAZ	RAZ
52	RAZ	RAZ
53	RAZ	RAZ
54	RAZ	RAZ
55	RAZ	RAZ
56	RAZ	RAZ
57	RAZ	RAZ
58	RAZ	RAZ
59	RAZ	RAZ
60	RAZ	RAZ
61	RAZ	RAZ
62	RAZ	RAZ
63	RAZ	RAZ

3.2.4 Decoding Error Type

If a valid error is logged in MCA_STATUS or MCA_DESTAT of an MCA bank:

1. Read the values of this bank's MCA_IPID and MCA_STATUS registers.

2. Use Table 31 [Blocks Capable of Supporting MCA Banks] to look up the block associated with the values of MCA_IPID[HwId] and MCA_IPID[McaType].
3. In 3.2.5 [MCA Banks], find the sub-section associated with the block in error.
4. In this sub-section, find the MCA_STATUS table.
5. In the table, look up the row associated with the MCA_STATUS[ErrorCodeExt] value.
6. The error type in this row is the logged error. The MCA_STATUS, MCA_ADDR and MCA_SYND tables contain information associated with this error.
7. If there is an error in both MCA_STATUS and MCA_DESTAT, the registers contain the same error if MCA_STATUS[Deferred] is set. If MCA_STATUS[Deferred] is not set, MCA_DESTAT contains information for a different error than MCA_STATUS.

3.2.5 MCA Banks

3.2.5.1 LS

MSR0000_0400...MSRC000_2000 [LS Machine Check Control Thread 0] (MCA::LS::MCA_CTL_LS)

Read-write. Reset: 0000_0000_0000_0000h.

0=Disables error reporting for the corresponding error. 1=Enables error reporting via machine check exception for the corresponding error. The MCA::LS::MCA_CTL_LS register must be enabled by the corresponding enable bit in Core::X86::Msr::MCG_CTL. Does not affect error detection, correction, or logging.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst0_n[31:0]_aliasMSRLEGACY; MSR0000_0400

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst0_n[31:0]_aliasMSR; MSRC000_2000

Bits	Description
63:24	Reserved.
23	STORE_DATA_OTHER. Read-write. Reset: 0. A parity error was detected in an STLF, SCB EMEM entry, store data mask or SRB store data by any access
22	HWA. Read-write. Reset: 0. A hardware assertion error was reported
21	SystemReadDataErrorWcb. Read-write. Reset: 0. A SystemReadDataError error was reported on read data returned from L2 for a WCB store
20	SystemReadDataErrorScb. Read-write. Reset: 0. A SystemReadDataError error was reported on read data returned from L2 for an SCB store
19	SystemReadDataErrorLoad. Read-write. Reset: 0. A SystemReadDataError error was reported on read data returned from L2 for a load
18	SCB_POISON. Read-write. Reset: 0. A poisoned line was detected in an SCB entry by any access
17	WCB. Read-write. Reset: 0. A parity error was detected in a WCB entry by any access
16	SCB_DATA. Read-write. Reset: 0. A parity error was detected in an SCB entry data field by any access
15	SCB_ADDR. Read-write. Reset: 0. A parity error was detected in an SCB entry address field by any access
14	SCB_STATE. Read-write. Reset: 0. A parity error was detected in an SCB entry state field by any access
13	MAB. Read-write. Reset: 0. A parity error was detected in a MAB entry by any access
12	LDQ. Read-write. Reset: 0. A parity error was detected in an LDQ entry by any access
11	STQ. Read-write. Reset: 0. A parity error was detected in an STQ entry by any access
10	PWC. Read-write. Reset: 0. A parity error was detected in a PWC entry by any access
9	L2DTLB. Read-write. Reset: 0. A parity error was detected in an L2 TLB entry by any access
8	L1DTLB. Read-write. Reset: 0. A parity error was detected in an L1 TLB entry by any access.
7	EMEM_RMW. Read-write. Reset: 0. An ECC error was detected on an EMEM read-modify-write by a store
6	EMEM_LOAD. Read-write. Reset: 0. An ECC error was detected on an EMEM read by a load.
5	DC_TAG_STORE. Read-write. Reset: 0. An ECC error or poison bit mismatch was detected on a tag read by a store.
4	DC_TAG_LOAD. Read-write. Reset: 0. An ECC error or poison bit mismatch was detected on a tag read by a load.
3	DC_TAG_VICTIM. Read-write. Reset: 0. An ECC error or poison bit mismatch was detected on a tag read by a probe or victimization.
2	DC_DATA_RMW. Read-write. Reset: 0. An ECC error was detected on a data cache read-modify-write by a store
1	DC_DATA_LOAD. Read-write. Reset: 0. An ECC error or L2 poison was detected on a data cache read by a load (note PhysLoc is set to zero and Poison is set to 1 for L2 poison).
0	DC_DATA_VICTIM. Read-write. Reset: 0. An ECC error was detected on a data cache read by a probe or victimization

MSR0000_0001...MSRC000_2001 [LS Machine Check Status Thread 0] (MCA::LS::MCA_STATUS_LS)

Reset: Cold,0000_0000_0000_0000h.

Logs information associated with errors.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst0_n[31:0]_aliasMSRSLLEGACY; MSR0000_0001

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst0_n[31:0]_aliasMSRLEGACY; MSR0000_0401

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst0_n[31:0]_aliasMSR; MSRC000_2001

Bits	Description
63	Val. Reset: Cold,0. 1=A valid error has been detected. This bit should be cleared by software after the register has been read. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
62	Overflow. Reset: Cold,0. 1=An error was detected while the valid bit (Val) was set; at least one error was not logged. Overflow is set independently of whether the existing error is overwritten. See 3.1.3 [Machine Check Errors]. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
61	UC. Reset: Cold,0. 1=The error was not corrected by hardware. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
60	En. Reset: Cold,0. 1=MCA error reporting is enabled for this error, as indicated by the corresponding bit in MCA::LS::MCA_CTL_LS. This bit is a copy of bit in MCA::LS::MCA_CTL_LS for this error. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
59	MiscV. Reset: Cold,0. 1=Valid thresholding in MCA::LS::MCA_MISC0_LS. In certain modes, MISC registers are owned by platform firmware and will RAZ when read by non-SMM code. Therefore, it is possible for MiscV=1 and the MISC register to read as all zeros. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
58	AddrV. Reset: Cold,0. 1=MCA::LS::MCA_ADDR_LS contains address information associated with the error. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
57	PCC. Reset: Cold,0. 1=Hardware context held by the processor may have been corrupted. Continued operation of the system may have unpredictable results. The error is not recoverable or survivable, and the system should be reinitialized. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
56	ErrCoreIdVal. Reset: Cold,0. 1=The ErrCoreId field is valid. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
55	TCC. Reset: Cold,0. 1=Hardware context of the process thread to which the error was reported may have been corrupted. Continued operation of the thread may have unpredictable results. The thread must be terminated. Only meaningful when MCA::LS::MCA_STATUS_LS[PCC]=0. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
54	RESERV54. Reset: Cold,0. MCA_STATUS Register Reserved bit. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
53	SyndV. Reset: Cold,0. 1=This error logged information in MCA::LS::MCA_SYND_LS. If MCA::LS::MCA_SYND_LS[ErrorPriority] is the same as the priority of the error in MCA::LS::MCA_STATUS_LS, then the information in MCA::LS::MCA_SYND_LS is associated with the error in MCA::LS::MCA_STATUS_LS. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
52	Reserved.
51:47	RESERV47. Reset: Cold,00h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
46	CECC. Reset: Cold,0. 1=The error was a correctable ECC error according to the restrictions of the ECC algorithm. UC indicates whether the error was actually corrected by the processor. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
45	UECC. Reset: Cold,0. 1=The error was an uncorrectable ECC error according to the restrictions of the ECC algorithm. UC indicates whether the error was actually corrected by the processor.

	AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
44	Deferred. Reset: Cold,0. 1=A deferred error was created. A deferred error is the result of an uncorrectable data error which did not immediately cause a processor exception; an exception is deferred until the erroneous data is consumed.
	AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
43	Poison. Reset: Cold,0. 1=The error was the result of attempting to consume poisoned data.
	AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
42:41	RESERV41. Reset: Cold,0h. MCA_STATUS Register Reserved bits.
	AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
40	Scrub. Reset: Cold,0. 1=The error was the result of a scrub operation.
	AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
39:38	RESERV38. Reset: Cold,0h. MCA_STATUS Register Reserved bits.
	AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
37:32	ErrCoreId. Reset: Cold,00h. When ErrCoreIdVal=1 this field indicates which core within the processor is associated with the error; Otherwise this field is reserved.
	AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
31:30	RESERV30. Reset: Cold,0h. MCA_STATUS Register Reserved bits.
	AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
29:24	AddrLsb. Reset: Cold,00h. Specifies the least significant valid bit of the address contained in MCA::LS::MCA_ADDR_LS[ErrorAddr]. A value of 0 indicates that MCA::LS::MCA_ADDR_LS[56:0] contains a valid byte address. A value of 6 indicates that MCA::LS::MCA_ADDR_LS[56:6] contains a valid cache line address and that MCA::LS::MCA_ADDR_LS[5:0] are not part of the address and should be ignored by error handling software. A value of 12 indicates that MCA::LS::MCA_ADDR_LS[56:12] contain a valid 4KB memory page and that MCA::LS::MCA_ADDR_LS[11:0] should be ignored by error handling software.
	AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
23:22	RESERV22. Reset: Cold,0h. MCA_STATUS Register Reserved bits.
	AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
21:16	ErrorCodeExt. Reset: Cold,00h. Extended Error Code. This field is used to identify the error type for root cause analysis. This field indicates which bit position in MCA::LS::MCA_CTL_LS enables error reporting for the logged error.
	AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
15:0	ErrorCode. Reset: Cold,0000h. Error code for this error. See 3.1.3.3 [Error Codes] for details on decoding this field.
	AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.

Table 37: MCA_STATUS_LS

Error Type	ErrorCode Ext	UC	PCC	TCC	Deferred	Poison	AddrV
DC_DATA_VICTIM	0x0	0	0	0	0/1	0	1
DC_DATA_LOAD	0x1	0/1	0	0/1	0	0/1	1
DC_DATA_RMW	0x2	0	0	0	0/1	0	1
DC_TAG_VICTIM	0x3	0/1	0/1	0/1	0/1	0	0
DC_TAG_LOAD	0x4	0/1	0/1	0/1	0/1	0	0
DC_TAG_STORE	0x5	0/1	0/1	0/1	0/1	0	0

EMEM_LO AD	0x6	1	1	1	0	0	1
EMEM_RM W	0x7	0/1	0/1	0/1	0	0	0
L1DTLB	0x8	0	0	0	0	0	0
L2DTLB	0x9	0	0	0	0	0	1
PWC	0xa	0	0	0	0	0	1
STQ	0xb	1	1	1	0	0	0
LDQ	0xc	1	1	1	0	0	0
MAB	0xd	1	1	1	0	0	0
SCB_STATE	0xe	1	1	1	0	0	0
SCB_ADDR	0xf	1	1	1	0	0	0
SCB_DATA	0x10	1	1	1	0	0	0
WCB	0x11	1	1	1	0	0	0
SCB_POISON	0x12	0	0	0	1	0	0
SystemRead DataErrorLoad	0x13	1	0	1	0	0	1
SystemRead DataErrorSnb	0x14	1	1	1	0	0	1
SystemRead DataErrorWcb	0x15	1	1	1	0	0	0
HWA	0x16	1	1	1	0	0	0
STORE_DATA_OTHER	0x17	1	1	1	0	0	0

MSR0000_0000...MSRC000_2002 [LS Machine Check Address Thread 0] (MCA::LS::MCA_ADDR_LS)

Reset: Cold,0000_0000_0000_0000h.

MCA::LS::MCA_ADDR_LS stores an address and other information associated with the error in MCA::LS::MCA_STATUS_LS. The register is only meaningful if MCA::LS::MCA_STATUS_LS[Val]=1 and MCA::LS::MCA_STATUS_LS[AddrV]=1.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst0_n[31:0]_aliasMSRLSLEGACY; MSR0000_0000

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst0_n[31:0]_aliasMSRLEGACY; MSR0000_0402

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst0_n[31:0]_aliasMSR; MSRC000_2002

Bits	Description
63:57	Reserved.
56:0	ErrorAddr. Read-write, Volatile. Reset: Cold,000_0000_0000_0000h. Unless otherwise specified by an error, contains the address associated with the error logged in MCA::LS::MCA_STATUS_LS. For physical addresses, the most significant bit is given by Core::X86::Cpuid::LongModeInfo[PhysAddrSize].

Table 38: MCA_ADDR_LS

Error Type	Bits	Description
DC_DATA_VICTIM	[56:52] [51:6] [5] [4:0]	Reserved Physical address Reserved Which data word had the error
DC_DATA_LOAD	[56:52]	Reserved

	[51:1] [0]	Physical address Reserved
DC_DATA_RMW	[56:52] [51:6] [5:0]	Reserved Physical address Reserved
DC_TAG_VICTIM	[57:0]	Reserved
DC_TAG_LOAD	[57:0]	Reserved
DC_TAG_STORE	[57:0]	Reserved
EMEM_LOAD	[56:52] [51:1] [0]	Reserved Physical address Reserved
EMEM_RMW	[57:0]	Reserved
L1DTLB	[57:0]	Reserved
L2DTLB	[56:52] [51:12] [11:0]	Reserved Physical address Reserved
PWC	[56:52] [51:12] [11:0]	Reserved Physical address Reserved
STQ	[57:0]	Reserved
LDQ	[57:0]	Reserved
MAB	[57:0]	Reserved
SCB_STATE	[57:0]	Reserved
SCB_ADDR	[57:0]	Reserved
SCB_DATA	[57:0]	Reserved
WCB	[57:0]	Reserved
SCB_POISON	[57:0]	Reserved
SystemReadDataErrorLoad	[56:52] [51:1] [0]	Reserved Physical address Reserved
SystemReadDataErrorScb	[56:52] [51:6] [5:0]	Reserved Physical address Reserved
SystemReadDataErrorWcb	[57:0]	Reserved
HWA	[57:0]	Reserved
STORE_DATA_OTHER	[57:0]	Reserved

MSR0000_0403...MSRC000_2003 [LS Machine Check Miscellaneous 0 Thread 0] (MCA::LS::MCA_MISC0_LS)

Log miscellaneous information associated with errors.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst0_n[31:0]_aliasMSRLEGACY; MSR0000_0403

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst0_n[31:0]_aliasMSR; MSRC000_2003

Bits	Description
63	Valid. Reset: 1. 1=A valid CntP field is present in this register. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read-only.
62	CntP. Reset: 1. 1=A valid threshold counter is present. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read-only.
61	Locked. Reset: 0. 1=Writes to this register are ignored. This bit is set by BIOS to indicate that this register is not available for OS use. BIOS should set this bit if ThresholdIntType is set to SMI. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read-only.
60	IntP. Reset: 1. 1=ThresholdIntType can be used to generate interrupts. 0=ThresholdIntType and interrupt generation are not supported. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::LS::MCA_MISC0_LS[Locked]) ? Read-write : Read-only.
59:56	Reserved.
55:52	LvtOffset. Reset: 0h. One per die. For error thresholding interrupts, specifies the address of the LVT entry in the APIC registers as follows: LVT address = (LvtOffset shifted left 4 bits) + 500h (see Core::X86::Apic::ExtendedInterruptLvtEntries). AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::LS::MCA_MISC0_LS[Locked]) ? Read-write : Read-only.
51	CntEn. Reset: 0. 1=Count thresholding errors. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::LS::MCA_MISC0_LS[Locked]) ? Read-write : Read-only.
50:49	ThresholdIntType. Reset: Cold,0h. Specifies the type of interrupt signaled when Ovrflw is set and IntP==1. 00b = No interrupt. 01b = APIC based interrupt (see Core::X86::Msr::McaIntrCfg[ThresholdLvtOffset]). 10b = SMI trigger event. 11b = Reserved. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::LS::MCA_MISC0_LS[Locked]) ? Read-write : Read-only.
48	Ovrflw. Reset: Cold,0. Set by hardware when ErrCnt transitions from FFEh to FFFh. When this field is set, ErrCnt no longer increments. When this bit is set, the interrupt selected by the ThresholdIntType field is generated. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::LS::MCA_MISC0_LS[Locked]) ? Read-write : Read-only.
47:44	Reserved.
43:32	ErrCnt. Reset: Cold,000h. This is written by software to set the starting value of the error counter. This is incremented by hardware when errors are logged. When this counter overflows, it stays at FFFh (no rollover). The threshold value, written by software, is (FFFh - the desired error count (the number of errors necessary in order for an interrupt to be taken)); the desired error count of 0 (a write value of FFFh) is not supported. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::LS::MCA_MISC0_LS[Locked]) ? Read-write : Read-only.
31:24	BlkPtr. Read-write. Reset: 00h. 00h=Extended MISC MSR block is not valid. 01h=Extended MSR block is valid.
23:0	Reserved.

MSRC000_2004 [LS Machine Check Configuration Thread 0] (MCA::LS::MCA_CONFIG_LS)

Reset: 0000_0002_0000_0125h.

Controls configuration of the associated machine check bank.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst0_n[31:0]_aliasMSR; MSRC000_2004

Bits	Description
63:39	Reserved.
38:37	DeferredIntType. Read-write. Reset: 0h. Specifies the type of interrupt signaled when a deferred error is logged. 00b = No interrupt. 01b = APIC based interrupt (see Core::X86::Msr::McaIntrCfg[DeferredLvtOffset]). 10b = SMI trigger event. 11b = Reserved.
36:35	Reserved.
34	LogDeferredInMcaStat. Read-write. Reset: 0. Init: BIOS,1. 1=Log deferred errors in MCA::LS::MCA_STATUS_LS and MCA::LS::MCA_ADDR_LS in addition to MCA::LS::MCA_DESTAT_LS and MCA::LS::MCA_DEADDR_LS. 0=Only log deferred errors in MCA::LS::MCA_DESTAT_LS and MCA::LS::MCA_DEADDR_LS. This bit does not affect logging of deferred errors in MCA::LS::MCA_SYND_LS, MCA::LS::MCA_MISC0_LS.
33	Reserved.
32	McaXEnable. Read-write. Reset: 0. Init: BIOS,1. Check: 1. 1=Software has acknowledged support for the MCAX feature set. 0=Software has not acknowledged support for the MCAX feature set. All uncorrected and fatal errors will cause an ErrorEvent packet to be generated. Deferred error interrupts are configured via Core::X86::Msr::McaIntrCfg.
31:9	Reserved.
8	McaLsbInStatusSupported. Read-only. Reset: 1. 1=MCA::LS::MCA_CONFIG_LS[McaLsbInStatusSupported] indicates that AddrLsb is located in McaStatus registers.
7:6	Reserved.
5	DeferredIntTypeSupported. Read-only. Reset: 1. 1=MCA::LS::MCA_CONFIG_LS[DeferredIntType] controls the type of interrupt generated on a deferred error. Deferred errors are supported in this bank only if MCA::LS::MCA_CONFIG_LS[DeferredErrorLoggingSupported]=1.
4:3	Reserved.
2	DeferredErrorLoggingSupported. Read-only. Reset: 1. 1=Deferred errors are supported in this MCA bank, and MCA::LS::MCA_CONFIG_LS[LogDeferredInMcaStat] controls the logging behavior of these errors. MCA::LS::MCA_DESTAT_LS and MCA::LS::MCA_DEADDR_LS are supported in this MCA bank. 0=Deferred errors are not supported in this bank.
1	Reserved.
0	McaX. Read-only. Reset: 1. 1=This bank provides Machine Check Architecture Extensions. Up to 4 additional MISC registers (MISC1-MISC4) are supported. MCA::LS::MCA_MISC0_LS[BlkPtr] indicates the presence of the additional MISC registers, but is not used to determine their MSR numbers. Deferred error interrupt type is specifiable by MCA bank. MCA::LS::MCA_STATUS_LS[TCC] is present.

MSRC000_2005 [LS IP Identification Thread 0] (MCA::LS::MCA_IPID_LS)

Reset: 0010_00B0_0000_0000h.

The MCA::LS::MCA_IPID_LS register is used by software to determine what IP type and revision is associated with the MCA bank.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst0_n[31:0]_aliasMSR; MSRC000_2005

Bits	Description
63:48	McaType . Read-only. Reset: 0010h. The McaType of the MCA bank within this IP.
47:44	InstanceIdHi . Read-write. Reset: 0h. The HI value instance ID of this IP. This is initialized to a unique ID per instance of this register.
43:32	HardwareID . Read-only. Reset: 0B0h. The Hardware ID of the IP associated with this MCA bank.
31:0	InstanceId . Read-write. Reset: 0000_0000h. The instance ID of this IP. This is initialized to a unique ID per instance of this register.
	Init: _ccd0_lthree0_core0_thread0_inst0_n0_aliasMSR: 2000_AE00h
	Init: _ccd0_lthree0_core0_thread1_inst0_n1_aliasMSR: 2000_AF00h
	Init: _ccd0_lthree0_core1_thread0_inst0_n2_aliasMSR: 2002_AE00h
	Init: _ccd0_lthree0_core1_thread1_inst0_n3_aliasMSR: 2002_AF00h
	Init: _ccd0_lthree0_core2_thread0_inst0_n4_aliasMSR: 2004_AE00h
	Init: _ccd0_lthree0_core2_thread1_inst0_n5_aliasMSR: 2004_AF00h
	Init: _ccd0_lthree0_core3_thread0_inst0_n6_aliasMSR: 2006_AE00h
	Init: _ccd0_lthree0_core3_thread1_inst0_n7_aliasMSR: 2006_AF00h
	Init: _ccd0_lthree0_core4_thread0_inst0_n8_aliasMSR: 2008_AE00h
	Init: _ccd0_lthree0_core4_thread1_inst0_n9_aliasMSR: 2008_AF00h
	Init: _ccd0_lthree0_core5_thread0_inst0_n10_aliasMSR: 200A_AE00h
	Init: _ccd0_lthree0_core5_thread1_inst0_n11_aliasMSR: 200A_AF00h
	Init: _ccd0_lthree0_core6_thread0_inst0_n12_aliasMSR: 200C_AE00h
	Init: _ccd0_lthree0_core6_thread1_inst0_n13_aliasMSR: 200C_AF00h
	Init: _ccd0_lthree0_core7_thread0_inst0_n14_aliasMSR: 200E_AE00h
	Init: _ccd0_lthree0_core7_thread1_inst0_n15_aliasMSR: 200E_AF00h
	Init: _ccd1_lthree0_core0_thread0_inst0_n16_aliasMSR: 2080_AE00h
	Init: _ccd1_lthree0_core0_thread1_inst0_n17_aliasMSR: 2080_AF00h
	Init: _ccd1_lthree0_core1_thread0_inst0_n18_aliasMSR: 2082_AE00h
	Init: _ccd1_lthree0_core1_thread1_inst0_n19_aliasMSR: 2082_AF00h
	Init: _ccd1_lthree0_core2_thread0_inst0_n20_aliasMSR: 2084_AE00h
	Init: _ccd1_lthree0_core2_thread1_inst0_n21_aliasMSR: 2084_AF00h
	Init: _ccd1_lthree0_core3_thread0_inst0_n22_aliasMSR: 2086_AE00h
	Init: _ccd1_lthree0_core3_thread1_inst0_n23_aliasMSR: 2086_AF00h
	Init: _ccd1_lthree0_core4_thread0_inst0_n24_aliasMSR: 2088_AE00h
	Init: _ccd1_lthree0_core4_thread1_inst0_n25_aliasMSR: 2088_AF00h
	Init: _ccd1_lthree0_core5_thread0_inst0_n26_aliasMSR: 208A_AE00h
	Init: _ccd1_lthree0_core5_thread1_inst0_n27_aliasMSR: 208A_AF00h
	Init: _ccd1_lthree0_core6_thread0_inst0_n28_aliasMSR: 208C_AE00h
	Init: _ccd1_lthree0_core6_thread1_inst0_n29_aliasMSR: 208C_AF00h
	Init: _ccd1_lthree0_core7_thread0_inst0_n30_aliasMSR: 208E_AE00h
	Init: _ccd1_lthree0_core7_thread1_inst0_n31_aliasMSR: 208E_AF00h

MSRC000_2006 [LS Machine Check Syndrome Thread 0] (MCA::LS::MCA_SYND_LS)

Read-write, Volatile. Reset: Cold, 0000_0000_0000_0000h.	
Logs physical location information associated with error in MCA::LS::MCA_STATUS_LS Thread 0	
_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst0_n[31:0]_aliasMSR; MSRC000_2006	
Bits	Description
63:39	Reserved.
38:32	Syndrom . Read-write, Volatile. Reset: Cold, 00h. Contains the syndrome, if any, associated with the error logged in MCA::LS::MCA_STATUS_LS. The low-order bit of the syndrome is stored in bit 0, and the syndrome has a length specified by MCA::LS::MCA_SYND_LS[Length]. The Syndrome field is only valid when MCA::LS::MCA_SYND_LS[Length] is not 0.
31:27	Reserved.
26:24	ErrorPriority . Read-write, Volatile. Reset: Cold, 0h. Encodes the priority of the error logged in MCA::LS::MCA_SYND_LS. 3'b000 = No error; 3'b001 = Reserved; 3'b010 = Corrected Error; 3'b011 = Deferred Error; 3'b100 = Uncorrected Error; 3'b101 = Fatal Error; all others reserved.
23:18	Length . Read-write, Volatile. Reset: Cold, 00h. Specifies the length in bits of the syndrome contained in MCA::LS::MCA_SYND_LS[Syndrome]. A value of 0 indicates that there is no valid syndrome in MCA::LS::MCA_SYND_LS. For example, a syndrome length of 9 means that MCA::LS::MCA_SYND_LS[Syndrome] bits [8:0] contains a valid syndrome.
17:0	ErrorInformation . Read-write, Volatile. Reset: Cold, 0_0000h. Contains error-specific information about the location of the error. Decoding is available in Table 39 [MCA_SYND_LS].

Table 39: MCA_SYND_LS

Error Type	Bits	Description
DC_DATA_VICTIM	[17]	1
	[16]	1
	[15:14]	Reserved
	[13:8]	Cache line index
	[7:3]	Reserved
	[2:0]	Cache line way
DC_DATA_LOAD	[17]	1
	[16]	1
	[15:14]	Reserved
	[13:8]	Cache line index
	[7:3]	Reserved
	[2:0]	Cache line way
DC_DATA_RMW	[17]	0
	[16]	1
	[15:5]	Reserved
	[4:0]	Which data word had the error
DC_TAG_VICTIM	[17]	1
	[16]	1
	[15:14]	Reserved
	[13:8]	Cache line index
	[7:3]	Reserved
	[2:0]	Cache line way
DC_TAG_LOAD	[17]	1
	[16]	1
	[15:14]	Reserved

	[13:8]	Cache line index
	[7:3]	Reserved
	[2:0]	Cache line way
DC_TAG_STORE	[17]	1
	[16]	1
	[15:14]	Reserved
	[13:8]	Cache line index
	[7:3]	Reserved
	[2:0]	Cache line way
EMEM_LOAD	[17]	1
	[16]	0
	[15:14]	Reserved
	[13:8]	Cache line index
	[7:0]	Reserved
EMEM_RMW	[17]	0
	[16]	1
	[15:5]	Reserved
	[4:0]	Which data word had the error
L1DTLB	[17]	0
	[16]	1
	[15:7]	Reserved
	[6:0]	TLB entry index
L2DTLB	[17]	1
	[16]	1
	[15:12]	Reserved
	[11:7]	TLB way
	[6:0]	TLB entry index
PWC	[17]	0
	[16]	1
	[15:6]	Reserved
	[5:0]	PWC entry index
STQ	[17]	0
	[16]	1
	[15:6]	Reserved
	[5:0]	STQ entry index
LDQ	[17]	0
	[16]	1
	[15:6]	Reserved
	[5:0]	LDQ entry index
MAB	[17]	0
	[16]	1
	[15:5]	Reserved
	[4:0]	MAB entry index
SCB_STATE	[17]	0
	[16]	1
	[15:4]	Reserved
	[3:0]	SCB entry index

SCB_ADDR	[17] [16] [15:4] [3:0]	0 1 Reserved SCB entry index
SCB_DATA	[17] [16] [15:4] [3:0]	0 1 Reserved SCB entry index
WCB	[17] [16] [15:3] [2:0]	0 1 Reserved WCB entry index
SCB_POISON	[17] [16] [15:4] [3:0]	0 1 Reserved SCB entry index
SystemReadDataErrorLoad	[17] [16] [15:2] [1:0]	0 0 Reserved SystemReadDataError response error type
SystemReadDataErrorScb	[17] [16] [15:2] [1:0]	0 0 Reserved SystemReadDataError response error type
SystemReadDataErrorWcb	[17] [16] [15:2] [1:0]	0 0 Reserved SystemReadDataError response error type
HWA	[17] [16] [15:8] [7] [6] [5:0]	0 0 Reserved MCA was signaled Reserved assertion type
STORE_DATA_OTHER	[17] [16] [15:9] [8:7] [6] [5:0]	0 0 Reserved Error Type, 11 = STLF, 10 = SCB EMEM, 01 = Store Data Mask, 00 = SRB Store Data if 1 then [5:0] are STQ index, if 0 then [3:0] are SCB index if bit 6 is 1 then STQ index if bit 6 is 0 then [5:4] are 2'b0 and [3:0] are STQ index

MSRC000_2008 [LS Machine Check Deferred Error Status Thread 0] (MCA::LS::MCA_DESTAT_LS)

Reset: Cold,0000_0000_0000_0000h.

Holds status information for the first deferred error seen in this bank.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst0_n[31:0]_aliasMSR; MSRC000_2008

Bits	Description
63	Val. Read-write, Volatile. Reset: Cold,0. 1=A valid error has been detected (whether it is enabled or not).
62	Overflow. Read-write, Volatile. Reset: Cold,0. 1=An error was detected while the valid bit (Val) was set; at least one error was not logged. Overflow is set independently of whether the existing error is overwritten. (See the section on overwrite priorities.)
61:59	RESERV4. Read-write. Reset: Cold,0h.
58	AddrV. Read-write, Volatile. Reset: Cold,0. 1=MCA::LS::MCA_DEADDR_LS contains address information associated with the error.
57:54	RESERV3. Read-write. Reset: Cold,0h.
53	SyndV. Read-write, Volatile. Reset: Cold,0. 1=This error logged information in MCA::LS::MCA_SYND_LS. If MCA::LS::MCA_SYND_LS[ErrorPriority] is the same as the priority of the error in MCA::LS::MCA_STATUS_LS, then the information in MCA::LS::MCA_SYND_LS is associated with the error in MCA::LS::MCA_DESTAT_LS.
52:45	RESERV2. Read-write. Reset: Cold,00h.
44	Deferred. Read-write, Volatile. Reset: Cold,0. 1=A deferred error was created. A deferred error is the result of an uncorrectable data error which did not immediately cause a processor exception; poison is created and an exception is deferred until the poison data is consumed.
43:30	RESERV1. Read-write. Reset: Cold,0000h.
29:24	AddrLsb. Read-write, Volatile. Reset: Cold,00h. Specifies the least significant valid bit of the address contained in MCA::LS::MCA_ADDR_LS[ErrorAddr]. A value of 0 indicates that MCA::LS::MCA_ADDR_LS[56:0] contains a valid byte address. A value of 6 indicates that MCA::LS::MCA_ADDR_LS[56:6] contains a valid cache line address and that MCA::LS::MCA_ADDR_LS[5:0] are not part of the address and should be ignored by error handling software. A value of 12 indicates that MCA::LS::MCA_ADDR_LS[56:12] contain a valid 4KB memory page and that MCA::LS::MCA_ADDR_LS[11:0] should be ignored by error handling software.
23:22	RESERV0. Read-write. Reset: Cold,0h.
21:16	ErrorCodeExt. Read-write, Volatile. Reset: Cold,00h. Logs an extended error code when an error is detected. This model-specific field is used in conjunction with ErrorCode? to identify the error sub-type for root cause analysis.
15:0	ErrorCode. Read-write, Volatile. Reset: Cold,0000h. Error code for this error.

MSRC000_2009 [LS Deferred Error Address Thread 0] (MCA::LS::MCA_DEADDR_LS)

Reset: Cold,0000_0000_0000_0000h.

The MCA::LS::MCA_DEADDR_LS register stores the address associated with the error in MCA::LS::MCA_DESTAT_LS. The register is only meaningful if MCA::LS::MCA_DESTAT_LS[Val]=1 and MCA::LS::MCA_DESTAT_LS[AddrV]=1. The lowest valid bit of the address is defined by MCA::LS::MCA_DESTAT_LS[AddrLsb].

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst0_n[31:0]_aliasMSR; MSRC000_2009

Bits	Description
63:57	Reserved.
56:0	ErrorAddr. Read-write, Volatile. Reset: Cold,000_0000_0000_0000h. Contains the address, if any, associated with the error logged in MCA::LS::MCA_DESTAT_LS. The lowest-order valid bit of the address is specified in MCA::LS::MCA_DESTAT_LS[AddrLsb].

MSRC001_0400 [LS Machine Check Control Mask Thread 0] (MCA::LS::MCA_CTL_MASK_LS)

Read-write. Reset: 0000_0000_0000_0000h.

Inhibit detection of an error source.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst0_n[31:0]_aliasMSR; MSRC001_0400

Bits	Description
63:24	Reserved.
23	STORE_DATA_OTHER. Read-write. Reset: 0. A parity error was detected in an STLF, SCB EMEM entry, store data mask or SRB store data by any access
22	HWA. Read-write. Reset: 0. A hardware assertion error was reported
21	SystemReadDataErrorWcb. Read-write. Reset: 0. Init: BIOS,1. A SystemReadDataError error was reported on read data returned from L2 for a WCB store
20	SystemReadDataErrorScb. Read-write. Reset: 0. Init: BIOS,1. A SystemReadDataError error was reported on read data returned from L2 for an SCB store
19	SystemReadDataErrorLoad. Read-write. Reset: 0. Init: BIOS,1. A SystemReadDataError error was reported on read data returned from L2 for a load
18	SCB_POISON. Read-write. Reset: 0. A poisoned line was detected in an SCB entry by any access
17	WCB. Read-write. Reset: 0. A parity error was detected in a WCB entry by any access
16	SCB_DATA. Read-write. Reset: 0. A parity error was detected in an SCB entry data field by any access
15	SCB_ADDR. Read-write. Reset: 0. A parity error was detected in an SCB entry address field by any access
14	SCB_STATE. Read-write. Reset: 0. A parity error was detected in an SCB entry state field by any access
13	MAB. Read-write. Reset: 0. A parity error was detected in a MAB entry by any access
12	LDQ. Read-write. Reset: 0. A parity error was detected in an LDQ entry by any access
11	STQ. Read-write. Reset: 0. A parity error was detected in an STQ entry by any access
10	PWC. Read-write. Reset: 0. A parity error was detected in a PWC entry by any access
9	L2DTLB. Read-write. Reset: 0. A parity error was detected in an L2 TLB entry by any access
8	L1DTLB. Read-write. Reset: 0. A parity error was detected in an L1 TLB entry by any access.
7	EMEM_RMW. Read-write. Reset: 0. An ECC error was detected on an EMEM read-modify-write by a store
6	EMEM_LOAD. Read-write. Reset: 0. An ECC error was detected on an EMEM read by a load.
5	DC_TAG_STORE. Read-write. Reset: 0. An ECC error or poison bit mismatch was detected on a tag read by a store.
4	DC_TAG_LOAD. Read-write. Reset: 0. An ECC error or poison bit mismatch was detected on a tag read by a load.
3	DC_TAG_VICTIM. Read-write. Reset: 0. An ECC error or poison bit mismatch was detected on a tag read by a probe or victimization.
2	DC_DATA_RMW. Read-write. Reset: 0. An ECC error was detected on a data cache read-modify-write by a store
1	DC_DATA_LOAD. Read-write. Reset: 0. An ECC error or L2 poison was detected on a data cache read by a load (note PhysLoc is set to zero and Poison is set to 1 for L2 poison).
0	DC_DATA_VICTIM. Read-write. Reset: 0. An ECC error was detected on a data cache read by a probe or victimization

3.2.5.2 IF

MSR0000_0404...MSRC000_2010 [IF Machine Check Control Thread 0] (MCA::IF::MCA_CTL_IF)

Read-write. Reset: 0000_0000_0000_0000h.

0=Disables error reporting for the corresponding error. 1=Enables error reporting via machine check exception for the corresponding error. The MCA::IF::MCA_CTL_IF register must be enabled by the corresponding enable bit in Core::X86::Msr::MCG_CTL. Does not affect error detection, correction, or logging.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst1_n[31:0]_aliasMSRLEGACY; MSR0000_0404

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst1_n[31:0]_aliasMSR; MSRC000_2010

Bits	Description
63:19	Reserved.
18	CtMceError . Read-write. Reset: 0. CT MCE.
17	BsrParity . Read-write. Reset: 0. BSR Parity Error.
16	L2TlbMultiHit . Read-write. Reset: 0. L2-TLB Multi-Hit
15	L1TlbMultiHit . Read-write. Reset: 0. L1-TLB Multi-Hit.
14	HwAssert . Read-write. Reset: 0. Hardware Assertion Error.
13	SystemReadDataError . Read-write. Reset: 0. L2 Cache Error Response.
12	L2RespPoison . Read-write. Reset: 0. L2 Cache Response Poison Error. Error is the result of consuming poison data.
11	L2BtbMultiHit . Read-write. Reset: 0. BP L2-BTB Multi-Hit Error.
10	L1BtbMultiHit . Read-write. Reset: 0. BP L1-BTB Multi-Hit Error.
9	BpqSnpParT1 . Read-write. Reset: 0. BPQ Thread 1 Snoop Parity Error.
8	RSVD_8 . Read-write. Reset: 0. Reserved. Will never trigger.
7	L2ItlbParity . Read-write. Reset: 0. L2-TLB Parity Error.
6	L1ItlbParity . Read-write. Reset: 0. L1-TLB Parity Error.
5	RSVD_5 . Read-write. Reset: 0. Reserved. Will never trigger.
4	DqParity . Read-write. Reset: 0. PRQ Parity Error.
3	DataParity . Read-write. Reset: 0. IC Data Array Parity Error.
2	TagParity . Read-write. Reset: 0. IC Full Tag Parity Error.
1	TagMultiHit . Read-write. Reset: 0. IC Microtag or Full Tag Multi-hit Error.
0	OcUtagParity . Read-write. Reset: 0. Op Cache Microtag Parity Error. Parity errors on PA and other relevant uTag fields are reported, independent of any utag probing. The parity error way and index are logged.

MSR0000_0405...MSRC000_2011 [IF Machine Check Status Thread 0] (MCA::IF::MCA_STATUS_IF)

Reset: Cold,0000_0000_0000_0000h.

Logs information associated with errors.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst1_n[31:0]_aliasMSRLEGACY; MSR0000_0405

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst1_n[31:0]_aliasMSR; MSRC000_2011

Bits	Description
63	Val. Reset: Cold,0. 1=A valid error has been detected. This bit should be cleared by software after the register has been read. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
62	Overflow. Reset: Cold,0. 1=An error was detected while the valid bit (Val) was set; at least one error was not logged. Overflow is set independently of whether the existing error is overwritten. See 3.1.3 [Machine Check Errors]. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
61	UC. Reset: Cold,0. 1=The error was not corrected by hardware. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
60	En. Reset: Cold,0. 1=MCA error reporting is enabled for this error, as indicated by the corresponding bit in MCA::IF::MCA_CTL_IF. This bit is a copy of bit in MCA::IF::MCA_CTL_IF for this error. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
59	MiscV. Reset: Cold,0. 1=Valid thresholding in MCA::IF::MCA_MISC0_IF. In certain modes, MISC registers are owned by platform firmware and will RAZ when read by non-SMM code. Therefore, it is possible for MiscV=1 and the MISC register to read as all zeros. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
58	AddrV. Reset: Cold,0. 1=MCA::IF::MCA_ADDR_IF contains address information associated with the error. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
57	PCC. Reset: Cold,0. 1=Hardware context held by the processor may have been corrupted. Continued operation of the system may have unpredictable results. The error is not recoverable or survivable, and the system should be reinitialized. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
56	ErrCoreIdVal. Reset: Cold,0. 1=The ErrCoreId field is valid. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
55	TCC. Reset: Cold,0. 1=Hardware context of the process thread to which the error was reported may have been corrupted. Continued operation of the thread may have unpredictable results. The thread must be terminated. Only meaningful when MCA::IF::MCA_STATUS_IF[PCC]=0. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
54	RESERV54. Reset: Cold,0. MCA_STATUS Register Reserved bit. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
53	SyndV. Reset: Cold,0. 1=This error logged information in MCA::IF::MCA_SYND_IF. If MCA::IF::MCA_SYND_IF[ErrorPriority] is the same as the priority of the error in MCA::IF::MCA_STATUS_IF, then the information in MCA::IF::MCA_SYND_IF is associated with the error in MCA::IF::MCA_STATUS_IF. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
52	Reserved.
51:47	RESERV47. Reset: Cold,00h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
46	CECC. Reset: Cold,0. 1=The error was a correctable ECC error according to the restrictions of the ECC algorithm. UC indicates whether the error was actually corrected by the processor. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
45	UECC. Reset: Cold,0. 1=The error was an uncorrectable ECC error according to the restrictions of the ECC algorithm. UC indicates whether the error was actually corrected by the processor. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.

44	Deferred. Reset: Cold,0. 1=A deferred error was created. A deferred error is the result of an uncorrectable data error which did not immediately cause a processor exception; an exception is deferred until the erroneous data is consumed. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
43	Poison. Reset: Cold,0. 1=The error was the result of attempting to consume poisoned data. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
42:41	RESERV41. Reset: Cold,0h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
40	Scrub. Reset: Cold,0. 1=The error was the result of a scrub operation. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
39:38	RESERV38. Reset: Cold,0h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
37:32	ErrCoreId. Reset: Cold,00h. When ErrCoreIdVal=1 this field indicates which core within the processor is associated with the error; Otherwise this field is reserved. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
31:30	RESERV30. Reset: Cold,0h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
29:24	AddrLsb. Reset: Cold,00h. Specifies the least significant valid bit of the address contained in MCA::IF::MCA_ADDR_IF[ErrorAddr]. A value of 0 indicates that MCA::IF::MCA_ADDR_IF[56:0] contains a valid byte address. A value of 6 indicates that MCA::IF::MCA_ADDR_IF[56:6] contains a valid cache line address and that MCA::IF::MCA_ADDR_IF[5:0] are not part of the address and should be ignored by error handling software. A value of 12 indicates that MCA::IF::MCA_ADDR_IF[56:12] contain a valid 4KB memory page and that MCA::IF::MCA_ADDR_IF[11:0] should be ignored by error handling software. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
23:22	RESERV22. Reset: Cold,0h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
21:16	ErrorCodeExt. Reset: Cold,00h. Extended Error Code. This field is used to identify the error type for root cause analysis. This field indicates which bit position in MCA::IF::MCA_CTL_IF enables error reporting for the logged error. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
15:0	ErrorCode. Reset: Cold,0000h. Error code for this error. See 3.1.3.3 [Error Codes] for details on decoding this field. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.

Table 40: MCA_STATUS_IF

Error Type	ErrorCode Ext	UC	PCC	TCC	Deferred	Poison	AddrV
OcUtagParity	0x0	1	1	1	0	0	0
TagMultiHit	0x1	0	0	0	0	0	1
TagParity	0x2	0	0	0	0	0	1
DataParity	0x3	0	0	0	0	0	1
DqParity	0x4	1	1	1	0	0	0
RSVD_5	0x5	1	1	1	0	0	0
L1ItlbParity	0x6	0	0	0	0	0	1
L2ItlbParity	0x7	0	0	0	0	0	1
RSVD_8	0x8	1	1	1	0	0	0
BpqSnpParT1	0x9	0	0	0	0	0	0

L1BtbMultiHit	0xa	0	0	0	0	0	0
L2BtbMultiHit	0xb	0	0	0	0	0	0
L2RespPoison	0xc	1	0	1	0	1	1
SystemReadDataError	0xd	1	0	1	0	0	1
HwAssert	0xe	1	1	1	0	0	0
L1TlbMultiHit	0xf	0	0	0	0	0	1
L2TlbMultiHit	0x10	0	0	0	0	0	1
BsrParity	0x11	1	1	1	0	0	0
CtMceError	0x12	1	1	1	0	0	0

MSR0000_0406...MSRC000_2012 [IF Machine Check Address Thread 0] (MCA::IF::MCA_ADDR_IF)

Reset: Cold,0000_0000_0000_0000h.

MCA::IF::MCA_ADDR_IF stores an address and other information associated with the error in MCA::IF::MCA_STATUS_IF. The register is only meaningful if MCA::IF::MCA_STATUS_IF[Val]=1 and MCA::IF::MCA_STATUS_IF[AddrV]=1.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst1_n[31:0]_aliasMSRLEGACY; MSR0000_0406

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst1_n[31:0]_aliasMSR; MSRC000_2012

Bits	Description
63:57	Reserved.
56:0	ErrorAddr. Read-write, Volatile. Reset: Cold,000_0000_0000_0000h. Unless otherwise specified by an error, contains the address associated with the error logged in MCA::IF::MCA_STATUS_IF. For physical addresses, the most significant bit is given by Core::X86::Cpuid::LongModeInfo[PhysAddrSize].

Table 41: MCA_ADDR_IF

Error Type	Bits	Description
OcUtagParity	[56:0]	Reserved
TagMultiHit	[56:52] [51:0]	Reserved Physical Address
TagParity	[56:52] [51:0]	Reserved Physical Address
DataParity	[56:0]	VA
DqParity	[56:0]	Reserved
RSVD_5	[56:0]	Reserved
L1ItlbParity	[56:0]	VA
L2ItlbParity	[56:0]	VA
RSVD_8	[56:0]	Reserved
BpqSnpParT1	[56:0]	Reserved
L1BtbMultiHit	[56:0]	Reserved
L2BtbMultiHit	[56:0]	Reserved
L2RespPoison	[56:0]	VA
SystemReadDataError	[56:0]	VA
HwAssert	[56:0]	Reserved
L1TlbMultiHit	[56:0]	VA
L2TlbMultiHit	[56:0]	VA

BsrParity	[56:0]	Reserved
CtMceError	[56:0]	Reserved

MSR0000_0407...MSRC000_2013 [IF Machine Check Miscellaneous 0 Thread 0] (MCA::IF::MCA_MISC0_IF)

Log miscellaneous information associated with errors.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst1_n[31:0]_aliasMSRLEGACY; MSR0000_0407

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst1_n[31:0]_aliasMSR; MSRC000_2013

Bits	Description
63	Valid. Reset: 1. 1=A valid CntP field is present in this register. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read-only.
62	CntP. Reset: 1. 1=A valid threshold counter is present. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read-only.
61	Locked. Reset: 0. 1=Writes to this register are ignored. This bit is set by BIOS to indicate that this register is not available for OS use. BIOS should set this bit if ThresholdIntType is set to SMI. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read-only.
60	IntP. Reset: 1. 1=ThresholdIntType can be used to generate interrupts. 0=ThresholdIntType and interrupt generation are not supported. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::IF::MCA_MISC0_IF[Locked]) ? Read-write : Read-only.
59:56	Reserved.
55:52	LvtOffset. Reset: 0h. One per die. For error thresholding interrupts, specifies the address of the LVT entry in the APIC registers as follows: LVT address = (LvtOffset shifted left 4 bits) + 500h (see Core::X86::Apic::ExtendedInterruptLvtEntries). AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::IF::MCA_MISC0_IF[Locked]) ? Read-write : Read-only.
51	CntEn. Reset: 0. 1=Count thresholding errors. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::IF::MCA_MISC0_IF[Locked]) ? Read-write : Read-only.
50:49	ThresholdIntType. Reset: Cold,0h. Specifies the type of interrupt signaled when Ovrflw is set and IntP==1. 00b = No interrupt. 01b = APIC based interrupt (see Core::X86::Msr::McaIntrCfg[ThresholdLvtOffset]). 10b = SMI trigger event. 11b = Reserved. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::IF::MCA_MISC0_IF[Locked]) ? Read-write : Read-only.
48	Ovrflw. Reset: Cold,0. Set by hardware when ErrCnt transitions from FFEh to FFFh. When this field is set, ErrCnt no longer increments. When this bit is set, the interrupt selected by the ThresholdIntType field is generated. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::IF::MCA_MISC0_IF[Locked]) ? Read-write : Read-only.
47:44	Reserved.
43:32	ErrCnt. Reset: Cold,000h. This is written by software to set the starting value of the error counter. This is incremented by hardware when errors are logged. When this counter overflows, it stays at FFFh (no rollover). The threshold value, written by software, is (FFFh - the desired error count (the number of errors necessary in order for an interrupt to be taken)); the desired error count of 0 (a write value of FFFh) is not supported. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::IF::MCA_MISC0_IF[Locked]) ? Read-write : Read-only.
31:24	BlkPtr. Read-write. Reset: 00h. 00h=Extended MISC MSR block is not valid. 01h=Extended MSR block is valid.
23:0	Reserved.

MSRC000_2014 [IF Machine Check Configuration Thread 0] (MCA::IF::MCA_CONFIG_IF)

Reset: 0000_0002_0000_0121h.

Controls configuration of the associated machine check bank.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst1_n[31:0]_aliasMSR; MSRC000_2014

Bits	Description
63:39	Reserved.
38:37	DeferredIntType. Read-write. Reset: 0h. Specifies the type of interrupt signaled when a deferred error is logged. 00b = No interrupt. 01b = APIC based interrupt (see Core::X86::Msr::McaIntrCfg[DeferredLvtOffset]). 10b = SMI trigger event. 11b = Reserved.
36:33	Reserved.
32	McaXEnable. Read-write. Reset: 0. Init: BIOS,1. Check: 1. 1=Software has acknowledged support for the MCAX feature set. 0=Software has not acknowledged support for the MCAX feature set. All uncorrected and fatal errors will cause an ErrorEvent packet to be generated. Deferred error interrupts are configured via Core::X86::Msr::McaIntrCfg.
31:9	Reserved.
8	McaLsbInStatusSupported. Read-only. Reset: 1. 1=MCA::IF::MCA_CONFIG_IF[McaLsbInStatusSupported] indicates that AddrLsb is located in McaStatus registers.
7:6	Reserved.
5	DeferredIntTypeSupported. Read-only. Reset: 1. 1=MCA::IF::MCA_CONFIG_IF[DeferredIntType] controls the type of interrupt generated on a deferred error. Deferred errors are supported in this bank only if MCA::IF::MCA_CONFIG_IF[DeferredErrorLoggingSupported]=1.
4:3	Reserved.
2	DeferredErrorLoggingSupported. Read-only. Reset: 0. 1=Deferred errors are supported in this MCA bank, and the LogDeferredInMcaStat field in this register controls the logging behavior of these errors. 0=Deferred errors are not supported in this bank.
1	Reserved.
0	McaX. Read-only. Reset: 1. 1=This bank provides Machine Check Architecture Extensions. Up to 4 additional MISC registers (MISC1-MISC4) are supported. MCA::IF::MCA_MISC0_IF[BlkPtr] indicates the presence of the additional MISC registers, but is not used to determine their MSR numbers. Deferred error interrupt type is specifiable by MCA bank. MCA::IF::MCA_STATUS_IF[TCC] is present.

MSRC000_2015 [IF IP Identification Thread 0] (MCA::IF::MCA_IPID_IF)

Reset: 0001_00B0_0000_0000h.

The MCA::IF::MCA_IPID_IF register is used by software to determine what IP type and revision is associated with the MCA bank.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst1_n[31:0]_aliasMSR; MSRC000_2015

Bits	Description
63:48	McaType . Read-only. Reset: 0001h. The McaType of the MCA bank within this IP.
47:44	InstanceIdHi . Read-write. Reset: 0h. The HI value instance ID of this IP. This is initialized to a unique ID per instance of this register.
43:32	HardwareID . Read-only. Reset: 0B0h. The Hardware ID of the IP associated with this MCA bank.
31:0	InstanceId . Read-write. Reset: 0000_0000h. The instance ID of this IP. This is initialized to a unique ID per instance of this register.
	Init: _ccd0_lthree0_core0_thread0_inst1_n0_aliasMSR: 2000_AA00h
	Init: _ccd0_lthree0_core0_thread1_inst1_n1_aliasMSR: 2000_AB00h
	Init: _ccd0_lthree0_core1_thread0_inst1_n2_aliasMSR: 2002_AA00h
	Init: _ccd0_lthree0_core1_thread1_inst1_n3_aliasMSR: 2002_AB00h
	Init: _ccd0_lthree0_core2_thread0_inst1_n4_aliasMSR: 2004_AA00h
	Init: _ccd0_lthree0_core2_thread1_inst1_n5_aliasMSR: 2004_AB00h
	Init: _ccd0_lthree0_core3_thread0_inst1_n6_aliasMSR: 2006_AA00h
	Init: _ccd0_lthree0_core3_thread1_inst1_n7_aliasMSR: 2006_AB00h
	Init: _ccd0_lthree0_core4_thread0_inst1_n8_aliasMSR: 2008_AA00h
	Init: _ccd0_lthree0_core4_thread1_inst1_n9_aliasMSR: 2008_AB00h
	Init: _ccd0_lthree0_core5_thread0_inst1_n10_aliasMSR: 200A_AA00h
	Init: _ccd0_lthree0_core5_thread1_inst1_n11_aliasMSR: 200A_AB00h
	Init: _ccd0_lthree0_core6_thread0_inst1_n12_aliasMSR: 200C_AA00h
	Init: _ccd0_lthree0_core6_thread1_inst1_n13_aliasMSR: 200C_AB00h
	Init: _ccd0_lthree0_core7_thread0_inst1_n14_aliasMSR: 200E_AA00h
	Init: _ccd0_lthree0_core7_thread1_inst1_n15_aliasMSR: 200E_AB00h
	Init: _ccd1_lthree0_core0_thread0_inst1_n16_aliasMSR: 2080_AA00h
	Init: _ccd1_lthree0_core0_thread1_inst1_n17_aliasMSR: 2080_AB00h
	Init: _ccd1_lthree0_core1_thread0_inst1_n18_aliasMSR: 2082_AA00h
	Init: _ccd1_lthree0_core1_thread1_inst1_n19_aliasMSR: 2082_AB00h
	Init: _ccd1_lthree0_core2_thread0_inst1_n20_aliasMSR: 2084_AA00h
	Init: _ccd1_lthree0_core2_thread1_inst1_n21_aliasMSR: 2084_AB00h
	Init: _ccd1_lthree0_core3_thread0_inst1_n22_aliasMSR: 2086_AA00h
	Init: _ccd1_lthree0_core3_thread1_inst1_n23_aliasMSR: 2086_AB00h
	Init: _ccd1_lthree0_core4_thread0_inst1_n24_aliasMSR: 2088_AA00h
	Init: _ccd1_lthree0_core4_thread1_inst1_n25_aliasMSR: 2088_AB00h
	Init: _ccd1_lthree0_core5_thread0_inst1_n26_aliasMSR: 208A_AA00h
	Init: _ccd1_lthree0_core5_thread1_inst1_n27_aliasMSR: 208A_AB00h
	Init: _ccd1_lthree0_core6_thread0_inst1_n28_aliasMSR: 208C_AA00h
	Init: _ccd1_lthree0_core6_thread1_inst1_n29_aliasMSR: 208C_AB00h
	Init: _ccd1_lthree0_core7_thread0_inst1_n30_aliasMSR: 208E_AA00h
	Init: _ccd1_lthree0_core7_thread1_inst1_n31_aliasMSR: 208E_AB00h

MSRC000_2016 [IF Machine Check Syndrome Thread 0] (MCA::IF::MCA_SYND_IF)

Read-write, Volatile. Reset: Cold, 0000_0000_0000_0000h.	
Logs physical location information associated with error in MCA::IF::MCA_STATUS_IF Thread 0	
_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst1_n[31:0]_aliasMSR; MSRC000_2016	
Bits	Description
63:33	Reserved.
32	Syndromes. Read-write, Volatile. Reset: Cold, 0. Contains the syndrome, if any, associated with the error logged in MCA::IF::MCA_STATUS_IF. The low-order bit of the syndrome is stored in bit 0, and the syndrome has a length specified by MCA::IF::MCA_SYND_IF[Length]. The Syndrome field is only valid when MCA::IF::MCA_SYND_IF[Length] is not 0.
31:27	Reserved.
26:24	ErrorPriority. Read-write, Volatile. Reset: Cold, 0h. Encodes the priority of the error logged in MCA::IF::MCA_SYND_IF. 3'b000 = No error; 3'b001 = Reserved; 3'b010 = Corrected Error; 3'b011 = Deferred Error; 3'b100 = Uncorrected Error; 3'b101 = Fatal Error; all others reserved.
23:18	Length. Read-write, Volatile. Reset: Cold, 00h. Specifies the length in bits of the syndrome contained in MCA::IF::MCA_SYND_IF[Syndrome]. A value of 0 indicates that there is no valid syndrome in MCA::IF::MCA_SYND_IF. For example, a syndrome length of 9 means that MCA::IF::MCA_SYND_IF[Syndrome] bits [8:0] contains a valid syndrome.
17:0	ErrorInformation. Read-write, Volatile. Reset: Cold, 0_0000h. Contains error-specific information about the location of the error. Decoding is available in Table 42 [MCA_SYND_IF].

Table 42: MCA_SYND_IF

Error Type	Bits	Description
OcUtagParity	[17:16]	Reserved
	[15:8]	Way bit vector
	[7:6]	Reserved
	[5:0]	Index
TagMultiHit	[17:16]	Reserved
	[15:8]	Way bit vector
	[7:6]	Reserved
	[5:0]	Index
TagParity	[17]	Reserved
	[16]	Way Valid
	[15:8]	Reserved
	[7:0]	Way bit vector
DataParity	[17:15]	Reserved
	[14:12]	Data Bank
	[11:8]	Sub-Bank
	[7:0]	Index
DqParity	[17]	Reserved
	[16]	PA Error Valid
	[15:0]	Way bit vector
RSVD_5	[17:0]	Reserved
L1ItlbParity	[17:6]	Reserved
	[5:0]	Index
L2ItlbParity	[17:16]	Reserved
	[15:8]	Way bit vector
	[7:6]	Reserved

	[5:0]	Index
RSVD_8	[17:0]	Reserved
BpqSnpParT1	[17:16] [15:8] [7:6] [5:0]	Reserved Way bit vector Reserved Index
L1BtbMultiHit	[17:12] [11:8] [7:0]	Reserved Way bit vector Index
L2BtbMultiHit	[17:12] [11:9] [8:0]	Reserved Table Index
L2RespPoison	[17:0]	Reserved
SystemReadDataError	[17:4] [3] [2] [1] [0]	Reserved Protection Violation Transaction Error Target Abort Master Abort
HwAssert	[17:5] [4:0]	Assertion log Code
L1TlbMultiHit	[17:6] [5:0]	Reserved Index
L2TlbMultiHit	[17:16] [15:8] [7:6] [5:0]	Reserved Way bit vector Reserved Index
BsrParity	[17:8] [7:0]	Reserved Index
CtMceError	[17:2] [1:0]	Reserved Thread bit vector

MSRC001_0401 [IF Machine Check Control Mask Thread 0] (MCA::IF::MCA_CTL_MASK_IF)

Read-write. Reset: 0000_0000_0000_0000h.

Inhibit detection of an error source.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst1_n[31:0]_aliasMSR; MSRC001_0401

Bits	Description
63:19	Reserved.
18	CtMceError . Read-write. Reset: 0. CT MCE.
17	BsrParity . Read-write. Reset: 0. BSR Parity Error.
16	L2TlbMultiHit . Read-write. Reset: 0. Init: BIOS,1. L2-TLB Multi-Hit
15	L1TlbMultiHit . Read-write. Reset: 0. L1-TLB Multi-Hit.
14	HwAssert . Read-write. Reset: 0. Hardware Assertion Error.
13	SystemReadDataError . Read-write. Reset: 0. Init: BIOS,1. L2 Cache Error Response.
12	L2RespPoison . Read-write. Reset: 0. L2 Cache Response Poison Error. Error is the result of consuming poison data.
11	L2BtbMultiHit . Read-write. Reset: 0. Init: BIOS,1. BP L2-BTB Multi-Hit Error.
10	L1BtbMultiHit . Read-write. Reset: 0. BP L1-BTB Multi-Hit Error.
9	BpqSnpParT1 . Read-write. Reset: 0. BPQ Thread 1 Snooper Parity Error.
8	RSVD_8 . Read-write. Reset: 0. Reserved. Will never trigger.
7	L2ItlbParity . Read-write. Reset: 0. L2-TLB Parity Error.
6	L1ItlbParity . Read-write. Reset: 0. L1-TLB Parity Error.
5	RSVD_5 . Read-write. Reset: 0. Reserved. Will never trigger.
4	DqParity . Read-write. Reset: 0. PRQ Parity Error.
3	DataParity . Read-write. Reset: 0. IC Data Array Parity Error.
2	TagParity . Read-write. Reset: 0. IC Full Tag Parity Error.
1	TagMultiHit . Read-write. Reset: 0. IC Microtag or Full Tag Multi-hit Error.
0	OcUtagParity . Read-write. Reset: 0. Op Cache Microtag Parity Error. Parity errors on PA and other relevant uTag fields are reported, independent of any utag probing. The parity error way and index are logged.

3.2.5.3 L2**MSR0000_0408...MSRC000_2020 [L2 Machine Check Control Thread 0] (MCA::L2::MCA_CTL_L2)**

Read-write. Reset: 0000_0000_0000_0000h.

0=Disables error reporting for the corresponding error. 1=Enables error reporting via machine check exception for the corresponding error. The MCA::L2::MCA_CTL_L2 register must be enabled by the corresponding enable bit in Core::X86::Msr::MCG_CTL. Does not affect error detection, correction, or logging.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst2_n[31:0]_aliasMSRLEGACY; MSR0000_0408

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst2_n[31:0]_aliasMSR; MSRC000_2020

Bits	Description
63:5	Reserved.
4	Sdp . Read-write. Reset: 0. SDP Read Response Parity Error
3	Hwa . Read-write. Reset: 0. Hardware Assert Error.
2	Data . Read-write. Reset: 0. L2M Data Array ECC Error.
1	Tag . Read-write. Reset: 0. L2M Tag or State Array ECC Error.
0	MultiHit . Read-write. Reset: 0. L2M Tag Multiple-Way-Hit error.

MSR0000_0409...MSRC000_2021 [L2 Machine Check Status Thread 0] (MCA::L2::MCA_STATUS_L2)

Reset: Cold,0000_0000_0000_0000h.

Logs information associated with errors.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst2_n[31:0]_aliasMSRLEGACY; MSR0000_0409

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst2_n[31:0]_aliasMSR; MSRC000_2021

Bits	Description
63	Val. Reset: Cold,0. 1=A valid error has been detected. This bit should be cleared by software after the register has been read. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
62	Overflow. Reset: Cold,0. 1=An error was detected while the valid bit (Val) was set; at least one error was not logged. Overflow is set independently of whether the existing error is overwritten. See 3.1.3 [Machine Check Errors]. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
61	UC. Reset: Cold,0. 1=The error was not corrected by hardware. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
60	En. Reset: Cold,0. 1=MCA error reporting is enabled for this error, as indicated by the corresponding bit in MCA::L2::MCA_CTL_L2. This bit is a copy of bit in MCA::L2::MCA_CTL_L2 for this error. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
59	MiscV. Reset: Cold,0. 1=Valid thresholding in MCA::L2::MCA_MISC0_L2. In certain modes, MISC registers are owned by platform firmware and will RAZ when read by non-SMM code. Therefore, it is possible for MiscV=1 and the MISC register to read as all zeros. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
58	AddrV. Reset: Cold,0. 1=MCA::L2::MCA_ADDR_L2 contains address information associated with the error. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
57	PCC. Reset: Cold,0. 1=Hardware context held by the processor may have been corrupted. Continued operation of the system may have unpredictable results. The error is not recoverable or survivable, and the system should be reinitialized. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
56	ErrCoreIdVal. Reset: Cold,0. 1=The ErrCoreId field is valid. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
55	TCC. Reset: Cold,0. 1=Hardware context of the process thread to which the error was reported may have been corrupted. Continued operation of the thread may have unpredictable results. The thread must be terminated. Only meaningful when MCA::L2::MCA_STATUS_L2[PCC]=0. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
54	RESERV54. Reset: Cold,0. MCA_STATUS Register Reserved bit. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
53	SyndV. Reset: Cold,0. 1=This error logged information in MCA::L2::MCA_SYND_L2. If MCA::L2::MCA_SYND_L2[ErrorPriority] is the same as the priority of the error in MCA::L2::MCA_STATUS_L2, then the information in MCA::L2::MCA_SYND_L2 is associated with the error in MCA::L2::MCA_STATUS_L2. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
52	Reserved.
51:47	RESERV47. Reset: Cold,00h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
46	CECC. Reset: Cold,0. 1=The error was a correctable ECC error according to the restrictions of the ECC algorithm. UC indicates whether the error was actually corrected by the processor. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
45	UECC. Reset: Cold,0. 1=The error was an uncorrectable ECC error according to the restrictions of the ECC algorithm. UC indicates whether the error was actually corrected by the processor. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.

44	Deferred. Reset: Cold,0. 1=A deferred error was created. A deferred error is the result of an uncorrectable data error which did not immediately cause a processor exception; an exception is deferred until the erroneous data is consumed. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
43	Poison. Reset: Cold,0. 1=The error was the result of attempting to consume poisoned data. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
42:41	RESERV41. Reset: Cold,0h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
40	Scrub. Reset: Cold,0. 1=The error was the result of a scrub operation. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
39:38	RESERV38. Reset: Cold,0h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
37:32	ErrCoreId. Reset: Cold,00h. When ErrCoreIdVal=1 this field indicates which core within the processor is associated with the error; Otherwise this field is reserved. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
31:30	RESERV30. Reset: Cold,0h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
29:24	AddrLsb. Reset: Cold,00h. Specifies the least significant valid bit of the address contained in MCA::L2::MCA_ADDR_L2[ErrorAddr]. A value of 0 indicates that MCA::L2::MCA_ADDR_L2[55:0] contains a valid byte address. A value of 6 indicates that MCA::L2::MCA_ADDR_L2[55:6] contains a valid cache line address and that MCA::L2::MCA_ADDR_L2[5:0] are not part of the address and should be ignored by error handling software. A value of 12 indicates that MCA::L2::MCA_ADDR_L2[55:12] contain a valid 4KB memory page and that MCA::L2::MCA_ADDR_L2[11:0] should be ignored by error handling software. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
23:22	RESERV22. Reset: Cold,0h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
21:16	ErrorCodeExt. Reset: Cold,00h. Extended Error Code. This field is used to identify the error type for root cause analysis. This field indicates which bit position in MCA::L2::MCA_CTL_L2 enables error reporting for the logged error. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
15:0	ErrorCode. Reset: Cold,0000h. Error code for this error. See 3.1.3.3 [Error Codes] for details on decoding this field. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.

Table 43: MCA_STATUS_L2

Error Type	ErrorCode Ext	UC	PCC	TCC	Deferred	Poison	AddrV
MultiHit	0x0	1	1	1	0	0	1
Tag	0x1	0/1	0/1	0/1	0	0	1
Data	0x2	0/1	0/1	0/1	0/1	0	1
Hwa	0x3	1	1	1	0	0	1
Sdp	0x4	0/1	0/1	0/1	0/1	0	0

MSR0000_040A...MSRC000_2022 [L2 Machine Check Address Thread 0] (MCA::L2::MCA_ADDR_L2)

Reset: Cold,0000_0000_0000_0000h.

MCA::L2::MCA_ADDR_L2 stores an address and other information associated with the error in MCA::L2::MCA_STATUS_L2. The register is only meaningful if MCA::L2::MCA_STATUS_L2[Val]=1 and MCA::L2::MCA_STATUS_L2[AddrV]=1.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst2_n[31:0]_aliasMSRLEGACY; MSR0000_040A

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst2_n[31:0]_aliasMSR; MSRC000_2022

Bits	Description
63:56	Reserved.
55:0	ErrorAddr. Read-write, Volatile. Reset: Cold,00_0000_0000_0000h. Unless otherwise specified by an error, contains the address associated with the error logged in MCA::L2::MCA_STATUS_L2. For physical addresses, the most significant bit is given by Core::X86::CpuId::LongModeInfo[PhysAddrSize].

Table 44: MCA_ADDR_L2

Error Type	Bits	Description
MultiHit	[55:52]	Reserved
	[51:6]	Physical Address
	[5:0]	Reserved
Tag	[55:52]	Reserved
	[51:6]	Physical Address
	[5:0]	Reserved
Data	[55:52]	Reserved
	[51:6]	Physical Address
	[5:0]	Reserved
Hwa	[31:0]	Reserved
Sdp	[55:0]	Reserved

MSR0000_040B...MSRC000_2023 [L2 Machine Check Miscellaneous 0 Thread 0] (MCA::L2::MCA_MISC0_L2)

Log miscellaneous information associated with errors.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst2_n[31:0]_aliasMSRLEGACY; MSR0000_040B

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst2_n[31:0]_aliasMSR; MSRC000_2023

Bits	Description
63	Valid. Reset: 1. 1=A valid CntP field is present in this register. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read-only.
62	CntP. Reset: 1. 1=A valid threshold counter is present. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read-only.
61	Locked. Reset: 0. 1=Writes to this register are ignored. This bit is set by BIOS to indicate that this register is not available for OS use. BIOS should set this bit if ThresholdIntType is set to SMI. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read-only.
60	IntP. Reset: 1. 1=ThresholdIntType can be used to generate interrupts. 0=ThresholdIntType and interrupt generation are not supported. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::L2::MCA_MISC0_L2[Locked]) ? Read-write : Read-only.
59:56	Reserved.
55:52	LvtOffset. Reset: 0h. One per die. For error thresholding interrupts, specifies the address of the LVT entry in the APIC registers as follows: LVT address = (LvtOffset shifted left 4 bits) + 500h (see Core::X86::Apic::ExtendedInterruptLvtEntries). AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::L2::MCA_MISC0_L2[Locked]) ? Read-write : Read-only.
51	CntEn. Reset: 0. 1=Count thresholding errors. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::L2::MCA_MISC0_L2[Locked]) ? Read-write : Read-only.
50:49	ThresholdIntType. Reset: Cold,0h. Specifies the type of interrupt signaled when Ovrlw is set and IntP==1. 00b = No interrupt. 01b = APIC based interrupt (see Core::X86::Msr::McaIntrCfg[ThresholdLvtOffset]). 10b = SMI trigger event. 11b = Reserved. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::L2::MCA_MISC0_L2[Locked]) ? Read-write : Read-only.
48	Ovrlw. Reset: Cold,0. Set by hardware when ErrCnt transitions from FFEh to FFFh. When this field is set, ErrCnt no longer increments. When this bit is set, the interrupt selected by the ThresholdIntType field is generated. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::L2::MCA_MISC0_L2[Locked]) ? Read-write : Read-only.
47:44	Reserved.
43:32	ErrCnt. Reset: Cold,000h. This is written by software to set the starting value of the error counter. This is incremented by hardware when errors are logged. When this counter overflows, it stays at FFFh (no rollover). The threshold value, written by software, is (FFFh - the desired error count (the number of errors necessary in order for an interrupt to be taken)); the desired error count of 0 (a write value of FFFh) is not supported. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::L2::MCA_MISC0_L2[Locked]) ? Read-write : Read-only.
31:24	BlkPtr. Read-write. Reset: 00h. 00h=Extended MISC MSR block is not valid. 01h=Extended MSR block is valid.
23:0	Reserved.

MSRC000_2024 [L2 Machine Check Configuration Thread 0] (MCA::L2::MCA_CONFIG_L2)

Reset: 0000_0000_0000_0125h.	
Controls configuration of the associated machine check bank.	
_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst2_n[31:0]_aliasMSR; MSRC000_2024	
Bits	Description
63:39	Reserved.
38:37	DeferredIntType. Read-write. Reset: 0h. Specifies the type of interrupt signaled when a deferred error is logged. 00b = No interrupt. 01b = APIC based interrupt (see Core::X86::Msr::McaIntrCfg[DeferredLvtOffset]). 10b = SMI trigger event. 11b = Reserved.
36:35	Reserved.
34	LogDeferredInMcaStat. Read-write. Reset: 0. Init: BIOS,1. 1=Log deferred errors in MCA::L2::MCA_STATUS_L2 and MCA::L2::MCA_ADDR_L2 in addition to MCA::L2::MCA_DESTAT_L2 and MCA::L2::MCA_DEADDR_L2. 0=Only log deferred errors in MCA::L2::MCA_DESTAT_L2 and MCA::L2::MCA_DEADDR_L2. This bit does not affect logging of deferred errors in MCA::L2::MCA_SYND_L2, MCA::L2::MCA_MISC0_L2.
33	Reserved.
32	McaXEnable. Read-write. Reset: 0. Init: BIOS,1. Check: 1. 1=Software has acknowledged support for the MCAX feature set. 0=Software has not acknowledged support for the MCAX feature set. All uncorrected and fatal errors will cause an ErrorEvent packet to be generated. Deferred error interrupts are configured via Core::X86::Msr::McaIntrCfg.
31:9	Reserved.
8	McaLsbInStatusSupported. Read-only. Reset: 1. 1=MCA::L2::MCA_CONFIG_L2[McaLsbInStatusSupported] indicates that AddrLsb is located in McaStatus registers.
7:6	Reserved.
5	DeferredIntTypeSupported. Read-only. Reset: 1. 1=MCA::L2::MCA_CONFIG_L2[DeferredIntType] controls the type of interrupt generated on a deferred error. Deferred errors are supported in this bank only if MCA::L2::MCA_CONFIG_L2[DeferredErrorLoggingSupported]=1.
4:3	Reserved.
2	DeferredErrorLoggingSupported. Read-only. Reset: 1. 1=Deferred errors are supported in this MCA bank, and MCA::L2::MCA_CONFIG_L2[LogDeferredInMcaStat] controls the logging behavior of these errors. MCA::L2::MCA_DESTAT_L2 and MCA::L2::MCA_DEADDR_L2 are supported in this MCA bank. 0=Deferred errors are not supported in this bank.
1	Reserved.
0	McaX. Read-only. Reset: 1. 1=This bank provides Machine Check Architecture Extensions. Up to 4 additional MISC registers (MISC1-MISC4) are supported. MCA::L2::MCA_MISC0_L2[BlkPtr] indicates the presence of the additional MISC registers, but is not used to determine their MSR numbers. Deferred error interrupt type is specifiable by MCA bank. MCA::L2::MCA_STATUS_L2[TCC] is present.

MSRC000_2025 [L2 IP Identification Thread 0] (MCA::L2::MCA_IPID_L2)

Reset: 0002_00B0_0000_0000h.

The MCA::L2::MCA_IPID_L2 register is used by software to determine what IP type and revision is associated with the MCA bank.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst2_n[31:0]_aliasMSR; MSRC000_2025

Bits	Description
63:48	McaType . Read-only. Reset: 0002h. The McaType of the MCA bank within this IP.
47:44	InstanceIdHi . Read-write. Reset: 0h. The HI value instance ID of this IP. This is initialized to a unique ID per instance of this register.
43:32	HardwareID . Read-only. Reset: 0B0h. The Hardware ID of the IP associated with this MCA bank.
31:0	InstanceId . Read-write. Reset: 0000_0000h. The instance ID of this IP. This is initialized to a unique ID per instance of this register.
	Init: _ccd0_lthree0_core0_thread0_inst2_n0_aliasMSR: 2000_8A00h
	Init: _ccd0_lthree0_core0_thread1_inst2_n1_aliasMSR: 2000_8B00h
	Init: _ccd0_lthree0_core1_thread0_inst2_n2_aliasMSR: 2002_8A00h
	Init: _ccd0_lthree0_core1_thread1_inst2_n3_aliasMSR: 2002_8B00h
	Init: _ccd0_lthree0_core2_thread0_inst2_n4_aliasMSR: 2004_8A00h
	Init: _ccd0_lthree0_core2_thread1_inst2_n5_aliasMSR: 2004_8B00h
	Init: _ccd0_lthree0_core3_thread0_inst2_n6_aliasMSR: 2006_8A00h
	Init: _ccd0_lthree0_core3_thread1_inst2_n7_aliasMSR: 2006_8B00h
	Init: _ccd0_lthree0_core4_thread0_inst2_n8_aliasMSR: 2008_8A00h
	Init: _ccd0_lthree0_core4_thread1_inst2_n9_aliasMSR: 2008_8B00h
	Init: _ccd0_lthree0_core5_thread0_inst2_n10_aliasMSR: 200A_8A00h
	Init: _ccd0_lthree0_core5_thread1_inst2_n11_aliasMSR: 200A_8B00h
	Init: _ccd0_lthree0_core6_thread0_inst2_n12_aliasMSR: 200C_8A00h
	Init: _ccd0_lthree0_core6_thread1_inst2_n13_aliasMSR: 200C_8B00h
	Init: _ccd0_lthree0_core7_thread0_inst2_n14_aliasMSR: 200E_8A00h
	Init: _ccd0_lthree0_core7_thread1_inst2_n15_aliasMSR: 200E_8B00h
	Init: _ccd1_lthree0_core0_thread0_inst2_n16_aliasMSR: 2080_8A00h
	Init: _ccd1_lthree0_core0_thread1_inst2_n17_aliasMSR: 2080_8B00h
	Init: _ccd1_lthree0_core1_thread0_inst2_n18_aliasMSR: 2082_8A00h
	Init: _ccd1_lthree0_core1_thread1_inst2_n19_aliasMSR: 2082_8B00h
	Init: _ccd1_lthree0_core2_thread0_inst2_n20_aliasMSR: 2084_8A00h
	Init: _ccd1_lthree0_core2_thread1_inst2_n21_aliasMSR: 2084_8B00h
	Init: _ccd1_lthree0_core3_thread0_inst2_n22_aliasMSR: 2086_8A00h
	Init: _ccd1_lthree0_core3_thread1_inst2_n23_aliasMSR: 2086_8B00h
	Init: _ccd1_lthree0_core4_thread0_inst2_n24_aliasMSR: 2088_8A00h
	Init: _ccd1_lthree0_core4_thread1_inst2_n25_aliasMSR: 2088_8B00h
	Init: _ccd1_lthree0_core5_thread0_inst2_n26_aliasMSR: 208A_8A00h
	Init: _ccd1_lthree0_core5_thread1_inst2_n27_aliasMSR: 208A_8B00h
	Init: _ccd1_lthree0_core6_thread0_inst2_n28_aliasMSR: 208C_8A00h
	Init: _ccd1_lthree0_core6_thread1_inst2_n29_aliasMSR: 208C_8B00h
	Init: _ccd1_lthree0_core7_thread0_inst2_n30_aliasMSR: 208E_8A00h
	Init: _ccd1_lthree0_core7_thread1_inst2_n31_aliasMSR: 208E_8B00h

MSRC000_2026 [L2 Machine Check Syndrome Thread 0] (MCA::L2::MCA_SYND_L2)

Read-write, Volatile. Reset: Cold, 0000_0000_0000_0000h.	
Logs physical location information associated with error in MCA::L2::MCA_STATUS_L2 Thread 0	
_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst2_n[31:0]_aliasMSR; MSRC000_2026	
Bits	Description
63:51	Reserved.
50:32	Syndrom . Read-write, Volatile. Reset: Cold, 0_0000h. Contains the syndrome, if any, associated with the error logged in MCA::L2::MCA_STATUS_L2. The low-order bit of the syndrome is stored in bit 0, and the syndrome has a length specified by MCA::L2::MCA_SYND_L2[Length]. The Syndrome field is only valid when MCA::L2::MCA_SYND_L2[Length] is not 0.
31:27	Reserved.
26:24	ErrorPriority . Read-write, Volatile. Reset: Cold, 0h. Encodes the priority of the error logged in MCA::L2::MCA_SYND_L2. 3'b000 = No error; 3'b001 = Reserved; 3'b010 = Corrected Error; 3'b011 = Deferred Error; 3'b100 = Uncorrected Error; 3'b101 = Fatal Error; all others reserved.
23:18	Length . Read-write, Volatile. Reset: Cold, 00h. Specifies the length in bits of the syndrome contained in MCA::L2::MCA_SYND_L2[Syndrome]. A value of 0 indicates that there is no valid syndrome in MCA::L2::MCA_SYND_L2. For example, a syndrome length of 9 means that MCA::L2::MCA_SYND_L2[Syndrome] bits [8:0] contains a valid syndrome.
17:0	ErrorInformation . Read-write, Volatile. Reset: Cold, 0_0000h. Contains error-specific information about the location of the error. Decoding is available in Table 45 [MCA_SYND_L2].

Table 45: MCA_SYND_L2

Error Type	Bits	Description
MultiHit	[18:8] [7:0]	Index One-hot way vector
Tag	[17:14] [13:3] [2:0]	Reserved Index Way
Data	[17:17] [16] [15:5] [4] [3] [2:0]	Reserved Poison Index TopBotLoc Reserved Way
Hwa	[17:0]	Reserved
Sdp	[17:17] [16:6] [5:3] [2:0]	Reserved Addr[16:6] Addr[5:3] L2Way

MSRC000_2028 [L2 Machine Check Deferred Error Status Thread 0] (MCA::L2::MCA_DESTAT_L2)

Reset: Cold,0000_0000_0000_0000h.

Holds status information for the first deferred error seen in this bank.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst2_n[31:0]_aliasMSR; MSRC000_2028

Bits	Description
63	Val. Read-write, Volatile. Reset: Cold,0. 1=A valid error has been detected (whether it is enabled or not).
62	Overflow. Read-write, Volatile. Reset: Cold,0. 1=An error was detected while the valid bit (Val) was set; at least one error was not logged. Overflow is set independently of whether the existing error is overwritten. (See the section on overwrite priorities.)
61:59	RESERV4. Read-write. Reset: Cold,0h.
58	AddrV. Read-write, Volatile. Reset: Cold,0. 1=MCA::L2::MCA_DEADDR_L2 contains address information associated with the error.
57:54	RESERV3. Read-write. Reset: Cold,0h.
53	SyndV. Read-write, Volatile. Reset: Cold,0. 1=This error logged information in MCA::L2::MCA_SYND_L2. If MCA::L2::MCA_SYND_L2[ErrorPriority] is the same as the priority of the error in MCA::L2::MCA_STATUS_L2, then the information in MCA::L2::MCA_SYND_L2 is associated with the error in MCA::L2::MCA_DESTAT_L2.
52:45	RESERV2. Read-write. Reset: Cold,00h.
44	Deferred. Read-write, Volatile. Reset: Cold,0. 1=A deferred error was created. A deferred error is the result of an uncorrectable data error which did not immediately cause a processor exception; poison is created and an exception is deferred until the poison data is consumed.
43:30	RESERV1. Read-write. Reset: Cold,0000h.
29:24	AddrLsb. Read-write, Volatile. Reset: Cold,00h. Specifies the least significant valid bit of the address contained in MCA::L2::MCA_ADDR_L2[ErrorAddr]. A value of 0 indicates that MCA::L2::MCA_ADDR_L2[55:0] contains a valid byte address. A value of 6 indicates that MCA::L2::MCA_ADDR_L2[55:6] contains a valid cache line address and that MCA::L2::MCA_ADDR_L2[5:0] are not part of the address and should be ignored by error handling software. A value of 12 indicates that MCA::L2::MCA_ADDR_L2[55:12] contain a valid 4KB memory page and that MCA::L2::MCA_ADDR_L2[11:0] should be ignored by error handling software.
23:22	RESERV0. Read-write. Reset: Cold,0h.
21:16	ErrorCodeExt. Read-write, Volatile. Reset: Cold,00h. Logs an extended error code when an error is detected. This model-specific field is used in conjunction with ErrorCode? to identify the error sub-type for root cause analysis.
15:0	ErrorCode. Read-write, Volatile. Reset: Cold,0000h. Error code for this error.

MSRC000_2029 [L2 Deferred Error Address Thread 0] (MCA::L2::MCA_DEADDR_L2)

Reset: Cold,0000_0000_0000_0000h.

The MCA::L2::MCA_DEADDR_L2 register stores the address associated with the error in MCA::L2::MCA_DESTAT_L2. The register is only meaningful if MCA::L2::MCA_DESTAT_L2[Val]=1 and MCA::L2::MCA_DESTAT_L2[AddrV]=1. The lowest valid bit of the address is defined by MCA::L2::MCA_DESTAT_L2[AddrLsb].

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst2_n[31:0]_aliasMSR; MSRC000_2029

Bits	Description
63:56	Reserved.
55:0	ErrorAddr. Read-write, Volatile. Reset: Cold,00_0000_0000_0000h. Contains the address, if any, associated with the error logged in MCA::L2::MCA_DESTAT_L2. The lowest-order valid bit of the address is specified in MCA::L2::MCA_DESTAT_L2[AddrLsb].

MSRC001_0402 [L2 Machine Check Control Mask Thread 0] (MCA::L2::MCA_CTL_MASK_L2)

Read-write. Reset: 0000_0000_0000_0000h.

Inhibit detection of an error source.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst2_n[31:0]_aliasMSR; MSRC001_0402

Bits	Description
63:5	Reserved.
4	Sdp. Read-write. Reset: 0. SDP Read Response Parity Error
3	Hwa. Read-write. Reset: 0. Init: BIOS,1. Hardware Assert Error.
2	Data. Read-write. Reset: 0. L2M Data Array ECC Error.
1	Tag. Read-write. Reset: 0. L2M Tag or State Array ECC Error.
0	MultiHit. Read-write. Reset: 0. L2M Tag Multiple-Way-Hit error.

3.2.5.4 DE**MSR0000_040C...MSRC000_2030 [DE Machine Check Control Thread 0] (MCA::DE::MCA_CTL_DE)**

Read-write. Reset: 0000_0000_0000_0000h.

0=Disables error reporting for the corresponding error. 1=Enables error reporting via machine check exception for the corresponding error. The MCA::DE::MCA_CTL_DE register must be enabled by the corresponding enable bit in Core::X86::Msr::MCG_CTL. Does not affect error detection, correction, or logging.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst3_n[31:0]_aliasMSRLEGACY; MSR0000_040C

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst3_n[31:0]_aliasMSR; MSRC000_2030

Bits	Description
63:10	Reserved.
9	HwAssertMca. Read-write. Reset: 0. Hardware Assertion MCA Error
8	OCBQ. Read-write. Reset: 0. Micro-op buffer parity error.
7	UcSeq. Read-write. Reset: 0. Patch RAM sequencer parity error
6	UcDat. Read-write. Reset: 0. Patch RAM data parity error
5	Faq. Read-write. Reset: 0. Fetch address FIFO parity error
4	Idq. Read-write. Reset: 0. Instruction dispatch queue parity error
3	UopQ. Read-write. Reset: 0. Micro-op Queue parity error
2	Ibq. Read-write. Reset: 0. IBB Register File parity error
1	OcDat. Read-write. Reset: 0. Micro-op cache DATA Array parity error
0	OcTag. Read-write. Reset: 0. Micro-op cache TAG Array parity error

MSR0000_040D...MSRC000_2031 [DE Machine Check Status Thread 0] (MCA::DE::MCA_STATUS_DE)

Reset: Cold,0000_0000_0000_0000h.

Logs information associated with errors.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst3_n[31:0]_aliasMSRLEGACY; MSR0000_040D

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst3_n[31:0]_aliasMSR; MSRC000_2031

Bits	Description
63	Val. Reset: Cold,0. 1=A valid error has been detected. This bit should be cleared by software after the register has been read. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
62	Overflow. Reset: Cold,0. 1=An error was detected while the valid bit (Val) was set; at least one error was not logged. Overflow is set independently of whether the existing error is overwritten. See 3.1.3 [Machine Check Errors]. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
61	UC. Reset: Cold,0. 1=The error was not corrected by hardware. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
60	En. Reset: Cold,0. 1=MCA error reporting is enabled for this error, as indicated by the corresponding bit in MCA::DE::MCA_CTL_DE. This bit is a copy of bit in MCA::DE::MCA_CTL_DE for this error. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
59	MiscV. Reset: Cold,0. 1=Valid thresholding in MCA::DE::MCA_MISC0_DE. In certain modes, MISC registers are owned by platform firmware and will RAZ when read by non-SMM code. Therefore, it is possible for MiscV=1 and the MISC register to read as all zeros. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
58	AddrV. Reset: Cold,0. 1=MCA::DE::MCA_ADDR_DE contains address information associated with the error. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
57	PCC. Reset: Cold,0. 1=Hardware context held by the processor may have been corrupted. Continued operation of the system may have unpredictable results. The error is not recoverable or survivable, and the system should be reinitialized. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
56	ErrCoreIdVal. Reset: Cold,0. 1=The ErrCoreId field is valid. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
55	TCC. Reset: Cold,0. 1=Hardware context of the process thread to which the error was reported may have been corrupted. Continued operation of the thread may have unpredictable results. The thread must be terminated. Only meaningful when MCA::DE::MCA_STATUS_DE[PCC]=0. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
54	RESERV54. Reset: Cold,0. MCA_STATUS Register Reserved bit. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
53	SyndV. Reset: Cold,0. 1=This error logged information in MCA::DE::MCA_SYND_DE. If MCA::DE::MCA_SYND_DE[ErrorPriority] is the same as the priority of the error in MCA::DE::MCA_STATUS_DE, then the information in MCA::DE::MCA_SYND_DE is associated with the error in MCA::DE::MCA_STATUS_DE. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
52	Reserved.
51:47	RESERV47. Reset: Cold,00h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
46	CECC. Reset: Cold,0. 1=The error was a correctable ECC error according to the restrictions of the ECC algorithm. UC indicates whether the error was actually corrected by the processor. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
45	UECC. Reset: Cold,0. 1=The error was an uncorrectable ECC error according to the restrictions of the ECC algorithm. UC indicates whether the error was actually corrected by the processor. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.

44	Deferred. Reset: Cold,0. 1=A deferred error was created. A deferred error is the result of an uncorrectable data error which did not immediately cause a processor exception; an exception is deferred until the erroneous data is consumed. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
43	Poison. Reset: Cold,0. 1=The error was the result of attempting to consume poisoned data. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
42:41	RESERV41. Reset: Cold,0h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
40	Scrub. Reset: Cold,0. 1=The error was the result of a scrub operation. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
39:38	RESERV38. Reset: Cold,0h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
37:32	ErrCoreId. Reset: Cold,00h. When ErrCoreIdVal=1 this field indicates which core within the processor is associated with the error; Otherwise this field is reserved. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
31:30	RESERV30. Reset: Cold,0h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
29:24	AddrLsb. Reset: Cold,00h. Specifies the least significant valid bit of the address contained in MCA::DE::MCA_ADDR_DE[ErrorAddr]. A value of 0 indicates that MCA::DE::MCA_ADDR_DE[55:0] contains a valid byte address. A value of 6 indicates that MCA::DE::MCA_ADDR_DE[55:6] contains a valid cache line address and that MCA::DE::MCA_ADDR_DE[5:0] are not part of the address and should be ignored by error handling software. A value of 12 indicates that MCA::DE::MCA_ADDR_DE[55:12] contain a valid 4KB memory page and that MCA::DE::MCA_ADDR_DE[11:0] should be ignored by error handling software. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
23:22	RESERV22. Reset: Cold,0h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
21:16	ErrorCodeExt. Reset: Cold,00h. Extended Error Code. This field is used to identify the error type for root cause analysis. This field indicates which bit position in MCA::DE::MCA_CTL_DE enables error reporting for the logged error. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
15:0	ErrorCode. Reset: Cold,0000h. Error code for this error. See 3.1.3.3 [Error Codes] for details on decoding this field. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.

Table 46: MCA_STATUS_DE

Error Type	ErrorCode Ext	UC	PCC	TCC	Deferred	Poison	AddrV
OcTag	0x0					0	0
OcDat	0x1					0	0
Ibq	0x2					0	0
UopQ	0x3					0	0
Idq	0x4					0	0
Faq	0x5					0	0
UcDat	0x6					0	0
UcSeq	0x7					0	0
OCBQ	0x8					0	0
HwAssertMc a	0x9					0	0

MSR0000_040E...MSRC000_2032 [DE Machine Check Address Thread 0] (MCA::DE::MCA_ADDR_DE)

Read-only. Reset: Cold,0000_0000_0000_0000h.

MCA::DE::MCA_ADDR_DE stores an address and other information associated with the error in MCA::DE::MCA_STATUS_DE. The register is only meaningful if MCA::DE::MCA_STATUS_DE[Val]=1 and MCA::DE::MCA_STATUS_DE[AddrV]=1.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst3_n[31:0]_aliasMSRLEGACY; MSR0000_040E

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst3_n[31:0]_aliasMSR; MSRC000_2032

Bits	Description
63:0	ErrorAddr. Read-only. Reset: Cold,0000_0000_0000_0000h. Contains the address, if any, associated with the error logged in MCA::DE::MCA_STATUS_DE.

Table 47: MCA_ADDR_DE

Error Type	Bits	Description
OcTag	[55:0]	Reserved
OcDat	[55:0]	Reserved
Ibq	[55:0]	Reserved
UopQ	[55:0]	Reserved
Idq	[55:0]	Reserved
Faq	[55:0]	Reserved
UcDat	[55:0]	Reserved
UcSeq	[55:0]	Reserved
OCBQ	[55:0]	Reserved
HwAssertMca	[55:0]	Reserved

**MSR0000_040F...MSRC000_2033 [DE Machine Check Miscellaneous 0 Thread 0]
(MCA::DE::MCA_MISC0_DE)**

Log miscellaneous information associated with errors.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst3_n[31:0]_aliasMSRLEGACY; MSR0000_040F

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst3_n[31:0]_aliasMSR; MSRC000_2033

Bits	Description
63	Valid. Reset: 1. 1=A valid CntP field is present in this register. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read-only.
62	CntP. Reset: 1. 1=A valid threshold counter is present. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read-only.
61	Locked. Reset: 0. 1=Writes to this register are ignored. This bit is set by BIOS to indicate that this register is not available for OS use. BIOS should set this bit if ThresholdIntType is set to SMI. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read-only.
60	IntP. Reset: 1. 1=ThresholdIntType can be used to generate interrupts. 0=ThresholdIntType and interrupt generation are not supported. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::DE::MCA_MISC0_DE[Locked]) ? Read-write : Read-only.
59:56	Reserved.
55:52	LvtOffset. Reset: 0h. One per die. For error thresholding interrupts, specifies the address of the LVT entry in the APIC registers as follows: LVT address = (LvtOffset shifted left 4 bits) + 500h (see Core::X86::Apic::ExtendedInterruptLvtEntries). AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::DE::MCA_MISC0_DE[Locked]) ? Read-write : Read-only.
51	CntEn. Reset: 0. 1=Count thresholding errors. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::DE::MCA_MISC0_DE[Locked]) ? Read-write : Read-only.
50:49	ThresholdIntType. Reset: Cold,0h. Specifies the type of interrupt signaled when Ovrflw is set and IntP==1. 00b = No interrupt. 01b = APIC based interrupt (see Core::X86::Msr::McaIntrCfg[ThresholdLvtOffset]). 10b = SMI trigger event. 11b = Reserved. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::DE::MCA_MISC0_DE[Locked]) ? Read-write : Read-only.
48	Ovrflw. Reset: Cold,0. Set by hardware when ErrCnt transitions from FFEh to FFFh. When this field is set, ErrCnt no longer increments. When this bit is set, the interrupt selected by the ThresholdIntType field is generated. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::DE::MCA_MISC0_DE[Locked]) ? Read-write : Read-only.
47:44	Reserved.
43:32	ErrCnt. Reset: Cold,000h. This is written by software to set the starting value of the error counter. This is incremented by hardware when errors are logged. When this counter overflows, it stays at FFFh (no rollover). The threshold value, written by software, is (FFFh - the desired error count (the number of errors necessary in order for an interrupt to be taken)); the desired error count of 0 (a write value of FFFh) is not supported. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::DE::MCA_MISC0_DE[Locked]) ? Read-write : Read-only.
31:24	BlkPtr. Read-write. Reset: 00h. 00h=Extended MISC MSR block is not valid. 01h=Extended MSR block is valid.
23:0	Reserved.

MSRC000_2034 [DE Machine Check Configuration Thread 0] (MCA::DE::MCA_CONFIG_DE)

Reset: 0000_0002_0000_0121h.

Controls configuration of the associated machine check bank.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst3_n[31:0]_aliasMSR; MSRC000_2034

Bits	Description
63:39	Reserved.
38:37	DeferredIntType. Read-write. Reset: 0h. Specifies the type of interrupt signaled when a deferred error is logged. 00b = No interrupt. 01b = APIC based interrupt (see Core::X86::Msr::McaIntrCfg[DeferredLvtOffset]). 10b = SMI trigger event. 11b = Reserved.
36:33	Reserved.
32	McaXEnable. Read-write. Reset: 0. Init: BIOS,1. Check: 1. 1=Software has acknowledged support for the MCAX feature set. 0=Software has not acknowledged support for the MCAX feature set. All uncorrected and fatal errors will cause an ErrorEvent packet to be generated. Deferred error interrupts are configured via Core::X86::Msr::McaIntrCfg.
31:9	Reserved.
8	McaLsbInStatusSupported. Read-only. Reset: 1. 1=MCA::DE::MCA_CONFIG_DE[McaLsbInStatusSupported] indicates that AddrLsb is located in McaStatus registers.
7:6	Reserved.
5	DeferredIntTypeSupported. Read-only. Reset: 1. 1=MCA::DE::MCA_CONFIG_DE[DeferredIntType] controls the type of interrupt generated on a deferred error. Deferred errors are supported in this bank only if MCA::DE::MCA_CONFIG_DE[DeferredErrorLoggingSupported]=1.
4:3	Reserved.
2	DeferredErrorLoggingSupported. Read-only. Reset: 0. 1=Deferred errors are supported in this MCA bank, and the LogDeferredInMcaStat field in this register controls the logging behavior of these errors. 0=Deferred errors are not supported in this bank.
1	Reserved.
0	McaX. Read-only. Reset: 1. 1=This bank provides Machine Check Architecture Extensions. Up to 4 additional MISC registers (MISC1-MISC4) are supported. MCA::DE::MCA_MISC0_DE[BlkPtr] indicates the presence of the additional MISC registers, but is not used to determine their MSR numbers. Deferred error interrupt type is specifiable by MCA bank. MCA::DE::MCA_STATUS_DE[TCC] is present.

MSRC000_2035 [DE IP Identification Thread 0] (MCA::DE::MCA_IPID_DE)

Reset: 0003_00B0_0000_0000h.

The MCA::DE::MCA_IPID_DE register is used by software to determine what IP type and revision is associated with the MCA bank.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst3_n[31:0]_aliasMSR; MSRC000_2035

Bits	Description
63:48	McaType . Read-only. Reset: 0003h. The McaType of the MCA bank within this IP.
47:44	InstanceIdHi . Read-write. Reset: 0h. The HI value instance ID of this IP. This is initialized to a unique ID per instance of this register.
43:32	HardwareID . Read-only. Reset: 0B0h. The Hardware ID of the IP associated with this MCA bank.
31:0	InstanceId . Read-write. Reset: 0000_0000h. The instance ID of this IP. This is initialized to a unique ID per instance of this register.
	Init: _ccd0_lthree0_core0_thread0_inst3_n0_aliasMSR: 2000_9600h
	Init: _ccd0_lthree0_core0_thread1_inst3_n1_aliasMSR: 2000_9700h
	Init: _ccd0_lthree0_core1_thread0_inst3_n2_aliasMSR: 2002_9600h
	Init: _ccd0_lthree0_core1_thread1_inst3_n3_aliasMSR: 2002_9700h
	Init: _ccd0_lthree0_core2_thread0_inst3_n4_aliasMSR: 2004_9600h
	Init: _ccd0_lthree0_core2_thread1_inst3_n5_aliasMSR: 2004_9700h
	Init: _ccd0_lthree0_core3_thread0_inst3_n6_aliasMSR: 2006_9600h
	Init: _ccd0_lthree0_core3_thread1_inst3_n7_aliasMSR: 2006_9700h
	Init: _ccd0_lthree0_core4_thread0_inst3_n8_aliasMSR: 2008_9600h
	Init: _ccd0_lthree0_core4_thread1_inst3_n9_aliasMSR: 2008_9700h
	Init: _ccd0_lthree0_core5_thread0_inst3_n10_aliasMSR: 200A_9600h
	Init: _ccd0_lthree0_core5_thread1_inst3_n11_aliasMSR: 200A_9700h
	Init: _ccd0_lthree0_core6_thread0_inst3_n12_aliasMSR: 200C_9600h
	Init: _ccd0_lthree0_core6_thread1_inst3_n13_aliasMSR: 200C_9700h
	Init: _ccd0_lthree0_core7_thread0_inst3_n14_aliasMSR: 200E_9600h
	Init: _ccd0_lthree0_core7_thread1_inst3_n15_aliasMSR: 200E_9700h
	Init: _ccd1_lthree0_core0_thread0_inst3_n16_aliasMSR: 2080_9600h
	Init: _ccd1_lthree0_core0_thread1_inst3_n17_aliasMSR: 2080_9700h
	Init: _ccd1_lthree0_core1_thread0_inst3_n18_aliasMSR: 2082_9600h
	Init: _ccd1_lthree0_core1_thread1_inst3_n19_aliasMSR: 2082_9700h
	Init: _ccd1_lthree0_core2_thread0_inst3_n20_aliasMSR: 2084_9600h
	Init: _ccd1_lthree0_core2_thread1_inst3_n21_aliasMSR: 2084_9700h
	Init: _ccd1_lthree0_core3_thread0_inst3_n22_aliasMSR: 2086_9600h
	Init: _ccd1_lthree0_core3_thread1_inst3_n23_aliasMSR: 2086_9700h
	Init: _ccd1_lthree0_core4_thread0_inst3_n24_aliasMSR: 2088_9600h
	Init: _ccd1_lthree0_core4_thread1_inst3_n25_aliasMSR: 2088_9700h
	Init: _ccd1_lthree0_core5_thread0_inst3_n26_aliasMSR: 208A_9600h
	Init: _ccd1_lthree0_core5_thread1_inst3_n27_aliasMSR: 208A_9700h
	Init: _ccd1_lthree0_core6_thread0_inst3_n28_aliasMSR: 208C_9600h
	Init: _ccd1_lthree0_core6_thread1_inst3_n29_aliasMSR: 208C_9700h
	Init: _ccd1_lthree0_core7_thread0_inst3_n30_aliasMSR: 208E_9600h
	Init: _ccd1_lthree0_core7_thread1_inst3_n31_aliasMSR: 208E_9700h

MSRC000_2036 [DE Machine Check Syndrome Thread 0] (MCA::DE::MCA_SYND_DE)

Read-write, Volatile. Reset: Cold, 0000_0000_0000_0000h.	
Logs physical location information associated with error in MCA::DE::MCA_STATUS_DE Thread 0	
_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst3_n[31:0]_aliasMSR; MSRC000_2036	
Bits	Description
63:33	Reserved.
32	Syndromes. Read-write, Volatile. Reset: Cold, 0. Contains the syndrome, if any, associated with the error logged in MCA::DE::MCA_STATUS_DE. The low-order bit of the syndrome is stored in bit 0, and the syndrome has a length specified by MCA::DE::MCA_SYND_DE[Length]. The Syndrome field is only valid when MCA::DE::MCA_SYND_DE[Length] is not 0.
31:27	Reserved.
26:24	ErrorPriority. Read-write, Volatile. Reset: Cold, 0h. Encodes the priority of the error logged in MCA::DE::MCA_SYND_DE. 3'b000 = No error; 3'b001 = Reserved; 3'b010 = Corrected Error; 3'b011 = Deferred Error; 3'b100 = Uncorrected Error; 3'b101 = Fatal Error; all others reserved.
23:18	Length. Read-write, Volatile. Reset: Cold, 00h. Specifies the length in bits of the syndrome contained in MCA::DE::MCA_SYND_DE[Syndrome]. A value of 0 indicates that there is no valid syndrome in MCA::DE::MCA_SYND_DE. For example, a syndrome length of 9 means that MCA::DE::MCA_SYND_DE[Syndrome] bits [8:0] contains a valid syndrome.
17:0	ErrorInformation. Read-write, Volatile. Reset: Cold, 0_0000h. Contains error-specific information about the location of the error. Decoding is available in Table 48 [MCA_SYND_DE].

Table 48: MCA_SYND_DE

Error Type	Bits	Description
OcTag	[17:0]	Reserved
OcDat	[17:0]	Reserved
Ibq	[17:0]	Reserved
UopQ	[17:0]	Reserved
Idq	[17:0]	Reserved
Faq	[17:0]	Reserved
UcDat	[17:0]	Reserved
UcSeq	[17:0]	Reserved
OCBQ	[17:0]	Reserved
HwAssertMca	[17:0]	Reserved

MSRC001_0403 [DE Machine Check Control Mask Thread 0] (MCA::DE::MCA_CTL_MASK_DE)

Read-write. Reset: 0000_0000_0000_0000h.

Inhibit detection of an error source.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst3_n[31:0]_aliasMSR; MSRC001_0403

Bits	Description
63:10	Reserved.
9	HwAssertMca. Read-write. Reset: 0. Hardware Assertion MCA Error
8	OCBQ. Read-write. Reset: 0. Micro-op buffer parity error.
7	UcSeq. Read-write. Reset: 0. Patch RAM sequencer parity error
6	UcDat. Read-write. Reset: 0. Patch RAM data parity error
5	Faq. Read-write. Reset: 0. Fetch address FIFO parity error
4	Idq. Read-write. Reset: 0. Instruction dispatch queue parity error
3	UopQ. Read-write. Reset: 0. Micro-op Queue parity error
2	Ibq. Read-write. Reset: 0. IBB Register File parity error
1	OcDat. Read-write. Reset: 0. Micro-op cache DATA Array parity error
0	OcTag. Read-write. Reset: 0. Micro-op cache TAG Array parity error

3.2.5.5 EX**MSR0000_0414...MSRC000_2050 [EX Machine Check Control Thread 0] (MCA::EX::MCA_CTL_EX)**

Reset: 0000_0000_0000_0000h.

0=Disables error reporting for the corresponding error. 1=Enables error reporting via machine check exception for the corresponding error. The MCA::EX::MCA_CTL_EX register must be enabled by the corresponding enable bit in Core::X86::Msr::MCG_CTL. Does not affect error detection, correction, or logging.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst5_n[31:0]_aliasMSRLEGACY; MSR0000_0414

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst5_n[31:0]_aliasMSR; MSRC000_2050

Bits	Description
63:14	Reserved.
13	RETMAP. Read-write. Reset: 0. Retire Map parity error.
12	SPECMAP. Read-write. Reset: 0. Spec Map parity error.
11	HWA. Read-write. Reset: 0. Hardware Assertion Error.
10	BBQ. Read-write. Reset: 0. Branch Buffer Queue (BBQ) parity error.
9	SQ. Read-write. Reset: 0. Scheduler Queue parity error.
8	STATQ. Read-write. Reset: 0. Retire status queue parity error.
7	RETDISP. Read-write. Reset: 0. Retire Dispatch Queue parity error.
6	CHKPTQ. Read-write. Reset: 0. Checkpoint Queue (AKA Map_Disq) parity error.
5	PLDAL. Read-write. Reset: 0. EX payload parity error.
4	PLDAG. Read-write. Reset: 0. Address generator payload parity error.
3	IDRF. Read-write. Reset: 0. Immediate displacement register file parity error.
2	FRF. Read-write. Reset: 0. Flag register file (FRF) parity error.
1	PRF. Read-write. Reset: 0. Physical register file (PRF) parity error.
0	WDT. Read-only. Reset: 0. Watchdog Timeout.

MSR0000_0415...MSRC000_2051 [EX Machine Check Status Thread 0] (MCA::EX::MCA_STATUS_EX)

Reset: Cold,0000_0000_0000_0000h.

Logs information associated with errors.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst5_n[31:0]_aliasMSRLEGACY; MSR0000_0415

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst5_n[31:0]_aliasMSR; MSRC000_2051

Bits	Description
63	Val. Reset: Cold,0. 1=A valid error has been detected. This bit should be cleared by software after the register has been read. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
62	Overflow. Reset: Cold,0. 1=An error was detected while the valid bit (Val) was set; at least one error was not logged. Overflow is set independently of whether the existing error is overwritten. See 3.1.3 [Machine Check Errors]. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
61	UC. Reset: Cold,0. 1=The error was not corrected by hardware. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
60	En. Reset: Cold,0. 1=MCA error reporting is enabled for this error, as indicated by the corresponding bit in MCA::EX::MCA_CTL_EX. This bit is a copy of bit in MCA::EX::MCA_CTL_EX for this error. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
59	MiscV. Reset: Cold,0. 1=Valid thresholding in MCA::EX::MCA_MISC0_EX. In certain modes, MISC registers are owned by platform firmware and will RAZ when read by non-SMM code. Therefore, it is possible for MiscV=1 and the MISC register to read as all zeros. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
58	AddrV. Reset: Cold,0. 1=MCA::EX::MCA_ADDR_EX contains address information associated with the error. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
57	PCC. Reset: Cold,0. 1=Hardware context held by the processor may have been corrupted. Continued operation of the system may have unpredictable results. The error is not recoverable or survivable, and the system should be reinitialized. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
56	ErrCoreIdVal. Reset: Cold,0. 1=The ErrCoreId field is valid. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
55	TCC. Reset: Cold,0. 1=Hardware context of the process thread to which the error was reported may have been corrupted. Continued operation of the thread may have unpredictable results. The thread must be terminated. Only meaningful when MCA::EX::MCA_STATUS_EX[PCC]=0. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
54	RESERV54. Reset: Cold,0. MCA_STATUS Register Reserved bit. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
53	SyndV. Reset: Cold,0. 1=This error logged information in MCA::EX::MCA_SYND_EX. If MCA::EX::MCA_SYND_EX[ErrorPriority] is the same as the priority of the error in MCA::EX::MCA_STATUS_EX, then the information in MCA::EX::MCA_SYND_EX is associated with the error in MCA::EX::MCA_STATUS_EX. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
52	Reserved.
51:47	RESERV47. Reset: Cold,00h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
46	CECC. Reset: Cold,0. 1=The error was a correctable ECC error according to the restrictions of the ECC algorithm. UC indicates whether the error was actually corrected by the processor. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
45	UECC. Reset: Cold,0. 1=The error was an uncorrectable ECC error according to the restrictions of the ECC algorithm. UC indicates whether the error was actually corrected by the processor. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.

44	Deferred. Reset: Cold,0. 1=A deferred error was created. A deferred error is the result of an uncorrectable data error which did not immediately cause a processor exception; an exception is deferred until the erroneous data is consumed. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
43	Poison. Reset: Cold,0. 1=The error was the result of attempting to consume poisoned data. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
42:41	RESERV41. Reset: Cold,0h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
40	Scrub. Reset: Cold,0. 1=The error was the result of a scrub operation. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
39:38	RESERV38. Reset: Cold,0h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
37:32	ErrCoreId. Reset: Cold,00h. When ErrCoreIdVal=1 this field indicates which core within the processor is associated with the error; Otherwise this field is reserved. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
31:30	RESERV30. Reset: Cold,0h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
29:24	AddrLsb. Reset: Cold,00h. Specifies the least significant valid bit of the address contained in MCA::EX::MCA_ADDR_EX[ErrorAddr]. A value of 0 indicates that MCA::EX::MCA_ADDR_EX[56:0] contains a valid byte address. A value of 6 indicates that MCA::EX::MCA_ADDR_EX[56:6] contains a valid cache line address and that MCA::EX::MCA_ADDR_EX[5:0] are not part of the address and should be ignored by error handling software. A value of 12 indicates that MCA::EX::MCA_ADDR_EX[56:12] contain a valid 4KB memory page and that MCA::EX::MCA_ADDR_EX[11:0] should be ignored by error handling software. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
23:22	RESERV22. Reset: Cold,0h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
21:16	ErrorCodeExt. Reset: Cold,00h. Extended Error Code. This field is used to identify the error type for root cause analysis. This field indicates which bit position in MCA::EX::MCA_CTL_EX enables error reporting for the logged error. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
15:0	ErrorCode. Reset: Cold,0000h. Error code for this error. See 3.1.3.3 [Error Codes] for details on decoding this field. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.

Table 49: MCA_STATUS_EX

Error Type	ErrorCode Ext	UC	PCC	TCC	Deferred	Poison	AddrV
WDT	0x0	1	1	1	0	0	1
PRF	0x1	1	1	1	0	0	0
FRF	0x2	1	1	1	0	0	0
IDRF	0x3	1	1	1	0	0	0
PLDAG	0x4	1	1	1	0	0	0
PLDAL	0x5	1	1	1	0	0	0
CHKPTQ	0x6	1	1	1	0	0	0
RETDISP	0x7	1	1	1	0	0	0
STATQ	0x8	1	1	1	0	0	0
SQ	0x9	1	1	1	0	0	0
BBQ	0xa	1	1	1	0	0	0
HWA	0xb	1	1	1	0	0	0

SPECMAP	0xc	1	1	1	0	0	0
RETMAP	0xd	1	1	1	0	0	0

MSR0000_0416...MSRC000_2052 [EX Machine Check Address Thread 0] (MCA::EX::MCA_ADDR_EX)

Reset: Cold,0000_0000_0000_0000h.

MCA::EX::MCA_ADDR_EX stores an address and other information associated with the error in MCA::EX::MCA_STATUS_EX. The register is only meaningful if MCA::EX::MCA_STATUS_EX[Val]=1 and MCA::EX::MCA_STATUS_EX[AddrV]=1.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst5_n[31:0]_aliasMSRLEGACY; MSR0000_0416

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst5_n[31:0]_aliasMSR; MSRC000_2052

Bits	Description
63:57	Reserved.
56:0	ErrorAddr. Read-write, Volatile. Reset: Cold,000_0000_0000_0000h. Unless otherwise specified by an error, contains the address associated with the error logged in MCA::EX::MCA_STATUS_EX. For physical addresses, the most significant bit is given by Core::X86::CpuId::LongModeInfo[PhysAddrSize].

Table 50: MCA_ADDR_EX

Error Type	Bits	Description
WDT	[56:0]	Instruction Pointer (RIP)
PRF	[56:0]	Reserved
FRF	[56:0]	Reserved
IDRF	[56:0]	Reserved
PLDAG	[56:0]	Reserved
PLDAL	[56:0]	Reserved
CHKPTQ	[56:0]	Reserved
RETDISP	[56:0]	Reserved
STATQ	[56:0]	Reserved
SQ	[56:0]	Reserved
BBQ	[56:0]	Reserved
HWA	[56:0]	Reserved
SPECMAP	[56:0]	Reserved
RETMAP	[56:0]	Reserved

**MSR0000_0417...MSRC000_2053 [EX Machine Check Miscellaneous 0 Thread 0]
(MCA::EX::MCA_MISC0_EX)**

Log miscellaneous information associated with errors.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst5_n[31:0]_aliasMSRLEGACY; MSR0000_0417

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst5_n[31:0]_aliasMSR; MSRC000_2053

Bits	Description
63	Valid. Reset: 1. 1=A valid CntP field is present in this register. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read-only.
62	CntP. Reset: 1. 1=A valid threshold counter is present. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read-only.
61	Locked. Reset: 0. 1=Writes to this register are ignored. This bit is set by BIOS to indicate that this register is not available for OS use. BIOS should set this bit if ThresholdIntType is set to SMI. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read-only.
60	IntP. Reset: 1. 1=ThresholdIntType can be used to generate interrupts. 0=ThresholdIntType and interrupt generation are not supported. AccessType: (Core::X86::Msrr::HWCR[McStatusWrEn] !MCA::EX::MCA_MISC0_EX[Locked]) ? Read-write : Read-only.
59:56	Reserved.
55:52	LvtOffset. Reset: 0h. One per die. For error thresholding interrupts, specifies the address of the LVT entry in the APIC registers as follows: LVT address = (LvtOffset shifted left 4 bits) + 500h (see Core::X86::Apic::ExtendedInterruptLvtEntries). AccessType: (Core::X86::Msrr::HWCR[McStatusWrEn] !MCA::EX::MCA_MISC0_EX[Locked]) ? Read-write : Read-only.
51	CntEn. Reset: 0. 1=Count thresholding errors. AccessType: (Core::X86::Msrr::HWCR[McStatusWrEn] !MCA::EX::MCA_MISC0_EX[Locked]) ? Read-write : Read-only.
50:49	ThresholdIntType. Reset: Cold,0h. Specifies the type of interrupt signaled when Ovrflw is set and IntP==1. 00b = No interrupt. 01b = APIC based interrupt (see Core::X86::Msrr::McaIntrCfg[ThresholdLvtOffset]). 10b = SMI trigger event. 11b = Reserved. AccessType: (Core::X86::Msrr::HWCR[McStatusWrEn] !MCA::EX::MCA_MISC0_EX[Locked]) ? Read-write : Read-only.
48	Ovrflw. Reset: Cold,0. Set by hardware when ErrCnt transitions from FFEh to FFFh. When this field is set, ErrCnt no longer increments. When this bit is set, the interrupt selected by the ThresholdIntType field is generated. AccessType: (Core::X86::Msrr::HWCR[McStatusWrEn] !MCA::EX::MCA_MISC0_EX[Locked]) ? Read-write : Read-only.
47:44	Reserved.
43:32	ErrCnt. Reset: Cold,000h. This is written by software to set the starting value of the error counter. This is incremented by hardware when errors are logged. When this counter overflows, it stays at FFFh (no rollover). The threshold value, written by software, is (FFFh - the desired error count (the number of errors necessary in order for an interrupt to be taken)); the desired error count of 0 (a write value of FFFh) is not supported. AccessType: (Core::X86::Msrr::HWCR[McStatusWrEn] !MCA::EX::MCA_MISC0_EX[Locked]) ? Read-write : Read-only.
31:24	BlkPtr. Read-write. Reset: 00h. 00h=Extended MISC MSR block is not valid. 01h=Extended MSR block is valid.
23:0	Reserved.

MSRC000_2054 [EX Machine Check Configuration Thread 0] (MCA::EX::MCA_CONFIG_EX)

Reset: 0000_0002_0000_0121h.

Controls configuration of the associated machine check bank.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst5_n[31:0]_aliasMSR; MSRC000_2054

Bits	Description
63:39	Reserved.
38:37	DeferredIntType. Read-write. Reset: 0h. Specifies the type of interrupt signaled when a deferred error is logged. 00b = No interrupt. 01b = APIC based interrupt (see Core::X86::Msr::McaIntrCfg[DeferredLvtOffset]). 10b = SMI trigger event. 11b = Reserved.
36:33	Reserved.
32	McaXEnable. Read-write. Reset: 0. Init: BIOS,1. Check: 1. 1=Software has acknowledged support for the MCAX feature set. 0=Software has not acknowledged support for the MCAX feature set. All uncorrected and fatal errors will cause an ErrorEvent packet to be generated. Deferred error interrupts are configured via Core::X86::Msr::McaIntrCfg.
31:9	Reserved.
8	McaLsbInStatusSupported. Read-only. Reset: 1. 1=MCA::EX::MCA_CONFIG_EX[McaLsbInStatusSupported] indicates that AddrLsb is located in McaStatus registers.
7:6	Reserved.
5	DeferredIntTypeSupported. Read-only. Reset: 1. 1=MCA::EX::MCA_CONFIG_EX[DeferredIntType] controls the type of interrupt generated on a deferred error. Deferred errors are supported in this bank only if MCA::EX::MCA_CONFIG_EX[DeferredErrorLoggingSupported]=1.
4:3	Reserved.
2	DeferredErrorLoggingSupported. Read-only. Reset: 0. 1=Deferred errors are supported in this MCA bank, and the LogDeferredInMcaStat field in this register controls the logging behavior of these errors. 0=Deferred errors are not supported in this bank.
1	Reserved.
0	McaX. Read-only. Reset: 1. 1=This bank provides Machine Check Architecture Extensions. Up to 4 additional MISC registers (MISC1-MISC4) are supported. MCA::EX::MCA_MISC0_EX[BlkPtr] indicates the presence of the additional MISC registers, but is not used to determine their MSR numbers. Deferred error interrupt type is specifiable by MCA bank. MCA::EX::MCA_STATUS_EX[TCC] is present.

MSRC000_2055 [EX IP Identification Thread 0] (MCA::EX::MCA_IPID_EX)

Reset: 0005_00B0_0000_0000h.

The MCA::EX::MCA_IPID_EX register is used by software to determine what IP type and revision is associated with the MCA bank.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst5_n[31:0]_aliasMSR; MSRC000_2055

Bits	Description
63:48	McaType . Read-only. Reset: 0005h. The McaType of the MCA bank within this IP.
47:44	InstanceIdHi . Read-write. Reset: 0h. The HI value instance ID of this IP. This is initialized to a unique ID per instance of this register.
43:32	HardwareID . Read-only. Reset: 0B0h. The Hardware ID of the IP associated with this MCA bank.
31:0	InstanceId . Read-write. Reset: 0000_0000h. The instance ID of this IP. This is initialized to a unique ID per instance of this register.
	Init: _ccd0_lthree0_core0_thread0_inst5_n0_aliasMSR: 2000_9A00h
	Init: _ccd0_lthree0_core0_thread1_inst5_n1_aliasMSR: 2000_9B00h
	Init: _ccd0_lthree0_core1_thread0_inst5_n2_aliasMSR: 2002_9A00h
	Init: _ccd0_lthree0_core1_thread1_inst5_n3_aliasMSR: 2002_9B00h
	Init: _ccd0_lthree0_core2_thread0_inst5_n4_aliasMSR: 2004_9A00h
	Init: _ccd0_lthree0_core2_thread1_inst5_n5_aliasMSR: 2004_9B00h
	Init: _ccd0_lthree0_core3_thread0_inst5_n6_aliasMSR: 2006_9A00h
	Init: _ccd0_lthree0_core3_thread1_inst5_n7_aliasMSR: 2006_9B00h
	Init: _ccd0_lthree0_core4_thread0_inst5_n8_aliasMSR: 2008_9A00h
	Init: _ccd0_lthree0_core4_thread1_inst5_n9_aliasMSR: 2008_9B00h
	Init: _ccd0_lthree0_core5_thread0_inst5_n10_aliasMSR: 200A_9A00h
	Init: _ccd0_lthree0_core5_thread1_inst5_n11_aliasMSR: 200A_9B00h
	Init: _ccd0_lthree0_core6_thread0_inst5_n12_aliasMSR: 200C_9A00h
	Init: _ccd0_lthree0_core6_thread1_inst5_n13_aliasMSR: 200C_9B00h
	Init: _ccd0_lthree0_core7_thread0_inst5_n14_aliasMSR: 200E_9A00h
	Init: _ccd0_lthree0_core7_thread1_inst5_n15_aliasMSR: 200E_9B00h
	Init: _ccd1_lthree0_core0_thread0_inst5_n16_aliasMSR: 2080_9A00h
	Init: _ccd1_lthree0_core0_thread1_inst5_n17_aliasMSR: 2080_9B00h
	Init: _ccd1_lthree0_core1_thread0_inst5_n18_aliasMSR: 2082_9A00h
	Init: _ccd1_lthree0_core1_thread1_inst5_n19_aliasMSR: 2082_9B00h
	Init: _ccd1_lthree0_core2_thread0_inst5_n20_aliasMSR: 2084_9A00h
	Init: _ccd1_lthree0_core2_thread1_inst5_n21_aliasMSR: 2084_9B00h
	Init: _ccd1_lthree0_core3_thread0_inst5_n22_aliasMSR: 2086_9A00h
	Init: _ccd1_lthree0_core3_thread1_inst5_n23_aliasMSR: 2086_9B00h
	Init: _ccd1_lthree0_core4_thread0_inst5_n24_aliasMSR: 2088_9A00h
	Init: _ccd1_lthree0_core4_thread1_inst5_n25_aliasMSR: 2088_9B00h
	Init: _ccd1_lthree0_core5_thread0_inst5_n26_aliasMSR: 208A_9A00h
	Init: _ccd1_lthree0_core5_thread1_inst5_n27_aliasMSR: 208A_9B00h
	Init: _ccd1_lthree0_core6_thread0_inst5_n28_aliasMSR: 208C_9A00h
	Init: _ccd1_lthree0_core6_thread1_inst5_n29_aliasMSR: 208C_9B00h
	Init: _ccd1_lthree0_core7_thread0_inst5_n30_aliasMSR: 208E_9A00h
	Init: _ccd1_lthree0_core7_thread1_inst5_n31_aliasMSR: 208E_9B00h

MSRC000_2056 [EX Machine Check Syndrome Thread 0] (MCA::EX::MCA_SYND_EX)

Read-write, Volatile. Reset: Cold, 0000_0000_0000_0000h.

Logs physical location information associated with error in MCA::EX::MCA_STATUS_EX Thread 0

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst5_n[31:0]_aliasMSR; MSRC000_2056

Bits	Description
63:33	Reserved.
32	Syndrome. Read-write, Volatile. Reset: Cold, 0. Contains the syndrome, if any, associated with the error logged in MCA::EX::MCA_STATUS_EX. The low-order bit of the syndrome is stored in bit 0, and the syndrome has a length specified by MCA::EX::MCA_SYND_EX[Length]. The Syndrome field is only valid when MCA::EX::MCA_SYND_EX[Length] is not 0.
31:27	Reserved.
26:24	ErrorPriority. Read-write, Volatile. Reset: Cold, 0h. Encodes the priority of the error logged in MCA::EX::MCA_SYND_EX. 3'b000 = No error; 3'b001 = Reserved; 3'b010 = Corrected Error; 3'b011 = Deferred Error; 3'b100 = Uncorrected Error; 3'b101 = Fatal Error; all others reserved.
23:18	Length. Read-write, Volatile. Reset: Cold, 00h. Specifies the length in bits of the syndrome contained in MCA::EX::MCA_SYND_EX[Syndrome]. A value of 0 indicates that there is no valid syndrome in MCA::EX::MCA_SYND_EX. For example, a syndrome length of 9 means that MCA::EX::MCA_SYND_EX[Syndrome] bits [8:0] contains a valid syndrome.
17:0	ErrorInformation. Read-write, Volatile. Reset: Cold, 0_0000h. Contains error-specific information about the location of the error. Decoding is available in Table 51 [MCA_SYND_EX].

Table 51: MCA_SYND_EX

Error Type	Bits	Description
WDT	[17:0]	Reserved
PRF	[17:12] [11:0]	Reserved decoded read port
FRF	[17:5] [4] [3] [2] [1] [0]	Reserved BRU3 ALU3 ALU2 ALU1 ALU0
IDRF	[17:11] [10] [9] [8] [7] [6] [5] [4] [3] [2] [1] [0]	Reserved ALU3 BRU3 STU2 ALU2 AGU2 STU1 ALU1 AGU1 STU0 ALU0 AGU0
PLDAG	[17:11] [10] [9] [8]	Reserved ALU3 BRU3 STU2

	[7]	ALU2
	[6]	AGU2
	[5]	STU1
	[4]	ALU1
	[3]	AGU1
	[2]	STU0
	[1]	ALU0
	[0]	AGU0
PLDAL	[17:0]	Reserved
CHKPTQ	[17:4]	Reserved
	[3]	T1 on retire
	[2]	T0 on retire
	[1]	T1 on flush
	[0]	T0 on flush
RETDISP	[17:2]	Reserved
	[1]	T1
	[0]	T0
STATQ	[17:0]	Reserved
SQ	[17:11]	Reserved
	[10]	ALU3
	[9]	BRU3
	[8]	STU2
	[7]	ALU2
	[6]	AGU2
	[5]	STU1
	[4]	ALU1
	[3]	AGU1
	[2]	STU0
	[1]	ALU0
	[0]	AGU0
BBQ	[17:3]	Reserved
	[2]	on RIP update
	[1]	on FIP update
	[0]	on Last_Branch_From update
HWA	[17:6]	Reserved
	[5:0]	encoded error num
SPECMAP	[17:1]	Reserved
	[0]	1
RETMAP	[17:0]	Reserved

MSRC001_0405 [EX Machine Check Control Mask Thread 0] (MCA::EX::MCA_CTL_MASK_EX)

Read-write. Reset: 0000_0000_0000_0000h.

Inhibit detection of an error source.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst5_n[31:0]_aliasMSR; MSRC001_0405

Bits	Description
63:14	Reserved.
13	RETMAP . Read-write. Reset: 0. Retire Map parity error.
12	SPECMAP . Read-write. Reset: 0. Spec Map parity error.
11	HWA . Read-write. Reset: 0. Hardware Assertion Error.
10	BBQ . Read-write. Reset: 0. Branch Buffer Queue (BBQ) parity error.
9	SQ . Read-write. Reset: 0. Scheduler Queue parity error.
8	STATQ . Read-write. Reset: 0. Retire status queue parity error.
7	RETDISP . Read-write. Reset: 0. Retire Dispatch Queue parity error.
6	CHKPTQ . Read-write. Reset: 0. Checkpoint Queue (AKA Map_DispQ) parity error.
5	PLDAL . Read-write. Reset: 0. EX payload parity error.
4	PLDAG . Read-write. Reset: 0. Address generator payload parity error.
3	IDRF . Read-write. Reset: 0. Immediate displacement register file parity error.
2	FRF . Read-write. Reset: 0. Flag register file (FRF) parity error.
1	PRF . Read-write. Reset: 0. Physical register file (PRF) parity error.
0	WDT . Read-write. Reset: 0. Watchdog Timeout.

3.2.5.6 FP**MSR0000_0418...MSRC000_2060 [FP Machine Check Control Thread 0] (MCA::FP::MCA_CTL_FP)**

Read-write. Reset: 0000_0000_0000_0000h.

0=Disables error reporting for the corresponding error. 1=Enables error reporting via machine check exception for the corresponding error. The MCA::FP::MCA_CTL_FP register must be enabled by the corresponding enable bit in Core::X86::Msr::MCG_CTL. Does not affect error detection, correction, or logging.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst6_n[31:0]_aliasMSRLEGACY; MSR0000_0418

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst6_n[31:0]_aliasMSR; MSRC000_2060

Bits	Description
63:8	Reserved.
7	KRF . Read-write. Reset: 0. Physical K mask register file (KRF) parity error.
6	HWA . Read-write. Reset: 0. Hardware assertion.
5	SRF . Read-write. Reset: 0. Status register file (SRF) parity error.
4	RQ . Read-write. Reset: 0. Retire queue (RQ) parity error.
3	NSQ . Read-write. Reset: 0. NSQ parity error.
2	SCH . Read-write. Reset: 0. Schedule queue parity error.
1	FL . Read-write. Reset: 0. Freelist (FL) parity error.
0	PRF . Read-write. Reset: 0. Physical register file (PRF) parity error.

MSR0000_0419...MSRC000_2061 [FP Machine Check Status Thread 0] (MCA::FP::MCA_STATUS_FP)

Reset: Cold,0000_0000_0000_0000h.

Logs information associated with errors.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst6_n[31:0]_aliasMSRLEGACY; MSR0000_0419

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst6_n[31:0]_aliasMSR; MSRC000_2061

Bits	Description
63	Val. Reset: Cold,0. 1=A valid error has been detected. This bit should be cleared by software after the register has been read. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
62	Overflow. Reset: Cold,0. 1=An error was detected while the valid bit (Val) was set; at least one error was not logged. Overflow is set independently of whether the existing error is overwritten. See 3.1.3 [Machine Check Errors]. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
61	UC. Reset: Cold,0. 1=The error was not corrected by hardware. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
60	En. Reset: Cold,0. 1=MCA error reporting is enabled for this error, as indicated by the corresponding bit in MCA::FP::MCA_CTL_FP. This bit is a copy of bit in MCA::FP::MCA_CTL_FP for this error. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
59	MiscV. Reset: Cold,0. 1=Valid thresholding in MCA::FP::MCA_MISC0_FP. In certain modes, MISC registers are owned by platform firmware and will RAZ when read by non-SMM code. Therefore, it is possible for MiscV=1 and the MISC register to read as all zeros. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
58	AddrV. Reset: Cold,0. 1=MCA::FP::MCA_ADDR_FP contains address information associated with the error. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
57	PCC. Reset: Cold,0. 1=Hardware context held by the processor may have been corrupted. Continued operation of the system may have unpredictable results. The error is not recoverable or survivable, and the system should be reinitialized. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
56	ErrCoreIdVal. Reset: Cold,0. 1=The ErrCoreId field is valid. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
55	TCC. Reset: Cold,0. 1=Hardware context of the process thread to which the error was reported may have been corrupted. Continued operation of the thread may have unpredictable results. The thread must be terminated. Only meaningful when MCA::FP::MCA_STATUS_FP[PCC]=0. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
54	RESERV54. Reset: Cold,0. MCA_STATUS Register Reserved bit. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
53	SyndV. Reset: Cold,0. 1=This error logged information in MCA::FP::MCA_SYND_FP. If MCA::FP::MCA_SYND_FP[ErrorPriority] is the same as the priority of the error in MCA::FP::MCA_STATUS_FP, then the information in MCA::FP::MCA_SYND_FP is associated with the error in MCA::FP::MCA_STATUS_FP. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
52	Reserved.
51:47	RESERV47. Reset: Cold,00h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
46	CECC. Reset: Cold,0. 1=The error was a correctable ECC error according to the restrictions of the ECC algorithm. UC indicates whether the error was actually corrected by the processor. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
45	UECC. Reset: Cold,0. 1=The error was an uncorrectable ECC error according to the restrictions of the ECC algorithm. UC indicates whether the error was actually corrected by the processor. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.

44	Deferred. Reset: Cold,0. 1=A deferred error was created. A deferred error is the result of an uncorrectable data error which did not immediately cause a processor exception; an exception is deferred until the erroneous data is consumed. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
43	Poison. Reset: Cold,0. 1=The error was the result of attempting to consume poisoned data. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
42:41	RESERV41. Reset: Cold,0h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
40	Scrub. Reset: Cold,0. 1=The error was the result of a scrub operation. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
39:38	RESERV38. Reset: Cold,0h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
37:32	ErrCoreId. Reset: Cold,00h. When ErrCoreIdVal=1 this field indicates which core within the processor is associated with the error; Otherwise this field is reserved. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
31:30	RESERV30. Reset: Cold,0h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
29:24	AddrLsb. Reset: Cold,00h. Specifies the least significant valid bit of the address contained in MCA::FP::MCA_ADDR_FP[ErrorAddr]. A value of 0 indicates that MCA::FP::MCA_ADDR_FP[55:0] contains a valid byte address. A value of 6 indicates that MCA::FP::MCA_ADDR_FP[55:6] contains a valid cache line address and that MCA::FP::MCA_ADDR_FP[5:0] are not part of the address and should be ignored by error handling software. A value of 12 indicates that MCA::FP::MCA_ADDR_FP[55:12] contain a valid 4KB memory page and that MCA::FP::MCA_ADDR_FP[11:0] should be ignored by error handling software. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
23:22	RESERV22. Reset: Cold,0h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
21:16	ErrorCodeExt. Reset: Cold,00h. Extended Error Code. This field is used to identify the error type for root cause analysis. This field indicates which bit position in MCA::FP::MCA_CTL_FP enables error reporting for the logged error. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
15:0	ErrorCode. Reset: Cold,0000h. Error code for this error. See 3.1.3.3 [Error Codes] for details on decoding this field. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.

Table 52: MCA_STATUS_FP

Error Type	ErrorCode Ext	UC	PCC	TCC	Deferred	Poison	AddrV
PRF	0x0	1	1	1	0	0	0
FL	0x1	1	1	1	0	0	0
SCH	0x2	1	1	1	0	0	0
NSQ	0x3	1	1	1	0	0	0
RQ	0x4	1	1	1	0	0	0
SRF	0x5	1	1	1	0	0	0
HWA	0x6	1	1	1	0	0	0
KRF	0x7	1	1	1	0	0	0

MSR0000_041A...MSRC000_2062 [FP Machine Check Address Thread 0] (MCA::FP::MCA_ADDR_FP)

Read-only. Reset: Cold,0000_0000_0000_0000h.

MCA::FP::MCA_ADDR_FP stores an address and other information associated with the error in MCA::FP::MCA_STATUS_FP. The register is only meaningful if MCA::FP::MCA_STATUS_FP[Val]=1 and MCA::FP::MCA_STATUS_FP[AddrV]=1.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst6_n[31:0]_aliasMSRLEGACY; MSR0000_041A

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst6_n[31:0]_aliasMSR; MSRC000_2062

Bits	Description
63:0	ErrorAddr. Read-only. Reset: Cold,0000_0000_0000_0000h. Contains the address, if any, associated with the error logged in MCA::FP::MCA_STATUS_FP.

Table 53: MCA_ADDR_FP

Error Type	Bits	Description
PRF	[55:0]	Reserved
FL	[55:0]	Reserved
SCH	[55:0]	Reserved
NSQ	[55:0]	Reserved
RQ	[55:0]	Reserved
SRF	[55:0]	Reserved
HWA	[55:0]	Reserved
KRF	[55:0]	Reserved

MSR0000_041B...MSRC000_2063 [FP Machine Check Miscellaneous 0 Thread 0] (MCA::FP::MCA_MISC0_FP)

Log miscellaneous information associated with errors.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst6_n[31:0]_aliasMSRLEGACY; MSR0000_041B

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst6_n[31:0]_aliasMSR; MSRC000_2063

Bits	Description
63	Valid. Reset: 1. 1=A valid CntP field is present in this register. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read-only.
62	CntP. Reset: 1. 1=A valid threshold counter is present. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read-only.
61	Locked. Reset: 0. 1=Writes to this register are ignored. This bit is set by BIOS to indicate that this register is not available for OS use. BIOS should set this bit if ThresholdIntType is set to SMI. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read-only.
60	IntP. Reset: 1. 1=ThresholdIntType can be used to generate interrupts. 0=ThresholdIntType and interrupt generation are not supported. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::FP::MCA_MISC0_FP[Locked]) ? Read-write : Read-only.
59:56	Reserved.
55:52	LvtOffset. Reset: 0h. One per die. For error thresholding interrupts, specifies the address of the LVT entry in the APIC registers as follows: LVT address = (LvtOffset shifted left 4 bits) + 500h (see Core::X86::Apic::ExtendedInterruptLvtEntries). AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::FP::MCA_MISC0_FP[Locked]) ? Read-write : Read-only.
51	CntEn. Reset: 0. 1=Count thresholding errors. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::FP::MCA_MISC0_FP[Locked]) ? Read-write : Read-only.
50:49	ThresholdIntType. Reset: Cold,0h. Specifies the type of interrupt signaled when Ovrlw is set and IntP==1. 00b = No interrupt. 01b = APIC based interrupt (see Core::X86::Msr::McaIntrCfg[ThresholdLvtOffset]). 10b = SMI trigger event. 11b = Reserved. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::FP::MCA_MISC0_FP[Locked]) ? Read-write : Read-only.
48	Ovrlw. Reset: Cold,0. Set by hardware when ErrCnt transitions from FFEh to FFFh. When this field is set, ErrCnt no longer increments. When this bit is set, the interrupt selected by the ThresholdIntType field is generated. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::FP::MCA_MISC0_FP[Locked]) ? Read-write : Read-only.
47:44	Reserved.
43:32	ErrCnt. Reset: Cold,000h. This is written by software to set the starting value of the error counter. This is incremented by hardware when errors are logged. When this counter overflows, it stays at FFFh (no rollover). The threshold value, written by software, is (FFFh - the desired error count (the number of errors necessary in order for an interrupt to be taken)); the desired error count of 0 (a write value of FFFh) is not supported. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::FP::MCA_MISC0_FP[Locked]) ? Read-write : Read-only.
31:24	BlkPtr. Read-write. Reset: 00h. 00h=Extended MISC MSR block is not valid. 01h=Extended MSR block is valid.
23:0	Reserved.

MSRC000_2064 [FP Machine Check Configuration Thread 0] (MCA::FP::MCA_CONFIG_FP)

Reset: 0000_0002_0000_0121h.

Controls configuration of the associated machine check bank.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst6_n[31:0]_aliasMSR; MSRC000_2064

Bits	Description
63:39	Reserved.
38:37	DeferredIntType. Read-write. Reset: 0h. Specifies the type of interrupt signaled when a deferred error is logged. 00b = No interrupt. 01b = APIC based interrupt (see Core::X86::Msr::McaIntrCfg[DeferredLvtOffset]). 10b = SMI trigger event. 11b = Reserved.
36:33	Reserved.
32	McaXEnable. Read-write. Reset: 0. Init: BIOS,1. Check: 1. 1=Software has acknowledged support for the MCAX feature set. 0=Software has not acknowledged support for the MCAX feature set. All uncorrected and fatal errors will cause an ErrorEvent packet to be generated. Deferred error interrupts are configured via Core::X86::Msr::McaIntrCfg.
31:9	Reserved.
8	McaLsbInStatusSupported. Read-only. Reset: 1. 1=MCA::FP::MCA_CONFIG_FP[McaLsbInStatusSupported] indicates that AddrLsb is located in McaStatus registers.
7:6	Reserved.
5	DeferredIntTypeSupported. Read-only. Reset: 1. 1=MCA::FP::MCA_CONFIG_FP[DeferredIntType] controls the type of interrupt generated on a deferred error. Deferred errors are supported in this bank only if MCA::FP::MCA_CONFIG_FP[DeferredErrorLoggingSupported]=1.
4:3	Reserved.
2	DeferredErrorLoggingSupported. Read-only. Reset: 0. 1=Deferred errors are supported in this MCA bank, and the LogDeferredInMcaStat field in this register controls the logging behavior of these errors. 0=Deferred errors are not supported in this bank.
1	Reserved.
0	McaX. Read-only. Reset: 1. 1=This bank provides Machine Check Architecture Extensions. Up to 4 additional MISC registers (MISC1-MISC4) are supported. MCA::FP::MCA_MISC0_FP[BlkPtr] indicates the presence of the additional MISC registers, but is not used to determine their MSR numbers. Deferred error interrupt type is specifiable by MCA bank. MCA::FP::MCA_STATUS_FP[TCC] is present.

MSRC000_2065 [FP IP Identification Thread 0] (MCA::FP::MCA_IPID_FP)

Reset: 0006_00B0_0000_0000h.

The MCA::FP::MCA_IPID_FP register is used by software to determine what IP type and revision is associated with the MCA bank.

_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst6_n[31:0]_aliasMSR; MSRC000_2065

Bits	Description
63:48	McaType . Read-only. Reset: 0006h. The McaType of the MCA bank within this IP.
47:44	InstanceIdHi . Read-write. Reset: 0h. The HI value instance ID of this IP. This is initialized to a unique ID per instance of this register.
43:32	HardwareID . Read-only. Reset: 0B0h. The Hardware ID of the IP associated with this MCA bank.
31:0	InstanceId . Read-write. Reset: 0000_0000h. The instance ID of this IP. This is initialized to a unique ID per instance of this register.
	Init: _ccd0_lthree0_core0_thread0_inst6_n0_aliasMSR: 2000_8600h
	Init: _ccd0_lthree0_core0_thread1_inst6_n1_aliasMSR: 2000_8700h
	Init: _ccd0_lthree0_core1_thread0_inst6_n2_aliasMSR: 2002_8600h
	Init: _ccd0_lthree0_core1_thread1_inst6_n3_aliasMSR: 2002_8700h
	Init: _ccd0_lthree0_core2_thread0_inst6_n4_aliasMSR: 2004_8600h
	Init: _ccd0_lthree0_core2_thread1_inst6_n5_aliasMSR: 2004_8700h
	Init: _ccd0_lthree0_core3_thread0_inst6_n6_aliasMSR: 2006_8600h
	Init: _ccd0_lthree0_core3_thread1_inst6_n7_aliasMSR: 2006_8700h
	Init: _ccd0_lthree0_core4_thread0_inst6_n8_aliasMSR: 2008_8600h
	Init: _ccd0_lthree0_core4_thread1_inst6_n9_aliasMSR: 2008_8700h
	Init: _ccd0_lthree0_core5_thread0_inst6_n10_aliasMSR: 200A_8600h
	Init: _ccd0_lthree0_core5_thread1_inst6_n11_aliasMSR: 200A_8700h
	Init: _ccd0_lthree0_core6_thread0_inst6_n12_aliasMSR: 200C_8600h
	Init: _ccd0_lthree0_core6_thread1_inst6_n13_aliasMSR: 200C_8700h
	Init: _ccd0_lthree0_core7_thread0_inst6_n14_aliasMSR: 200E_8600h
	Init: _ccd0_lthree0_core7_thread1_inst6_n15_aliasMSR: 200E_8700h
	Init: _ccd1_lthree0_core0_thread0_inst6_n16_aliasMSR: 2080_8600h
	Init: _ccd1_lthree0_core0_thread1_inst6_n17_aliasMSR: 2080_8700h
	Init: _ccd1_lthree0_core1_thread0_inst6_n18_aliasMSR: 2082_8600h
	Init: _ccd1_lthree0_core1_thread1_inst6_n19_aliasMSR: 2082_8700h
	Init: _ccd1_lthree0_core2_thread0_inst6_n20_aliasMSR: 2084_8600h
	Init: _ccd1_lthree0_core2_thread1_inst6_n21_aliasMSR: 2084_8700h
	Init: _ccd1_lthree0_core3_thread0_inst6_n22_aliasMSR: 2086_8600h
	Init: _ccd1_lthree0_core3_thread1_inst6_n23_aliasMSR: 2086_8700h
	Init: _ccd1_lthree0_core4_thread0_inst6_n24_aliasMSR: 2088_8600h
	Init: _ccd1_lthree0_core4_thread1_inst6_n25_aliasMSR: 2088_8700h
	Init: _ccd1_lthree0_core5_thread0_inst6_n26_aliasMSR: 208A_8600h
	Init: _ccd1_lthree0_core5_thread1_inst6_n27_aliasMSR: 208A_8700h
	Init: _ccd1_lthree0_core6_thread0_inst6_n28_aliasMSR: 208C_8600h
	Init: _ccd1_lthree0_core6_thread1_inst6_n29_aliasMSR: 208C_8700h
	Init: _ccd1_lthree0_core7_thread0_inst6_n30_aliasMSR: 208E_8600h
	Init: _ccd1_lthree0_core7_thread1_inst6_n31_aliasMSR: 208E_8700h

MSRC000_2066 [FP Machine Check Syndrome Thread 0] (MCA::FP::MCA_SYND_FP)

Read-write, Volatile. Reset: Cold, 0000_0000_0000_0000h.	
Logs physical location information associated with error in MCA::FP::MCA_STATUS_FP Thread 0	
_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst6_n[31:0]_aliasMSR; MSRC000_2066	
Bits	Description
63:33	Reserved.
32	Syndrom . Read-write, Volatile. Reset: Cold, 0. Contains the syndrome, if any, associated with the error logged in MCA::FP::MCA_STATUS_FP. The low-order bit of the syndrome is stored in bit 0, and the syndrome has a length specified by MCA::FP::MCA_SYND_FP[Length]. The Syndrome field is only valid when MCA::FP::MCA_SYND_FP[Length] is not 0.
31:27	Reserved.
26:24	ErrorPriority . Read-write, Volatile. Reset: Cold, 0h. Encodes the priority of the error logged in MCA::FP::MCA_SYND_FP. 3'b000 = No error; 3'b001 = Reserved; 3'b010 = Corrected Error; 3'b011 = Deferred Error; 3'b100 = Uncorrected Error; 3'b101 = Fatal Error; all others reserved.
23:18	Length . Read-write, Volatile. Reset: Cold, 00h. Specifies the length in bits of the syndrome contained in MCA::FP::MCA_SYND_FP[Syndrome]. A value of 0 indicates that there is no valid syndrome in MCA::FP::MCA_SYND_FP. For example, a syndrome length of 9 means that MCA::FP::MCA_SYND_FP[Syndrome] bits [8:0] contains a valid syndrome.
17:0	ErrorInformation . Read-write, Volatile. Reset: Cold, 0_0000h. Contains error-specific information about the location of the error. Decoding is available in Table 54 [MCA_SYND_FP].

Table 54: MCA_SYND_FP

Error Type	Bits	Description
PRF	[17:0]	Reserved
FL	[17:0]	Reserved
SCH	[17:0]	Reserved
NSQ	[17:0]	Reserved
RQ	[17:0]	Reserved
SRF	[17:0]	Reserved
HWA	[17:0]	Reserved
KRF	[17:0]	Reserved

MSRC001_0406 [FP Machine Check Control Mask Thread 0] (MCA::FP::MCA_CTL_MASK_FP)

Read-write. Reset: 0000_0000_0000_0000h.	
Inhibit detection of an error source.	
_ccd[1:0]_lthree0_core[7:0]_thread[1:0]_inst6_n[31:0]_aliasMSR; MSRC001_0406	
Bits	Description
63:8	Reserved.
7	KRF . Read-write. Reset: 0. Physical K mask register file (KRF) parity error.
6	HWA . Read-write. Reset: 0. Init: BIOS, 1. Hardware assertion.
5	SRF . Read-write. Reset: 0. Status register file (SRF) parity error.
4	RQ . Read-write. Reset: 0. Retire queue (RQ) parity error.
3	NSQ . Read-write. Reset: 0. NSQ parity error.
2	SCH . Read-write. Reset: 0. Schedule queue parity error.
1	FL . Read-write. Reset: 0. Freelist (FL) parity error.
0	PRF . Read-write. Reset: 0. Physical register file (PRF) parity error.

MSR0000_041C...MSRC000_20E0 [L3 Machine Check Control] (MCA::L3::MCA_CTL_L3)

Read-write. Reset: 0000_0000_0000_0000h.

0=Disables error reporting for the corresponding error. 1=Enables error reporting via machine check exception for the corresponding error. The MCA::L3::MCA_CTL_L3 register must be enabled by the corresponding enable bit in Core::X86::Msrr::MCG_CTL. Does not affect error detection, correction, or logging.

_ccd[1:0]_lthree0_inst7_n[8,0]_aliasMSRLEGACY; MSR0000_041C

_ccd[1:0]_lthree0_inst8_n[9,1]_aliasMSRLEGACY; MSR0000_0420

_ccd[1:0]_lthree0_inst9_n[10,2]_aliasMSRLEGACY; MSR0000_0424

_ccd[1:0]_lthree0_inst10_n[11,3]_aliasMSRLEGACY; MSR0000_0428

_ccd[1:0]_lthree0_inst11_n[12,4]_aliasMSRLEGACY; MSR0000_042C

_ccd[1:0]_lthree0_inst12_n[13,5]_aliasMSRLEGACY; MSR0000_0430

_ccd[1:0]_lthree0_inst13_n[14,6]_aliasMSRLEGACY; MSR0000_0434

_ccd[1:0]_lthree0_inst14_n[15,7]_aliasMSRLEGACY; MSR0000_0438

_ccd[1:0]_lthree0_inst7_n[8,0]_aliasMSR; MSRC000_2070

_ccd[1:0]_lthree0_inst8_n[9,1]_aliasMSR; MSRC000_2080

_ccd[1:0]_lthree0_inst9_n[10,2]_aliasMSR; MSRC000_2090

_ccd[1:0]_lthree0_inst10_n[11,3]_aliasMSR; MSRC000_20A0

_ccd[1:0]_lthree0_inst11_n[12,4]_aliasMSR; MSRC000_20B0

_ccd[1:0]_lthree0_inst12_n[13,5]_aliasMSR; MSRC000_20C0

_ccd[1:0]_lthree0_inst13_n[14,6]_aliasMSR; MSRC000_20D0

_ccd[1:0]_lthree0_inst14_n[15,7]_aliasMSR; MSRC000_20E0

Bits	Description
63:9	Reserved.
8	XiWcbParityPoison. Read-write. Reset: 0. Xi Wcb Parity Poison Creation Event
7	Hwa. Read-write. Reset: 0. L3 Hardware Assertion.
6	XiVictimQueue. Read-write. Reset: 0. L3 Victim Queue Data Fabric Error.
5	SdpParity. Read-write. Reset: 0. SDP Parity Error from XI.
4	DataArray. Read-write. Reset: 0. L3M Data ECC Error.
3	MultiHitTag. Read-write. Reset: 0. L3M Tag Multi-way-hit Error.
2	Tag. Read-write. Reset: 0. L3M Tag ECC Error.
1	MultiHitShadowTag. Read-write. Reset: 0. Shadow Tag Macro Multi-way-hit Error.
0	ShadowTag. Read-write. Reset: 0. Shadow Tag Macro ECC Error.

MSR0000_041D...MSRC000_20E1 [L3 Machine Check Status] (MCA::L3::MCA_STATUS_L3)

Reset: Cold,0000_0000_0000_0000h.

Logs information associated with errors.

_ccd[1:0]_lthree0_inst7_n[8,0]_aliasMSRLEGACY; MSR0000_041D
_ccd[1:0]_lthree0_inst8_n[9,1]_aliasMSRLEGACY; MSR0000_0421
_ccd[1:0]_lthree0_inst9_n[10,2]_aliasMSRLEGACY; MSR0000_0425
_ccd[1:0]_lthree0_inst10_n[11,3]_aliasMSRLEGACY; MSR0000_0429
_ccd[1:0]_lthree0_inst11_n[12,4]_aliasMSRLEGACY; MSR0000_042D
_ccd[1:0]_lthree0_inst12_n[13,5]_aliasMSRLEGACY; MSR0000_0431
_ccd[1:0]_lthree0_inst13_n[14,6]_aliasMSRLEGACY; MSR0000_0435
_ccd[1:0]_lthree0_inst14_n[15,7]_aliasMSRLEGACY; MSR0000_0439
_ccd[1:0]_lthree0_inst7_n[8,0]_aliasMSR; MSRC000_2071
_ccd[1:0]_lthree0_inst8_n[9,1]_aliasMSR; MSRC000_2081
_ccd[1:0]_lthree0_inst9_n[10,2]_aliasMSR; MSRC000_2091
_ccd[1:0]_lthree0_inst10_n[11,3]_aliasMSR; MSRC000_20A1
_ccd[1:0]_lthree0_inst11_n[12,4]_aliasMSR; MSRC000_20B1
_ccd[1:0]_lthree0_inst12_n[13,5]_aliasMSR; MSRC000_20C1
_ccd[1:0]_lthree0_inst13_n[14,6]_aliasMSR; MSRC000_20D1
_ccd[1:0]_lthree0_inst14_n[15,7]_aliasMSR; MSRC000_20E1

Bits	Description
63	Val. Reset: Cold,0. 1=A valid error has been detected. This bit should be cleared by software after the register has been read. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
62	Overflow. Reset: Cold,0. 1=An error was detected while the valid bit (Val) was set; at least one error was not logged. Overflow is set independently of whether the existing error is overwritten. See 3.1.3 [Machine Check Errors]. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
61	UC. Reset: Cold,0. 1=The error was not corrected by hardware. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
60	En. Reset: Cold,0. 1=MCA error reporting is enabled for this error, as indicated by the corresponding bit in MCA::L3::MCA_CTL_L3. This bit is a copy of bit in MCA::L3::MCA_CTL_L3 for this error. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
59	MiscV. Reset: Cold,0. 1=Valid thresholding in MCA::L3::MCA_MISC0_L3. In certain modes, MISC registers are owned by platform firmware and will RAZ when read by non-SMM code. Therefore, it is possible for MiscV=1 and the MISC register to read as all zeros. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
58	AddrV. Reset: Cold,0. 1=MCA::L3::MCA_ADDR_L3 contains address information associated with the error. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
57	PCC. Reset: Cold,0. 1=Hardware context held by the processor may have been corrupted. Continued operation of the system may have unpredictable results. The error is not recoverable or survivable, and the system should be reinitialized. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
56	ErrCoreIdVal. Reset: Cold,0. 1=The ErrCoreId field is valid. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
55	TCC. Reset: Cold,0. 1=Hardware context of the process thread to which the error was reported may have been corrupted. Continued operation of the thread may have unpredictable results. The thread must be terminated. Only meaningful when MCA::L3::MCA_STATUS_L3[PCC]=0. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
54	RESERV54. Reset: Cold,0. MCA_STATUS Register Reserved bit. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.

53	SyndV. Reset: Cold,0. 1=This error logged information in MCA::L3::MCA_SYND_L3. If MCA::L3::MCA_SYND_L3[ErrorPriority] is the same as the priority of the error in MCA::L3::MCA_STATUS_L3, then the information in MCA::L3::MCA_SYND_L3 is associated with the error in MCA::L3::MCA_STATUS_L3. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
52	Reserved.
51:47	RESERV47. Reset: Cold,00h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
46	CECC. Reset: Cold,0. 1=The error was a correctable ECC error according to the restrictions of the ECC algorithm. UC indicates whether the error was actually corrected by the processor. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
45	UECC. Reset: Cold,0. 1=The error was an uncorrectable ECC error according to the restrictions of the ECC algorithm. UC indicates whether the error was actually corrected by the processor. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
44	Deferred. Reset: Cold,0. 1=A deferred error was created. A deferred error is the result of an uncorrectable data error which did not immediately cause a processor exception; an exception is deferred until the erroneous data is consumed. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
43	Poison. Reset: Cold,0. 1=The error was the result of attempting to consume poisoned data. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
42:41	RESERV41. Reset: Cold,0h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
40	Scrub. Reset: Cold,0. 1=The error was the result of a scrub operation. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
39:38	RESERV38. Reset: Cold,0h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
37:32	ErrCoreId. Reset: Cold,00h. When ErrCoreIdVal=1 this field indicates which core within the processor is associated with the error; Otherwise this field is reserved. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
31:30	RESERV30. Reset: Cold,0h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
29:24	AddrLsb. Reset: Cold,00h. Specifies the least significant valid bit of the address contained in MCA::L3::MCA_ADDR_L3[ErrorAddr]. A value of 0 indicates that MCA::L3::MCA_ADDR_L3[55:0] contains a valid byte address. A value of 6 indicates that MCA::L3::MCA_ADDR_L3[55:6] contains a valid cache line address and that MCA::L3::MCA_ADDR_L3[5:0] are not part of the address and should be ignored by error handling software. A value of 12 indicates that MCA::L3::MCA_ADDR_L3[55:12] contain a valid 4KB memory page and that MCA::L3::MCA_ADDR_L3[11:0] should be ignored by error handling software. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
23:22	RESERV22. Reset: Cold,0h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
21:16	ErrorCodeExt. Reset: Cold,00h. Extended Error Code. This field is used to identify the error type for root cause analysis. This field indicates which bit position in MCA::L3::MCA_CTL_L3 enables error reporting for the logged error. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
15:0	ErrorCode. Reset: Cold,0000h. Error code for this error. See 3.1.3.3 [Error Codes] for details on decoding this field. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.

Table 55: MCA_STATUS_L3

Error Type	ErrorCode Ext	UC	PCC	TCC	Deferred	Poison	AddrV
ShadowTag	0x0					-	-
MultiHitShadowTag	0x1					-	-
Tag	0x2					-	-
MultiHitTag	0x3					-	-
DataArray	0x4					-	-
SdpParity	0x5					-	-
XiVictimQueue	0x6					-	-
Hwa	0x7					-	-
XiWcbParity Poison	0x8					-	-

MSR0000_041E...MSRC000_20E2 [L3 Machine Check Address] (MCA::L3::MCA_ADDR_L3)

Reset: Cold,0000_0000_0000_0000h.

MCA::L3::MCA_ADDR_L3 stores an address and other information associated with the error in MCA::L3::MCA_STATUS_L3. The register is only meaningful if MCA::L3::MCA_STATUS_L3[Val]=1 and MCA::L3::MCA_STATUS_L3[AddrV]=1.

_ccd[1:0]_lthree0_inst7_n[8,0]_aliasMSRLEGACY; MSR0000_041E_ccd[1:0]_lthree0_inst8_n[9,1]_aliasMSRLEGACY; MSR0000_0422_ccd[1:0]_lthree0_inst9_n[10,2]_aliasMSRLEGACY; MSR0000_0426_ccd[1:0]_lthree0_inst10_n[11,3]_aliasMSRLEGACY; MSR0000_042A_ccd[1:0]_lthree0_inst11_n[12,4]_aliasMSRLEGACY; MSR0000_042E_ccd[1:0]_lthree0_inst12_n[13,5]_aliasMSRLEGACY; MSR0000_0432_ccd[1:0]_lthree0_inst13_n[14,6]_aliasMSRLEGACY; MSR0000_0436_ccd[1:0]_lthree0_inst14_n[15,7]_aliasMSRLEGACY; MSR0000_043A_ccd[1:0]_lthree0_inst7_n[8,0]_aliasMSR; MSRC000_2072_ccd[1:0]_lthree0_inst8_n[9,1]_aliasMSR; MSRC000_2082_ccd[1:0]_lthree0_inst9_n[10,2]_aliasMSR; MSRC000_2092_ccd[1:0]_lthree0_inst10_n[11,3]_aliasMSR; MSRC000_20A2_ccd[1:0]_lthree0_inst11_n[12,4]_aliasMSR; MSRC000_20B2_ccd[1:0]_lthree0_inst12_n[13,5]_aliasMSR; MSRC000_20C2_ccd[1:0]_lthree0_inst13_n[14,6]_aliasMSR; MSRC000_20D2_ccd[1:0]_lthree0_inst14_n[15,7]_aliasMSR; MSRC000_20E2**Bits Description**

63:56 Reserved.

55:0 **ErrorAddr.** Read-write, Volatile. Reset: Cold,00_0000_0000_0000h. Unless otherwise specified by an error, contains the address associated with the error logged in MCA::L3::MCA_STATUS_L3. For physical addresses, the most significant bit is given by Core::X86::Cpuid::LongModeInfo[PhysAddrSize].

Table 56: MCA_ADDR_L3

Error Type	Bits	Description
ShadowTag	[55:16] [15:0]	Reserved 16'b{7'b{Index}, 3'b{Slice}, 6'b{0}}
MultiHitShadowTag	[55:16] [15:0]	Reserved 16'b{7'b{Index}, 3'b{Slice}, 6'b{0}}
Tag	[55:21] [20:0]	Reserved 21'b{1'b{Odd/Even}, 7'b{Index}, 4'b{Bank[3:0]}, 3'b{Slice}, 6'b{0}}

MultiHitTag	[55:21] [20:0]	Reserved 21'b{1'b{Odd/Even}, 7'b{Index}, 4'b{Bank[3:0]}, 3'b{Slice}, 6'b{0}}
DataArray	[55:52] [51:0]	Reserved Physical Address
SdpParity	[55:52] [51:0]	Reserved Physical Address
XiVictimQueue	[55:52] [51:0]	Reserved Physical Address
Hwa	[55:34] [33:0]	Reserved Reserved
XiWcbParityPoison	[55:52] [51:0]	Reserved Physical Address

MSR0000_041F...MSRC000_20E3 [L3 Machine Check Miscellaneous 0] (MCA::L3::MCA_MISC0_L3)

Log miscellaneous information associated with errors.

_ccd[1:0]_lthree0_inst7_n[8,0]_aliasMSRLEGACY; MSR0000_041F
 _ccd[1:0]_lthree0_inst8_n[9,1]_aliasMSRLEGACY; MSR0000_0423
 _ccd[1:0]_lthree0_inst9_n[10,2]_aliasMSRLEGACY; MSR0000_0427
 _ccd[1:0]_lthree0_inst10_n[11,3]_aliasMSRLEGACY; MSR0000_042B
 _ccd[1:0]_lthree0_inst11_n[12,4]_aliasMSRLEGACY; MSR0000_042F
 _ccd[1:0]_lthree0_inst12_n[13,5]_aliasMSRLEGACY; MSR0000_0433
 _ccd[1:0]_lthree0_inst13_n[14,6]_aliasMSRLEGACY; MSR0000_0437
 _ccd[1:0]_lthree0_inst14_n[15,7]_aliasMSRLEGACY; MSR0000_043B
 _ccd[1:0]_lthree0_inst7_n[8,0]_aliasMSR; MSRC000_2073
 _ccd[1:0]_lthree0_inst8_n[9,1]_aliasMSR; MSRC000_2083
 _ccd[1:0]_lthree0_inst9_n[10,2]_aliasMSR; MSRC000_2093
 _ccd[1:0]_lthree0_inst10_n[11,3]_aliasMSR; MSRC000_20A3
 _ccd[1:0]_lthree0_inst11_n[12,4]_aliasMSR; MSRC000_20B3
 _ccd[1:0]_lthree0_inst12_n[13,5]_aliasMSR; MSRC000_20C3
 _ccd[1:0]_lthree0_inst13_n[14,6]_aliasMSR; MSRC000_20D3
 _ccd[1:0]_lthree0_inst14_n[15,7]_aliasMSR; MSRC000_20E3

Bits	Description
63	Valid. Reset: 1. 1=A valid CntP field is present in this register. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read-only.
62	CntP. Reset: 1. 1=A valid threshold counter is present. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read-only.
61	Locked. Reset: 0. 1=Writes to this register are ignored. This bit is set by BIOS to indicate that this register is not available for OS use. BIOS should set this bit if ThresholdIntType is set to SMI. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read-only.
60	IntP. Reset: 1. 1=ThresholdIntType can be used to generate interrupts. 0=ThresholdIntType and interrupt generation are not supported. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::L3::MCA_MISC0_L3[Locked]) ? Read-write : Read-only.
59:56	Reserved.
55:52	LvtOffset. Reset: 0h. One per die. For error thresholding interrupts, specifies the address of the LVT entry in the APIC registers as follows: LVT address = (LvtOffset shifted left 4 bits) + 500h (see Core::X86::Apic::ExtendedInterruptLvtEntries). AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::L3::MCA_MISC0_L3[Locked]) ? Read-write : Read-only.
51	CntEn. Reset: 0. 1=Count thresholding errors. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::L3::MCA_MISC0_L3[Locked]) ? Read-write : Read-only.
50:49	ThresholdIntType. Reset: Cold,0h. Specifies the type of interrupt signaled when Ovrflw is set and IntP==1. 00b = No interrupt. 01b = APIC based interrupt (see Core::X86::Msr::McaIntrCfg[ThresholdLvtOffset]). 10b = SMI trigger event. 11b = Reserved. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::L3::MCA_MISC0_L3[Locked]) ? Read-write : Read-only.
48	Ovrflw. Reset: Cold,0. Set by hardware when ErrCnt transitions from FFEh to FFFh. When this field is set, ErrCnt no longer increments. When this bit is set, the interrupt selected by the ThresholdIntType field is generated. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::L3::MCA_MISC0_L3[Locked]) ? Read-write : Read-only.
47:44	Reserved.
43:32	ErrCnt. Reset: Cold,000h. This is written by software to set the starting value of the error counter. This is incremented by hardware when errors are logged. When this counter overflows, it stays at FFFh (no rollover). The threshold value, written by software, is (FFFh - the desired error count (the number of errors necessary in order for an interrupt to be taken)); the desired error count of 0 (a write value of FFFh) is not supported.

	AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::L3::MCA_MISC0_L3[Locked]) ? Read-write : Read-only.
31:24	BlkPtr. Read-write. Reset: 00h. 00h=Extended MISC MSR block is not valid. 01h=Extended MSR block is valid.
23:0	Reserved.

MSRC000_20[7...E]4 [L3 Machine Check Configuration] (MCA::L3::MCA_CONFIG_L3)

Reset: 0000_0000_0000_0125h.

Controls configuration of the associated machine check bank.

_ccd[1:0]_lthree0_inst7_n[8,0]_aliasMSR; MSRC000_2074

_ccd[1:0]_lthree0_inst8_n[9,1]_aliasMSR; MSRC000_2084

_ccd[1:0]_lthree0_inst9_n[10,2]_aliasMSR; MSRC000_2094

_ccd[1:0]_lthree0_inst10_n[11,3]_aliasMSR; MSRC000_20A4

_ccd[1:0]_lthree0_inst11_n[12,4]_aliasMSR; MSRC000_20B4

_ccd[1:0]_lthree0_inst12_n[13,5]_aliasMSR; MSRC000_20C4

_ccd[1:0]_lthree0_inst13_n[14,6]_aliasMSR; MSRC000_20D4

_ccd[1:0]_lthree0_inst14_n[15,7]_aliasMSR; MSRC000_20E4

Bits	Description
63:39	Reserved.
38:37	DeferredIntType. Read-write. Reset: 0h. Specifies the type of interrupt signaled when a deferred error is logged. 00b = No interrupt. 01b = APIC based interrupt (see Core::X86::Msr::McaIntrCfg[DeferredLvtOffset]). 10b = SMI trigger event. 11b = Reserved.
36:35	Reserved.
34	LogDeferredInMcaStat. Read-write. Reset: 0. Init: BIOS,1. 1=Log deferred errors in MCA::L3::MCA_STATUS_L3 and MCA::L3::MCA_ADDR_L3 in addition to MCA::L3::MCA_DESTAT_L3 and MCA::L3::MCA_DEADDR_L3. 0=Only log deferred errors in MCA::L3::MCA_DESTAT_L3 and MCA::L3::MCA_DEADDR_L3. This bit does not affect logging of deferred errors in MCA::L3::MCA_SYND_L3, MCA::L3::MCA_MISC0_L3.
33	Reserved.
32	McaXEnable. Read-write. Reset: 0. Init: BIOS,1. Check: 1. 1=Software has acknowledged support for the MCAX feature set. 0=Software has not acknowledged support for the MCAX feature set. All uncorrected and fatal errors will cause an ErrorEvent packet to be generated. Deferred error interrupts are configured via Core::X86::Msr::McaIntrCfg.
31:9	Reserved.
8	McaLsbInStatusSupported. Read-only. Reset: 1. 1=MCA::L3::MCA_CONFIG_L3[McaLsbInStatusSupported] indicates that AddrLsb is located in McaStatus registers.
7:6	Reserved.
5	DeferredIntTypeSupported. Read-only. Reset: 1. 1=MCA::L3::MCA_CONFIG_L3[DeferredIntType] controls the type of interrupt generated on a deferred error. Deferred errors are supported in this bank only if MCA::L3::MCA_CONFIG_L3[DeferredErrorLoggingSupported]=1.
4:3	Reserved.
2	DeferredErrorLoggingSupported. Read-only. Reset: 1. 1=Deferred errors are supported in this MCA bank, and MCA::L3::MCA_CONFIG_L3[LogDeferredInMcaStat] controls the logging behavior of these errors. MCA::L3::MCA_DESTAT_L3 and MCA::L3::MCA_DEADDR_L3 are supported in this MCA bank. 0=Deferred errors are not supported in this bank.
1	Reserved.
0	McaX. Read-only. Reset: 1. 1=This bank provides Machine Check Architecture Extensions. Up to 4 additional MISC registers (MISC1-MISC4) are supported. MCA::L3::MCA_MISC0_L3[BlkPtr] indicates the presence of the additional MISC registers, but is not used to determine their MSR numbers. Deferred error interrupt type is specifiable by MCA bank. MCA::L3::MCA_STATUS_L3[TCC] is present.

MSRC000_20[7...E]5 [L3 IP Identification] (MCA::L3::MCA_IPID_L3)

Reset: 0007_00B0_0000_0000h.

The MCA::L3::MCA_IPID_L3 register is used by software to determine what IP type and revision is associated with the MCA bank.

_ccd[1:0]_lthree0_inst7_n[8,0]_aliasMSR; MSRC000_2075

_ccd[1:0]_lthree0_inst8_n[9,1]_aliasMSR; MSRC000_2085

_ccd[1:0]_lthree0_inst9_n[10,2]_aliasMSR; MSRC000_2095

_ccd[1:0]_lthree0_inst10_n[11,3]_aliasMSR; MSRC000_20A5

_ccd[1:0]_lthree0_inst11_n[12,4]_aliasMSR; MSRC000_20B5

_ccd[1:0]_lthree0_inst12_n[13,5]_aliasMSR; MSRC000_20C5

_ccd[1:0]_lthree0_inst13_n[14,6]_aliasMSR; MSRC000_20D5

_ccd[1:0]_lthree0_inst14_n[15,7]_aliasMSR; MSRC000_20E5

Bits	Description
63:48	McaType . Read-only. Reset: 0007h. The McaType of the MCA bank within this IP.
47:44	InstanceIdHi . Read-write. Reset: 0h. The HI value instance ID of this IP. This is initialized to a unique ID per instance of this register.
43:32	HardwareID . Read-only. Reset: 0B0h. The Hardware ID of the IP associated with this MCA bank.
31:0	InstanceId . Read-write. Reset: 0000_0000h. The instance ID of this IP. This is initialized to a unique ID per instance of this register.
	Init: _ccd0_lthree0_inst7_n0_aliasMSR: 2035_0000h
	Init: _ccd0_lthree0_inst8_n1_aliasMSR: 2035_0100h
	Init: _ccd0_lthree0_inst9_n2_aliasMSR: 2035_0200h
	Init: _ccd0_lthree0_inst10_n3_aliasMSR: 2035_0300h
	Init: _ccd0_lthree0_inst11_n4_aliasMSR: 2035_0400h
	Init: _ccd0_lthree0_inst12_n5_aliasMSR: 2035_0500h
	Init: _ccd0_lthree0_inst13_n6_aliasMSR: 2035_0600h
	Init: _ccd0_lthree0_inst14_n7_aliasMSR: 2035_0700h
	Init: _ccd1_lthree0_inst7_n8_aliasMSR: 20B5_0000h
	Init: _ccd1_lthree0_inst8_n9_aliasMSR: 20B5_0100h
	Init: _ccd1_lthree0_inst9_n10_aliasMSR: 20B5_0200h
	Init: _ccd1_lthree0_inst10_n11_aliasMSR: 20B5_0300h
	Init: _ccd1_lthree0_inst11_n12_aliasMSR: 20B5_0400h
	Init: _ccd1_lthree0_inst12_n13_aliasMSR: 20B5_0500h
	Init: _ccd1_lthree0_inst13_n14_aliasMSR: 20B5_0600h
	Init: _ccd1_lthree0_inst14_n15_aliasMSR: 20B5_0700h

MSRC000_20[7...E]6 [L3 Machine Check Syndrome] (MCA::L3::MCA_SYND_L3)

Read-write, Volatile. Reset: Cold, 0000_0000_0000_0000h.	
Logs physical location information associated with error in MCA::L3::MCA_STATUS_L3 Thread 0	
_ccd[1:0]_lthree0_inst7_n[8,0]_aliasMSR; MSRC000_2076	
_ccd[1:0]_lthree0_inst8_n[9,1]_aliasMSR; MSRC000_2086	
_ccd[1:0]_lthree0_inst9_n[10,2]_aliasMSR; MSRC000_2096	
_ccd[1:0]_lthree0_inst10_n[11,3]_aliasMSR; MSRC000_20A6	
_ccd[1:0]_lthree0_inst11_n[12,4]_aliasMSR; MSRC000_20B6	
_ccd[1:0]_lthree0_inst12_n[13,5]_aliasMSR; MSRC000_20C6	
_ccd[1:0]_lthree0_inst13_n[14,6]_aliasMSR; MSRC000_20D6	
_ccd[1:0]_lthree0_inst14_n[15,7]_aliasMSR; MSRC000_20E6	
Bits	Description
63:51	Reserved.
50:32	Syndrome. Read-write, Volatile. Reset: Cold, 0_0000h. Contains the syndrome, if any, associated with the error logged in MCA::L3::MCA_STATUS_L3. The low-order bit of the syndrome is stored in bit 0, and the syndrome has a length specified by MCA::L3::MCA_SYND_L3[Length]. The Syndrome field is only valid when MCA::L3::MCA_SYND_L3[Length] is not 0.
31:27	Reserved.
26:24	ErrorPriority. Read-write, Volatile. Reset: Cold, 0h. Encodes the priority of the error logged in MCA::L3::MCA_SYND_L3. 3'b000 = No error; 3'b001 = Reserved; 3'b010 = Corrected Error; 3'b011 = Deferred Error; 3'b100 = Uncorrected Error; 3'b101 = Fatal Error; all others reserved.
23:18	Length. Read-write, Volatile. Reset: Cold, 00h. Specifies the length in bits of the syndrome contained in MCA::L3::MCA_SYND_L3[Syndrome]. A value of 0 indicates that there is no valid syndrome in MCA::L3::MCA_SYND_L3. For example, a syndrome length of 9 means that MCA::L3::MCA_SYND_L3[Syndrome] bits [8:0] contains a valid syndrome.
17:0	ErrorInformation. Read-write, Volatile. Reset: Cold, 0_0000h. Contains error-specific information about the location of the error. Decoding is available in Table 57 [MCA_SYND_L3].

Table 57: MCA_SYND_L3

Error Type	Bits	Description
ShadowTag	[17:16]	Reserved
	[15:8]	Pack
	[7:3]	Reserved
	[2:0]	Way
MultiHitShadowTag	[17:12]	Reserved
	[11:8]	Pack
	[7:0]	Reserved
Tag	[17:14]	4'b1100
	[13]	Reserved
	[12]	PA[20].
	[11]	Bank[3]
	[10:8]	Bank[2:0]
	[7:4]	Reserved
MultiHitTag	[3:0]	Way
	[17:0]	Reserved
DataArray	[17:16]	2'b11
	[15]	0 when error is in Ecc[9:0]/Data[127:0]. 1 when error is in Ecc[18:10]/Data[255:128].
	[14]	1'b0
	[13]	Reserved

	[12]	Reserved
	[11]	Reserved
	[10:8]	Bank[2:0]
	[7:4]	Reserved
	[3:0]	Way
SdpParity	[17:0]	Reserved
XiVictimQueue	[17:0]	Reserved
Hwa	[17:0]	Reserved
XiWcbParityPoison	[17:0]	Reserved

MSRC000_20[7...E]8 [L3 Machine Check Deferred Error Status] (MCA::L3::MCA_DESTAT_L3)

Reset: Cold,0000_0000_0000_0000h.

Holds status information for the first deferred error seen in this bank.

_ccd[1:0]_lthree0_inst7_n[8,0]_aliasMSR; MSRC000_2078

_ccd[1:0]_lthree0_inst8_n[9,1]_aliasMSR; MSRC000_2088

_ccd[1:0]_lthree0_inst9_n[10,2]_aliasMSR; MSRC000_2098

_ccd[1:0]_lthree0_inst10_n[11,3]_aliasMSR; MSRC000_20A8

_ccd[1:0]_lthree0_inst11_n[12,4]_aliasMSR; MSRC000_20B8

_ccd[1:0]_lthree0_inst12_n[13,5]_aliasMSR; MSRC000_20C8

_ccd[1:0]_lthree0_inst13_n[14,6]_aliasMSR; MSRC000_20D8

_ccd[1:0]_lthree0_inst14_n[15,7]_aliasMSR; MSRC000_20E8

Bits	Description
63	Val. Read-write, Volatile. Reset: Cold,0. 1=A valid error has been detected (whether it is enabled or not).
62	Overflow. Read-write, Volatile. Reset: Cold,0. 1=An error was detected while the valid bit (Val) was set; at least one error was not logged. Overflow is set independently of whether the existing error is overwritten. (See the section on overwrite priorities.)
61:59	RESERV4. Read-write. Reset: Cold,0h.
58	AddrV. Read-write, Volatile. Reset: Cold,0. 1=MCA::L3::MCA_DEADDR_L3 contains address information associated with the error.
57:54	RESERV3. Read-write. Reset: Cold,0h.
53	SyndV. Read-write, Volatile. Reset: Cold,0. 1=This error logged information in MCA::L3::MCA_SYND_L3. If MCA::L3::MCA_SYND_L3[ErrorPriority] is the same as the priority of the error in MCA::L3::MCA_STATUS_L3, then the information in MCA::L3::MCA_SYND_L3 is associated with the error in MCA::L3::MCA_DESTAT_L3.
52:45	RESERV2. Read-write. Reset: Cold,00h.
44	Deferred. Read-write, Volatile. Reset: Cold,0. 1=A deferred error was created. A deferred error is the result of an uncorrectable data error which did not immediately cause a processor exception; poison is created and an exception is deferred until the poison data is consumed.
43:30	RESERV1. Read-write. Reset: Cold,0000h.
29:24	AddrLsb. Read-write, Volatile. Reset: Cold,00h. Specifies the least significant valid bit of the address contained in MCA::L3::MCA_ADDR_L3[ErrorAddr]. A value of 0 indicates that MCA::L3::MCA_ADDR_L3[55:0] contains a valid byte address. A value of 6 indicates that MCA::L3::MCA_ADDR_L3[55:6] contains a valid cache line address and that MCA::L3::MCA_ADDR_L3[5:0] are not part of the address and should be ignored by error handling software. A value of 12 indicates that MCA::L3::MCA_ADDR_L3[55:12] contain a valid 4KB memory page and that MCA::L3::MCA_ADDR_L3[11:0] should be ignored by error handling software.
23:22	RESERV0. Read-write. Reset: Cold,0h.
21:16	ErrorCodeExt. Read-write, Volatile. Reset: Cold,00h. Logs an extended error code when an error is detected. This model-specific field is used in conjunction with ErrorCode? to identify the error sub-type for root cause analysis.
15:0	ErrorCode. Read-write, Volatile. Reset: Cold,0000h. Error code for this error.

MSRC000_20[7...E]9 [L3 Deferred Error Address] (MCA::L3::MCA_DEADDR_L3)

Reset: Cold,0000_0000_0000_0000h.

The MCA::L3::MCA_DEADDR_L3 register stores the address associated with the error in MCA::L3::MCA_DESTAT_L3. The register is only meaningful if MCA::L3::MCA_DESTAT_L3[Val]=1 and MCA::L3::MCA_DESTAT_L3[AddrV]=1. The lowest valid bit of the address is defined by MCA::L3::MCA_DESTAT_L3[AddrLsb].

_ccd[1:0]_lthree0_inst7_n[8,0]_aliasMSR; MSRC000_2079

_ccd[1:0]_lthree0_inst8_n[9,1]_aliasMSR; MSRC000_2089

_ccd[1:0]_lthree0_inst9_n[10,2]_aliasMSR; MSRC000_2099

_ccd[1:0]_lthree0_inst10_n[11,3]_aliasMSR; MSRC000_20A9

_ccd[1:0]_lthree0_inst11_n[12,4]_aliasMSR; MSRC000_20B9

_ccd[1:0]_lthree0_inst12_n[13,5]_aliasMSR; MSRC000_20C9

_ccd[1:0]_lthree0_inst13_n[14,6]_aliasMSR; MSRC000_20D9

_ccd[1:0]_lthree0_inst14_n[15,7]_aliasMSR; MSRC000_20E9

Bits	Description
63:56	Reserved.
55:0	ErrorAddr. Read-write, Volatile. Reset: Cold,00_0000_0000_0000h. Contains the address, if any, associated with the error logged in MCA::L3::MCA_DESTAT_L3. The lowest-order valid bit of the address is specified in MCA::L3::MCA_DESTAT_L3[AddrLsb].

MSRC001_040[7...E] [L3 Machine Check Control Mask] (MCA::L3::MCA_CTL_MASK_L3)

Read-write. Reset: 0000_0000_0000_0000h.

Inhibit detection of an error source.

_ccd[1:0]_lthree0_inst7_n[8,0]_aliasMSR; MSRC001_0407

_ccd[1:0]_lthree0_inst8_n[9,1]_aliasMSR; MSRC001_0408

_ccd[1:0]_lthree0_inst9_n[10,2]_aliasMSR; MSRC001_0409

_ccd[1:0]_lthree0_inst10_n[11,3]_aliasMSR; MSRC001_040A

_ccd[1:0]_lthree0_inst11_n[12,4]_aliasMSR; MSRC001_040B

_ccd[1:0]_lthree0_inst12_n[13,5]_aliasMSR; MSRC001_040C

_ccd[1:0]_lthree0_inst13_n[14,6]_aliasMSR; MSRC001_040D

_ccd[1:0]_lthree0_inst14_n[15,7]_aliasMSR; MSRC001_040E

Bits	Description
63:9	Reserved.
8	XiWcbParityPoison. Read-write. Reset: 0. Xi Wcb Parity Poison Creation Event
7	Hwa. Read-write. Reset: 0. Init: BIOS,1. L3 Hardware Assertion.
6	XiVictimQueue. Read-write. Reset: 0. L3 Victim Queue Data Fabric Error.
5	SdpParity. Read-write. Reset: 0. SDP Parity Error from XI.
4	DataArray. Read-write. Reset: 0. L3M Data ECC Error.
3	MultiHitTag. Read-write. Reset: 0. L3M Tag Multi-way-hit Error.
2	Tag. Read-write. Reset: 0. L3M Tag ECC Error.
1	MultiHitShadowTag. Read-write. Reset: 0. Shadow Tag Macro Multi-way-hit Error.
0	ShadowTag. Read-write. Reset: 0. Shadow Tag Macro ECC Error.

3.2.5.8 CS

MSR0000_045C...MSRC000_2180 [CS Machine Check Control] (MCA::CS::MCA_CTL_CS)

Read-write. Reset: 0000_0000_0000_0000h.

0=Disables error reporting for the corresponding error. 1=Enables error reporting via machine check exception for the corresponding error. The MCA::CS::MCA_CTL_CS register must be enabled by the corresponding enable bit in Core::X86::Msr::MCG_CTL. Does not affect error detection, correction, or logging.

_instCS0_n0_aliasMSRLEGACY; MSR0000_045C

_instCS1_n1_aliasMSRLEGACY; MSR0000_0460

_instCS0_n0_aliasMSR; MSRC000_2170

_instCS1_n1_aliasMSR; MSRC000_2180

Bits	Description
63:18	Reserved.
17	HWA . Read-write. Reset: 0. Hardware Assert Error.
16	FTI_ND_SEC_VIOL . Read-write. Reset: 0. Security Violation: A security violation was detected on an incoming request from the transport layer.
15	FTI_ND_ADDR_VIOL . Read-write. Reset: 0. Address Violation: An address violation was detected on an incoming request from the transport layer.
14	FTI_ND_ILL_REQ . Read-write. Reset: 0. Illegal Request: An illegal request was received from the transport layer.
13	SPF_ECC_ERR . Read-write. Reset: 0. Probe Filter ECC Error: An ECC error occurred on a probe filter access.
12	SPF_PRT_ERR . Read-write. Reset: 0. Probe Filter Protocol Error: Indicates a Cache Coherence Issue.
11	CNTR_UNFL . Read-write. Reset: 0. Counter underflow error.
10	CNTR_OVFL . Read-write. Reset: 0. Counter overflow error.
9	SDP_UNEXP_RETRY . Read-write. Reset: 0. SDP read response had an unexpected RETRY error.
8	SDP_RSP_NO_MTCH . Read-write. Reset: 0. SDP read response had no match in the CS queue.
7	ATM_PAR_ERR . Read-write. Reset: 0. Atomic Request Parity Error: Parity error on read of an atomic transaction.
6	SDP_PAR_ERR . Read-write. Reset: 0. Read Response Parity Error: Parity error on incoming read response data.
5	FTI_PAR_ERR . Read-write. Reset: 0. Request or Probe Parity Error: Parity error on incoming request or probe response data.
4	FTI_RSP_NO_MTCH . Read-write. Reset: 0. Unexpected Response: A response was received from the transport layer which does not match any request.
3	FTI_ILL_RSP . Read-write. Reset: 0. Illegal Response: An illegal response was received from the transport layer.
2	FTI_SEC_VIOL . Read-write. Reset: 0. Security Violation: A security violation was detected on an incoming request from the transport layer.
1	FTI_ADDR_VIOL . Read-write. Reset: 0. Address Violation: An address violation was detected on an incoming request from the transport layer.
0	FTI_ILL_REQ . Read-write. Reset: 0. Illegal Request: An illegal request was received from the transport layer.

MSR0000_045D...MSRC000_2181 [CS Machine Check Status] (MCA::CS::MCA_STATUS_CS)

Reset: Cold,0000_0000_0000_0000h.

Logs information associated with errors.

_instCS0_n0_aliasMSRLEGACY; MSR0000_045D

_instCS1_n1_aliasMSRLEGACY; MSR0000_0461

_instCS0_n0_aliasMSR; MSRC000_2171

_instCS1_n1_aliasMSR; MSRC000_2181

Bits	Description
63	Val. Reset: Cold,0. 1=A valid error has been detected. This bit should be cleared by software after the register has been read. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
62	Overflow. Reset: Cold,0. 1=An error was detected while the valid bit (Val) was set; at least one error was not logged. Overflow is set independently of whether the existing error is overwritten. See 3.1.3 [Machine Check Errors]. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
61	UC. Reset: Cold,0. 1=The error was not corrected by hardware. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
60	En. Reset: Cold,0. 1=MCA error reporting is enabled for this error, as indicated by the corresponding bit in MCA::CS::MCA_CTL_CS. This bit is a copy of bit in MCA::CS::MCA_CTL_CS for this error. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
59	MiscV. Reset: Cold,0. 1=Valid thresholding in MCA::CS::MCA_MISC0_CS. In certain modes, MISC registers are owned by platform firmware and will RAZ when read by non-SMM code. Therefore, it is possible for MiscV=1 and the MISC register to read as all zeros. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
58	AddrV. Reset: Cold,0. 1=MCA::CS::MCA_ADDR_CS contains address information associated with the error. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
57	PCC. Reset: Cold,0. 1=Hardware context held by the processor may have been corrupted. Continued operation of the system may have unpredictable results. The error is not recoverable or survivable, and the system should be reinitialized. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
56	ErrCoreIdVal. Reset: Cold,0. 1=The ErrCoreId field is valid. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
55	TCC. Reset: Cold,0. 1=Hardware context of the process thread to which the error was reported may have been corrupted. Continued operation of the thread may have unpredictable results. The thread must be terminated. Only meaningful when MCA::CS::MCA_STATUS_CS[PCC]=0. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
54	RESERV54. Reset: Cold,0. MCA_STATUS Register Reserved bit. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
53	SyndV. Reset: Cold,0. 1=This error logged information in MCA::CS::MCA_SYND_CS. If MCA::CS::MCA_SYND_CS[ErrorPriority] is the same as the priority of the error in MCA::CS::MCA_STATUS_CS, then the information in MCA::CS::MCA_SYND_CS is associated with the error in MCA::CS::MCA_STATUS_CS. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
52	Reserved.
51:47	RESERV47. Reset: Cold,00h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
46	CECC. Reset: Cold,0. 1=The error was a correctable ECC error according to the restrictions of the ECC algorithm. UC indicates whether the error was actually corrected by the processor. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
45	UECC. Reset: Cold,0. 1=The error was an uncorrectable ECC error according to the restrictions of the ECC algorithm. UC indicates whether the error was actually corrected by the processor.

	AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
44	Deferred. Reset: Cold,0. 1=A deferred error was created. A deferred error is the result of an uncorrectable data error which did not immediately cause a processor exception; an exception is deferred until the erroneous data is consumed.
	AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
43	Poison. Reset: Cold,0. 1=The error was the result of attempting to consume poisoned data.
	AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
42:41	RESERV41. Reset: Cold,0h. MCA_STATUS Register Reserved bits.
	AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
40	Scrub. Reset: Cold,0. 1=The error was the result of a scrub operation.
	AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
39:38	RESERV38. Reset: Cold,0h. MCA_STATUS Register Reserved bits.
	AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
37:32	ErrCoreId. Reset: Cold,00h. When ErrCoreIdVal=1 this field indicates which core within the processor is associated with the error; Otherwise this field is reserved.
	AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
31:30	RESERV30. Reset: Cold,0h. MCA_STATUS Register Reserved bits.
	AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
29:24	AddrLsb. Reset: Cold,00h. Specifies the least significant valid bit of the address contained in MCA::CS::MCA_ADDR_CS[ErrorAddr]. A value of 0 indicates that MCA::CS::MCA_ADDR_CS[55:0] contains a valid byte address. A value of 6 indicates that MCA::CS::MCA_ADDR_CS[55:6] contains a valid cache line address and that MCA::CS::MCA_ADDR_CS[5:0] are not part of the address and should be ignored by error handling software. A value of 12 indicates that MCA::CS::MCA_ADDR_CS[55:12] contain a valid 4KB memory page and that MCA::CS::MCA_ADDR_CS[11:0] should be ignored by error handling software.
	AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
23:22	RESERV22. Reset: Cold,0h. MCA_STATUS Register Reserved bits.
	AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
21:16	ErrorCodeExt. Reset: Cold,00h. Extended Error Code. This field is used to identify the error type for root cause analysis. This field indicates which bit position in MCA::CS::MCA_CTL_CS enables error reporting for the logged error.
	AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
15:0	ErrorCode. Reset: Cold,0000h. Error code for this error. See 3.1.3.3 [Error Codes] for details on decoding this field.
	AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.

Table 58: MCA_STATUS_CS

Error Type	ErrorCode Ext	UC	PCC	TCC	Deferred	Poison	AddrV
FTI_ILL_REQ	0x0	0	0	0	1	0	1
FTI_ADDR_VIOL	0x1	0	0	0	1	0	1
FTI_SEC_VIOL	0x2	0	0	0	1	0	1
FTI_ILL_RSP	0x3	1	1	1	0	0	0
FTI_RSP_NO_MTCH	0x4	1	1	1	0	0	0
FTI_PAR_ERR	0x5	0	0	0	1	0	1

SDP_PAR_ERR	0x6	0	0	0	1	0	1
ATM_PAR_ERR	0x7	0	0	0	1	0	1
SDP_RSP_NO_MTCH	0x8	1	1	1	0	0	0
SDP_UNEXP_RETRY	0x9	1	1	1	0	0	1
CNTR_OVF_L	0xa	1	1	1	0	0	0
CNTR_UNF_L	0xb	1	1	1	0	0	0
SPF_PRT_ERR	0xc	1	1	1	0	0	0
SPF_ECC_ERR	0xd	0/1	0/1	0/1	0	0	1
FTI_IL_L_REQ	0xe	0	0	0	1	0	1
FTI_ADDR_VIOL	0xf	0	0	0	1	0	1
FTI_SEC_VIOL	0x10	0	0	0	1	0	1
HWA	0x11	1	1	1	0	0	0

MSR0000_045E...MSRC000_2182 [CS Machine Check Address] (MCA::CS::MCA_ADDR_CS)

Reset: Cold,0000_0000_0000_0000h.

MCA::CS::MCA_ADDR_CS stores an address and other information associated with the error in MCA::CS::MCA_STATUS_CS. The register is only meaningful if MCA::CS::MCA_STATUS_CS[Val]=1 and MCA::CS::MCA_STATUS_CS[AddrV]=1.

_instCS0_n0_aliasMSRLEGACY; MSR0000_045E

_instCS1_n1_aliasMSRLEGACY; MSR0000_0462

_instCS0_n0_aliasMSR; MSRC000_2172

_instCS1_n1_aliasMSR; MSRC000_2182

Bits	Description
63:56	Reserved.
55:0	ErrorAddr. Read-write, Volatile. Reset: Cold,00_0000_0000_0000h. Unless otherwise specified by an error, contains the address associated with the error logged in MCA::CS::MCA_STATUS_CS. For physical addresses, the most significant bit is given by Core::X86::Cpuid::LongModeInfo[PhysAddrSize].

Table 59: MCA_ADDR_CS

Error Type	Bits	Description
FTI_IL_L_REQ	[47:2]	Address
FTI_ADDR_VIOL	[47:2]	Address
FTI_SEC_VIOL	[47:2]	Address
FTI_IL_L_RSP	[56:0]	Reserved
FTI_RSP_NO_MTCH	[56:0]	Reserved
FTI_PAR_ERR	[47:2]	Address
SDP_PAR_ERR	[47:2]	Address
ATM_PAR_ERR	[47:2]	Address
SDP_RSP_NO_MTCH	[56:0]	Reserved
SDP_UNEXP_RETRY	[47:2]	Address

CNTR_OVFL	[56:0]	Reserved
CNTR_UNFL	[56:0]	Reserved
SPF_PRT_ERR	[56:0]	Reserved
SPF_ECC_ERR	[47:2]	Address
FTI_ND_ILL_REQ	[47:2]	Address
FTI_ND_ADDR_VIOL	[47:2]	Address
FTI_ND_SEC_VIOL	[47:2]	Address
HWA	[47:2]	Address

MSR0000_045F...MSRC000_2183 [CS Machine Check Miscellaneous 0] (MCA::CS::MCA_MISC0_CS)

Log miscellaneous information associated with errors.	
_instCS0_n0_aliasMSRLEGACY; MSR0000_045F	
_instCS1_n1_aliasMSRLEGACY; MSR0000_0463	
_instCS0_n0_aliasMSR; MSRC000_2173	
_instCS1_n1_aliasMSR; MSRC000_2183	
Bits	Description
63	Valid. Reset: 1. 1=A valid CntP field is present in this register. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read-only.
62	CntP. Reset: 1. 1=A valid threshold counter is present. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read-only.
61	Locked. Reset: 0. 1=Writes to this register are ignored. This bit is set by BIOS to indicate that this register is not available for OS use. BIOS should set this bit if ThresholdIntType is set to SMI. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read-only.
60	IntP. Reset: 1. 1=ThresholdIntType can be used to generate interrupts. 0=ThresholdIntType and interrupt generation are not supported. AccessType: (Core::X86::Msrr::HWCR[McStatusWrEn] !MCA::CS::MCA_MISC0_CS[Locked]) ? Read-write : Read-only.
59:56	Reserved.
55:52	LvtOffset. Reset: 0h. One per die. For error thresholding interrupts, specifies the address of the LVT entry in the APIC registers as follows: LVT address = (LvtOffset shifted left 4 bits) + 500h (see Core::X86::Apic::ExtendedInterruptLvtEntries). AccessType: (Core::X86::Msrr::HWCR[McStatusWrEn] !MCA::CS::MCA_MISC0_CS[Locked]) ? Read-write : Read-only.
51	CntEn. Reset: 0. 1=Count thresholding errors. AccessType: (Core::X86::Msrr::HWCR[McStatusWrEn] !MCA::CS::MCA_MISC0_CS[Locked]) ? Read-write : Read-only.
50:49	ThresholdIntType. Reset: Cold,0h. Specifies the type of interrupt signaled when Ovrflw is set and IntP==1. 00b = No interrupt. 01b = APIC based interrupt (see Core::X86::Msrr::McaIntrCfg[ThresholdLvtOffset]). 10b = SMI trigger event. 11b = Reserved. AccessType: (Core::X86::Msrr::HWCR[McStatusWrEn] !MCA::CS::MCA_MISC0_CS[Locked]) ? Read-write : Read-only.
48	Ovrflw. Reset: Cold,0. Set by hardware when ErrCnt transitions from FFEh to FFFh. When this field is set, ErrCnt no longer increments. When this bit is set, the interrupt selected by the ThresholdIntType field is generated. AccessType: (Core::X86::Msrr::HWCR[McStatusWrEn] !MCA::CS::MCA_MISC0_CS[Locked]) ? Read-write : Read-only.
47:44	Reserved.
43:32	ErrCnt. Reset: Cold,000h. This is written by software to set the starting value of the error counter. This is incremented by hardware when errors are logged. When this counter overflows, it stays at FFFh (no rollover). The threshold value, written by software, is (FFFh - the desired error count (the number of errors necessary in order for an interrupt to be taken)); the desired error count of 0 (a write value of FFFh) is not supported. AccessType: (Core::X86::Msrr::HWCR[McStatusWrEn] !MCA::CS::MCA_MISC0_CS[Locked]) ? Read-write : Read-only.
31:24	BlkPtr. Read-write. Reset: 00h. 00h=Extended MISC MSR block is not valid. 01h=Extended MSR block is valid.
23:0	Reserved.

MSRC000_21[7...8]4 [CS Machine Check Configuration] (MCA::CS::MCA_CONFIG_CS)

Reset: 0000_0000_0000_0125h.

Controls configuration of the associated machine check bank.

_instCS0_n0_aliasMSR; MSRC000_2174

_instCS1_n1_aliasMSR; MSRC000_2184

Bits	Description
63:39	Reserved.
38:37	DeferredIntType . Read-write. Reset: 0h. Specifies the type of interrupt signaled when a deferred error is logged. 00b = No interrupt. 01b = APIC based interrupt (see Core::X86::Msr::McaIntrCfg[DeferredLvtOffset]). 10b = SMI trigger event. 11b = Reserved.
36:35	Reserved.
34	LogDeferredInMcaStat . Read-write. Reset: 0. Init: BIOS,1. 1=Log deferred errors in MCA::CS::MCA_STATUS_CS and MCA::CS::MCA_ADDR_CS in addition to MCA::CS::MCA_DESTAT_CS and MCA::CS::MCA_DEADDR_CS. 0=Only log deferred errors in MCA::CS::MCA_DESTAT_CS and MCA::CS::MCA_DEADDR_CS. This bit does not affect logging of deferred errors in MCA::CS::MCA_SYND_CS, MCA::CS::MCA_MISC0_CS.
33	Reserved.
32	McaXEnable . Read-write. Reset: 0. Init: BIOS,1. Check: 1. 1=Software has acknowledged support for the MCAX feature set. 0=Software has not acknowledged support for the MCAX feature set. All uncorrected and fatal errors will cause an ErrorEvent packet to be generated. Deferred error interrupts are configured via Core::X86::Msr::McaIntrCfg.
31:9	Reserved.
8	McaLsbInStatusSupported . Read-only. Reset: 1. 1=MCA::CS::MCA_CONFIG_CS[McaLsbInStatusSupported] indicates that AddrLsb is located in McaStatus registers.
7:6	Reserved.
5	DeferredIntTypeSupported . Read-only. Reset: 1. 1=MCA::CS::MCA_CONFIG_CS[DeferredIntType] controls the type of interrupt generated on a deferred error. Deferred errors are supported in this bank only if MCA::CS::MCA_CONFIG_CS[DeferredErrorLoggingSupported]=1.
4:3	Reserved.
2	DeferredErrorLoggingSupported . Read-only. Reset: 1. 1=Deferred errors are supported in this MCA bank, and MCA::CS::MCA_CONFIG_CS[LogDeferredInMcaStat] controls the logging behavior of these errors. MCA::CS::MCA_DESTAT_CS and MCA::CS::MCA_DEADDR_CS are supported in this MCA bank. 0=Deferred errors are not supported in this bank.
1	Reserved.
0	McaX . Read-only. Reset: 1. 1=This bank provides Machine Check Architecture Extensions. Up to 4 additional MISC registers (MISC1-MISC4) are supported. MCA::CS::MCA_MISC0_CS[BlkPtr] indicates the presence of the additional MISC registers, but is not used to determine their MSR numbers. Deferred error interrupt type is specifiable by MCA bank. MCA::CS::MCA_STATUS_CS[TCC] is present.

MSRC000_21[7...8]5 [CS IP Identification] (MCA::CS::MCA_IPID_CS)

Reset: 0002_002E_0000_0000h.

The MCA::CS::MCA_IPID_CS register is used by software to determine what IP type and revision is associated with the MCA bank.

_instCS0_n0_aliasMSR; MSRC000_2175

_instCS1_n1_aliasMSR; MSRC000_2185

Bits	Description
63:48	McaType . Read-only. Reset: 0002h. The McaType of the MCA bank within this IP.
47:44	InstanceIdHi . Read-write. Reset: 0h. The HI value instance ID of this IP. This is initialized to a unique ID per instance of this register.
43:32	HardwareID . Read-only. Reset: 02Eh. The Hardware ID of the IP associated with this MCA bank.
31:0	InstanceId . Read-write. Reset: 0000_0000h. The instance ID of this IP. This is initialized to a unique ID per instance of this register.
	Init: _instCS0_n0_aliasMSR: 1F00_0000h
	Init: _instCS1_n1_aliasMSR: 1F00_0100h

MSRC000_21[7...8]6 [CS Machine Check Syndrome] (MCA::CS::MCA_SYND_CS)

Read-write, Volatile. Reset: Cold, 0000_0000_0000_0000h.

Logs physical location information associated with error in MCA::CS::MCA_STATUS_CS Thread 0

_instCS0_n0_aliasMSR; MSRC000_2176

_instCS1_n1_aliasMSR; MSRC000_2186

Bits	Description
63:41	Reserved.
40:32	Syndrome . Read-write, Volatile. Reset: Cold, 000h. Contains the syndrome, if any, associated with the error logged in MCA::CS::MCA_STATUS_CS. The low-order bit of the syndrome is stored in bit 0, and the syndrome has a length specified by MCA::CS::MCA_SYND_CS[Length]. The Syndrome field is only valid when MCA::CS::MCA_SYND_CS[Length] is not 0.
31:27	Reserved.
26:24	ErrorPriority . Read-write, Volatile. Reset: Cold, 0h. Encodes the priority of the error logged in MCA::CS::MCA_SYND_CS. 3'b000 = No error; 3'b001 = Reserved; 3'b010 = Corrected Error; 3'b011 = Deferred Error; 3'b100 = Uncorrected Error; 3'b101 = Fatal Error; all others reserved.
23:18	Length . Read-write, Volatile. Reset: Cold, 00h. Specifies the length in bits of the syndrome contained in MCA::CS::MCA_SYND_CS[Syndrome]. A value of 0 indicates that there is no valid syndrome in MCA::CS::MCA_SYND_CS. For example, a syndrome length of 9 means that MCA::CS::MCA_SYND_CS[Syndrome] bits [8:0] contains a valid syndrome.
17:0	ErrorInformation . Read-write, Volatile. Reset: Cold, 0_0000h. Contains error-specific information about the location of the error. Decoding is available in Table 60 [MCA_SYND_CS].

Table 60: MCA_SYND_CS

Error Type	Bits	Description
FTI_ILL_REQ	[17:0]	
FTI_ADDR_VIOL	[17:0]	
FTI_SEC_VIOL	[17:0]	
FTI_ILL_RSP	[17:0]	
FTI_RSP_NO_MTCH	[17:0]	
FTI_PAR_ERR	[6:0]	
SDP_PAR_ERR	[6:0]	
ATM_PAR_ERR	[6:0]	
SDP_RSP_NO_MTCH	[7:0]	
SDP_UNEXP_RETRY	[6:0]	
CNTR_OVFL	[17:0]	

CNTR_UNFL	[17:0]	
SPF_PRT_ERR	[17:0]	
SPF_ECC_ERR	[17:0]	
FTI_ND_ILL_REQ	[17:0]	
FTI_ND_ADDR_VIOL	[17:0]	
FTI_ND_SEC_VIOL	[17:0]	
HWA	[17:0]	

MSRC000_21[7...8]8 [CS Machine Check Deferred Error Status] (MCA::CS::MCA_DESTAT_CS)

Reset: Cold,0000_0000_0000_0000h.

Holds status information for the first deferred error seen in this bank.

_instCS0_n0_aliasMSR; MSRC000_2178

_instCS1_n1_aliasMSR; MSRC000_2188

Bits	Description
63	Val. Read-write, Volatile. Reset: Cold,0. 1=A valid error has been detected (whether it is enabled or not).
62	Overflow. Read-write, Volatile. Reset: Cold,0. 1=An error was detected while the valid bit (Val) was set; at least one error was not logged. Overflow is set independently of whether the existing error is overwritten. (See the section on overwrite priorities.)
61:59	RESERV4. Read-write. Reset: Cold,0h.
58	AddrV. Read-write, Volatile. Reset: Cold,0. 1=MCA::CS::MCA_DEADDR_CS contains address information associated with the error.
57:54	RESERV3. Read-write. Reset: Cold,0h.
53	SyndV. Read-write, Volatile. Reset: Cold,0. 1=This error logged information in MCA::CS::MCA_SYND_CS. If MCA::CS::MCA_SYND_CS[ErrorPriority] is the same as the priority of the error in MCA::CS::MCA_STATUS_CS, then the information in MCA::CS::MCA_SYND_CS is associated with the error in MCA::CS::MCA_DESTAT_CS.
52:45	RESERV2. Read-write. Reset: Cold,00h.
44	Deferred. Read-write, Volatile. Reset: Cold,0. 1=A deferred error was created. A deferred error is the result of an uncorrectable data error which did not immediately cause a processor exception; poison is created and an exception is deferred until the poison data is consumed.
43:30	RESERV1. Read-write. Reset: Cold,0000h.
29:24	AddrLsb. Read-write, Volatile. Reset: Cold,00h. Specifies the least significant valid bit of the address contained in MCA::CS::MCA_ADDR_CS[ErrorAddr]. A value of 0 indicates that MCA::CS::MCA_ADDR_CS[55:0] contains a valid byte address. A value of 6 indicates that MCA::CS::MCA_ADDR_CS[55:6] contains a valid cache line address and that MCA::CS::MCA_ADDR_CS[5:0] are not part of the address and should be ignored by error handling software. A value of 12 indicates that MCA::CS::MCA_ADDR_CS[55:12] contain a valid 4KB memory page and that MCA::CS::MCA_ADDR_CS[11:0] should be ignored by error handling software.
23:22	RESERV0. Read-write. Reset: Cold,0h.
21:16	ErrorCodeExt. Read-write, Volatile. Reset: Cold,00h. Logs an extended error code when an error is detected. This model-specific field is used in conjunction with ErrorCode? to identify the error sub-type for root cause analysis.
15:0	ErrorCode. Read-write, Volatile. Reset: Cold,0000h. Error code for this error.

MSRC000_21[7...8]9 [CS Deferred Error Address] (MCA::CS::MCA_DEADDR_CS)

Reset: Cold,0000_0000_0000_0000h.

The MCA::CS::MCA_DEADDR_CS register stores the address associated with the error in MCA::CS::MCA_DESTAT_CS. The register is only meaningful if MCA::CS::MCA_DESTAT_CS[Val]=1 and MCA::CS::MCA_DESTAT_CS[AddrV]=1. The lowest valid bit of the address is defined by MCA::CS::MCA_DESTAT_CS[AddrLsb].

_instCS0_n0_aliasMSR; MSRC000_2179

_instCS1_n1_aliasMSR; MSRC000_2189

Bits	Description
63:56	Reserved.
55:0	ErrorAddr. Read-write, Volatile. Reset: Cold,00_0000_0000_0000h. Contains the address, if any, associated with the error logged in MCA::CS::MCA_DESTAT_CS. The lowest-order valid bit of the address is specified in MCA::CS::MCA_DESTAT_CS[AddrLsb].

MSRC001_041[7...8] [CS Machine Check Control Mask] (MCA::CS::MCA_CTL_MASK_CS)

Read-write. Reset: 0000_0000_0000_0000h.

Inhibit detection of an error source.

_instCS0_n0_aliasMSR; MSRC001_0417

_instCS1_n1_aliasMSR; MSRC001_0418

Bits	Description
63:18	Reserved.
17	HWA. Read-write. Reset: 0. Hardware Assert Error.
16	FTI_ND_SEC_VIOL. Read-write. Reset: 0. Security Violation: A security violation was detected on an incoming request from the transport layer.
15	FTI_ND_ADDR_VIOL. Read-write. Reset: 0. Address Violation: An address violation was detected on an incoming request from the transport layer.
14	FTI_ND_ILL_REQ. Read-write. Reset: 0. Illegal Request: An illegal request was received from the transport layer.
13	SPF_ECC_ERR. Read-write. Reset: 0. Probe Filter ECC Error: An ECC error occurred on a probe filter access.
12	SPF_PRT_ERR. Read-write. Reset: 0. Probe Filter Protocol Error: Indicates a Cache Coherence Issue.
11	CNTR_UNFL. Read-write. Reset: 0. Counter underflow error.
10	CNTR_OVFL. Read-write. Reset: 0. Counter overflow error.
9	SDP_UNEXP_RETRY. Read-write. Reset: 0. SDP read response had an unexpected RETRY error.
8	SDP_RSP_NO_MTCH. Read-write. Reset: 0. SDP read response had no match in the CS queue.
7	ATM_PAR_ERR. Read-write. Reset: 0. Atomic Request Parity Error: Parity error on read of an atomic transaction.
6	SDP_PAR_ERR. Read-write. Reset: 0. Read Response Parity Error: Parity error on incoming read response data.
5	FTI_PAR_ERR. Read-write. Reset: 0. Request or Probe Parity Error: Parity error on incoming request or probe response data.
4	FTI_RSP_NO_MTCH. Read-write. Reset: 0. Unexpected Response: A response was received from the transport layer which does not match any request.
3	FTI_ILL_RSP. Read-write. Reset: 0. Illegal Response: An illegal response was received from the transport layer.
2	FTI_SEC_VIOL. Read-write. Reset: 0. Security Violation: A security violation was detected on an incoming request from the transport layer.
1	FTI_ADDR_VIOL. Read-write. Reset: 0. Address Violation: An address violation was detected on an incoming request from the transport layer.
0	FTI_ILL_REQ. Read-write. Reset: 0. Illegal Request: An illegal request was received from the transport layer.

3.2.5.9 PIE

MSR0000_0470...MSRC000_21C0 [PIE Machine Check Control] (MCA::PIE::MCA_CTL_PIE)

Read-write. Reset: 0000_0000_0000_0000h.

0=Disables error reporting for the corresponding error. 1=Enables error reporting via machine check exception for the corresponding error. The MCA::PIE::MCA_CTL_PIE register must be enabled by the corresponding enable bit in Core::X86::Msr::MCG_CTL. Does not affect error detection, correction, or logging.

_inst[PIE0,BCST]_n0_aliasMSRLEGACY; MSR0000_0470

_inst[PIE0,BCST]_n0_aliasMSR; MSRC000_21C0

Bits	Description
63:8	Reserved.
7	RSLVFCI . Read-write. Reset: 0. Register access during DF Cstate: Register access is detected from SMN during DF Cstate.
6	CNLI . Read-write. Reset: 0. Error is detected in CXL™ Link.
5	WDT . Read-write. Reset: 0. Watch Dog Timer: A watch dog timer expired.
4	DEF . Read-write. Reset: 0. A deferred error was detected in the DF.
3	FTI_DAT_STAT . Read-write. Reset: 0. Poison data consumption: Poison data was written to an internal PIE register.
2	GMI . Read-write. Reset: 0. Link Error: An error occurred on a GMI or xGMI link.
1	CSW . Read-write. Reset: 0. Register security violation: A security violation was detected on an access to an internal PIE register.
0	HW_ASSERT . Read-write. Reset: 0. Hardware Assert: A hardware assert was detected.

MSR0000_0471...MSRC000_21C1 [PIE Machine Check Status] (MCA::PIE::MCA_STATUS_PIE)

Reset: Cold,0000_0000_0000_0000h.

Logs information associated with errors.

_inst[PIE0,BCST]_n0_aliasMSRLEGACY; MSR0000_0471

_inst[PIE0,BCST]_n0_aliasMSR; MSRC000_21C1

Bits	Description
63	Val. Reset: Cold,0. 1=A valid error has been detected. This bit should be cleared by software after the register has been read. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
62	Overflow. Reset: Cold,0. 1=An error was detected while the valid bit (Val) was set; at least one error was not logged. Overflow is set independently of whether the existing error is overwritten. See 3.1.3 [Machine Check Errors]. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
61	UC. Reset: Cold,0. 1=The error was not corrected by hardware. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
60	En. Reset: Cold,0. 1=MCA error reporting is enabled for this error, as indicated by the corresponding bit in MCA::PIE::MCA_CTL_PIE. This bit is a copy of bit in MCA::PIE::MCA_CTL_PIE for this error. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
59	MiscV. Reset: Cold,0. 1=Valid thresholding in MCA::PIE::MCA_MISC0_PIE. In certain modes, MISC registers are owned by platform firmware and will RAZ when read by non-SMM code. Therefore, it is possible for MiscV=1 and the MISC register to read as all zeros. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
58	AddrV. Reset: Cold,0. 1=MCA::PIE::MCA_ADDR_PIE contains address information associated with the error. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
57	PCC. Reset: Cold,0. 1=Hardware context held by the processor may have been corrupted. Continued operation of the system may have unpredictable results. The error is not recoverable or survivable, and the system should be reinitialized. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
56	ErrCoreIdVal. Reset: Cold,0. 1=The ErrCoreId field is valid. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
55	TCC. Reset: Cold,0. 1=Hardware context of the process thread to which the error was reported may have been corrupted. Continued operation of the thread may have unpredictable results. The thread must be terminated. Only meaningful when MCA::PIE::MCA_STATUS_PIE[PCC]=0. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
54	RESERV54. Reset: Cold,0. MCA_STATUS Register Reserved bit. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
53	SyndV. Reset: Cold,0. 1=This error logged information in MCA::PIE::MCA_SYND_PIE. If MCA::PIE::MCA_SYND_PIE[ErrorPriority] is the same as the priority of the error in MCA::PIE::MCA_STATUS_PIE, then the information in MCA::PIE::MCA_SYND_PIE is associated with the error in MCA::PIE::MCA_STATUS_PIE. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
52	Reserved.
51:47	RESERV47. Reset: Cold,00h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
46	CECC. Reset: Cold,0. 1=The error was a correctable ECC error according to the restrictions of the ECC algorithm. UC indicates whether the error was actually corrected by the processor. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
45	UECC. Reset: Cold,0. 1=The error was an uncorrectable ECC error according to the restrictions of the ECC algorithm. UC indicates whether the error was actually corrected by the processor. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.

44	Deferred. Reset: Cold,0. 1=A deferred error was created. A deferred error is the result of an uncorrectable data error which did not immediately cause a processor exception; an exception is deferred until the erroneous data is consumed. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
43	Poison. Reset: Cold,0. 1=The error was the result of attempting to consume poisoned data. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
42:41	RESERV41. Reset: Cold,0h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
40	Scrub. Reset: Cold,0. 1=The error was the result of a scrub operation. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
39:38	RESERV38. Reset: Cold,0h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
37:32	ErrCoreId. Reset: Cold,00h. When ErrCoreIdVal=1 this field indicates which core within the processor is associated with the error; Otherwise this field is reserved. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
31:30	RESERV30. Reset: Cold,0h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
29:24	AddrLsb. Reset: Cold,00h. Specifies the least significant valid bit of the address contained in MCA::PIE::MCA_ADDR_PIE[ErrorAddr]. A value of 0 indicates that MCA::PIE::MCA_ADDR_PIE[55:0] contains a valid byte address. A value of 6 indicates that MCA::PIE::MCA_ADDR_PIE[55:6] contains a valid cache line address and that MCA::PIE::MCA_ADDR_PIE[5:0] are not part of the address and should be ignored by error handling software. A value of 12 indicates that MCA::PIE::MCA_ADDR_PIE[55:12] contain a valid 4KB memory page and that MCA::PIE::MCA_ADDR_PIE[11:0] should be ignored by error handling software. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
23:22	RESERV22. Reset: Cold,0h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
21:16	ErrorCodeExt. Reset: Cold,00h. Extended Error Code. This field is used to identify the error type for root cause analysis. This field indicates which bit position in MCA::PIE::MCA_CTL_PIE enables error reporting for the logged error. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
15:0	ErrorCode. Reset: Cold,0000h. Error code for this error. See 3.1.3.3 [Error Codes] for details on decoding this field. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.

Table 61: MCA_STATUS_PIE

Error Type	ErrorCode Ext	UC	PCC	TCC	Deferred	Poison	AddrV
HW_ASSERT	0x0	1	1	1	0	0	0
CSW	0x1	0	0	0	1	0	0
GMI	0x2	0/1	0/1	0/1	0	0	0
FTI_DAT_STAT	0x3	1	1	1	0	0	0
DEF	0x4	0	0	0	1	0	0
WDT	0x5	1	1	1	0	0	1
CNLI	0x6	0/1	0/1	0/1	0	0	0
RSLVFCI	0x7	0	0	0	0/1	0	0

MSR0000_0472...MSRC000_21C2 [PIE Machine Check Address] (MCA::PIE::MCA_ADDR_PIE)

Reset: Cold,0000_0000_0000_0000h.

MCA::PIE::MCA_ADDR_PIE stores an address and other information associated with the error in MCA::PIE::MCA_STATUS_PIE. The register is only meaningful if MCA::PIE::MCA_STATUS_PIE[Val]=1 and MCA::PIE::MCA_STATUS_PIE[AddrV]=1.

_inst[PIE0,BCST]_n0_aliasMSRLEGACY; MSR0000_0472

_inst[PIE0,BCST]_n0_aliasMSR; MSRC000_21C2

Bits	Description
63:56	Reserved.
55:0	ErrorAddr. Read-write, Volatile. Reset: Cold,00_0000_0000_0000h. Unless otherwise specified by an error, contains the address associated with the error logged in MCA::PIE::MCA_STATUS_PIE. For physical addresses, the most significant bit is given by Core::X86::CpuId::LongModeInfo[PhysAddrSize].

Table 62: MCA_ADDR_PIE

Error Type	Bits	Description
HW_ASSERT	[56:0]	Reserved
CSW	[56:0]	Reserved
GMI	[56:0]	Reserved
FTI_DAT_STAT	[56:0]	Reserved
DEF	[56:0]	Reserved
WDT	[56:0]	Reserved
CNLI	[56:0]	Reserved
RSLVFCI	[56:0]	Reserved

MSR0000_0473...MSRC000_21C3 [PIE Machine Check Miscellaneous 0] (MCA::PIE::MCA_MISC0_PIE)

Log miscellaneous information associated with errors.

_inst[PIE0,BCST]_n0_aliasMSRLEGACY; MSR0000_0473

_inst[PIE0,BCST]_n0_aliasMSR; MSRC000_21C3

Bits	Description
63	Valid. Reset: 1. 1=A valid CntP field is present in this register. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read-only.
62	CntP. Reset: 1. 1=A valid threshold counter is present. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read-only.
61	Locked. Reset: 0. 1=Writes to this register are ignored. This bit is set by BIOS to indicate that this register is not available for OS use. BIOS should set this bit if ThresholdIntType is set to SMI. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read-only.
60	IntP. Reset: 1. 1=ThresholdIntType can be used to generate interrupts. 0=ThresholdIntType and interrupt generation are not supported. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::PIE::MCA_MISC0_PIE[Locked]) ? Read-write : Read-only.
59:56	Reserved.
55:52	LvtOffset. Reset: 0h. One per die. For error thresholding interrupts, specifies the address of the LVT entry in the APIC registers as follows: LVT address = (LvtOffset shifted left 4 bits) + 500h (see Core::X86::Apic::ExtendedInterruptLvtEntries). AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::PIE::MCA_MISC0_PIE[Locked]) ? Read-write : Read-only.
51	CntEn. Reset: 0. 1=Count thresholding errors. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::PIE::MCA_MISC0_PIE[Locked]) ? Read-write : Read-only.
50:49	ThresholdIntType. Reset: Cold,0h. Specifies the type of interrupt signaled when Ovrflw is set and IntP==1. 00b = No interrupt. 01b = APIC based interrupt (see Core::X86::Msr::McaIntrCfg[ThresholdLvtOffset]). 10b = SMI trigger event. 11b = Reserved. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::PIE::MCA_MISC0_PIE[Locked]) ? Read-write : Read-only.
48	Ovrflw. Reset: Cold,0. Set by hardware when ErrCnt transitions from FFEh to FFFh. When this field is set, ErrCnt no longer increments. When this bit is set, the interrupt selected by the ThresholdIntType field is generated. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::PIE::MCA_MISC0_PIE[Locked]) ? Read-write : Read-only.
47:44	Reserved.
43:32	ErrCnt. Reset: Cold,000h. This is written by software to set the starting value of the error counter. This is incremented by hardware when errors are logged. When this counter overflows, it stays at FFFh (no rollover). The threshold value, written by software, is (FFFh - the desired error count (the number of errors necessary in order for an interrupt to be taken)); the desired error count of 0 (a write value of FFFh) is not supported. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::PIE::MCA_MISC0_PIE[Locked]) ? Read-write : Read-only.
31:24	BlkPtr. Read-write. Reset: 00h. 00h=Extended MISC MSR block is not valid. 01h=Extended MSR block is valid.
23:0	Reserved.

MSRC000_21C4 [PIE Machine Check Configuration] (MCA::PIE::MCA_CONFIG_PIE)

Reset: 0000_0002_0000_0125h.

Controls configuration of the associated machine check bank.

_inst[PIE0,BCST]_n0_aliasMSR; MSRC000_21C4

Bits	Description
63:39	Reserved.
38:37	DeferredIntType. Read-write. Reset: 0h. Specifies the type of interrupt signaled when a deferred error is logged. 00b = No interrupt. 01b = APIC based interrupt (see Core::X86::Msr::McaIntrCfg[DeferredLvtOffset]). 10b = SMI trigger event. 11b = Reserved.
36:35	Reserved.
34	LogDeferredInMcaStat. Read-write. Reset: 0. Init: BIOS,1. 1=Log deferred errors in MCA::PIE::MCA_STATUS_PIE and MCA::PIE::MCA_ADDR_PIE in addition to MCA::PIE::MCA_DESTAT_PIE and MCA::PIE::MCA_DEADDR_PIE. 0=Only log deferred errors in MCA::PIE::MCA_DESTAT_PIE and MCA::PIE::MCA_DEADDR_PIE. This bit does not affect logging of deferred errors in MCA::PIE::MCA_SYND_PIE, MCA::PIE::MCA_MISC0_PIE.
33	Reserved.
32	McaXEnable. Read-write. Reset: 0. Init: BIOS,1. Check: 1. 1=Software has acknowledged support for the MCAX feature set. 0=Software has not acknowledged support for the MCAX feature set. All uncorrected and fatal errors will cause an ErrorEvent packet to be generated. Deferred error interrupts are configured via Core::X86::Msr::McaIntrCfg.
31:9	Reserved.
8	McaLsbInStatusSupported. Read-only. Reset: 1. 1=MCA::PIE::MCA_CONFIG_PIE[McaLsbInStatusSupported] indicates that AddrLsb is located in McaStatus registers.
7:6	Reserved.
5	DeferredIntTypeSupported. Read-only. Reset: 1. 1=MCA::PIE::MCA_CONFIG_PIE[DeferredIntType] controls the type of interrupt generated on a deferred error. Deferred errors are supported in this bank only if MCA::PIE::MCA_CONFIG_PIE[DeferredErrorLoggingSupported]=1.
4:3	Reserved.
2	DeferredErrorLoggingSupported. Read-only. Reset: 1. 1=Deferred errors are supported in this MCA bank, and MCA::PIE::MCA_CONFIG_PIE[LogDeferredInMcaStat] controls the logging behavior of these errors. MCA::PIE::MCA_DESTAT_PIE and MCA::PIE::MCA_DEADDR_PIE are supported in this MCA bank. 0=Deferred errors are not supported in this bank.
1	Reserved.
0	McaX. Read-only. Reset: 1. 1=This bank provides Machine Check Architecture Extensions. Up to 4 additional MISC registers (MISC1-MISC4) are supported. MCA::PIE::MCA_MISC0_PIE[BlkPtr] indicates the presence of the additional MISC registers, but is not used to determine their MSR numbers. Deferred error interrupt type is specifiable by MCA bank. MCA::PIE::MCA_STATUS_PIE[TCC] is present.

MSRC000_21C5 [PIE IP Identification] (MCA::PIE::MCA_IPID_PIE)

Reset: 0001_002E_0000_0000h.

The MCA::PIE::MCA_IPID_PIE register is used by software to determine what IP type and revision is associated with the MCA bank.

_inst[PIE0,BCST]_n0_aliasMSR; MSRC000_21C5

Bits	Description
63:48	McaType. Read-only. Reset: 0001h. The McaType of the MCA bank within this IP.
47:44	InstanceIdHi. Read-write. Reset: 0h. The HI value instance ID of this IP. This is initialized to a unique ID per instance of this register.
43:32	HardwareID. Read-only. Reset: 02Eh. The Hardware ID of the IP associated with this MCA bank.
31:0	InstanceId. Read-write. Reset: 0000_0000h. Init: 1F00_0B00h. The instance ID of this IP. This is initialized to a unique ID per instance of this register.

MSRC000_21C6 [PIE Machine Check Syndrome] (MCA::PIE::MCA_SYND_PIE)

Read-write, Volatile. Reset: Cold, 0000_0000_0000_0000h.

Logs physical location information associated with error in MCA::PIE::MCA_STATUS_PIE Thread 0

_inst[PIE0, BCST]_n0_aliasMSR; MSRC000_21C6

Bits	Description
63:46	Reserved.
45:32	Syndrom . Read-write, Volatile. Reset: Cold, 0000h. Contains the syndrome, if any, associated with the error logged in MCA::PIE::MCA_STATUS_PIE. The low-order bit of the syndrome is stored in bit 0, and the syndrome has a length specified by MCA::PIE::MCA_SYND_PIE[Length]. The Syndrome field is only valid when MCA::PIE::MCA_SYND_PIE[Length] is not 0.
31:27	Reserved.
26:24	ErrorPriority . Read-write, Volatile. Reset: Cold, 0h. Encodes the priority of the error logged in MCA::PIE::MCA_SYND_PIE. 3'b000 = No error; 3'b001 = Reserved; 3'b010 = Corrected Error; 3'b011 = Deferred Error; 3'b100 = Uncorrected Error; 3'b101 = Fatal Error; all others reserved.
23:18	Length . Read-write, Volatile. Reset: Cold, 00h. Specifies the length in bits of the syndrome contained in MCA::PIE::MCA_SYND_PIE[Syndrome]. A value of 0 indicates that there is no valid syndrome in MCA::PIE::MCA_SYND_PIE. For example, a syndrome length of 9 means that MCA::PIE::MCA_SYND_PIE[Syndrome] bits [8:0] contains a valid syndrome.
17:0	ErrorInformation . Read-write, Volatile. Reset: Cold, 0_0000h. Contains error-specific information about the location of the error. Decoding is available in Table 63 [MCA_SYND_PIE].

Table 63: MCA_SYND_PIE

Error Type	Bits	Description
HW_ASSERT	[17:16] [15:8] [7:6] [5:0]	Reserved Block Instance ID Reserved Hardware Assert ID
CSW	[17] [16:13] [12:0]	
GMI	[17:17] [16:2] [1:0]	
FTI_DAT_STAT	[3:0]	
DEF	[17:0]	Reserved
WDT	[17:5] [3:1] [0:0]	
CNLI	[17:8] [7:6] [5:4] [3:3] [2:0]	Reserved Reserved
RSLVFCI	[17] [16] [15] [14] [13]	

	[12:0]	
--	--------	--

MSRC000_21C8 [PIE Machine Check Deferred Error Status] (MCA::PIE::MCA_DESTAT_PIE)

Reset: Cold,0000_0000_0000_0000h.

Holds status information for the first deferred error seen in this bank.

_inst[PIE0,BCST]_n0_aliasMSR; MSRC000_21C8

Bits	Description
63	Val. Read-write, Volatile. Reset: Cold,0. 1=A valid error has been detected (whether it is enabled or not).
62	Overflow. Read-write, Volatile. Reset: Cold,0. 1=An error was detected while the valid bit (Val) was set; at least one error was not logged. Overflow is set independently of whether the existing error is overwritten. (See the section on overwrite priorities.)
61:59	RESERV4. Read-write. Reset: Cold,0h.
58	AddrV. Read-write, Volatile. Reset: Cold,0. 1=MCA::PIE::MCA_DEADDR_PIE contains address information associated with the error.
57:54	RESERV3. Read-write. Reset: Cold,0h.
53	SyndV. Read-write, Volatile. Reset: Cold,0. 1=This error logged information in MCA::PIE::MCA_SYND_PIE. If MCA::PIE::MCA_SYND_PIE[ErrorPriority] is the same as the priority of the error in MCA::PIE::MCA_STATUS_PIE, then the information in MCA::PIE::MCA_SYND_PIE is associated with the error in MCA::PIE::MCA_DESTAT_PIE.
52:45	RESERV2. Read-write. Reset: Cold,00h.
44	Deferred. Read-write, Volatile. Reset: Cold,0. 1=A deferred error was created. A deferred error is the result of an uncorrectable data error which did not immediately cause a processor exception; poison is created and an exception is deferred until the poison data is consumed.
43:30	RESERV1. Read-write. Reset: Cold,0000h.
29:24	AddrLsb. Read-write, Volatile. Reset: Cold,00h. Specifies the least significant valid bit of the address contained in MCA::PIE::MCA_ADDR_PIE[ErrorAddr]. A value of 0 indicates that MCA::PIE::MCA_ADDR_PIE[55:0] contains a valid byte address. A value of 6 indicates that MCA::PIE::MCA_ADDR_PIE[55:6] contains a valid cache line address and that MCA::PIE::MCA_ADDR_PIE[5:0] are not part of the address and should be ignored by error handling software. A value of 12 indicates that MCA::PIE::MCA_ADDR_PIE[55:12] contain a valid 4KB memory page and that MCA::PIE::MCA_ADDR_PIE[11:0] should be ignored by error handling software.
23:22	RESERV0. Read-write. Reset: Cold,0h.
21:16	ErrorCodeExt. Read-write, Volatile. Reset: Cold,00h. Logs an extended error code when an error is detected. This model-specific field is used in conjunction with ErrorCode? to identify the error sub-type for root cause analysis.
15:0	ErrorCode. Read-write, Volatile. Reset: Cold,0000h. Error code for this error.

MSRC000_21C9 [PIE Deferred Error Address] (MCA::PIE::MCA_DEADDR_PIE)

Reset: Cold,0000_0000_0000_0000h.

The MCA::PIE::MCA_DEADDR_PIE register stores the address associated with the error in MCA::PIE::MCA_DESTAT_PIE. The register is only meaningful if MCA::PIE::MCA_DESTAT_PIE[Val]=1 and MCA::PIE::MCA_DESTAT_PIE[AddrV]=1. The lowest valid bit of the address is defined by MCA::PIE::MCA_DESTAT_PIE[AddrLsb].

_inst[PIE0,BCST]_n0_aliasMSR; MSRC000_21C9

Bits	Description
63:56	Reserved.
55:0	ErrorAddr. Read-write, Volatile. Reset: Cold,00_0000_0000_0000h. Contains the address, if any, associated with the error logged in MCA::PIE::MCA_DESTAT_PIE. The lowest-order valid bit of the address is specified in MCA::PIE::MCA_DESTAT_PIE[AddrLsb].

MSRC001_041C [PIE Machine Check Control Mask] (MCA::PIE::MCA_CTL_MASK_PIE)

Read-write. Reset: 0000_0000_0000_0000h.

Inhibit detection of an error source.

_inst[PIE0,BCST]_n0_aliasMSR; MSRC001_041C

Bits	Description
63:8	Reserved.
7	RSLVFCI . Read-write. Reset: 0. Register access during DF Cstate: Register access is detected from SMN during DF Cstate.
6	CNLI . Read-write. Reset: 0. Error is detected in CXL Link.
5	WDT . Read-write. Reset: 0. Watch Dog Timer: A watch dog timer expired.
4	DEF . Read-write. Reset: 0. A deferred error was detected in the DF.
3	FTI_DAT_STAT . Read-write. Reset: 0. Poison data consumption: Poison data was written to an internal PIE register.
2	GMI . Read-write. Reset: 0. Link Error: An error occurred on a GMI or xGMI link.
1	CSW . Read-write. Reset: 0. Register security violation: A security violation was detected on an access to an internal PIE register.
0	HW_ASSERT . Read-write. Reset: 0. Hardware Assert: A hardware assert was detected.

3.2.5.10 UMC**MSR0000_0454...MSRC000_2160 [UMC Machine Check Control] (MCA::UMC::MCA_CTL_UMC)**

Read-write. Reset: 0000_0000_0000_0000h.

0=Disables error reporting for the corresponding error. 1=Enables error reporting via machine check exception for the corresponding error. The MCA::UMC::MCA_CTL_UMC register must be enabled by the corresponding enable bit in Core::X86::Msr::MCG_CTL. Does not affect error detection, correction, or logging.

_instUMCWPHY0UMC_n0_umc0_aliasMSRLEGACY; MSR0000_0454

_instUMCWPHY1UMC_n1_umc0_aliasMSRLEGACY; MSR0000_0458

_instUMCWPHY0UMC_n0_umc0_aliasMSR; MSRC000_2150

_instUMCWPHY1UMC_n1_umc0_aliasMSR; MSRC000_2160

Bits	Description
63:12	Reserved.
11	RdCrcErr . Read-write. Reset: 0. Read CRC error. CRC error occurred on a DRAM read from any subchannel
10	ThrttlErr . Read-write. Reset: 0. Indicates that UMC is throttling
9	EcsErr . Read-write. Reset: 0. ECS Error. Indicates that a device exceeded the ECS Error Threshold Count.
8	EcsRowErr . Read-write. Reset: 0. ECS Row Error. Indicates that a single device row exceeded four code word errors.
7	AesSramEccErr . Read-write. Reset: 0. AES SRAM ECC error. An ECC error occurred on a AES SRAM in the processor.
6	DcqSramEccErr . Read-write. Reset: 0. DCQ SRAM ECC error. An ECC error occurred on a DCQ SRAM in the processor.
5	WriteDataCrcErr . Read-write. Reset: 0. Write data CRC error. A write data CRC error occurred on the DRAM data bus.
4	AddressCommandParityErr . Read-write. Reset: 0. Address/Command parity error. A parity error occurred on the DRAM address/command bus.
3	ApbErr . Read-write. Reset: 0. Advanced peripheral bus error. An error occurred on the advanced peripheral bus.
2	SdpParityErr . Read-write. Reset: 0. SDP parity error. A parity error was detected on write data from the data fabric in the processor.
1	WriteDataPoisonErr . Read-write. Reset: 0. Data poison error. The system tried to write poison data to DRAM and either DRAM does not support ECC or UMC_CH.EccCtrl.WrEccEn is cleared.
0	DramEccErr . Read-write. Reset: 0. DRAM ECC error. An ECC error occurred on a DRAM read.

MSR0000_0455...MSRC000_2161 [UMC Machine Check Status] (MCA::UMC::MCA_STATUS_UMC)

Reset: Cold,0000_0000_0000_0000h.

Logs information associated with errors.

_instUMCWPHY0UMC_n0_umc0_aliasMSRLEGACY; MSR0000_0455

_instUMCWPHY1UMC_n1_umc0_aliasMSRLEGACY; MSR0000_0459

_instUMCWPHY0UMC_n0_umc0_aliasMSR; MSRC000_2151

_instUMCWPHY1UMC_n1_umc0_aliasMSR; MSRC000_2161

Bits	Description
63	Val. Reset: Cold,0. 1=A valid error has been detected. This bit should be cleared by software after the register has been read. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
62	Overflow. Reset: Cold,0. 1=An error was detected while the valid bit (Val) was set; at least one error was not logged. Overflow is set independently of whether the existing error is overwritten. See 3.1.3 [Machine Check Errors]. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
61	UC. Reset: Cold,0. 1=The error was not corrected by hardware. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
60	En. Reset: Cold,0. 1=MCA error reporting is enabled for this error, as indicated by the corresponding bit in MCA::UMC::MCA_CTL_UMC. This bit is a copy of bit in MCA::UMC::MCA_CTL_UMC for this error. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
59	MiscV. Reset: Cold,0. 1=Valid thresholding in MCA::UMC::MCA_MISC0_UMC. In certain modes, MISC registers are owned by platform firmware and will RAZ when read by non-SMM code. Therefore, it is possible for MiscV=1 and the MISC register to read as all zeros. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
58	AddrV. Reset: Cold,0. 1=MCA::UMC::MCA_ADDR_UMC contains address information associated with the error. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
57	PCC. Reset: Cold,0. 1=Hardware context held by the processor may have been corrupted. Continued operation of the system may have unpredictable results. The error is not recoverable or survivable, and the system should be reinitialized. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
56	ErrCoreIdVal. Reset: Cold,0. 1=The ErrCoreId field is valid. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
55	TCC. Reset: Cold,0. 1=Hardware context of the process thread to which the error was reported may have been corrupted. Continued operation of the thread may have unpredictable results. The thread must be terminated. Only meaningful when MCA::UMC::MCA_STATUS_UMC[PCC]=0. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
54	RESERV54. Reset: Cold,0. MCA_STATUS Register Reserved bit. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
53	SyndV. Reset: Cold,0. 1=This error logged information in MCA::UMC::MCA_SYND_UMC. If MCA::UMC::MCA_SYND_UMC[ErrorPriority] is the same as the priority of the error in MCA::UMC::MCA_STATUS_UMC, then the information in MCA::UMC::MCA_SYND_UMC is associated with the error in MCA::UMC::MCA_STATUS_UMC. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
52	Reserved.
51:47	RESERV47. Reset: Cold,00h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
46	CECC. Reset: Cold,0. 1=The error was a correctable ECC error according to the restrictions of the ECC algorithm. UC indicates whether the error was actually corrected by the processor. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.

45	UECC. Reset: Cold,0. 1=The error was an uncorrectable ECC error according to the restrictions of the ECC algorithm. UC indicates whether the error was actually corrected by the processor. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
44	Deferred. Reset: Cold,0. 1=A deferred error was created. A deferred error is the result of an uncorrectable data error which did not immediately cause a processor exception; an exception is deferred until the erroneous data is consumed. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
43	Poison. Reset: Cold,0. 1=The error was the result of attempting to consume poisoned data. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
42:41	RESERV41. Reset: Cold,0h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
40	Scrub. Reset: Cold,0. 1=The error was the result of a scrub operation. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
39:38	RESERV38. Reset: Cold,0h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
37:32	ErrCoreId. Reset: Cold,00h. When ErrCoreIdVal=1 this field indicates which core within the processor is associated with the error; Otherwise this field is reserved. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
31:30	RESERV30. Reset: Cold,0h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
29:24	AddrLsb. Reset: Cold,00h. Specifies the least significant valid bit of the address contained in MCA::UMC::MCA_ADDR_UMC[ErrorAddr]. A value of 0 indicates that MCA::UMC::MCA_ADDR_UMC[55:0] contains a valid byte address. A value of 6 indicates that MCA::UMC::MCA_ADDR_UMC[55:6] contains a valid cache line address and that MCA::UMC::MCA_ADDR_UMC[5:0] are not part of the address and should be ignored by error handling software. A value of 12 indicates that MCA::UMC::MCA_ADDR_UMC[55:12] contain a valid 4KB memory page and that MCA::UMC::MCA_ADDR_UMC[11:0] should be ignored by error handling software. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
23:22	RESERV22. Reset: Cold,0h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
21:16	ErrorCodeExt. Reset: Cold,00h. Extended Error Code. This field is used to identify the error type for root cause analysis. This field indicates which bit position in MCA::UMC::MCA_CTL_UMC enables error reporting for the logged error. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
15:0	ErrorCode. Reset: Cold,0000h. Error code for this error. See 3.1.3.3 [Error Codes] for details on decoding this field. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.

Table 64: MCA_STATUS_UMC

Error Type	ErrorCode Ext	UC	PCC	TCC	Deferred	Poison	AddrV
DramEccErr	0x0	0/1	0/1	0/1	0/1	0	1
WriteDataPoisonErr	0x1	1	1	1	0	0	0
SdpParityErr	0x2	1	1	1	0	0	0
ApbErr	0x3	1	1	1	0	0	1
AddressCommandParityErr	0x4	0/1	0/1	0/1	0	0	0/1

WriteDataCr cErr	0x5	0/1	0/1	0/1	0	0	0/1
DcqSramEcc Err	0x6	0/1	0/1	0/1	0	0	0
AesSramEcc Err	0x7	0/1	0/1	0/1	0	0	0
EcsRowErr	0x8	0	0	0	0	0	0
EcsErr	0x9	0	0	0	0	0	0
ThrttlErr	0xa	0	0	0	0	0	0
RdCrcErr	0xb	0	0	0	1	0	1

MSR0000_0456...MSRC000_2162 [UMC Machine Check Address] (MCA::UMC::MCA_ADDR_UMC)

Reset: Cold,0000_0000_0000_0000h.

MCA::UMC::MCA_ADDR_UMC stores an address and other information associated with the error in MCA::UMC::MCA_STATUS_UMC. The register is only meaningful if MCA::UMC::MCA_STATUS_UMC[Val]=1 and MCA::UMC::MCA_STATUS_UMC[AddrV]=1.

_instUMCWPHY0UMC_n0_umc0_aliasMSRLEGACY; MSR0000_0456

_instUMCWPHY1UMC_n1_umc0_aliasMSRLEGACY; MSR0000_045A

_instUMCWPHY0UMC_n0_umc0_aliasMSR; MSRC000_2152

_instUMCWPHY1UMC_n1_umc0_aliasMSR; MSRC000_2162

Bits	Description
63:56	Reserved.
55:0	ErrorAddr. Read-write, Volatile. Reset: Cold,00_0000_0000_0000h. Unless otherwise specified by an error, contains the address associated with the error logged in MCA::UMC::MCA_STATUS_UMC. For physical addresses, the most significant bit is given by Core::X86::Cpuid::LongModeInfo[PhysAddrSize].

Table 65: MCA_ADDR_UMC

Error Type	Bits	Description
DramEccErr	[55:39]	Reserved
	[39:4]	Reserved
WriteDataPoisonErr	[56:0]	Reserved
SdpParityErr	[56:0]	Reserved
ApbErr	[55:30]	Reserved
	[29:0]	Reserved
AddressCommandParityErr	[55:38]	Reserved
	[37:36]	Reserved
	[35:32]	Chip Select
	[31:0]	Reserved
WriteDataCrcErr	[55:38]	Reserved
	[37:36]	Reserved
	[35:32]	Chip Select
	[31:0]	Reserved
DcqSramEccErr	[56:0]	Reserved
AesSramEccErr	[56:0]	Reserved
EcsRowErr	[56:0]	Reserved
EcsErr	[56:0]	Reserved
ThrttlErr	[56:0]	Reserved
RdCrcErr	[55:39]	Reserved
	[39:4]	Reserved

MSR0000_0457...MSRC000_2163 [UMC Machine Check Miscellaneous 0] (MCA::UMC::MCA_MISC0_UMC)

Log miscellaneous information associated with errors.

_instUMCWPHY0UMC_n0_umc0_aliasMSRLEGACY; MSR0000_0457

_instUMCWPHY1UMC_n1_umc0_aliasMSRLEGACY; MSR0000_045B

_instUMCWPHY0UMC_n0_umc0_aliasMSR; MSRC000_2153

_instUMCWPHY1UMC_n1_umc0_aliasMSR; MSRC000_2163

Bits	Description
63	Valid. Reset: 1. 1=A valid CntP field is present in this register. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read-only.
62	CntP. Reset: 1. 1=A valid threshold counter is present. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read-only.
61	Locked. Reset: 0. 1=Writes to this register are ignored. This bit is set by BIOS to indicate that this register is not available for OS use. BIOS should set this bit if ThresholdIntType is set to SMI. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read-only.
60	IntP. Reset: 1. 1=ThresholdIntType can be used to generate interrupts. 0=ThresholdIntType and interrupt generation are not supported. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::UMC::MCA_MISC0_UMC[Locked]) ? Read-write : Read-only.
59:56	Reserved.
55:52	LvtOffset. Reset: 0h. One per die. For error thresholding interrupts, specifies the address of the LVT entry in the APIC registers as follows: LVT address = (LvtOffset shifted left 4 bits) + 500h (see Core::X86::Apic::ExtendedInterruptLvtEntries). AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::UMC::MCA_MISC0_UMC[Locked]) ? Read-write : Read-only.
51	CntEn. Reset: 0. 1=Count thresholding errors. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::UMC::MCA_MISC0_UMC[Locked]) ? Read-write : Read-only.
50:49	ThresholdIntType. Reset: Cold,0h. Specifies the type of interrupt signaled when Ovrflw is set and IntP==1. 00b = No interrupt. 01b = APIC based interrupt (see Core::X86::Msr::McaIntrCfg[ThresholdLvtOffset]). 10b = SMI trigger event. 11b = Reserved. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::UMC::MCA_MISC0_UMC[Locked]) ? Read-write : Read-only.
48	Ovrflw. Reset: Cold,0. Set by hardware when ErrCnt transitions from FFEh to FFFh. When this field is set, ErrCnt no longer increments. When this bit is set, the interrupt selected by the ThresholdIntType field is generated. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::UMC::MCA_MISC0_UMC[Locked]) ? Read-write : Read-only.
47:44	Reserved.
43:32	ErrCnt. Reset: Cold,000h. This is written by software to set the starting value of the error counter. This is incremented by hardware when errors are logged. When this counter overflows, it stays at FFFh (no rollover). The threshold value, written by software, is (FFFh - the desired error count (the number of errors necessary in order for an interrupt to be taken)); the desired error count of 0 (a write value of FFFh) is not supported. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::UMC::MCA_MISC0_UMC[Locked]) ? Read-write : Read-only.
31:24	BlkPtr. Read-write. Reset: 01h. 00h=Extended MISC MSR block is not valid. 01h=Extended MSR block is valid.
23:0	Reserved.

MSRC000_21[5...6]4 [UMC Machine Check Configuration] (MCA::UMC::MCA_CONFIG_UMC)

Reset: 0000_0002_0000_0125h.

Controls configuration of the associated machine check bank.

_instUMCWPHY0UMC_n0_umc0_aliasMSR; MSRC000_2154

_instUMCWPHY1UMC_n1_umc0_aliasMSR; MSRC000_2164

Bits	Description
63:39	Reserved.
38:37	DeferredIntType . Read-write. Reset: 0h. Specifies the type of interrupt signaled when a deferred error is logged. 00b = No interrupt. 01b = APIC based interrupt (see Core::X86::Msr::McaIntrCfg[DeferredLvtOffset]). 10b = SMI trigger event. 11b = Reserved.
36:35	Reserved.
34	LogDeferredInMcaStat . Read-write. Reset: 0. Init: BIOS,1. 1=Log deferred errors in MCA::UMC::MCA_STATUS_UMC and MCA::UMC::MCA_ADDR_UMC in addition to MCA::UMC::MCA_DESTAT_UMC and MCA::UMC::MCA_DEADDR_UMC. 0=Only log deferred errors in MCA::UMC::MCA_DESTAT_UMC and MCA::UMC::MCA_DEADDR_UMC. This bit does not affect logging of deferred errors in MCA::UMC::MCA_SYND_UMC, MCA::UMC::MCA_MISC0_UMC.
33	Reserved.
32	McaXEnable . Read-write. Reset: 0. Init: BIOS,1. Check: 1. 1=Software has acknowledged support for the MCAX feature set. 0=Software has not acknowledged support for the MCAX feature set. All uncorrected and fatal errors will cause an ErrorEvent packet to be generated. Deferred error interrupts are configured via Core::X86::Msr::McaIntrCfg.
31:9	Reserved.
8	McaLsbInStatusSupported . Read-only. Reset: 1. 1=MCA::UMC::MCA_CONFIG_UMC[McaLsbInStatusSupported] indicates that AddrLsb is located in McaStatus registers.
7:6	Reserved.
5	DeferredIntTypeSupported . Read-only. Reset: 1. 1=MCA::UMC::MCA_CONFIG_UMC[DeferredIntType] controls the type of interrupt generated on a deferred error. Deferred errors are supported in this bank only if MCA::UMC::MCA_CONFIG_UMC[DeferredErrorLoggingSupported]=1.
4:3	Reserved.
2	DeferredErrorLoggingSupported . Read-only. Reset: 1. 1=Deferred errors are supported in this MCA bank, and MCA::UMC::MCA_CONFIG_UMC[LogDeferredInMcaStat] controls the logging behavior of these errors. MCA::UMC::MCA_DESTAT_UMC and MCA::UMC::MCA_DEADDR_UMC are supported in this MCA bank. 0=Deferred errors are not supported in this bank.
1	Reserved.
0	McaX . Read-only. Reset: 1. 1=This bank provides Machine Check Architecture Extensions. Up to 4 additional MISC registers (MISC1-MISC4) are supported. MCA::UMC::MCA_MISC0_UMC[BlkPtr] indicates the presence of the additional MISC registers, but is not used to determine their MSR numbers. Deferred error interrupt type is specifiable by MCA bank. MCA::UMC::MCA_STATUS_UMC[TCC] is present.

MSRC000_21[5...6]5 [UMC IP Identification] (MCA::UMC::MCA_IPID_UMC)

Reset: 0000_0096_0000_0000h.

The MCA::UMC::MCA_IPID_UMC register is used by software to determine what IP type and revision is associated with the MCA bank.

_instUMCWPHY0UMC_n0_umc0_aliasMSR; MSRC000_2155

_instUMCWPHY1UMC_n1_umc0_aliasMSR; MSRC000_2165

Bits	Description
63:48	McaType . Read-only. Reset: 0000h. The McaType of the MCA bank within this IP.
47:44	InstanceIdHi . Read-write. Reset: 0h. The HI value instance ID of this IP. This is initialized to a unique ID per instance of this register.
43:32	HardwareID . Read-only. Reset: 096h. The Hardware ID of the IP associated with this MCA bank.
31:0	InstanceId . Read-write. Reset: 0000_0000h. The instance ID of this IP. This is initialized to a unique ID per instance of this register.
	Init: _instUMCWPHY0UMC_n0_umc0_aliasMSR: 0005_0F00h
	Init: _instUMCWPHY1UMC_n1_umc0_aliasMSR: 0015_0F00h

MSRC000_21[5...6]6 [UMC Machine Check Syndrome] (MCA::UMC::MCA_SYND_UMC)

Read-write, Volatile. Reset: Cold, 0000_0000_0000_0000h.

Logs physical location information associated with error in MCA::UMC::MCA_STATUS_UMC Thread 0

_instUMCWPHY0UMC_n0_umc0_aliasMSR; MSRC000_2156

_instUMCWPHY1UMC_n1_umc0_aliasMSR; MSRC000_2166

Bits	Description
63:32	Syndrom . Read-write, Volatile. Reset: Cold, 0000_0000h. Contains the syndrome, if any, associated with the error logged in MCA::UMC::MCA_STATUS_UMC. The low-order bit of the syndrome is stored in bit 0, and the syndrome has a length specified by MCA::UMC::MCA_SYND_UMC[Length]. The Syndrome field is only valid when MCA::UMC::MCA_SYND_UMC[Length] is not 0.
31:27	Reserved.
26:24	ErrorPriority . Read-write, Volatile. Reset: Cold, 0h. Encodes the priority of the error logged in MCA::UMC::MCA_SYND_UMC. 3'b000 = No error; 3'b001 = Reserved; 3'b010 = Corrected Error; 3'b011 = Deferred Error; 3'b100 = Uncorrected Error; 3'b101 = Fatal Error; all others reserved.
23:18	Length . Read-write, Volatile. Reset: Cold, 00h. Specifies the length in bits of the syndrome contained in MCA::UMC::MCA_SYND_UMC[Syndrome]. A value of 0 indicates that there is no valid syndrome in MCA::UMC::MCA_SYND_UMC. For example, a syndrome length of 9 means that MCA::UMC::MCA_SYND_UMC[Syndrome] bits [8:0] contains a valid syndrome.
17:0	ErrorInformation . Read-write, Volatile. Reset: Cold, 0_0000h. Contains error-specific information about the location of the error. Decoding is available in Table 66 [MCA_SYND_UMC].

Table 66: MCA_SYND_UMC

Error Type	Bits	Description
DramEccErr	[17:16]	Reserved
	[15]	Software-Managed Bad Symbol ID Error
	[14]	Reserved
	[13:8]	Symbol. Only contains valid information on a corrected error.
	[7:4]	Cid. Specifies the rank multiply ID for supported DIMMs.
	[3]	Sub channel
	[2:0]	Chip Select
WriteDataPoisonErr	[17:0]	Reserved
SdpParityErr	[17:0]	Reserved
ApbErr	[17:0]	Reserved
AddressCommandParityErr	[17:0]	Reserved

WriteDataCrcErr	[17:0]	Reserved
DcqSramEccErr	[17:14] [13:0]	Reserved Reserved
AesSramEccErr	[17] [16:8] [7:4] [3:2] [1:0]	Reserved Reserved Reserved Reserved Reserved
EcsRowErr	[17:0]	Reserved
EcsErr	[17:0]	Reserved
ThrtldErr	[17:0]	Reserved
RdCrcErr	[17:8] [7:4] [3] [2:0]	Reserved Cid. Specifies the rank multiply ID for supported DIMMs. Sub channel Chip Select

MSRC000_21[5...6]E [UMC Machine Check Syndrome Extended] (MCA::UMC::MCA_SYND1_UMC)

Read-write, Volatile. Reset: Cold, 0000_0000_0000_0000h.

Logs physical location information associated with error in MCA::UMC::MCA_STATUS_UMC Thread 0

_instUMCWPHY0UMC_n0_umc0_aliasMSR; MSRC000_215E

_instUMCWPHY1UMC_n1_umc0_aliasMSR; MSRC000_216E

Bits	Description
63:0	Syndrome. Read-write, Volatile. Reset: Cold, 0000_0000_0000_0000h. Contains the syndrome, if any, associated with the error logged in MCA::UMC::MCA_STATUS_UMC. The low-order bit of the syndrome is stored in bit 0, and the syndrome has a length specified by MCA::UMC::MCA_SYND_UMC[Length]. The Syndrome field is only valid when MCA::UMC::MCA_SYND_UMC[Length] is not 0.

MSRC000_21[5...6]F [UMC Machine Check Syndrome Extended] (MCA::UMC::MCA_SYND2_UMC)

Read-write, Volatile. Reset: Cold, 0000_0000_0000_0000h.

Logs physical location information associated with error in MCA::UMC::MCA_STATUS_UMC Thread 0

_instUMCWPHY0UMC_n0_umc0_aliasMSR; MSRC000_215F

_instUMCWPHY1UMC_n1_umc0_aliasMSR; MSRC000_216F

Bits	Description
63:0	Syndrome. Read-write, Volatile. Reset: Cold, 0000_0000_0000_0000h. Contains the syndrome, if any, associated with the error logged in MCA::UMC::MCA_STATUS_UMC. The low-order bit of the syndrome is stored in bit 0, and the syndrome has a length specified by MCA::UMC::MCA_SYND_UMC[Length]. The Syndrome field is only valid when MCA::UMC::MCA_SYND_UMC[Length] is not 0.

MSRC000_21[5...6]8 [UMC Machine Check Deferred Error Status] (MCA::UMC::MCA_DESTAT_UMC)

Reset: Cold,0000_0000_0000_0000h.

Holds status information for the first deferred error seen in this bank.

_instUMCWPHY0UMC_n0_umc0_aliasMSR; MSRC000_2158

_instUMCWPHY1UMC_n1_umc0_aliasMSR; MSRC000_2168

Bits	Description
63	Val. Read-write, Volatile. Reset: Cold,0. 1=A valid error has been detected (whether it is enabled or not).
62	Overflow. Read-write, Volatile. Reset: Cold,0. 1=An error was detected while the valid bit (Val) was set; at least one error was not logged. Overflow is set independently of whether the existing error is overwritten. (See the section on overwrite priorities.)
61:59	RESERV4. Read-write. Reset: Cold,0h.
58	AddrV. Read-write, Volatile. Reset: Cold,0. 1=MCA::UMC::MCA_DEADDR_UMC contains address information associated with the error.
57:54	RESERV3. Read-write. Reset: Cold,0h.
53	SyndV. Read-write, Volatile. Reset: Cold,0. 1=This error logged information in MCA::UMC::MCA_SYND_UMC. If MCA::UMC::MCA_SYND_UMC[ErrorPriority] is the same as the priority of the error in MCA::UMC::MCA_STATUS_UMC, then the information in MCA::UMC::MCA_SYND_UMC is associated with the error in MCA::UMC::MCA_DESTAT_UMC.
52:45	RESERV2. Read-write. Reset: Cold,00h.
44	Deferred. Read-write, Volatile. Reset: Cold,0. 1=A deferred error was created. A deferred error is the result of an uncorrectable data error which did not immediately cause a processor exception; poison is created and an exception is deferred until the poison data is consumed.
43:30	RESERV1. Read-write. Reset: Cold,0000h.
29:24	AddrLsb. Read-write, Volatile. Reset: Cold,00h. Specifies the least significant valid bit of the address contained in MCA::UMC::MCA_ADDR_UMC[ErrorAddr]. A value of 0 indicates that MCA::UMC::MCA_ADDR_UMC[55:0] contains a valid byte address. A value of 6 indicates that MCA::UMC::MCA_ADDR_UMC[55:6] contains a valid cache line address and that MCA::UMC::MCA_ADDR_UMC[5:0] are not part of the address and should be ignored by error handling software. A value of 12 indicates that MCA::UMC::MCA_ADDR_UMC[55:12] contain a valid 4KB memory page and that MCA::UMC::MCA_ADDR_UMC[11:0] should be ignored by error handling software.
23:22	RESERV0. Read-write. Reset: Cold,0h.
21:16	ErrorCodeExt. Read-write, Volatile. Reset: Cold,00h. Logs an extended error code when an error is detected. This model-specific field is used in conjunction with ErrorCode? to identify the error sub-type for root cause analysis.
15:0	ErrorCode. Read-write, Volatile. Reset: Cold,0000h. Error code for this error.

MSRC000_21[5...6]9 [UMC Deferred Error Address] (MCA::UMC::MCA_DEADDR_UMC)

Reset: Cold,0000_0000_0000_0000h.

The MCA::UMC::MCA_DEADDR_UMC register stores the address associated with the error in MCA::UMC::MCA_DESTAT_UMC. The register is only meaningful if MCA::UMC::MCA_DESTAT_UMC[Val]=1 and MCA::UMC::MCA_DESTAT_UMC[AddrV]=1. The lowest valid bit of the address is defined by MCA::UMC::MCA_DESTAT_UMC[AddrLsb].

_instUMCWPHY0UMC_n0_umc0_aliasMSR; MSRC000_2159

_instUMCWPHY1UMC_n1_umc0_aliasMSR; MSRC000_2169

Bits	Description
63:56	Reserved.
55:0	ErrorAddr. Read-write, Volatile. Reset: Cold,00_0000_0000_0000h. Contains the address, if any, associated with the error logged in MCA::UMC::MCA_DESTAT_UMC. The lowest-order valid bit of the address is specified in MCA::UMC::MCA_DESTAT_UMC[AddrLsb].

MSRC000_21[5...6]A [UMC Machine Check Miscellaneous 1] (MCA::UMC::MCA_MISC1_UMC)

Log miscellaneous information associated with errors, as defined by each error type.

_instUMCWPHY0UMC_n0_umc0_aliasMSR; MSRC000_215A

_instUMCWPHY1UMC_n1_umc0_aliasMSR; MSRC000_216A

Bits	Description
63	Valid. Reset: 1. 1=A valid CntP field is present in this register. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read-only.
62	CntP. Reset: 1. 1=A valid threshold counter is present. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read-only.
61	Locked. Reset: 0. 1=Writes to this register are ignored. This bit is set by BIOS to indicate that this register is not available for OS use. BIOS should set this bit if ThresholdIntType is set to SMI. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read-only.
60	IntP. Reset: 1. 1=ThresholdIntType can be used to generate interrupts. 0=ThresholdIntType and interrupt generation are not supported. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::UMC::MCA_MISC1_UMC[Locked]) ? Read-write : Read-only.
59:52	Reserved.
51	CntEn. Reset: 0. 1=Count thresholding errors. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::UMC::MCA_MISC1_UMC[Locked]) ? Read-write : Read-only.
50:49	ThresholdIntType. Reset: Cold,0h. Specifies the type of interrupt signaled when Ovrflw is set. 00b = No interrupt. 01b = APIC based interrupt (see Core::X86::Msr::McalntrCfg[ThresholdLvtOffset]) to all cores. 10b = SMI trigger event. 11b = Reserved. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::UMC::MCA_MISC1_UMC[Locked]) ? Read-write : Read-only.
48	Ovrflw. Reset: Cold,0. Set by hardware when ErrCnt transitions from FFEh to FFFh; also set by hardware if ErrCnt is initialized to FFFh and transitions from FFFh to 000h. When this field is set, ErrCnt no longer increments. When this bit is set, the interrupt selected by the ThresholdIntType field is generated. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::UMC::MCA_MISC1_UMC[Locked]) ? Read-write : Read-only.
47:44	Reserved.
43:32	ErrCnt. Reset: Cold,000h. This is written by software to set the starting value of the error counter. This is incremented by hardware when errors are logged. When this counter overflows, it stays at FFFh (no rollover). The threshold value, written by software, is (FFFh - the desired error count (the number of errors necessary in order for an interrupt to be taken)); the desired error count of 0 (a write value of FFFh) is not supported. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::UMC::MCA_MISC1_UMC[Locked]) ? Read-write : Read-only.
31:24	BlkPtr. Read-write. Reset: 01h. 00h=Extended MISC MSR block is not valid. 01h=Extended MSR block is valid.
23:0	Reserved.

MSRC001_041[5...6] [UMC Machine Check Control Mask] (MCA::UMC::MCA_CTL_MASK_UMC)

Read-write. Reset: 0000_0000_0000_0000h.	
Inhibit detection of an error source.	
_instUMCWPHY0UMC_n0_umc0_aliasMSR; MSRC001_0415	
_instUMCWPHY1UMC_n1_umc0_aliasMSR; MSRC001_0416	
Bits	Description
63:12	Reserved.
11	RdCrcErr. Read-write. Reset: 0. Read CRC error. CRC error occurred on a DRAM read from any subchannel
10	ThrttlErr. Read-write. Reset: 0. Indicates that UMC is throttling
9	EcsErr. Read-write. Reset: 0. ECS Error. Indicates that a device exceeded the ECS Error Threshold Count.
8	EcsRowErr. Read-write. Reset: 0. ECS Row Error. Indicates that a single device row exceeded four code word errors.
7	AesSramEccErr. Read-write. Reset: 0. AES SRAM ECC error. An ECC error occurred on a AES SRAM in the processor.
6	DcqSramEccErr. Read-write. Reset: 0. DCQ SRAM ECC error. An ECC error occurred on a DCQ SRAM in the processor.
5	WriteDataCrcErr. Read-write. Reset: 0. Write data CRC error. A write data CRC error occurred on the DRAM data bus.
4	AddressCommandParityErr. Read-write. Reset: 0. Address/Command parity error. A parity error occurred on the DRAM address/command bus.
3	ApbErr. Read-write. Reset: 0. Advanced peripheral bus error. An error occurred on the advanced peripheral bus.
2	SdpParityErr. Read-write. Reset: 0. SDP parity error. A parity error was detected on write data from the data fabric in the processor.
1	WriteDataPoisonErr. Read-write. Reset: 0. Data poison error. The system tried to write poison data to DRAM and either DRAM does not support ECC or UMC_CH.EccCtrl.WrEccEn is cleared.
0	DramEccErr. Read-write. Reset: 0. DRAM ECC error. An ECC error occurred on a DRAM read.

3.2.5.11 PB**MSR0000_0440...MSRC000_2100 [PB Machine Check Control] (MCA::PB::MCA_CTL_PB)**

Read-write. Reset: 0000_0000_0000_0000h.	
0=Disables error reporting for the corresponding error. 1=Enables error reporting via machine check exception for the corresponding error. The MCA::PB::MCA_CTL_PB register must be enabled by the corresponding enable bit in Core::X86::Msr::MCG_CTL. Does not affect error detection, correction, or logging.	
_ccd[1:0]_instPBCCD_n[1:0]_aliasMSRLEGACY; MSR0000_0440	
_ccd[1:0]_instPBCCD_n[1:0]_aliasMSR; MSRC000_2100	
Bits	Description
63:1	Reserved.
0	EccError. Read-write. Reset: 0. An ECC error in the Parameter Block RAM array.

MSR0000_0441...MSRC000_2101 [PB Machine Check Status] (MCA::PB::MCA_STATUS_PB)

Reset: Cold,0000_0000_0000_0000h.

Logs information associated with errors.

_ccd[1:0]_instPBCCD_n[1:0]_aliasMSRLEGACY; MSR0000_0441

_ccd[1:0]_instPBCCD_n[1:0]_aliasMSR; MSRC000_2101

Bits	Description
63	Val. Reset: Cold,0. 1=A valid error has been detected. This bit should be cleared by software after the register has been read. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
62	Overflow. Reset: Cold,0. 1=An error was detected while the valid bit (Val) was set; at least one error was not logged. Overflow is set independently of whether the existing error is overwritten. See 3.1.3 [Machine Check Errors]. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
61	UC. Reset: Cold,0. 1=The error was not corrected by hardware. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
60	En. Reset: Cold,0. 1=MCA error reporting is enabled for this error, as indicated by the corresponding bit in MCA::PB::MCA_CTL_PB. This bit is a copy of bit in MCA::PB::MCA_CTL_PB for this error. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
59	MiscV. Reset: Cold,0. 1=Valid thresholding in MCA::PB::MCA_MISC0_PB. In certain modes, MISC registers are owned by platform firmware and will RAZ when read by non-SMM code. Therefore, it is possible for MiscV=1 and the MISC register to read as all zeros. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
58	AddrV. Reset: Cold,0. 1=MCA::PB::MCA_ADDR_PB contains address information associated with the error. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
57	PCC. Reset: Cold,0. 1=Hardware context held by the processor may have been corrupted. Continued operation of the system may have unpredictable results. The error is not recoverable or survivable, and the system should be reinitialized. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
56	ErrCoreIdVal. Reset: Cold,0. 1=The ErrCoreId field is valid. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
55	TCC. Reset: Cold,0. 1=Hardware context of the process thread to which the error was reported may have been corrupted. Continued operation of the thread may have unpredictable results. The thread must be terminated. Only meaningful when MCA::PB::MCA_STATUS_PB[PCC]=0. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
54	RESERV54. Reset: Cold,0. MCA_STATUS Register Reserved bit. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
53	SyndV. Reset: Cold,0. 1=This error logged information in MCA::PB::MCA_SYND_PB. If MCA::PB::MCA_SYND_PB[ErrorPriority] is the same as the priority of the error in MCA::PB::MCA_STATUS_PB, then the information in MCA::PB::MCA_SYND_PB is associated with the error in MCA::PB::MCA_STATUS_PB. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
52	Reserved.
51:47	RESERV47. Reset: Cold,00h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
46	CECC. Reset: Cold,0. 1=The error was a correctable ECC error according to the restrictions of the ECC algorithm. UC indicates whether the error was actually corrected by the processor. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
45	UECC. Reset: Cold,0. 1=The error was an uncorrectable ECC error according to the restrictions of the ECC algorithm. UC indicates whether the error was actually corrected by the processor. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.

44	Deferred. Reset: Cold,0. 1=A deferred error was created. A deferred error is the result of an uncorrectable data error which did not immediately cause a processor exception; an exception is deferred until the erroneous data is consumed. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
43	Poison. Reset: Cold,0. 1=The error was the result of attempting to consume poisoned data. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
42:41	RESERV41. Reset: Cold,0h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
40	Scrub. Reset: Cold,0. 1=The error was the result of a scrub operation. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
39:38	RESERV38. Reset: Cold,0h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
37:32	ErrCoreId. Reset: Cold,00h. When ErrCoreIdVal=1 this field indicates which core within the processor is associated with the error; Otherwise this field is reserved. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
31:30	RESERV30. Reset: Cold,0h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
29:24	AddrLsb. Reset: Cold,00h. Specifies the least significant valid bit of the address contained in MCA::PB::MCA_ADDR_PB[ErrorAddr]. A value of 0 indicates that MCA::PB::MCA_ADDR_PB[55:0] contains a valid byte address. A value of 6 indicates that MCA::PB::MCA_ADDR_PB[55:6] contains a valid cache line address and that MCA::PB::MCA_ADDR_PB[5:0] are not part of the address and should be ignored by error handling software. A value of 12 indicates that MCA::PB::MCA_ADDR_PB[55:12] contain a valid 4KB memory page and that MCA::PB::MCA_ADDR_PB[11:0] should be ignored by error handling software. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
23:22	RESERV22. Reset: Cold,0h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
21:16	ErrorCodeExt. Reset: Cold,00h. Extended Error Code. This field is used to identify the error type for root cause analysis. This field indicates which bit position in MCA::PB::MCA_CTL_PB enables error reporting for the logged error. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
15:0	ErrorCode. Reset: Cold,0000h. Error code for this error. See 3.1.3.3 [Error Codes] for details on decoding this field. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.

Table 67: MCA_STATUS_PB

Error Type	ErrorCode Ext	UC	PCC	TCC	Deferred	Poison	AddrV
EccError	0x0	0/1	0/1	0/1	0	0	0

MSR0000_0442...MSRC000_2102 [PB Machine Check Address] (MCA::PB::MCA_ADDR_PB)

Read-only. Reset: Cold,0000_0000_0000_0000h.

MCA::PB::MCA_ADDR_PB stores an address and other information associated with the error in MCA::PB::MCA_STATUS_PB. The register is only meaningful if MCA::PB::MCA_STATUS_PB[Val]=1 and MCA::PB::MCA_STATUS_PB[AddrV]=1.

_ccd[1:0]_instPBCCD_n[1:0]_aliasMSRLEGACY; MSR0000_0442

_ccd[1:0]_instPBCCD_n[1:0]_aliasMSR; MSRC000_2102

Bits	Description
63:0	ErrorAddr. Read-only. Reset: Cold,0000_0000_0000_0000h. Contains the address, if any, associated with the error logged in MCA::PB::MCA_STATUS_PB.

Table 68: MCA_ADDR_PB

Error Type	Bits	Description
EccError	[56:0]	Reserved

MSR0000_0443...MSRC000_2103 [PB Machine Check Miscellaneous 0] (MCA::PB::MCA_MISC0_PB)	
Log miscellaneous information associated with errors.	
_ccd[1:0]_instPBCCD_n[1:0]_aliasMSRLEGACY; MSR0000_0443	
_ccd[1:0]_instPBCCD_n[1:0]_aliasMSR; MSRC000_2103	
Bits	Description
63	Valid. Reset: 1. 1=A valid CntP field is present in this register. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read-only.
62	CntP. Reset: 1. 1=A valid threshold counter is present. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read-only.
61	Locked. Reset: 0. 1=Writes to this register are ignored. This bit is set by BIOS to indicate that this register is not available for OS use. BIOS should set this bit if ThresholdIntType is set to SMI. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read-only.
60	IntP. Reset: 1. 1=ThresholdIntType can be used to generate interrupts. 0=ThresholdIntType and interrupt generation are not supported. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::PB::MCA_MISC0_PB[Locked]) ? Read-write : Read-only.
59:56	Reserved.
55:52	LvtOffset. Reset: 0h. One per die. For error thresholding interrupts, specifies the address of the LVT entry in the APIC registers as follows: LVT address = (LvtOffset shifted left 4 bits) + 500h (see Core::X86::Apic::ExtendedInterruptLvtEntries). AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::PB::MCA_MISC0_PB[Locked]) ? Read-write : Read-only.
51	CntEn. Reset: 0. 1=Count thresholding errors. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::PB::MCA_MISC0_PB[Locked]) ? Read-write : Read-only.
50:49	ThresholdIntType. Reset: Cold,0h. Specifies the type of interrupt signaled when Ovrflw is set and IntP==1. 00b = No interrupt. 01b = APIC based interrupt (see Core::X86::Msr::McaIntrCfg[ThresholdLvtOffset]). 10b = SMI trigger event. 11b = Reserved. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::PB::MCA_MISC0_PB[Locked]) ? Read-write : Read-only.
48	Ovrflw. Reset: Cold,0. Set by hardware when ErrCnt transitions from FFEh to FFFh. When this field is set, ErrCnt no longer increments. When this bit is set, the interrupt selected by the ThresholdIntType field is generated. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::PB::MCA_MISC0_PB[Locked]) ? Read-write : Read-only.
47:44	Reserved.
43:32	ErrCnt. Reset: Cold,000h. This is written by software to set the starting value of the error counter. This is incremented by hardware when errors are logged. When this counter overflows, it stays at FFFh (no rollover). The threshold value, written by software, is (FFFh - the desired error count (the number of errors necessary in order for an interrupt to be taken)); the desired error count of 0 (a write value of FFFh) is not supported. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::PB::MCA_MISC0_PB[Locked]) ? Read-write : Read-only.
31:24	BlkPtr. Read-write. Reset: 00h. 00h=Extended MISC MSR block is not valid. 01h=Extended MSR block is valid.
23:0	Reserved.

MSRC000_2104 [PB Machine Check Configuration] (MCA::PB::MCA_CONFIG_PB)

Reset: 0000_0000_0000_0121h.

Controls configuration of the associated machine check bank.

_ccd[1:0]_instPBCCD_n[1:0]_aliasMSR; MSRC000_2104

Bits	Description
63:39	Reserved.
38:37	DeferredIntType. Read-write. Reset: 0h. Specifies the type of interrupt signaled when a deferred error is logged. 00b = No interrupt. 01b = APIC based interrupt (see Core::X86::Msr::McaIntrCfg[DeferredLvtOffset]). 10b = SMI trigger event. 11b = Reserved.
36:33	Reserved.
32	McaXEnable. Read-write. Reset: 0. Init: BIOS,1. Check: 1. 1=Software has acknowledged support for the MCAX feature set. 0=Software has not acknowledged support for the MCAX feature set. All uncorrected and fatal errors will cause an ErrorEvent packet to be generated. Deferred error interrupts are configured via Core::X86::Msr::McaIntrCfg.
31:9	Reserved.
8	McaLsbInStatusSupported. Read-only. Reset: 1. 1=MCA::PB::MCA_CONFIG_PB[McaLsbInStatusSupported] indicates that AddrLsb is located in McaStatus registers.
7:6	Reserved.
5	DeferredIntTypeSupported. Read-only. Reset: 1. 1=MCA::PB::MCA_CONFIG_PB[DeferredIntType] controls the type of interrupt generated on a deferred error. Deferred errors are supported in this bank only if MCA::PB::MCA_CONFIG_PB[DeferredErrorLoggingSupported]=1.
4:3	Reserved.
2	DeferredErrorLoggingSupported. Read-only. Reset: 0. 1=Deferred errors are supported in this MCA bank, and the LogDeferredInMcaStat field in this register controls the logging behavior of these errors. MCA_DESTAT and MCA_DEADDR are supported in this MCA bank. 0=Deferred errors are not supported in this bank.
1	Reserved.
0	McaX. Read-only. Reset: 1. 1=This bank provides Machine Check Architecture Extensions. Up to 4 additional MISC registers (MISC1-MISC4) are supported. MCA::PB::MCA_MISC0_PB[BlkPtr] indicates the presence of the additional MISC registers, but is not used to determine their MSR numbers. Deferred error interrupt type is specifiable by MCA bank. MCA::PB::MCA_STATUS_PB[TCC] is present.

MSRC000_2105 [PB IP Identification] (MCA::PB::MCA_IPID_PB)

Reset: 0000_0005_0000_0000h.

The MCA::PB::MCA_IPID_PB register is used by software to determine what IP type and revision is associated with the MCA bank.

_ccd[1:0]_instPBCCD_n[1:0]_aliasMSR; MSRC000_2105

Bits	Description
63:48	McaType. Read-only. Reset: 0000h. The McaType of the MCA bank within this IP.
47:44	InstanceIdHi. Read-write. Reset: 0h. The HI value instance ID of this IP. This is initialized to a unique ID per instance of this register.
43:32	HardwareID. Read-only. Reset: 005h. The Hardware ID of the IP associated with this MCA bank.
31:0	InstanceId. Read-write. Reset: 0000_0000h. The instance ID of this IP. This is initialized to a unique ID per instance of this register.
	Init: _ccd0_instPBCCD_n0_aliasMSR: 3008_2900h
	Init: _ccd1_instPBCCD_n1_aliasMSR: 3208_2900h

MSRC000_2106 [PB Machine Check Syndrome] (MCA::PB::MCA_SYND_PB)	
Read-write, Volatile. Reset: Cold, 0000_0000_0000_0000h.	
Logs physical location information associated with error in MCA::PB::MCA_STATUS_PB Thread 0	
_ccd[1:0]_instPBCCD_n[1:0]_aliasMSR; MSRC000_2106	
Bits	Description
63:32	Syndrone. Read-write, Volatile. Reset: Cold, 0000_0000h. Contains the syndrome, if any, associated with the error logged in MCA::PB::MCA_STATUS_PB. The low-order bit of the syndrome is stored in bit 0, and the syndrome has a length specified by MCA::PB::MCA_SYND_PB[Length]. The Syndrome field is only valid when MCA::PB::MCA_SYND_PB[Length] is not 0.
31:27	Reserved.
26:24	ErrorPriority. Read-write, Volatile. Reset: Cold, 0h. Encodes the priority of the error logged in MCA::PB::MCA_SYND_PB. 3'b000 = No error; 3'b001 = Reserved; 3'b010 = Corrected Error; 3'b011 = Deferred Error; 3'b100 = Uncorrected Error; 3'b101 = Fatal Error; all others reserved.
23:18	Length. Read-write, Volatile. Reset: Cold, 00h. Specifies the length in bits of the syndrome contained in MCA::PB::MCA_SYND_PB[Syndrome]. A value of 0 indicates that there is no valid syndrome in MCA::PB::MCA_SYND_PB. For example, a syndrome length of 9 means that MCA::PB::MCA_SYND_PB[Syndrome] bits [8:0] contains a valid syndrome.
17:0	ErrorInformation. Read-write, Volatile. Reset: Cold, 0_0000h. Contains error-specific information about the location of the error. Decoding is available in Table 69 [MCA_SYND_PB].

Table 69: MCA_SYND_PB

Error Type	Bits	Description
EccError	[8]	DEDB error
	[7:4]	Reserved
	[3:0]	IntReqVal

MSRC001_0410 [PB Machine Check Control Mask] (MCA::PB::MCA_CTL_MASK_PB)	
Read-write. Reset: 0000_0000_0000_0000h.	
Inhibit detection of an error source.	
_ccd[1:0]_instPBCCD_n[1:0]_aliasMSR; MSRC001_0410	
Bits	Description
63:1	Reserved.
0	EccError. Read-write. Reset: 0. An ECC error in the Parameter Block RAM array.

3.2.5.12 MP5

MSR0000_043C...MSRC000_20F0 (MCA::MP5::MCA_CTL_MP5)

Read-write. Reset: 0000_0000_0000_0000h.

_ccd[1:0]_instMP5MP5_n[1:0]_aliasMSRLEGACY; MSR0000_043C

_ccd[1:0]_instMP5MP5_n[1:0]_aliasMSR; MSRC000_20F0

Bits	Description
63:10	Reserved.
9	Mp5ITagBError. Read-write. Reset: 0. Instruction Tag Cache Bank B ECC or parity error.
8	Mp5ITagAError. Read-write. Reset: 0. Instruction Tag Cache Bank A ECC or parity error.
7	Mp5ICacheBError. Read-write. Reset: 0. Instruction Cache Bank B ECC or parity error.
6	Mp5ICacheAError. Read-write. Reset: 0. Instruction Cache Bank A ECC or parity error.
5	Mp5DTagBError. Read-write. Reset: 0. Data Tag Cache Bank B ECC or parity error.
4	Mp5DTagAError. Read-write. Reset: 0. Data Tag Cache Bank A ECC or parity error.
3	Mp5DCacheBError. Read-write. Reset: 0. Data Cache Bank B ECC or parity error.
2	Mp5DCacheAError. Read-write. Reset: 0. Data Cache Bank A ECC or parity error.
1	Mp5LowSramError. Read-write. Reset: 0. Low SRAM ECC or parity error.
0	Mp5HighSramError. Read-write. Reset: 0. High SRAM ECC or parity error.

MSR0000_043D...MSRC000_20F1 [MP5 Machine Check Status] (MCA::MP5::MCA_STATUS_MP5)

Reset: Cold,0000_0000_0000_0000h.

Logs information associated with errors.

_ccd[1:0]_instMP5MP5_n[1:0]_aliasMSRLEGACY; MSR0000_043D

_ccd[1:0]_instMP5MP5_n[1:0]_aliasMSR; MSRC000_20F1

Bits	Description
63	Val. Reset: Cold,0. 1=A valid error has been detected. This bit should be cleared by software after the register has been read. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
62	Overflow. Reset: Cold,0. 1=An error was detected while the valid bit (Val) was set; at least one error was not logged. Overflow is set independently of whether the existing error is overwritten. See 3.1.3 [Machine Check Errors]. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
61	UC. Reset: Cold,0. 1=The error was not corrected by hardware. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
60	En. Reset: Cold,0. 1=MCA error reporting is enabled for this error, as indicated by the corresponding bit in MCA::MP5::MCA_CTL_MP5. This bit is a copy of bit in MCA::MP5::MCA_CTL_MP5 for this error. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
59	MiscV. Reset: Cold,0. 1=Valid thresholding in MCA::MP5::MCA_MISC0_MP5. In certain modes, MISC registers are owned by platform firmware and will RAZ when read by non-SMM code. Therefore, it is possible for MiscV=1 and the MISC register to read as all zeros. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
58	AddrV. Reset: Cold,0. 1=MCA::MP5::MCA_ADDR_MP5 contains address information associated with the error. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
57	PCC. Reset: Cold,0. 1=Hardware context held by the processor may have been corrupted. Continued operation of the system may have unpredictable results. The error is not recoverable or survivable, and the system should be reinitialized. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
56	ErrCoreIdVal. Reset: Cold,0. 1=The ErrCoreId field is valid. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
55	TCC. Reset: Cold,0. 1=Hardware context of the process thread to which the error was reported may have been corrupted. Continued operation of the thread may have unpredictable results. The thread must be terminated. Only meaningful when MCA::MP5::MCA_STATUS_MP5[PCC]=0. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
54	RESERV54. Reset: Cold,0. MCA_STATUS Register Reserved bit. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
53	SyndV. Reset: Cold,0. 1=This error logged information in MCA::MP5::MCA_SYND_MP5. If MCA::MP5::MCA_SYND_MP5[ErrorPriority] is the same as the priority of the error in MCA::MP5::MCA_STATUS_MP5, then the information in MCA::MP5::MCA_SYND_MP5 is associated with the error in MCA::MP5::MCA_STATUS_MP5. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
52	Reserved.
51:47	RESERV47. Reset: Cold,00h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
46	CECC. Reset: Cold,0. 1=The error was a correctable ECC error according to the restrictions of the ECC algorithm. UC indicates whether the error was actually corrected by the processor. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
45	UECC. Reset: Cold,0. 1=The error was an uncorrectable ECC error according to the restrictions of the ECC algorithm. UC indicates whether the error was actually corrected by the processor.

	AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
44	Deferred. Reset: Cold,0. 1=A deferred error was created. A deferred error is the result of an uncorrectable data error which did not immediately cause a processor exception; an exception is deferred until the erroneous data is consumed.
	AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
43	Poison. Reset: Cold,0. 1=The error was the result of attempting to consume poisoned data.
	AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
42:41	RESERV41. Reset: Cold,0h. MCA_STATUS Register Reserved bits.
	AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
40	Scrub. Reset: Cold,0. 1=The error was the result of a scrub operation.
	AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
39:38	RESERV38. Reset: Cold,0h. MCA_STATUS Register Reserved bits.
	AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
37:32	ErrCoreId. Reset: Cold,00h. When ErrCoreIdVal=1 this field indicates which core within the processor is associated with the error; Otherwise this field is reserved.
	AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
31:30	RESERV30. Reset: Cold,0h. MCA_STATUS Register Reserved bits.
	AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
29:24	AddrLsb. Reset: Cold,00h. Specifies the least significant valid bit of the address contained in MCA::MP5::MCA_ADDR_MP5[ErrorAddr]. A value of 0 indicates that MCA::MP5::MCA_ADDR_MP5[55:0] contains a valid byte address. A value of 6 indicates that MCA::MP5::MCA_ADDR_MP5[55:6] contains a valid cache line address and that MCA::MP5::MCA_ADDR_MP5[5:0] are not part of the address and should be ignored by error handling software. A value of 12 indicates that MCA::MP5::MCA_ADDR_MP5[55:12] contain a valid 4KB memory page and that MCA::MP5::MCA_ADDR_MP5[11:0] should be ignored by error handling software.
	AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
23:22	RESERV22. Reset: Cold,0h. MCA_STATUS Register Reserved bits.
	AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
21:16	ErrorCodeExt. Reset: Cold,00h. Extended Error Code. This field is used to identify the error type for root cause analysis. This field indicates which bit position in MCA::MP5::MCA_CTL_MP5 enables error reporting for the logged error.
	AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
15:0	ErrorCode. Reset: Cold,0000h. Error code for this error. See 3.1.3.3 [Error Codes] for details on decoding this field.
	AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.

Table 70: MCA_STATUS_MP5

Error Type	ErrorCode Ext	UC	PCC	TCC	Deferred	Poison	AddrV
Mp5HighSramError	0x0	0/1	0/1	0/1	0	0	1
Mp5LowSramError	0x1	0/1	0/1	0/1	0	0	1
Mp5DCacheAError	0x2	0/1	0/1	0/1	0	0	1
Mp5DCacheBError	0x3	0/1	0/1	0/1	0	0	1
Mp5DTagAError	0x4	0/1	0/1	0/1	0	0	1
Mp5DTagB	0x5	0/1	0/1	0/1	0	0	1

Error							
Mp5ICache AError	0x6	0/1	0/1	0/1	0	0	1
Mp5ICache BError	0x7	0/1	0/1	0/1	0	0	1
Mp5ITagAE rror	0x8	0/1	0/1	0/1	0	0	1
Mp5ITagBEr ror	0x9	0/1	0/1	0/1	0	0	1

MSR0000_043E...MSRC000_20F2 [MP5 Machine Check Address] (MCA::MP5::MCA_ADDR_MP5)

Reset: Cold,0000_0000_0000_0000h.

MCA::MP5::MCA_ADDR_MP5 stores an address and other information associated with the error in MCA::MP5::MCA_STATUS_MP5. The register is only meaningful if MCA::MP5::MCA_STATUS_MP5[Val]=1 and MCA::MP5::MCA_STATUS_MP5[AddrV]=1.

_ccd[1:0]_instMP5MP5_n[1:0]_aliasMSRLEGACY; MSR0000_043E

_ccd[1:0]_instMP5MP5_n[1:0]_aliasMSR; MSRC000_20F2

Bits	Description
63:56	Reserved.
55:0	ErrorAddr. Read-write, Volatile. Reset: Cold,00_0000_0000_0000h. Unless otherwise specified by an error, contains the address associated with the error logged in MCA::MP5::MCA_STATUS_MP5. For physical addresses, the most significant bit is given by Core::X86::CpuId::LongModeInfo[PhysAddrSize].

Table 71: MCA_ADDR_MP5

Error Type	Bits	Description
Mp5HighSramError	[55:0]	Reserved
Mp5LowSramError	[55:0]	Reserved
Mp5DCacheAError	[55:0]	Reserved
Mp5DCacheBError	[55:0]	Reserved
Mp5DTagAError	[55:0]	Reserved
Mp5DTagBError	[55:0]	Reserved
Mp5ICacheAError	[55:0]	Reserved
Mp5ICacheBError	[55:0]	Reserved
Mp5ITagAError	[55:0]	Reserved
Mp5ITagBError	[55:0]	Reserved

MSR0000_043F...MSRC000_20F3 [MP5 Machine Check Miscellaneous 0] (MCA::MP5::MCA_MISC0_MP5)

Log miscellaneous information associated with errors.

_ccd[1:0]_instMP5MP5_n[1:0]_aliasMSRLEGACY; MSR0000_043F

_ccd[1:0]_instMP5MP5_n[1:0]_aliasMSR; MSRC000_20F3

Bits	Description
63	Valid. Reset: 1. 1=A valid CntP field is present in this register. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read-only.
62	CntP. Reset: 1. 1=A valid threshold counter is present. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read-only.
61	Locked. Reset: 0. 1=Writes to this register are ignored. This bit is set by BIOS to indicate that this register is not available for OS use. BIOS should set this bit if ThresholdIntType is set to SMI. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read-only.
60	IntP. Reset: 1. 1=ThresholdIntType can be used to generate interrupts. 0=ThresholdIntType and interrupt generation are not supported. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::MP5::MCA_MISC0_MP5[Locked]) ? Read-write : Read-only.
59:56	Reserved.
55:52	LvtOffset. Reset: 0h. One per die. For error thresholding interrupts, specifies the address of the LVT entry in the APIC registers as follows: LVT address = (LvtOffset shifted left 4 bits) + 500h (see Core::X86::Apic::ExtendedInterruptLvtEntries). AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::MP5::MCA_MISC0_MP5[Locked]) ? Read-write : Read-only.
51	CntEn. Reset: 0. 1=Count thresholding errors. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::MP5::MCA_MISC0_MP5[Locked]) ? Read-write : Read-only.
50:49	ThresholdIntType. Reset: Cold,0h. Specifies the type of interrupt signaled when Ovrlw is set and IntP==1. 00b = No interrupt. 01b = APIC based interrupt (see Core::X86::Msr::McaIntrCfg[ThresholdLvtOffset]). 10b = SMI trigger event. 11b = Reserved. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::MP5::MCA_MISC0_MP5[Locked]) ? Read-write : Read-only.
48	Ovrlw. Reset: Cold,0. Set by hardware when ErrCnt transitions from FFEh to FFFh. When this field is set, ErrCnt no longer increments. When this bit is set, the interrupt selected by the ThresholdIntType field is generated. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::MP5::MCA_MISC0_MP5[Locked]) ? Read-write : Read-only.
47:44	Reserved.
43:32	ErrCnt. Reset: Cold,000h. This is written by software to set the starting value of the error counter. This is incremented by hardware when errors are logged. When this counter overflows, it stays at FFFh (no rollover). The threshold value, written by software, is (FFFh - the desired error count (the number of errors necessary in order for an interrupt to be taken)); the desired error count of 0 (a write value of FFFh) is not supported. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::MP5::MCA_MISC0_MP5[Locked]) ? Read-write : Read-only.
31:24	BlkPtr. Read-write. Reset: 00h. 00h=Extended MISC MSR block is not valid. 01h=Extended MSR block is valid.
23:0	Reserved.

MSRC000_20F4 [MP5 Machine Check Configuration] (MCA::MP5::MCA_CONFIG_MP5)

Reset: 0000_0000_0000_0121h.

Controls configuration of the associated machine check bank.

_ccd[1:0]_instMP5MP5_n[1:0]_aliasMSR; MSRC000_20F4

Bits	Description
63:39	Reserved.
38:37	DeferredIntType. Read-write. Reset: 0h. Specifies the type of interrupt signaled when a deferred error is logged. 00b = No interrupt. 01b = APIC based interrupt (see Core::X86::Msr::McaIntrCfg[DeferredLvtOffset]). 10b = SMI trigger event. 11b = Reserved.
36:33	Reserved.
32	McaXEnable. Read-write. Reset: 0. Init: BIOS,1. Check: 1. 1=Software has acknowledged support for the MCAX feature set. 0=Software has not acknowledged support for the MCAX feature set. All uncorrected and fatal errors will cause an ErrorEvent packet to be generated. Deferred error interrupts are configured via Core::X86::Msr::McaIntrCfg.
31:9	Reserved.
8	McaLsbInStatusSupported. Read-only. Reset: 1. 1=MCA::MP5::MCA_CONFIG_MP5[McaLsbInStatusSupported] indicates that AddrLsb is located in McaStatus registers.
7:6	Reserved.
5	DeferredIntTypeSupported. Read-only. Reset: 1. 1=MCA::MP5::MCA_CONFIG_MP5[DeferredIntType] controls the type of interrupt generated on a deferred error. Deferred errors are supported in this bank only if MCA::MP5::MCA_CONFIG_MP5[DeferredErrorLoggingSupported]=1.
4:3	Reserved.
2	DeferredErrorLoggingSupported. Read-only. Reset: 0. 1=Deferred errors are supported in this MCA bank, and the LogDeferredInMcaStat field in this register controls the logging behavior of these errors. MCA_DESTAT and MCA_DEADDR are supported in this MCA bank. 0=Deferred errors are not supported in this bank.
1	Reserved.
0	McaX. Read-only. Reset: 1. 1=This bank provides Machine Check Architecture Extensions. Up to 4 additional MISC registers (MISC1-MISC4) are supported. MCA::MP5::MCA_MISC0_MP5[BlkPtr] indicates the presence of the additional MISC registers, but is not used to determine their MSR numbers. Deferred error interrupt type is specifiable by MCA bank. MCA::MP5::MCA_STATUS_MP5[TCC] is present.

MSRC000_20F5 [MP5 IP Identification] (MCA::MP5::MCA_IPID_MP5)

Reset: 0002_0001_0000_0000h.

The MCA::MP5::MCA_IPID_MP5 register is used by software to determine what IP type and revision is associated with the MCA bank.

_ccd[1:0]_instMP5MP5_n[1:0]_aliasMSR; MSRC000_20F5

Bits	Description
63:48	McaType. Read-only. Reset: 0002h. The McaType of the MCA bank within this IP.
47:44	InstanceIdHi. Read-write. Reset: 0h. The HI value instance ID of this IP. This is initialized to a unique ID per instance of this register.
43:32	HardwareID. Read-only. Reset: 001h. The Hardware ID of the IP associated with this MCA bank.
31:0	InstanceId. Read-write. Reset: 0000_0000h. The instance ID of this IP. This is initialized to a unique ID per instance of this register.
	Init: _ccd0_instMP5MP5_n0_aliasMSR: 3043_0400h
	Init: _ccd1_instMP5MP5_n1_aliasMSR: 3243_0400h

MSRC000_20F6 [MP5 Machine Check Syndrome] (MCA::MP5::MCA_SYND_MP5)	
Read-write, Volatile. Reset: Cold, 0000_0000_0000_0000h.	
Logs physical location information associated with error in MCA::MP5::MCA_STATUS_MP5 Thread 0	
_ccd[1:0]_instMP5MP5_n[1:0]_aliasMSR; MSRC000_20F6	
Bits	Description
63:33	Reserved.
32	Syndrom . Read-write, Volatile. Reset: Cold, 0. Contains the syndrome, if any, associated with the error logged in MCA::MP5::MCA_STATUS_MP5. The low-order bit of the syndrome is stored in bit 0, and the syndrome has a length specified by MCA::MP5::MCA_SYND_MP5[Length]. The Syndrome field is only valid when MCA::MP5::MCA_SYND_MP5[Length] is not 0.
31:27	Reserved.
26:24	ErrorPriority . Read-write, Volatile. Reset: Cold, 0h. Encodes the priority of the error logged in MCA::MP5::MCA_SYND_MP5. 3'b000 = No error; 3'b001 = Reserved; 3'b010 = Corrected Error; 3'b011 = Deferred Error; 3'b100 = Uncorrected Error; 3'b101 = Fatal Error; all others reserved.
23:18	Length . Read-write, Volatile. Reset: Cold, 00h. Specifies the length in bits of the syndrome contained in MCA::MP5::MCA_SYND_MP5[Syndrome]. A value of 0 indicates that there is no valid syndrome in MCA::MP5::MCA_SYND_MP5. For example, a syndrome length of 9 means that MCA::MP5::MCA_SYND_MP5[Syndrome] bits [8:0] contains a valid syndrome.
17:0	ErrorInformation . Read-write, Volatile. Reset: Cold, 0_0000h. Contains error-specific information about the location of the error. Decoding is available in Table 72 [MCA_SYND_MP5].

Table 72: MCA_SYND_MP5

Error Type	Bits	Description
Mp5HighSramError	[17:15]	Reserved
	[14:0]	Reserved
Mp5LowSramError	[17:15]	Reserved
	[14:0]	Reserved
Mp5DCacheAError	[17:8]	Reserved
	[7:0]	Reserved
Mp5DCacheBError	[17:8]	Reserved
	[7:0]	Reserved
Mp5DTagAError	[17:7]	Reserved
	[6:0]	Reserved
Mp5DTagBError	[17:7]	Reserved
	[6:0]	Reserved
Mp5ICacheAError	[17:8]	Reserved
	[7:0]	Reserved
Mp5ICacheBError	[17:8]	Reserved
	[7:0]	Reserved
Mp5ITagAError	[17:6]	Reserved
	[5:0]	Reserved
Mp5ITagBError	[17:6]	Reserved
	[5:0]	Reserved

MSRC001_040F [MP5 Machine Check Control Mask] (MCA::MP5::MCA_CTL_MASK_MP5)

Read-write. Reset: 0000_0000_0000_0000h.

Inhibit detection of an error source.

_ccd[1:0]_instMP5MP5_n[1:0]_aliasMSR; MSRC001_040F

Bits	Description
63:10	Reserved.
9	Mp5ITagBError. Read-write. Reset: 0. Instruction Tag Cache Bank B ECC or parity error.
8	Mp5ITagAError. Read-write. Reset: 0. Instruction Tag Cache Bank A ECC or parity error.
7	Mp5ICacheBError. Read-write. Reset: 0. Instruction Cache Bank B ECC or parity error.
6	Mp5ICacheAError. Read-write. Reset: 0. Instruction Cache Bank A ECC or parity error.
5	Mp5DTagBError. Read-write. Reset: 0. Data Tag Cache Bank B ECC or parity error.
4	Mp5DTagAError. Read-write. Reset: 0. Data Tag Cache Bank A ECC or parity error.
3	Mp5DCacheBError. Read-write. Reset: 0. Data Cache Bank B ECC or parity error.
2	Mp5DCacheAError. Read-write. Reset: 0. Data Cache Bank A ECC or parity error.
1	Mp5LowSramError. Read-write. Reset: 0. Low SRAM ECC or parity error.
0	Mp5HighSramError. Read-write. Reset: 0. High SRAM ECC or parity error.

3.2.5.13 NBIO**MSR0000_0464...MSRC000_2190 [NBIO Machine Check Control] (MCA::NBIO::MCA_CTL_NBIO)**

Read-write. Reset: 0000_0000_0000_0000h.

0=Disables error reporting for the corresponding error. 1=Enables error reporting via machine check exception for the corresponding error. The MCA::NBIO::MCA_CTL_NBIO register must be enabled by the corresponding enable bit in Core::X86::Msr::MCG_CTL. Does not affect error detection, correction, or logging.

_instIOHC_n0_aliasMSRLEGACY; MSR0000_0464

_instIOHC_n0_aliasMSR; MSRC000_2190

Bits	Description
63:6	Reserved.
5	Int_ErrEvent. Read-write. Reset: 0. Internal system fatal error event was detected.
4	IOHC_Internal_Poison. Read-write. Reset: 0. Internal Poison Error. Poison data was sent to an internal client.
3	Egress_Poison. Read-write. Reset: 0. SDP Egress Poison Error. Poison was propagated to an egress port.
2	Ext_ErrEvent. Read-write. Reset: 0. External SDP ErrEvent error. A system fatal error event from an SDP interface was detected.
1	PCIE_Sideband. Read-write. Reset: 0. PCIE error. A PCIe® error was logged in a PCIe® root port.
0	EccParityError. Read-write. Reset: 0. ECC or Parity error. An SRAM ECC or parity error was detected.

MSR0000_0465...MSRC000_2191 [NBIO Machine Check Status] (MCA::NBIO::MCA_STATUS_NBIO)

Reset: Cold,0000_0000_0000_0000h.

Logs information associated with errors.

_instIOHC_n0_aliasMSRLEGACY; MSR0000_0465

_instIOHC_n0_aliasMSR; MSRC000_2191

Bits	Description
63	Val. Reset: Cold,0. 1=A valid error has been detected. This bit should be cleared by software after the register has been read. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
62	Overflow. Reset: Cold,0. 1=An error was detected while the valid bit (Val) was set; at least one error was not logged. Overflow is set independently of whether the existing error is overwritten. See 3.1.3 [Machine Check Errors]. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
61	UC. Reset: Cold,0. 1=The error was not corrected by hardware. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
60	En. Reset: Cold,0. 1=MCA error reporting is enabled for this error, as indicated by the corresponding bit in MCA::NBIO::MCA_CTL_NBIO. This bit is a copy of bit in MCA::NBIO::MCA_CTL_NBIO for this error. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
59	MiscV. Reset: Cold,0. 1=Valid thresholding in MCA::NBIO::MCA_MISC0_NBIO. In certain modes, MISC registers are owned by platform firmware and will RAZ when read by non-SMM code. Therefore, it is possible for MiscV=1 and the MISC register to read as all zeros. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
58	AddrV. Reset: Cold,0. 1=MCA::NBIO::MCA_ADDR_NBIO contains address information associated with the error. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
57	PCC. Reset: Cold,0. 1=Hardware context held by the processor may have been corrupted. Continued operation of the system may have unpredictable results. The error is not recoverable or survivable, and the system should be reinitialized. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
56	ErrCoreIdVal. Reset: Cold,0. 1=The ErrCoreId field is valid. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
55	TCC. Reset: Cold,0. 1=Hardware context of the process thread to which the error was reported may have been corrupted. Continued operation of the thread may have unpredictable results. The thread must be terminated. Only meaningful when MCA::NBIO::MCA_STATUS_NBIO[PCC]=0. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
54	RESERV54. Reset: Cold,0. MCA_STATUS Register Reserved bit. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
53	SyndV. Reset: Cold,0. 1=This error logged information in MCA::NBIO::MCA_SYND_NBIO. If MCA::NBIO::MCA_SYND_NBIO[ErrorPriority] is the same as the priority of the error in MCA::NBIO::MCA_STATUS_NBIO, then the information in MCA::NBIO::MCA_SYND_NBIO is associated with the error in MCA::NBIO::MCA_STATUS_NBIO. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
52	Reserved.
51:47	RESERV47. Reset: Cold,00h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
46	CECC. Reset: Cold,0. 1=The error was a correctable ECC error according to the restrictions of the ECC algorithm. UC indicates whether the error was actually corrected by the processor. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
45	UECC. Reset: Cold,0. 1=The error was an uncorrectable ECC error according to the restrictions of the ECC algorithm. UC indicates whether the error was actually corrected by the processor.

	AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
44	Deferred. Reset: Cold,0. 1=A deferred error was created. A deferred error is the result of an uncorrectable data error which did not immediately cause a processor exception; an exception is deferred until the erroneous data is consumed.
	AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
43	Poison. Reset: Cold,0. 1=The error was the result of attempting to consume poisoned data.
	AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
42:41	RESERV41. Reset: Cold,0h. MCA_STATUS Register Reserved bits.
	AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
40	Scrub. Reset: Cold,0. 1=The error was the result of a scrub operation.
	AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
39:38	RESERV38. Reset: Cold,0h. MCA_STATUS Register Reserved bits.
	AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
37:32	ErrCoreId. Reset: Cold,00h. When ErrCoreIdVal=1 this field indicates which core within the processor is associated with the error; Otherwise this field is reserved.
	AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
31:30	RESERV30. Reset: Cold,0h. MCA_STATUS Register Reserved bits.
	AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
29:24	AddrLsb. Reset: Cold,00h. Specifies the least significant valid bit of the address contained in MCA::NBIO::MCA_ADDR_NBIO[ErrorAddr]. A value of 0 indicates that MCA::NBIO::MCA_ADDR_NBIO[55:0] contains a valid byte address. A value of 6 indicates that MCA::NBIO::MCA_ADDR_NBIO[55:6] contains a valid cache line address and that MCA::NBIO::MCA_ADDR_NBIO[5:0] are not part of the address and should be ignored by error handling software. A value of 12 indicates that MCA::NBIO::MCA_ADDR_NBIO[55:12] contain a valid 4KB memory page and that MCA::NBIO::MCA_ADDR_NBIO[11:0] should be ignored by error handling software.
	AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
23:22	RESERV22. Reset: Cold,0h. MCA_STATUS Register Reserved bits.
	AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
21:16	ErrorCodeExt. Reset: Cold,00h. Extended Error Code. This field is used to identify the error type for root cause analysis. This field indicates which bit position in MCA::NBIO::MCA_CTL_NBIO enables error reporting for the logged error.
	AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
15:0	ErrorCode. Reset: Cold,0000h. Error code for this error. See 3.1.3.3 [Error Codes] for details on decoding this field.
	AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.

Table 73: MCA_STATUS_NBIO

Error Type	ErrorCode Ext	UC	PCC	TCC	Deferred	Poison	AddrV
EccParityError	0x0	0/1	0/1	0/1	0/1	0	0
PCIE_Sideband	0x1	0/1	0/1	0/1	0/1	0	0
Ext_ErrEvent	0x2	1	1	1	0	0	0
Egress_Poison	0x3	0/1	0/1	0/1	0/1	0	0
IOHC_Internal_Poison	0x4	1	1	1	0	0	0
Int_ErrEvent	0x5	1	1	1	0	0	0

MSR0000_0466...MSRC000_2192 [NBIO Machine Check Address] (MCA::NBIO::MCA_ADDR_NBIO)

Read-only. Reset: Cold,0000_0000_0000_0000h.

MCA::NBIO::MCA_ADDR_NBIO stores an address and other information associated with the error in MCA::NBIO::MCA_STATUS_NBIO. The register is only meaningful if MCA::NBIO::MCA_STATUS_NBIO[Val]=1 and MCA::NBIO::MCA_STATUS_NBIO[AddrV]=1.

_instIOHC_n0_aliasMSRLEGACY; MSR0000_0466

_instIOHC_n0_aliasMSR; MSRC000_2192

Bits	Description
63:0	ErrorAddr. Read-only. Reset: Cold,0000_0000_0000_0000h. Contains the address, if any, associated with the error logged in MCA::NBIO::MCA_STATUS_NBIO.

Table 74: MCA_ADDR_NBIO

Error Type	Bits	Description
EccParityError	[56:0]	Reserved
PCIE_Sideband	[56:0]	Reserved
Ext_ErrEvent	[56:0]	Reserved
Egress_Poison	[56:0]	Reserved
IOHC_Internal_Poison	[56:0]	Reserved
Int_ErrEvent	[56:0]	Reserved

MSR0000_0467...MSRC000_2193 [NBIO Machine Check Miscellaneous 0] (MCA::NBIO::MCA_MISC0_NBIO)

Log miscellaneous information associated with errors.

_instIOHC_n0_aliasMSRLEGACY; MSR0000_0467

_instIOHC_n0_aliasMSR; MSRC000_2193

Bits	Description
63	Valid. Reset: 1. 1=A valid CntP field is present in this register. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read-only.
62	CntP. Reset: 1. 1=A valid threshold counter is present. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read-only.
61	Locked. Reset: 0. 1=Writes to this register are ignored. This bit is set by BIOS to indicate that this register is not available for OS use. BIOS should set this bit if ThresholdIntType is set to SMI. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read-only.
60	IntP. Reset: 1. 1=ThresholdIntType can be used to generate interrupts. 0=ThresholdIntType and interrupt generation are not supported. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::NBIO::MCA_MISC0_NBIO[Locked]) ? Read-write : Read-only.
59:56	Reserved.
55:52	LvtOffset. Reset: 0h. One per die. For error thresholding interrupts, specifies the address of the LVT entry in the APIC registers as follows: LVT address = (LvtOffset shifted left 4 bits) + 500h (see Core::X86::Apic::ExtendedInterruptLvtEntries). AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::NBIO::MCA_MISC0_NBIO[Locked]) ? Read-write : Read-only.
51	CntEn. Reset: 0. 1=Count thresholding errors. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::NBIO::MCA_MISC0_NBIO[Locked]) ? Read-write : Read-only.
50:49	ThresholdIntType. Reset: Cold,0h. Specifies the type of interrupt signaled when Ovrflw is set and IntP==1. 00b = No interrupt. 01b = APIC based interrupt (see Core::X86::Msr::McaIntrCfg[ThresholdLvtOffset]). 10b = SMI trigger event. 11b = Reserved. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::NBIO::MCA_MISC0_NBIO[Locked]) ? Read-write : Read-only.
48	Ovrflw. Reset: Cold,0. Set by hardware when ErrCnt transitions from FFEh to FFFh. When this field is set, ErrCnt no longer increments. When this bit is set, the interrupt selected by the ThresholdIntType field is generated. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::NBIO::MCA_MISC0_NBIO[Locked]) ? Read-write : Read-only.
47:44	Reserved.
43:32	ErrCnt. Reset: Cold,000h. This is written by software to set the starting value of the error counter. This is incremented by hardware when errors are logged. When this counter overflows, it stays at FFFh (no rollover). The threshold value, written by software, is (FFFh - the desired error count (the number of errors necessary in order for an interrupt to be taken)); the desired error count of 0 (a write value of FFFh) is not supported. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] !MCA::NBIO::MCA_MISC0_NBIO[Locked]) ? Read-write : Read-only.
31:24	BlkPtr. Read-write. Reset: 00h. 00h=Extended MISC MSR block is not valid. 01h=Extended MSR block is valid.
23:0	Reserved.

MSRC000_2194 [NBIO Machine Check Configuration] (MCA::NBIO::MCA_CONFIG_NBIO)

Reset: 0000_0002_0000_0125h.

Controls configuration of the associated machine check bank.

_instIOHC_n0_aliasMSR; MSRC000_2194

Bits	Description
63:39	Reserved.
38:37	DeferredIntType . Read-write. Reset: 0h. Specifies the type of interrupt signaled when a deferred error is logged. 00b = No interrupt. 01b = APIC based interrupt (see Core::X86::Msr::McaIntrCfg[DeferredLvtOffset]). 10b = SMI trigger event. 11b = Reserved.
36:35	Reserved.
34	LogDeferredInMcaStat . Read-write. Reset: 0. Init: BIOS,1. 1=Log deferred errors in MCA::NBIO::MCA_STATUS_NBIO and MCA::NBIO::MCA_ADDR_NBIO in addition to MCA::NBIO::MCA_DESTAT_NBIO and MCA::NBIO::MCA_DEADDR_NBIO. 0=Only log deferred errors in MCA::NBIO::MCA_DESTAT_NBIO and MCA::NBIO::MCA_DEADDR_NBIO. This bit does not affect logging of deferred errors in MCA::NBIO::MCA_SYND_NBIO, MCA::NBIO::MCA_MISC0_NBIO.
33	Reserved.
32	McaXEnable . Read-write. Reset: 0. Init: BIOS,1. Check: 1. 1=Software has acknowledged support for the MCAX feature set. 0=Software has not acknowledged support for the MCAX feature set. All uncorrected and fatal errors will cause an ErrorEvent packet to be generated. Deferred error interrupts are configured via Core::X86::Msr::McaIntrCfg.
31:9	Reserved.
8	McaLsbInStatusSupported . Read-only. Reset: 1. 1=MCA::NBIO::MCA_CONFIG_NBIO[McaLsbInStatusSupported] indicates that AddrLsb is located in McaStatus registers.
7:6	Reserved.
5	DeferredIntTypeSupported . Read-only. Reset: 1. 1=MCA::NBIO::MCA_CONFIG_NBIO[DeferredIntType] controls the type of interrupt generated on a deferred error. Deferred errors are supported in this bank only if MCA::NBIO::MCA_CONFIG_NBIO[DeferredErrorLoggingSupported]=1.
4:3	Reserved.
2	DeferredErrorLoggingSupported . Read-only. Reset: 1. 1=Deferred errors are supported in this MCA bank, and MCA::NBIO::MCA_CONFIG_NBIO[LogDeferredInMcaStat] controls the logging behavior of these errors. MCA::NBIO::MCA_DESTAT_NBIO and MCA::NBIO::MCA_DEADDR_NBIO are supported in this MCA bank. 0=Deferred errors are not supported in this bank.
1	Reserved.
0	McaX . Read-only. Reset: 1. 1=This bank provides Machine Check Architecture Extensions. Up to 4 additional MISC registers (MISC1-MISC4) are supported. MCA::NBIO::MCA_MISC0_NBIO[BlkPtr] indicates the presence of the additional MISC registers, but is not used to determine their MSR numbers. Deferred error interrupt type is specifiable by MCA bank. MCA::NBIO::MCA_STATUS_NBIO[TCC] is present.

MSRC000_2195 [NBIO IP Identification] (MCA::NBIO::MCA_IPID_NBIO)

Reset: 0000_0018_0000_0000h.

The MCA::NBIO::MCA_IPID_NBIO register is used by software to determine what IP type and revision is associated with the MCA bank.

_instIOHC_n0_aliasMSR; MSRC000_2195

Bits	Description
63:48	McaType . Read-only. Reset: 0000h. The McaType of the MCA bank within this IP.
47:44	InstanceIdHi . Read-write. Reset: 0h. The HI value instance ID of this IP. This is initialized to a unique ID per instance of this register.
43:32	HardwareID . Read-only. Reset: 018h. The Hardware ID of the IP associated with this MCA bank.
31:0	InstanceId . Read-write. Reset: 0000_0000h. Init: 13B1_7000h. The instance ID of this IP. This is initialized to a unique ID per instance of this register.

MSRC000_2196 [NBIO Machine Check Syndrome] (MCA::NBIO::MCA_SYND_NBIO)	
Read-write, Volatile. Reset: Cold, 0000_0000_0000_0000h.	
Logs physical location information associated with error in MCA::NBIO::MCA_STATUS_NBIO Thread 0	
_instIOHC_n0_aliasMSR; MSRC000_2196	
Bits	Description
63:33	Reserved.
32	Syndrom . Read-write, Volatile. Reset: Cold, 0. Contains the syndrome, if any, associated with the error logged in MCA::NBIO::MCA_STATUS_NBIO. The low-order bit of the syndrome is stored in bit 0, and the syndrome has a length specified by MCA::NBIO::MCA_SYND_NBIO[Length]. The Syndrome field is only valid when MCA::NBIO::MCA_SYND_NBIO[Length] is not 0.
31:27	Reserved.
26:24	ErrorPriority . Read-write, Volatile. Reset: Cold, 0h. Encodes the priority of the error logged in MCA::NBIO::MCA_SYND_NBIO. 3'b000 = No error; 3'b001 = Reserved; 3'b010 = Corrected Error; 3'b011 = Deferred Error; 3'b100 = Uncorrected Error; 3'b101 = Fatal Error; all others reserved.
23:18	Length . Read-write, Volatile. Reset: Cold, 00h. Specifies the length in bits of the syndrome contained in MCA::NBIO::MCA_SYND_NBIO[Syndrome]. A value of 0 indicates that there is no valid syndrome in MCA::NBIO::MCA_SYND_NBIO. For example, a syndrome length of 9 means that MCA::NBIO::MCA_SYND_NBIO[Syndrome] bits [8:0] contains a valid syndrome.
17:0	ErrorInformation . Read-write, Volatile. Reset: Cold, 0_0000h. Contains error-specific information about the location of the error. Decoding is available in Table 75 [MCA_SYND_NBIO].

Table 75: MCA_SYND_NBIO

Error Type	Bits	Description
EccParityError	[17:5] [4:0]	Group ID Structure ID
PCIE_Sideband	[5:0]	EgressPortNum
Ext_ErrEvent	[3:0]	Reserved
Egress_Poison	[5:0]	Egress Port Number
IOHC_Internal_Poison	[0]	0:CfgMaster 1:TrapClient
Int_ErrEvent	[0]	Reserved

MSRC000_2198 [NBIO Machine Check Deferred Error Status] (MCA::NBIO::MCA_DESTAT_NBIO)

Reset: Cold,0000_0000_0000_0000h.

Holds status information for the first deferred error seen in this bank.

_instIOHC_n0_aliasMSR; MSRC000_2198

Bits	Description
63	Val. Read-write, Volatile. Reset: Cold,0. 1=A valid error has been detected (whether it is enabled or not).
62	Overflow. Read-write, Volatile. Reset: Cold,0. 1=An error was detected while the valid bit (Val) was set; at least one error was not logged. Overflow is set independently of whether the existing error is overwritten. (See the section on overwrite priorities.)
61:59	RESERV4. Read-write. Reset: Cold,0h.
58	AddrV. Read-write, Volatile. Reset: Cold,0. 1=MCA::NBIO::MCA_DEADDR_NBIO contains address information associated with the error.
57:54	RESERV3. Read-write. Reset: Cold,0h.
53	SyndV. Read-write, Volatile. Reset: Cold,0. 1=This error logged information in MCA::NBIO::MCA_SYND_NBIO. If MCA::NBIO::MCA_SYND_NBIO[ErrorPriority] is the same as the priority of the error in MCA::NBIO::MCA_STATUS_NBIO, then the information in MCA::NBIO::MCA_SYND_NBIO is associated with the error in MCA::NBIO::MCA_DESTAT_NBIO.
52:45	RESERV2. Read-write. Reset: Cold,00h.
44	Deferred. Read-write, Volatile. Reset: Cold,0. 1=A deferred error was created. A deferred error is the result of an uncorrectable data error which did not immediately cause a processor exception; poison is created and an exception is deferred until the poison data is consumed.
43:30	RESERV1. Read-write. Reset: Cold,0000h.
29:24	AddrLsb. Read-write, Volatile. Reset: Cold,00h. Specifies the least significant valid bit of the address contained in MCA::NBIO::MCA_ADDR_NBIO[ErrorAddr]. A value of 0 indicates that MCA::NBIO::MCA_ADDR_NBIO[55:0] contains a valid byte address. A value of 6 indicates that MCA::NBIO::MCA_ADDR_NBIO[55:6] contains a valid cache line address and that MCA::NBIO::MCA_ADDR_NBIO[5:0] are not part of the address and should be ignored by error handling software. A value of 12 indicates that MCA::NBIO::MCA_ADDR_NBIO[55:12] contain a valid 4KB memory page and that MCA::NBIO::MCA_ADDR_NBIO[11:0] should be ignored by error handling software.
23:22	RESERV0. Read-write. Reset: Cold,0h.
21:16	ErrorCodeExt. Read-write, Volatile. Reset: Cold,00h. Logs an extended error code when an error is detected. This model-specific field is used in conjunction with ErrorCode? to identify the error sub-type for root cause analysis.
15:0	ErrorCode. Read-write, Volatile. Reset: Cold,0000h. Error code for this error.

MSRC001_0419 [NBIO Machine Check Control Mask] (MCA::NBIO::MCA_CTL_MASK_NBIO)

Read-write. Reset: 0000_0000_0000_0000h.

Inhibit detection of an error source.

_instIOHC_n0_aliasMSR; MSRC001_0419

Bits	Description
63:6	Reserved.
5	Int_ErrEvent. Read-write. Reset: 0. Init: BIOS,1. Internal system fatal error event was detected.
4	IOHC_Internal_Poison. Read-write. Reset: 0. Internal Poison Error. Poison data was sent to an internal client.
3	Egress_Poison. Read-write. Reset: 0. SDP Egress Poison Error. Poison was propagated to an egress port.
2	Ext_ErrEvent. Read-write. Reset: 0. Init: BIOS,1. External SDP ErrEvent error. A system fatal error event from an SDP interface was detected.
1	PCIE_Sideband. Read-write. Reset: 0. Init: BIOS,1. PCIe error. A PCIe® error was logged in a PCIe® root port.
0	EccParityError. Read-write. Reset: 0. ECC or Parity error. An SRAM ECC or parity error was detected.

3.2.5.14 KPX SERDES**MSR0000_0474...MSRC000_21E0 [KPX_SERDES Machine Check Control]
(MCA::KPX::SERDES::MCA_CTL_KPX_SERDES)**

Read-write. Reset: 0000_0000_0000_0000h.

0=Disables error reporting for the corresponding error. 1=Enables error reporting via machine check exception for the corresponding error. The MCA::KPX::SERDES::MCA_CTL_KPX_SERDES register must be enabled by the corresponding enable bit in Core::X86::Msr::MCG_CTL. Does not affect error detection, correction, or logging.

_instKPXSERDES_n0_aliasMSRLEGACY; MSR0000_0474

_instKPXSERDES_n1_aliasMSRLEGACY; MSR0000_0478

_instKPXSERDES_n0_aliasMSR; MSRC000_21D0

_instKPXSERDES_n1_aliasMSR; MSRC000_21E0

Bits	Description
63:4	Reserved.
3	APB. Read-write. Reset: 0. PHY APB error
2	ARCData. Read-write. Reset: 0. ARC data buffer parity error
1	ARCIns. Read-write. Reset: 0. ARC instruction buffer parity error
0	RAMECC. Read-write. Reset: 0. RAM ECC Error.

**MSR0000_0475...MSRC000_21E1 [KPX_SERDES Machine Check Status]
(MCA::KPX::SERDES::MCA_STATUS_KPX_SERDES)**

Reset: Cold,0000_0000_0000_0000h.

Logs information associated with errors.

_instKPXSERDES_n0_aliasMSRLEGACY; MSR0000_0475

_instKPXSERDES_n1_aliasMSRLEGACY; MSR0000_0479

_instKPXSERDES_n0_aliasMSR; MSRC000_21D1

_instKPXSERDES_n1_aliasMSR; MSRC000_21E1

Bits	Description
63	Val. Reset: Cold,0. 1=A valid error has been detected. This bit should be cleared by software after the register has been read. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
62	Overflow. Reset: Cold,0. 1=An error was detected while the valid bit (Val) was set; at least one error was not logged. Overflow is set independently of whether the existing error is overwritten. See 3.1.3 [Machine Check Errors]. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
61	UC. Reset: Cold,0. 1=The error was not corrected by hardware. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
60	En. Reset: Cold,0. 1=MCA error reporting is enabled for this error, as indicated by the corresponding bit in MCA::KPX::SERDES::MCA_CTL_KPX_SERDES. This bit is a copy of bit in MCA::KPX::SERDES::MCA_CTL_KPX_SERDES for this error. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
59	MiscV. Reset: Cold,0. 1=Valid thresholding in MCA::KPX::SERDES::MCA_MISC0_KPX_SERDES. In certain modes, MISC registers are owned by platform firmware and will RAZ when read by non-SMM code. Therefore, it is possible for MiscV=1 and the MISC register to read as all zeros. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
58	AddrV. Reset: Cold,0. 1=MCA::KPX::SERDES::MCA_ADDR_KPX_SERDES contains address information associated with the error. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
57	PCC. Reset: Cold,0. 1=Hardware context held by the processor may have been corrupted. Continued operation of the system may have unpredictable results. The error is not recoverable or survivable, and the system should be reinitialized. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
56	ErrCoreIdVal. Reset: Cold,0. 1=The ErrCoreId field is valid. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
55	TCC. Reset: Cold,0. 1=Hardware context of the process thread to which the error was reported may have been corrupted. Continued operation of the thread may have unpredictable results. The thread must be terminated. Only meaningful when MCA::KPX::SERDES::MCA_STATUS_KPX_SERDES[PCC]=0. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
54	RESERV54. Reset: Cold,0. MCA_STATUS Register Reserved bit. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
53	SyndV. Reset: Cold,0. 1=This error logged information in MCA::KPX::SERDES::MCA_SYND_KPX_SERDES. If MCA::KPX::SERDES::MCA_SYND_KPX_SERDES[ErrorPriority] is the same as the priority of the error in MCA::KPX::SERDES::MCA_STATUS_KPX_SERDES, then the information in MCA::KPX::SERDES::MCA_SYND_KPX_SERDES is associated with the error in MCA::KPX::SERDES::MCA_STATUS_KPX_SERDES. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
52	Reserved.
51:47	RESERV47. Reset: Cold,00h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.

46	CECC. Reset: Cold,0. 1=The error was a correctable ECC error according to the restrictions of the ECC algorithm. UC indicates whether the error was actually corrected by the processor. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
45	UECC. Reset: Cold,0. 1=The error was an uncorrectable ECC error according to the restrictions of the ECC algorithm. UC indicates whether the error was actually corrected by the processor. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
44	Deferred. Reset: Cold,0. 1=A deferred error was created. A deferred error is the result of an uncorrectable data error which did not immediately cause a processor exception; an exception is deferred until the erroneous data is consumed. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
43	Poison. Reset: Cold,0. 1=The error was the result of attempting to consume poisoned data. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
42:41	RESERV41. Reset: Cold,0h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
40	Scrub. Reset: Cold,0. 1=The error was the result of a scrub operation. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
39:38	RESERV38. Reset: Cold,0h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
37:32	ErrCoreId. Reset: Cold,00h. When ErrCoreIdVal=1 this field indicates which core within the processor is associated with the error; Otherwise this field is reserved. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
31:30	RESERV30. Reset: Cold,0h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
29:24	AddrLsb. Reset: Cold,00h. Specifies the least significant valid bit of the address contained in MCA::KPX::SERDES::MCA_ADDR_KPX_SERDES[ErrorAddr]. A value of 0 indicates that MCA::KPX::SERDES::MCA_ADDR_KPX_SERDES[55:0] contains a valid byte address. A value of 6 indicates that MCA::KPX::SERDES::MCA_ADDR_KPX_SERDES[55:6] contains a valid cache line address and that MCA::KPX::SERDES::MCA_ADDR_KPX_SERDES[5:0] are not part of the address and should be ignored by error handling software. A value of 12 indicates that MCA::KPX::SERDES::MCA_ADDR_KPX_SERDES[55:12] contain a valid 4KB memory page and that MCA::KPX::SERDES::MCA_ADDR_KPX_SERDES[11:0] should be ignored by error handling software. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
23:22	RESERV22. Reset: Cold,0h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
21:16	ErrorCodeExt. Reset: Cold,00h. Extended Error Code. This field is used to identify the error type for root cause analysis. This field indicates which bit position in MCA::KPX::SERDES::MCA_CTL_KPX_SERDES enables error reporting for the logged error. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
15:0	ErrorCode. Reset: Cold,0000h. Error code for this error. See 3.1.3.3 [Error Codes] for details on decoding this field. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.

Table 76: MCA_STATUS_KPX_SERDES

Error Type	ErrorCode Ext	UC	PCC	TCC	Deferred	Poison	AddrV
RAMECC	0x0					-	-
ARCIIns	0x1					-	-
ARCData	0x2					-	-
APB	0x3					-	-

**MSR0000_0476...MSRC000_21E2 [KPX_SERDES Machine Check Address]
(MCA::KPX::SERDES::MCA_ADDR_KPX_SERDES)**

Read-only. Reset: Cold,0000_0000_0000_0000h.

MCA::KPX::SERDES::MCA_ADDR_KPX_SERDES stores an address and other information associated with the error in MCA::KPX::SERDES::MCA_STATUS_KPX_SERDES. The register is only meaningful if

MCA::KPX::SERDES::MCA_STATUS_KPX_SERDES[Val]=1 and

MCA::KPX::SERDES::MCA_STATUS_KPX_SERDES[AddrV]=1.

_instKPIXSERDES_n0_aliasMSRLEGACY; MSR0000_0476

_instKPIXSERDES_n1_aliasMSRLEGACY; MSR0000_047A

_instKPIXSERDES_n0_aliasMSR; MSRC000_21D2

_instKPIXSERDES_n1_aliasMSR; MSRC000_21E2

Bits	Description
63:0	ErrorAddr. Read-only. Reset: Cold,0000_0000_0000_0000h. Contains the address, if any, associated with the error logged in MCA::KPX::SERDES::MCA_STATUS_KPX_SERDES.

Table 77: MCA_ADDR_KPX_SERDES

Error Type	Bits	Description
RAMECC	[56:0]	Reserved
ARCIns	[56:0]	Reserved
ARCDData	[56:0]	Reserved
APB	[56:0]	Reserved

**MSR0000_0477...MSRC000_21E3 [KPX_SERDES Machine Check Miscellaneous 0]
(MCA::KPX::SERDES::MCA_MISC0_KPX_SERDES)**

Log miscellaneous information associated with errors.

_instKPXSERDES_n0_aliasMSRLEGACY; MSR0000_0477

_instKPXSERDES_n1_aliasMSRLEGACY; MSR0000_047B

_instKPXSERDES_n0_aliasMSR; MSRC000_21D3

_instKPXSERDES_n1_aliasMSR; MSRC000_21E3

Bits	Description
63	Valid. Reset: 1. 1=A valid CntP field is present in this register. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read-only.
62	CntP. Reset: 1. 1=A valid threshold counter is present. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read-only.
61	Locked. Reset: 0. 1=Writes to this register are ignored. This bit is set by BIOS to indicate that this register is not available for OS use. BIOS should set this bit if ThresholdIntType is set to SMI. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read-only.
60	IntP. Reset: 1. 1=ThresholdIntType can be used to generate interrupts. 0=ThresholdIntType and interrupt generation are not supported. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] ! MCA::KPX::SERDES::MCA_MISC0_KPX_SERDES[Locked]) ? Read-write : Read-only.
59:56	Reserved.
55:52	LvtOffset. Reset: 0h. One per die. For error thresholding interrupts, specifies the address of the LVT entry in the APIC registers as follows: LVT address = (LvtOffset shifted left 4 bits) + 500h (see Core::X86::Apic::ExtendedInterruptLvtEntries). AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] ! MCA::KPX::SERDES::MCA_MISC0_KPX_SERDES[Locked]) ? Read-write : Read-only.
51	CntEn. Reset: 0. 1=Count thresholding errors. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] ! MCA::KPX::SERDES::MCA_MISC0_KPX_SERDES[Locked]) ? Read-write : Read-only.
50:49	ThresholdIntType. Reset: Cold,0h. Specifies the type of interrupt signaled when Ovrflw is set and IntP==1. 00b = No interrupt. 01b = APIC based interrupt (see Core::X86::Msr::McaIntrCfg[ThresholdLvtOffset]). 10b = SMI trigger event. 11b = Reserved. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] ! MCA::KPX::SERDES::MCA_MISC0_KPX_SERDES[Locked]) ? Read-write : Read-only.
48	Ovrflw. Reset: Cold,0. Set by hardware when ErrCnt transitions from FFEh to FFFh. When this field is set, ErrCnt no longer increments. When this bit is set, the interrupt selected by the ThresholdIntType field is generated. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] ! MCA::KPX::SERDES::MCA_MISC0_KPX_SERDES[Locked]) ? Read-write : Read-only.
47:44	Reserved.
43:32	ErrCnt. Reset: Cold,000h. This is written by software to set the starting value of the error counter. This is incremented by hardware when errors are logged. When this counter overflows, it stays at FFFh (no rollover). The threshold value, written by software, is (FFFh - the desired error count (the number of errors necessary in order for an interrupt to be taken)); the desired error count of 0 (a write value of FFFh) is not supported. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] ! MCA::KPX::SERDES::MCA_MISC0_KPX_SERDES[Locked]) ? Read-write : Read-only.
31:24	BlkPtr. Read-write. Reset: 00h. 00h=Extended MISC MSR block is not valid. 01h=Extended MSR block is valid.
23:0	Reserved.

**MSRC000_21[D...E]4 [KPX_SERDES Machine Check Configuration]
(MCA::KPX::SERDES::MCA_CONFIG_KPX_SERDES)**

Reset: 0000_0002_0000_0125h.

Controls configuration of the associated machine check bank.

_instKPXSERDES_n0_aliasMSR; MSRC000_21D4

_instKPXSERDES_n1_aliasMSR; MSRC000_21E4

Bits	Description
63:39	Reserved.
38:37	DeferredIntType. Read-write. Reset: 0h. Specifies the type of interrupt signaled when a deferred error is logged. 00b = No interrupt. 01b = APIC based interrupt (see Core::X86::Msr::McaIntrCfg[DeferredLvtOffset]). 10b = SMI trigger event. 11b = Reserved.
36:35	Reserved.
34	LogDeferredInMcaStat. Read-write. Reset: 0. Init: BIOS,1. 1=Log deferred errors in MCA::KPX::SERDES::MCA_STATUS_KPX_SERDES and MCA::KPX::SERDES::MCA_ADDR_KPX_SERDES in addition to MCA::KPX::SERDES::MCA_DESTAT_KPX_SERDES and MCA::KPX::SERDES::MCA_DEADDR_KPX_SERDES. 0=Only log deferred errors in MCA::KPX::SERDES::MCA_DESTAT_KPX_SERDES and MCA::KPX::SERDES::MCA_DEADDR_KPX_SERDES. This bit does not affect logging of deferred errors in MCA::KPX::SERDES::MCA_SYND_KPX_SERDES, MCA::KPX::SERDES::MCA_MISC0_KPX_SERDES.
33	Reserved.
32	McaXEnable. Read-write. Reset: 0. Init: BIOS,1. Check: 1. 1=Software has acknowledged support for the MCAX feature set. 0=Software has not acknowledged support for the MCAX feature set. All uncorrected and fatal errors will cause an ErrorEvent packet to be generated. Deferred error interrupts are configured via Core::X86::Msr::McaIntrCfg.
31:9	Reserved.
8	McaLsbInStatusSupported. Read-only. Reset: 1. 1=MCA::KPX::SERDES::MCA_CONFIG_KPX_SERDES[McaLsbInStatusSupported] indicates that AddrLsb is located in McaStatus registers.
7:6	Reserved.
5	DeferredIntTypeSupported. Read-only. Reset: 1. 1=MCA::KPX::SERDES::MCA_CONFIG_KPX_SERDES[DeferredIntType] controls the type of interrupt generated on a deferred error. Deferred errors are supported in this bank only if MCA::KPX::SERDES::MCA_CONFIG_KPX_SERDES[DeferredErrorLoggingSupported]=1.
4:3	Reserved.
2	DeferredErrorLoggingSupported. Read-only. Reset: 1. 1=Deferred errors are supported in this MCA bank, and MCA::KPX::SERDES::MCA_CONFIG_KPX_SERDES[LogDeferredInMcaStat] controls the logging behavior of these errors. MCA::KPX::SERDES::MCA_DESTAT_KPX_SERDES and MCA::KPX::SERDES::MCA_DEADDR_KPX_SERDES are supported in this MCA bank. 0=Deferred errors are not supported in this bank.
1	Reserved.
0	McaX. Read-only. Reset: 1. 1=This bank provides Machine Check Architecture Extensions. Up to 4 additional MISC registers (MISC1-MISC4) are supported. MCA::KPX::SERDES::MCA_MISC0_KPX_SERDES[BlkPtr] indicates the presence of the additional MISC registers, but is not used to determine their MSR numbers. Deferred error interrupt type is specifiable by MCA bank. MCA::KPX::SERDES::MCA_STATUS_KPX_SERDES[TCC] is present.

MSRC000_21[D...E]5 [KPX_SERDES IP Identification] (MCA::KPX::SERDES::MCA_IPID_KPX_SERDES)

Reset: 0000_0259_0000_0000h.

The MCA::KPX::SERDES::MCA_IPID_KPX_SERDES register is used by software to determine what IP type and revision is associated with the MCA bank.

_instKPIXSERDES_n0_aliasMSR; MSRC000_21D5_instKPIXSERDES_n1_aliasMSR; MSRC000_21E5

Bits	Description
63:48	McaType . Read-only. Reset: 0000h. The McaType of the MCA bank within this IP.
47:44	InstanceIdHi . Read-write. Reset: 0h. The HI value instance ID of this IP. This is initialized to a unique ID per instance of this register.
43:32	HardwareID . Read-only. Reset: 259h. The Hardware ID of the IP associated with this MCA bank.
31:0	InstanceId . Read-write. Reset: 0000_0000h. The instance ID of this IP. This is initialized to a unique ID per instance of this register.
	Init: <u>_instKPIXSERDES_n0_aliasMSR; 17F0_0400h</u>
	Init: <u>_instKPIXSERDES_n1_aliasMSR; 1800_0400h</u>

MSRC000_21[D...E]6 [KPX_SERDES Machine Check Syndrome] (MCA::KPX::SERDES::MCA_SYND_KPX_SERDES)

Read-write, Volatile. Reset: Cold, 0000_0000_0000_0000h.

Logs physical location information associated with error in MCA::KPX::SERDES::MCA_STATUS_KPX_SERDES Thread 0

_instKPIXSERDES_n0_aliasMSR; MSRC000_21D6_instKPIXSERDES_n1_aliasMSR; MSRC000_21E6

Bits	Description
63:33	Reserved.
32	Syndrome . Read-write, Volatile. Reset: Cold, 0. Contains the syndrome, if any, associated with the error logged in MCA::KPX::SERDES::MCA_STATUS_KPX_SERDES. The low-order bit of the syndrome is stored in bit 0, and the syndrome has a length specified by MCA::KPX::SERDES::MCA_SYND_KPX_SERDES[Length]. The Syndrome field is only valid when MCA::KPX::SERDES::MCA_SYND_KPX_SERDES[Length] is not 0.
31:27	Reserved.
26:24	ErrorPriority . Read-write, Volatile. Reset: Cold, 0h. Encodes the priority of the error logged in MCA::KPX::SERDES::MCA_SYND_KPX_SERDES. 3'b000 = No error; 3'b001 = Reserved; 3'b010 = Corrected Error; 3'b011 = Deferred Error; 3'b100 = Uncorrected Error; 3'b101 = Fatal Error; all others reserved.
23:18	Length . Read-write, Volatile. Reset: Cold, 00h. Specifies the length in bits of the syndrome contained in MCA::KPX::SERDES::MCA_SYND_KPX_SERDES[Syndrome]. A value of 0 indicates that there is no valid syndrome in MCA::KPX::SERDES::MCA_SYND_KPX_SERDES. For example, a syndrome length of 9 means that MCA::KPX::SERDES::MCA_SYND_KPX_SERDES[Syndrome] bits [8:0] contains a valid syndrome.
17:0	ErrorInformation . Read-write, Volatile. Reset: Cold, 0_0000h. Contains error-specific information about the location of the error. Decoding is available in Table 78 [MCA_SYND_KPX_SERDES].

Table 78: MCA_SYND_KPX_SERDES

Error Type	Bits	Description
RAMECC	[17:0]	Reserved
ARCIns	[17:0]	Reserved
ARCDData	[17:0]	Reserved
APB	[17:0]	Reserved

**MSRC000_21[D...E]8 [KPX_SERDES Machine Check Deferred Error Status]
(MCA::KPX::SERDES::MCA_DESTAT_KPX_SERDES)**

Reset: Cold,0000_0000_0000_0000h.

Holds status information for the first deferred error seen in this bank.

_instKPXSERDES_n0_aliasMSR; MSRC000_21D8

_instKPXSERDES_n1_aliasMSR; MSRC000_21E8

Bits	Description
63	Val. Read-write, Volatile. Reset: Cold,0. 1=A valid error has been detected (whether it is enabled or not).
62	Overflow. Read-write, Volatile. Reset: Cold,0. 1=An error was detected while the valid bit (Val) was set; at least one error was not logged. Overflow is set independently of whether the existing error is overwritten. (See the section on overwrite priorities.)
61:59	RESERV4. Read-write. Reset: Cold,0h.
58	AddrV. Read-write, Volatile. Reset: Cold,0. 1=MCA::KPX::SERDES::MCA_DEADDR_KPX_SERDES contains address information associated with the error.
57:54	RESERV3. Read-write. Reset: Cold,0h.
53	SyndV. Read-write, Volatile. Reset: Cold,0. 1=This error logged information in MCA::KPX::SERDES::MCA_SYND_KPX_SERDES. If MCA::KPX::SERDES::MCA_SYND_KPX_SERDES[ErrorPriority] is the same as the priority of the error in MCA::KPX::SERDES::MCA_STATUS_KPX_SERDES, then the information in MCA::KPX::SERDES::MCA_SYND_KPX_SERDES is associated with the error in MCA::KPX::SERDES::MCA_DESTAT_KPX_SERDES.
52:45	RESERV2. Read-write. Reset: Cold,00h.
44	Deferred. Read-write, Volatile. Reset: Cold,0. 1=A deferred error was created. A deferred error is the result of an uncorrectable data error which did not immediately cause a processor exception; poison is created and an exception is deferred until the poison data is consumed.
43:30	RESERV1. Read-write. Reset: Cold,0000h.
29:24	AddrLsb. Read-write, Volatile. Reset: Cold,00h. Specifies the least significant valid bit of the address contained in MCA::KPX::SERDES::MCA_ADDR_KPX_SERDES[ErrorAddr]. A value of 0 indicates that MCA::KPX::SERDES::MCA_ADDR_KPX_SERDES[55:0] contains a valid byte address. A value of 6 indicates that MCA::KPX::SERDES::MCA_ADDR_KPX_SERDES[55:6] contains a valid cache line address and that MCA::KPX::SERDES::MCA_ADDR_KPX_SERDES[5:0] are not part of the address and should be ignored by error handling software. A value of 12 indicates that MCA::KPX::SERDES::MCA_ADDR_KPX_SERDES[55:12] contain a valid 4KB memory page and that MCA::KPX::SERDES::MCA_ADDR_KPX_SERDES[11:0] should be ignored by error handling software.
23:22	RESERV0. Read-write. Reset: Cold,0h.
21:16	ErrorCodeExt. Read-write, Volatile. Reset: Cold,00h. Logs an extended error code when an error is detected. This model-specific field is used in conjunction with ErrorCode? to identify the error sub-type for root cause analysis.
15:0	ErrorCode. Read-write, Volatile. Reset: Cold,0000h. Error code for this error.

**MSRC001_041[D...E] [KPX_SERDES Machine Check Control Mask]
(MCA::KPX::SERDES::MCA_CTL_MASK_KPX_SERDES)**

Read-write. Reset: 0000_0000_0000_0000h.

Inhibit detection of an error source.

_instKPXSERDES_n0_aliasMSR; MSRC001_041D_instKPXSERDES_n1_aliasMSR; MSRC001_041E

Bits	Description
63:4	Reserved.
3	APB. Read-write. Reset: 0. PHY APB error
2	ARCData. Read-write. Reset: 0. ARC data buffer parity error
1	ARCIns. Read-write. Reset: 0. ARC instruction buffer parity error
0	RAMECC. Read-write. Reset: 0. RAM ECC Error.

3.2.5.15 KPX GMI
**MSR0000_044C...MSRC000_2140 [KPX_GMI Machine Check Control]
(MCA::KPX::GMI::MCA_CTL_KPX_GMI)**

Read-write. Reset: 0000_0000_0000_0000h.

0=Disables error reporting for the corresponding error. 1=Enables error reporting via machine check exception for the corresponding error. The MCA::KPX::GMI::MCA_CTL_KPX_GMI register must be enabled by the corresponding enable bit in Core::X86::Msr::MCG_CTL. Does not affect error detection, correction, or logging.

_inst[GMICONTAINER[1:0]KPXGMI]_n[2,0]_aliasMSRLEGACY; MSR0000_044C_ccd[1:0]_instGMICONTAINER12KPXGMI_n[3,1]_aliasMSRLEGACY; MSR0000_0450_inst[GMICONTAINER[1:0]KPXGMI]_n[2,0]_aliasMSR; MSRC000_2130_ccd[1:0]_instGMICONTAINER12KPXGMI_n[3,1]_aliasMSR; MSRC000_2140

Bits	Description
63:4	Reserved.
3	APB. Read-write. Reset: 0. PHY APB error
2	ARCData. Read-write. Reset: 0. ARC data buffer parity error
1	ARCIns. Read-write. Reset: 0. ARC instruction buffer parity error
0	RAMECC. Read-write. Reset: 0. RAM ECC Error.

**MSR0000_044D...MSRC000_2141 [KPX_GMI Machine Check Status]
(MCA::KPX::GMI::MCA_STATUS_KPX_GMI)**

Reset: Cold,0000_0000_0000_0000h.

Logs information associated with errors.

_inst[GMICONTAINER[1:0]KPXGMI]_n[2,0]_aliasMSRLEGACY; MSR0000_044D

_ccd[1:0]_instGMICONTAINER12KPXGMI_n[3,1]_aliasMSRLEGACY; MSR0000_0451

_inst[GMICONTAINER[1:0]KPXGMI]_n[2,0]_aliasMSR; MSRC000_2131

_ccd[1:0]_instGMICONTAINER12KPXGMI_n[3,1]_aliasMSR; MSRC000_2141

Bits	Description
63	Val. Reset: Cold,0. 1=A valid error has been detected. This bit should be cleared by software after the register has been read. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
62	Overflow. Reset: Cold,0. 1=An error was detected while the valid bit (Val) was set; at least one error was not logged. Overflow is set independently of whether the existing error is overwritten. See 3.1.3 [Machine Check Errors]. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
61	UC. Reset: Cold,0. 1=The error was not corrected by hardware. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
60	En. Reset: Cold,0. 1=MCA error reporting is enabled for this error, as indicated by the corresponding bit in MCA::KPX::GMI::MCA_CTL_KPX_GMI. This bit is a copy of bit in MCA::KPX::GMI::MCA_CTL_KPX_GMI for this error. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
59	MiscV. Reset: Cold,0. 1=Valid thresholding in MCA::KPX::GMI::MCA_MISC0_KPX_GMI. In certain modes, MISC registers are owned by platform firmware and will RAZ when read by non-SMM code. Therefore, it is possible for MiscV=1 and the MISC register to read as all zeros. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
58	AddrV. Reset: Cold,0. 1=MCA::KPX::GMI::MCA_ADDR_KPX_GMI contains address information associated with the error. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
57	PCC. Reset: Cold,0. 1=Hardware context held by the processor may have been corrupted. Continued operation of the system may have unpredictable results. The error is not recoverable or survivable, and the system should be reinitialized. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
56	ErrCoreIdVal. Reset: Cold,0. 1=The ErrCoreId field is valid. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
55	TCC. Reset: Cold,0. 1=Hardware context of the process thread to which the error was reported may have been corrupted. Continued operation of the thread may have unpredictable results. The thread must be terminated. Only meaningful when MCA::KPX::GMI::MCA_STATUS_KPX_GMI[PCC]=0. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
54	RESERV54. Reset: Cold,0. MCA_STATUS Register Reserved bit. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
53	SyndV. Reset: Cold,0. 1=This error logged information in MCA::KPX::GMI::MCA_SYND_KPX_GMI. If MCA::KPX::GMI::MCA_SYND_KPX_GMI[ErrorPriority] is the same as the priority of the error in MCA::KPX::GMI::MCA_STATUS_KPX_GMI, then the information in MCA::KPX::GMI::MCA_SYND_KPX_GMI is associated with the error in MCA::KPX::GMI::MCA_STATUS_KPX_GMI. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
52	Reserved.
51:47	RESERV47. Reset: Cold,00h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.

46	CECC. Reset: Cold,0. 1=The error was a correctable ECC error according to the restrictions of the ECC algorithm. UC indicates whether the error was actually corrected by the processor. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
45	UECC. Reset: Cold,0. 1=The error was an uncorrectable ECC error according to the restrictions of the ECC algorithm. UC indicates whether the error was actually corrected by the processor. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
44	Deferred. Reset: Cold,0. 1=A deferred error was created. A deferred error is the result of an uncorrectable data error which did not immediately cause a processor exception; an exception is deferred until the erroneous data is consumed. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
43	Poison. Reset: Cold,0. 1=The error was the result of attempting to consume poisoned data. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
42:41	RESERV41. Reset: Cold,0h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
40	Scrub. Reset: Cold,0. 1=The error was the result of a scrub operation. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
39:38	RESERV38. Reset: Cold,0h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
37:32	ErrCoreId. Reset: Cold,00h. When ErrCoreIdVal=1 this field indicates which core within the processor is associated with the error; Otherwise this field is reserved. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
31:30	RESERV30. Reset: Cold,0h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
29:24	AddrLsb. Reset: Cold,00h. Specifies the least significant valid bit of the address contained in MCA::KPX::GMI::MCA_ADDR_KPX_GMI[ErrorAddr]. A value of 0 indicates that MCA::KPX::GMI::MCA_ADDR_KPX_GMI[55:0] contains a valid byte address. A value of 6 indicates that MCA::KPX::GMI::MCA_ADDR_KPX_GMI[55:6] contains a valid cache line address and that MCA::KPX::GMI::MCA_ADDR_KPX_GMI[5:0] are not part of the address and should be ignored by error handling software. A value of 12 indicates that MCA::KPX::GMI::MCA_ADDR_KPX_GMI[55:12] contain a valid 4KB memory page and that MCA::KPX::GMI::MCA_ADDR_KPX_GMI[11:0] should be ignored by error handling software. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
23:22	RESERV22. Reset: Cold,0h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
21:16	ErrorCodeExt. Reset: Cold,00h. Extended Error Code. This field is used to identify the error type for root cause analysis. This field indicates which bit position in MCA::KPX::GMI::MCA_CTL_KPX_GMI enables error reporting for the logged error. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
15:0	ErrorCode. Reset: Cold,0000h. Error code for this error. See 3.1.3.3 [Error Codes] for details on decoding this field. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.

Table 79: MCA_STATUS_KPX_GMI

Error Type	ErrorCode Ext	UC	PCC	TCC	Deferred	Poison	AddrV
RAMECC	0x0					-	-
ARCIIns	0x1					-	-
ARCDData	0x2					-	-
APB	0x3					-	-

**MSR0000_044E...MSRC000_2142 [KPX_GMI Machine Check Address]
(MCA::KPX::GMI::MCA_ADDR_KPX_GMI)**

Read-only. Reset: Cold,0000_0000_0000_0000h.

MCA::KPX::GMI::MCA_ADDR_KPX_GMI stores an address and other information associated with the error in MCA::KPX::GMI::MCA_STATUS_KPX_GMI. The register is only meaningful if MCA::KPX::GMI::MCA_STATUS_KPX_GMI[Val]=1 and MCA::KPX::GMI::MCA_STATUS_KPX_GMI[AddrV]=1.

_inst[GMICONTAINER[1:0]KPXGMI]_n[2,0]_aliasMSRLEGACY; MSR0000_044E

_ccd[1:0]_instGMICONTAINER12KPXGMI_n[3,1]_aliasMSRLEGACY; MSR0000_0452

_inst[GMICONTAINER[1:0]KPXGMI]_n[2,0]_aliasMSR; MSRC000_2132

_ccd[1:0]_instGMICONTAINER12KPXGMI_n[3,1]_aliasMSR; MSRC000_2142

Bits	Description
63:0	ErrorAddr. Read-only. Reset: Cold,0000_0000_0000_0000h. Contains the address, if any, associated with the error logged in MCA::KPX::GMI::MCA_STATUS_KPX_GMI.

Table 80: MCA_ADDR_KPX_GMI

Error Type	Bits	Description
RAMECC	[56:0]	Reserved
ARCIns	[56:0]	Reserved
ARCDData	[56:0]	Reserved
APB	[56:0]	Reserved

**MSR0000_044F...MSRC000_2143 [KPX_GMI Machine Check Miscellaneous 0]
(MCA::KPX::GMI::MCA_MISC0_KPX_GMI)**

Log miscellaneous information associated with errors.

_inst[GMICONTAINER[1:0]KPXGMI]_n[2,0]_aliasMSRLEGACY; MSR0000_044F

_ccd[1:0]_instGMICONTAINER12KPXGMI_n[3,1]_aliasMSRLEGACY; MSR0000_0453

_inst[GMICONTAINER[1:0]KPXGMI]_n[2,0]_aliasMSR; MSRC000_2133

_ccd[1:0]_instGMICONTAINER12KPXGMI_n[3,1]_aliasMSR; MSRC000_2143

Bits	Description
63	Valid. Reset: 1. 1=A valid CntP field is present in this register. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read-only.
62	CntP. Reset: 1. 1=A valid threshold counter is present. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read-only.
61	Locked. Reset: 0. 1=Writes to this register are ignored. This bit is set by BIOS to indicate that this register is not available for OS use. BIOS should set this bit if ThresholdIntType is set to SMI. AccessType: Core::X86::Msr::HWCR[McStatusWrEn] ? Read-write : Read-only.
60	IntP. Reset: 1. 1=ThresholdIntType can be used to generate interrupts. 0=ThresholdIntType and interrupt generation are not supported. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] ! MCA::KPX::GMI::MCA_MISC0_KPX_GMI[Locked]) ? Read-write : Read-only.
59:56	Reserved.
55:52	LvtOffset. Reset: 0h. One per die. For error thresholding interrupts, specifies the address of the LVT entry in the APIC registers as follows: LVT address = (LvtOffset shifted left 4 bits) + 500h (see Core::X86::Apic::ExtendedInterruptLvtEntries). AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] ! MCA::KPX::GMI::MCA_MISC0_KPX_GMI[Locked]) ? Read-write : Read-only.
51	CntEn. Reset: 0. 1=Count thresholding errors. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] ! MCA::KPX::GMI::MCA_MISC0_KPX_GMI[Locked]) ? Read-write : Read-only.
50:49	ThresholdIntType. Reset: Cold,0h. Specifies the type of interrupt signaled when Ovrflw is set and IntP==1. 00b = No interrupt. 01b = APIC based interrupt (see Core::X86::Msr::McaIntrCfg[ThresholdLvtOffset]). 10b = SMI trigger event. 11b = Reserved. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] ! MCA::KPX::GMI::MCA_MISC0_KPX_GMI[Locked]) ? Read-write : Read-only.
48	Ovrflw. Reset: Cold,0. Set by hardware when ErrCnt transitions from FFEh to FFFh. When this field is set, ErrCnt no longer increments. When this bit is set, the interrupt selected by the ThresholdIntType field is generated. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] ! MCA::KPX::GMI::MCA_MISC0_KPX_GMI[Locked]) ? Read-write : Read-only.
47:44	Reserved.
43:32	ErrCnt. Reset: Cold,000h. This is written by software to set the starting value of the error counter. This is incremented by hardware when errors are logged. When this counter overflows, it stays at FFFh (no rollover). The threshold value, written by software, is (FFFh - the desired error count (the number of errors necessary in order for an interrupt to be taken)); the desired error count of 0 (a write value of FFFh) is not supported. AccessType: (Core::X86::Msr::HWCR[McStatusWrEn] ! MCA::KPX::GMI::MCA_MISC0_KPX_GMI[Locked]) ? Read-write : Read-only.
31:24	BlkPtr. Read-write. Reset: 00h. 00h=Extended MISC MSR block is not valid. 01h=Extended MSR block is valid.
23:0	Reserved.

**MSRC000_21[3...4]4 [KPX_GMI Machine Check Configuration]
(MCA::KPX::GMI::MCA_CONFIG_KPX_GMI)**

Reset: 0000_0002_0000_0125h.

Controls configuration of the associated machine check bank.

_inst[GMICONTAINER[1:0]KPXGMI]_n[2,0]_aliasMSR; MSRC000_2134

_ccd[1:0]_instGMICONTAINER12KPXGMI_n[3,1]_aliasMSR; MSRC000_2144

Bits	Description
63:39	Reserved.
38:37	DeferredIntType. Read-write. Reset: 0h. Specifies the type of interrupt signaled when a deferred error is logged. 00b = No interrupt. 01b = APIC based interrupt (see Core::X86::Msr::McaIntrCfg[DeferredLvtOffset]). 10b = SMI trigger event. 11b = Reserved.
36:35	Reserved.
34	LogDeferredInMcaStat. Read-write. Reset: 0. Init: BIOS,1. 1=Log deferred errors in MCA::KPX::GMI::MCA_STATUS_KPX_GMI and MCA::KPX::GMI::MCA_ADDR_KPX_GMI in addition to MCA::KPX::GMI::MCA_DESTAT_KPX_GMI and MCA::KPX::GMI::MCA_DEADDR_KPX_GMI. 0=Only log deferred errors in MCA::KPX::GMI::MCA_DESTAT_KPX_GMI and MCA::KPX::GMI::MCA_DEADDR_KPX_GMI. This bit does not affect logging of deferred errors in MCA::KPX::GMI::MCA_SYND_KPX_GMI, MCA::KPX::GMI::MCA_MISC0_KPX_GMI.
33	Reserved.
32	McaXEnable. Read-write. Reset: 0. Init: BIOS,1. Check: 1. 1=Software has acknowledged support for the MCAX feature set. 0=Software has not acknowledged support for the MCAX feature set. All uncorrected and fatal errors will cause an ErrorEvent packet to be generated. Deferred error interrupts are configured via Core::X86::Msr::McaIntrCfg.
31:9	Reserved.
8	McaLsbInStatusSupported. Read-only. Reset: 1. 1=MCA::KPX::GMI::MCA_CONFIG_KPX_GMI[McaLsbInStatusSupported] indicates that AddrLsb is located in McaStatus registers.
7:6	Reserved.
5	DeferredIntTypeSupported. Read-only. Reset: 1. 1=MCA::KPX::GMI::MCA_CONFIG_KPX_GMI[DeferredIntType] controls the type of interrupt generated on a deferred error. Deferred errors are supported in this bank only if MCA::KPX::GMI::MCA_CONFIG_KPX_GMI[DeferredErrorLoggingSupported]=1.
4:3	Reserved.
2	DeferredErrorLoggingSupported. Read-only. Reset: 1. 1=Deferred errors are supported in this MCA bank, and MCA::KPX::GMI::MCA_CONFIG_KPX_GMI[LogDeferredInMcaStat] controls the logging behavior of these errors. MCA::KPX::GMI::MCA_DESTAT_KPX_GMI and MCA::KPX::GMI::MCA_DEADDR_KPX_GMI are supported in this MCA bank. 0=Deferred errors are not supported in this bank.
1	Reserved.
0	McaX. Read-only. Reset: 1. 1=This bank provides Machine Check Architecture Extensions. Up to 4 additional MISC registers (MISC1-MISC4) are supported. MCA::KPX::GMI::MCA_MISC0_KPX_GMI[BlkPtr] indicates the presence of the additional MISC registers, but is not used to determine their MSR numbers. Deferred error interrupt type is specifiable by MCA bank. MCA::KPX::GMI::MCA_STATUS_KPX_GMI[TCC] is present.

MSRC000_21[3...4]5 [KPX_GMI IP Identification] (MCA::KPX::GMI::MCA_IPID_KPX_GMI)

Reset: 0000_0269_0000_0000h.

The MCA::KPX::GMI::MCA_IPID_KPX_GMI register is used by software to determine what IP type and revision is associated with the MCA bank.

_inst[GMICONTAINER[1:0]KPXGMI]_n[2,0]_aliasMSR; MSRC000_2135

_ccd[1:0]_instGMICONTAINER12KPXGMI_n[3,1]_aliasMSR; MSRC000_2145

Bits	Description
63:48	McaType . Read-only. Reset: 0000h. The McaType of the MCA bank within this IP.
47:44	InstanceIdHi . Read-write. Reset: 0h. The HI value instance ID of this IP. This is initialized to a unique ID per instance of this register.
43:32	HardwareID . Read-only. Reset: 269h. The Hardware ID of the IP associated with this MCA bank.
31:0	InstanceId . Read-write. Reset: 0000_0000h. The instance ID of this IP. This is initialized to a unique ID per instance of this register.
	Init: _ccd0_instGMICONTAINER12KPXGMI_n1_aliasMSR: 3090_0400h
	Init: _ccd1_instGMICONTAINER12KPXGMI_n3_aliasMSR: 3290_0400h
	Init: _instGMICONTAINER0KPXGMI_n0_aliasMSR: 1890_0400h
	Init: _instGMICONTAINER1KPXGMI_n2_aliasMSR: 18A0_0400h

MSRC000_21[3...4]6 [KPX_GMI Machine Check Syndrome] (MCA::KPX::GMI::MCA_SYND_KPX_GMI)

Read-write, Volatile. Reset: Cold, 0000_0000_0000_0000h.

Logs physical location information associated with error in MCA::KPX::GMI::MCA_STATUS_KPX_GMI Thread 0

_inst[GMICONTAINER[1:0]KPXGMI]_n[2,0]_aliasMSR; MSRC000_2136

_ccd[1:0]_instGMICONTAINER12KPXGMI_n[3,1]_aliasMSR; MSRC000_2146

Bits	Description
63:33	Reserved.
32	Syndrom . Read-write, Volatile. Reset: Cold, 0. Contains the syndrome, if any, associated with the error logged in MCA::KPX::GMI::MCA_STATUS_KPX_GMI. The low-order bit of the syndrome is stored in bit 0, and the syndrome has a length specified by MCA::KPX::GMI::MCA_SYND_KPX_GMI[Length]. The Syndrome field is only valid when MCA::KPX::GMI::MCA_SYND_KPX_GMI[Length] is not 0.
31:27	Reserved.
26:24	ErrorPriority . Read-write, Volatile. Reset: Cold, 0h. Encodes the priority of the error logged in MCA::KPX::GMI::MCA_SYND_KPX_GMI. 3'b000 = No error; 3'b001 = Reserved; 3'b010 = Corrected Error; 3'b011 = Deferred Error; 3'b100 = Uncorrected Error; 3'b101 = Fatal Error; all others reserved.
23:18	Length . Read-write, Volatile. Reset: Cold, 00h. Specifies the length in bits of the syndrome contained in MCA::KPX::GMI::MCA_SYND_KPX_GMI[Syndrome]. A value of 0 indicates that there is no valid syndrome in MCA::KPX::GMI::MCA_SYND_KPX_GMI. For example, a syndrome length of 9 means that MCA::KPX::GMI::MCA_SYND_KPX_GMI[Syndrome] bits [8:0] contains a valid syndrome.
17:0	ErrorInformation . Read-write, Volatile. Reset: Cold, 0_0000h. Contains error-specific information about the location of the error. Decoding is available in Table 81 [MCA_SYND_KPX_GMI].

Table 81: MCA_SYND_KPX_GMI

Error Type	Bits	Description
RAMECC	[17:0]	Reserved
ARCIns	[17:0]	Reserved
ARCDData	[17:0]	Reserved
APB	[17:0]	Reserved

**MSRC000_21[3...4]8 [KPX_GMI Machine Check Deferred Error Status]
(MCA::KPX::GMI::MCA_DESTAT_KPX_GMI)**

Reset: Cold,0000_0000_0000_0000h.

Holds status information for the first deferred error seen in this bank.

_inst[GMICONTAINER[1:0]KPXGMI]_n[2,0]_aliasMSR; MSRC000_2138

_ccd[1:0]_instGMICONTAINER12KPXGMI_n[3,1]_aliasMSR; MSRC000_2148

Bits	Description
63	Val. Read-write, Volatile. Reset: Cold,0. 1=A valid error has been detected (whether it is enabled or not).
62	Overflow. Read-write, Volatile. Reset: Cold,0. 1=An error was detected while the valid bit (Val) was set; at least one error was not logged. Overflow is set independently of whether the existing error is overwritten. (See the section on overwrite priorities.)
61:59	RESERV4. Read-write. Reset: Cold,0h.
58	AddrV. Read-write, Volatile. Reset: Cold,0. 1=MCA::KPX::GMI::MCA_DEADDR_KPX_GMI contains address information associated with the error.
57:54	RESERV3. Read-write. Reset: Cold,0h.
53	SyndV. Read-write, Volatile. Reset: Cold,0. 1=This error logged information in MCA::KPX::GMI::MCA_SYND_KPX_GMI. If MCA::KPX::GMI::MCA_SYND_KPX_GMI[ErrorPriority] is the same as the priority of the error in MCA::KPX::GMI::MCA_STATUS_KPX_GMI, then the information in MCA::KPX::GMI::MCA_SYND_KPX_GMI is associated with the error in MCA::KPX::GMI::MCA_DESTAT_KPX_GMI.
52:45	RESERV2. Read-write. Reset: Cold,00h.
44	Deferred. Read-write, Volatile. Reset: Cold,0. 1=A deferred error was created. A deferred error is the result of an uncorrectable data error which did not immediately cause a processor exception; poison is created and an exception is deferred until the poison data is consumed.
43:30	RESERV1. Read-write. Reset: Cold,0000h.
29:24	AddrLsb. Read-write, Volatile. Reset: Cold,00h. Specifies the least significant valid bit of the address contained in MCA::KPX::GMI::MCA_ADDR_KPX_GMI[ErrorAddr]. A value of 0 indicates that MCA::KPX::GMI::MCA_ADDR_KPX_GMI[55:0] contains a valid byte address. A value of 6 indicates that MCA::KPX::GMI::MCA_ADDR_KPX_GMI[55:6] contains a valid cache line address and that MCA::KPX::GMI::MCA_ADDR_KPX_GMI[5:0] are not part of the address and should be ignored by error handling software. A value of 12 indicates that MCA::KPX::GMI::MCA_ADDR_KPX_GMI[55:12] contain a valid 4KB memory page and that MCA::KPX::GMI::MCA_ADDR_KPX_GMI[11:0] should be ignored by error handling software.
23:22	RESERV0. Read-write. Reset: Cold,0h.
21:16	ErrorCodeExt. Read-write, Volatile. Reset: Cold,00h. Logs an extended error code when an error is detected. This model-specific field is used in conjunction with ErrorCode? to identify the error sub-type for root cause analysis.
15:0	ErrorCode. Read-write, Volatile. Reset: Cold,0000h. Error code for this error.

MSRC000_2149 [KPX_GMI Deferred Error Address] (MCA::KPX::GMI::MCA_DEADDR_KPX_GMI)

Read-only. Reset: Cold,0000_0000_0000_0000h.

The MCA::KPX::GMI::MCA_DEADDR_KPX_GMI register stores the address associated with the error in MCA::KPX::GMI::MCA_DESTAT_KPX_GMI. The register is only meaningful if MCA::KPX::GMI::MCA_DESTAT_KPX_GMI[Val]=1 and MCA::KPX::GMI::MCA_DESTAT_KPX_GMI[AddrV]=1. The lowest valid bit of the address is defined by MCA::KPX::GMI::MCA_DESTAT_KPX_GMI[AddrLsb].

_ccd[1:0]_instGMICONTAINER12KPXGMI_n[3,1]_aliasMSR; MSRC000_2149

Bits	Description
63:0	ErrorAddr. Read-only. Reset: Cold,0000_0000_0000_0000h. Contains the address, if any, associated with the error logged in MCA::KPX::GMI::MCA_DESTAT_KPX_GMI.

**MSRC001_041[3...4] [KPX_GMI Machine Check Control Mask]
(MCA::KPX::GMI::MCA_CTL_MASK_KPX_GMI)**

Read-write. Reset: 0000_0000_0000_0000h.

Inhibit detection of an error source.

_inst[GMICONTAINER[1:0]KPXGMI]_n[2,0]_aliasMSR; MSRC001_0413

_ccd[1:0]_instGMICONTAINER12KPXGMI_n[3,1]_aliasMSR; MSRC001_0414

Bits	Description
63:4	Reserved.
3	APB. Read-write. Reset: 0. PHY APB error
2	ARCData. Read-write. Reset: 0. ARC data buffer parity error
1	ARCIns. Read-write. Reset: 0. ARC instruction buffer parity error
0	RAMECC. Read-write. Reset: 0. RAM ECC Error.

3.2.5.16 PCS GMI

**MSR0000_0444...MSRC000_2110 [PCS_GMI Machine Check Control]
(MCA::PCS::GMI::MCA_CTL_PCS_GMI)**

Read-write. Reset: 0000_0000_0000_0000h.

0=Disables error reporting for the corresponding error. 1=Enables error reporting via machine check exception for the corresponding error. The MCA::PCS::GMI::MCA_CTL_PCS_GMI register must be enabled by the corresponding enable bit in Core::X86::Msr::MCG_CTL. Does not affect error detection, correction, or logging.

_inst[GMICONTAINER[1:0]PCSGMI]_n[2,0]_aliasMSRLEGACY; MSR0000_0444

_inst[GMICONTAINER[1:0]PCSGMI]_n[2,0]_aliasMSR; MSRC000_2110

Bits	Description
63:32	Reserved.
31	TwixDataLoss. Read-write. Reset: 0. For gmi3
30	LFDSFcinitTimeoutErr. Read-write. Reset: 0. For gmi3
29	LFDSTrainingTimeoutErr. Read-write. Reset: 0. For gmi3
28	RxCMDPktErr. Read-write. Reset: 0. RxCMDPktErr
27	LinkSubRxTimeoutErr. Read-write. Reset: 0. LinkSubRxTimeoutErr
26	LinkSubTxTimeoutErr. Read-write. Reset: 0. LinkSubTxTimeoutErr
25	RxReplayTimeoutErr. Read-write. Reset: 0. RxReplayTimeoutErr for xGMI
24	TxReplayTimeoutErr. Read-write. Reset: 0. TxReplayTimeoutErr for xGMI
23	SyncHdrErr_TwixRxBuff. Read-write. Reset: 0. SyncHdrErr for xGMI. TwixRxBuff for gmi3
22	ReplayAttemptErr. Read-write. Reset: 0. ReplayAttemptErr for xGMI
21	RecoveryRelockAttemptErr. Read-write. Reset: 0. RecoveryRelockAttemptErr
20	RecoveryAttemptErr. Read-write. Reset: 0. RecoveryAttemptErr
19	ReadySerialAttemptErr. Read-write. Reset: 0. ReadySerialAttemptErr
18	ReadySerialTimeoutErr. Read-write. Reset: 0. ReadySerialTimeoutErr
17	RecoveryTimeoutErr. Read-write. Reset: 0. RecoveryTimeoutErr
16	FCInitTimeoutErr. Read-write. Reset: 0. FCInitTimeoutErr
15	DataStartupLimitErr. Read-write. Reset: 0. DataStartupLimitErr
14	FlowCtrlCRCErr_TwixOffline. Read-write. Reset: 0. FlowCtrlCRCErr for xGMI. TwixOffline for gmi3
13	DeskewErr. Read-write. Reset: 0. DeskewErr
12	ElasticFifoOverflowErr. Read-write. Reset: 0. ElasticFifoOverflowErr
11	ReplaFifoUnderflowErr. Read-write. Reset: 0. ReplayFifoUnderflowErr
10	ReplayFifoOverflowErr. Read-write. Reset: 0. ReplayFifoOverflowErr
9	DataParityErr_TxTwixOverflow. Read-write. Reset: 0. DataParityErr for xGMI. TxTwixOverflow for gmi3
8	ReplayBufParityErr. Read-write. Reset: 0. ReplayBufParityErr
7	TxVcidDataErr_TxMetaDataErr_TxTwixFifoUnderflow. Read-write. Reset: 0. TxVcidDataErr for xGMI2. TXVcidDataErr for xGMI3. TxTwixFifoUnderflow for gmi3
6	BERExceededErr. Read-write. Reset: 0. BERExceededErr
5	CRCErr. Read-write. Reset: 0. CRCErr
4	RxFifoOverflowErr. Read-write. Reset: 0. RxFifoOverflowErr
3	RxFifoUnderflowErr. Read-write. Reset: 0. RxFifoUnderflowErr
2	FlowCtrlAckErr_ReplayParityTwix. Read-write. Reset: 0. FlowCtrlAckErr for xGMI. ReplayParityTwix for gmi3
1	TrainingErr. Read-write. Reset: 0. TrainingErr.
0	DataLossErr. Read-write. Reset: 0. DataLossErr

**MSR0000_0448...MSRC000_2120 [PCS_GMI Machine Check Control]
(MCA::PCS::GMI::MCA_CTL_PCS_GMI_1)**

Read-write. Reset: 0000_0000_0000_0000h.

0=Disables error reporting for the corresponding error. 1=Enables error reporting via machine check exception for the corresponding error. The MCA::PCS::GMI::MCA_CTL_PCS_GMI register must be enabled by the corresponding enable bit in Core::X86::Msr::MCG_CTL. Does not affect error detection, correction, or logging.

_ccd[1:0]_instGMICONTAINER12PCSGMI_n[3,1]_aliasMSRLEGACY; MSR0000_0448

_ccd[1:0]_instGMICONTAINER12PCSGMI_n[3,1]_aliasMSR; MSRC000_2120

Bits	Description
63:32	Reserved.
31	TwixDataLoss. Read-write. Reset: 0. TwixDataLoss
30	LFDSFcinitTimeoutErr. Read-write. Reset: 0. LFDSFcinitTimeoutErr
29	LFDSTrainingTimeoutErr. Read-write. Reset: 0. LFDSTrainingTimeoutErr
28	RxCMDPktErr. Read-write. Reset: 0. RxCMDPktErr
27	LinkSubRxTimeoutErr. Read-write. Reset: 0. LinkSubRxTimeoutErr
26	LinkSubTxTimeoutErr. Read-write. Reset: 0. LinkSubTxTimeoutErr
25	RxLfdsFifoUnderflowErr. Read-write. Reset: 0. RxLfdsFifoUnderflowErr
24	RxLfdsFifoOverflowErr. Read-write. Reset: 0. RxLfdsFifoOverflowErr
23	TwixRxBuff. Read-write. Reset: 0. TwixRxBuff
22	DeskewAbortErr. Read-write. Reset: 0. DeskewAbortErr
21	RecoveryRelockAttemptErr. Read-write. Reset: 0. RecoveryRelockAttemptErr
20	RecoveryAttemptErr. Read-write. Reset: 0. RecoveryAttemptErr
19	ReadySerialAttemptErr. Read-write. Reset: 0. ReadySerialAttemptErr
18	ReadySerialTimeoutErr. Read-write. Reset: 0. ReadySerialTimeoutErr
17	RecoveryTimeoutErr. Read-write. Reset: 0. RecoveryTimeoutErr
16	FCInitTimeoutErr. Read-write. Reset: 0. FCInitTimeoutErr
15	DataStartupLimitErr. Read-write. Reset: 0. DataStartupLimitErr
14	TwixOffline. Read-write. Reset: 0. TwixOffline
13	DeskewErr. Read-write. Reset: 0. DeskewErr
12	ElasticFifoOverflowErr. Read-write. Reset: 0. ElasticFifoOverflowErr
11	ReplayFifoUnderflowErr. Read-write. Reset: 0. ReplayFifoUnderflowErr
10	ReplayFifoOverflowErr. Read-write. Reset: 0. ReplayFifoOverflowErr
9	TxTwixOverflow. Read-write. Reset: 0. TxTwixOverflow
8	ReplayBufParityErr. Read-write. Reset: 0. ReplayBufParityErr
7	TxTwixFifoUnderflow. Read-write. Reset: 0. TxTwixFifoUnderflow
6	BERExceededErr. Read-write. Reset: 0. BERExceededErr
5	CRCErr. Read-write. Reset: 0. CRCErr
4	RxFifoOverflowErr. Read-write. Reset: 0. RxFifoOverflowErr
3	RxFifoUnderflowErr. Read-write. Reset: 0. RxFifoUnderflowErr
2	ReplayParityTwix. Read-write. Reset: 0. ReplayParityTwix
1	TrainingErr. Read-write. Reset: 0. TrainingErr.
0	DataLossErr. Read-write. Reset: 0. DataLossErr

**MSR0000_0445...MSRC000_2121 [PCS_GMI Machine Check Status]
(MCA::PCS::GMI::MCA_STATUS_PCS_GMI)**

Reset: Cold,0000_0000_0000_0000h.

Logs information associated with errors.

_inst[GMICONTAINER[1:0]PCSGMI]_n[2,0]_aliasMSRLEGACY; MSR0000_0445

_ccd[1:0]_instGMICONTAINER12PCSGMI_n[3,1]_aliasMSRLEGACY; MSR0000_0449

_inst[GMICONTAINER[1:0]PCSGMI]_n[2,0]_aliasMSR; MSRC000_2111

_ccd[1:0]_instGMICONTAINER12PCSGMI_n[3,1]_aliasMSR; MSRC000_2121

Bits	Description
63	Val. Reset: Cold,0. 1=A valid error has been detected. This bit should be cleared by software after the register has been read. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
62	Overflow. Reset: Cold,0. 1=An error was detected while the valid bit (Val) was set; at least one error was not logged. Overflow is set independently of whether the existing error is overwritten. See 3.1.3 [Machine Check Errors]. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
61	UC. Reset: Cold,0. 1=The error was not corrected by hardware. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
60	En. Reset: Cold,0. 1=MCA error reporting is enabled for this error, as indicated by the corresponding bit in MCA::PCS::GMI::MCA_CTL_PCS_GMI. This bit is a copy of bit in MCA::PCS::GMI::MCA_CTL_PCS_GMI for this error. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
59	MiscV. Reset: Cold,0. 1=Valid thresholding in MCA::PCS::GMI::MCA_MISC0_PCS_GMI. In certain modes, MISC registers are owned by platform firmware and will RAZ when read by non-SMM code. Therefore, it is possible for MiscV=1 and the MISC register to read as all zeros. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
58	AddrV. Reset: Cold,0. 1=MCA::PCS::GMI::MCA_ADDR_PCS_GMI contains address information associated with the error. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
57	PCC. Reset: Cold,0. 1=Hardware context held by the processor may have been corrupted. Continued operation of the system may have unpredictable results. The error is not recoverable or survivable, and the system should be reinitialized. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
56	ErrCoreIdVal. Reset: Cold,0. 1=The ErrCoreId field is valid. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
55	TCC. Reset: Cold,0. 1=Hardware context of the process thread to which the error was reported may have been corrupted. Continued operation of the thread may have unpredictable results. The thread must be terminated. Only meaningful when MCA::PCS::GMI::MCA_STATUS_PCS_GMI[PCC]=0. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
54	RESERV54. Reset: Cold,0. MCA_STATUS Register Reserved bit. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
53	SyndV. Reset: Cold,0. 1=This error logged information in MCA::PCS::GMI::MCA_SYND_PCS_GMI. If MCA::PCS::GMI::MCA_SYND_PCS_GMI[ErrorPriority] is the same as the priority of the error in MCA::PCS::GMI::MCA_STATUS_PCS_GMI, then the information in MCA::PCS::GMI::MCA_SYND_PCS_GMI is associated with the error in MCA::PCS::GMI::MCA_STATUS_PCS_GMI. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
52	Reserved.
51:47	RESERV47. Reset: Cold,00h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.

46	CECC. Reset: Cold,0. 1=The error was a correctable ECC error according to the restrictions of the ECC algorithm. UC indicates whether the error was actually corrected by the processor. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
45	UECC. Reset: Cold,0. 1=The error was an uncorrectable ECC error according to the restrictions of the ECC algorithm. UC indicates whether the error was actually corrected by the processor. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
44	Deferred. Reset: Cold,0. 1=A deferred error was created. A deferred error is the result of an uncorrectable data error which did not immediately cause a processor exception; an exception is deferred until the erroneous data is consumed. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
43	Poison. Reset: Cold,0. 1=The error was the result of attempting to consume poisoned data. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
42:41	RESERV41. Reset: Cold,0h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
40	Scrub. Reset: Cold,0. 1=The error was the result of a scrub operation. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
39:38	RESERV38. Reset: Cold,0h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
37:32	ErrCoreId. Reset: Cold,00h. When ErrCoreIdVal=1 this field indicates which core within the processor is associated with the error; Otherwise this field is reserved. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
31:30	RESERV30. Reset: Cold,0h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
29:24	AddrLsb. Reset: Cold,00h. Specifies the least significant valid bit of the address contained in MCA::PCS::GMI::MCA_ADDR_PCS_GMI[ErrorAddr]. A value of 0 indicates that MCA::PCS::GMI::MCA_ADDR_PCS_GMI[55:0] contains a valid byte address. A value of 6 indicates that MCA::PCS::GMI::MCA_ADDR_PCS_GMI[55:6] contains a valid cache line address and that MCA::PCS::GMI::MCA_ADDR_PCS_GMI[5:0] are not part of the address and should be ignored by error handling software. A value of 12 indicates that MCA::PCS::GMI::MCA_ADDR_PCS_GMI[55:12] contain a valid 4KB memory page and that MCA::PCS::GMI::MCA_ADDR_PCS_GMI[11:0] should be ignored by error handling software. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
23:22	RESERV22. Reset: Cold,0h. MCA_STATUS Register Reserved bits. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
21:16	ErrorCodeExt. Reset: Cold,00h. Extended Error Code. This field is used to identify the error type for root cause analysis. This field indicates which bit position in MCA::PCS::GMI::MCA_CTL_PCS_GMI enables error reporting for the logged error. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.
15:0	ErrorCode. Reset: Cold,0000h. Error code for this error. See 3.1.3.3 [Error Codes] for details on decoding this field. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read,Write-0-only,Error-on-write-1.

Table 82: MCA_STATUS_PCS_GMI

Error Type	ErrorCode Ext	UC	PCC	TCC	Deferred	Poison	AddrV
DataLossErr	0x0					-	-
TrainingErr	0x1					-	-
FlowCtrlAck Err_ReplayP	0x2					-	-

arityTwix							
RxFifoUnderflowErr	0x3					-	-
RxFifoOverflowErr	0x4					-	-
CRCErr	0x5					-	-
BERExceededErr	0x6					-	-
TxVcidDataErr_TxMetaDataErr_TxTwixFifoUnderflow	0x7					-	-
ReplayBufParityErr	0x8					-	-
DataParityErr_TxTwixOverflow	0x9					-	-
ReplayFifoOverflowErr	0xa					-	-
ReplaFifoUnderflowErr	0xb					-	-
ElasticFifoOverflowErr	0xc					-	-
DeskewErr	0xd					-	-
FlowCtrlCRCErr_TwixOffline	0xe					-	-
DataStartupLimitErr	0xf					-	-
FCInitTimeoutErr	0x10					-	-
RecoveryTimeoutErr	0x11					-	-
ReadySerialTimeoutErr	0x12					-	-
ReadySerialAttemptErr	0x13					-	-
RecoveryAttemptErr	0x14					-	-
RecoveryRelockAttemptErr	0x15					-	-
ReplayAttemptErr	0x16					-	-
SyncHdrErr_TwixRxBuff	0x17					-	-
TxReplayTimeoutErr	0x18					-	-
RxReplayTimeoutErr	0x19					-	-

LinkSubTxTimeoutErr	0x1a					-	-
LinkSubRxTimeoutErr	0x1b					-	-
RxCMDPktErr	0x1c					-	-
LFDSTrainingTimeoutErr	0x1d					-	-
LFDSFcinitTimeoutErr	0x1e					-	-
TwixDataLoss	0x1f					-	-

MSR0000_0446...MSRC000_2122 [PCS_GMI Machine Check Address] (MCA::PCS::GMI::MCA_ADDR_PCS_GMI)

Read-only. Reset: Cold,0000_0000_0000_0000h.

MCA::PCS::GMI::MCA_ADDR_PCS_GMI stores an address and other information associated with the error in MCA::PCS::GMI::MCA_STATUS_PCS_GMI. The register is only meaningful if MCA::PCS::GMI::MCA_STATUS_PCS_GMI[Val]=1 and MCA::PCS::GMI::MCA_STATUS_PCS_GMI[AddrV]=1.

_inst[GMICONTAINER[1:0]PCSGMI]_n[2,0]_aliasMSRLEGACY; MSR0000_0446

_ccd[1:0]_instGMICONTAINER12PCSGMI_n[3,1]_aliasMSRLEGACY; MSR0000_044A

_inst[GMICONTAINER[1:0]PCSGMI]_n[2,0]_aliasMSR; MSRC000_2122

_ccd[1:0]_instGMICONTAINER12PCSGMI_n[3,1]_aliasMSR; MSRC000_2122

Bits	Description
63:0	ErrorAddr. Read-only. Reset: Cold,0000_0000_0000_0000h. Contains the address, if any, associated with the error logged in MCA::PCS::GMI::MCA_STATUS_PCS_GMI.

Table 83: MCA_ADDR_PCS_GMI

Error Type	Bits	Description
DataLossErr	[56:0]	Reserved
TrainingErr	[56:0]	Reserved
FlowCtrlAckErr_ReplayParityTwix	[56:0]	Reserved
RxFifoUnderflowErr	[56:0]	Reserved
RxFifoOverflowErr	[56:0]	Reserved
CRCErr	[56:0]	Reserved
BERExceededErr	[56:0]	Reserved
TxVcidDataErr_TxMetaDataErr_TxTwixFifoUnderflow	[56:0]	Reserved
ReplayBufParityErr	[56:0]	Reserved
DataParityErr_TxTwixOverflow	[56:0]	Reserved
ReplayFifoOverflowErr	[56:0]	Reserved
ReplaFifoUnderflowErr	[56:0]	Reserved
ElasticFifoOverflowErr	[56:0]	Reserved
DeskewErr	[56:0]	Reserved
FlowCtrlCRCErr_TwixOffline	[56:0]	Reserved
DataStartupLimitErr	[56:0]	Reserved
FCInitTimeoutErr	[56:0]	Reserved
RecoveryTimeoutErr	[56:0]	Reserved
ReadySerialTimeoutErr	[56:0]	Reserved

ReadySerialAttemptErr	[56:0]	Reserved
RecoveryAttemptErr	[56:0]	Reserved
RecoveryRelockAttemptErr	[56:0]	Reserved
ReplayAttemptErr	[56:0]	Reserved
SyncHdrErr_TwixRxBuff	[56:0]	Reserved
TxReplayTimeoutErr	[56:0]	Reserved
RxReplayTimeoutErr	[56:0]	Reserved
LinkSubTxTimeoutErr	[56:0]	Reserved
LinkSubRxTimeoutErr	[56:0]	Reserved
RxCMDPktErr	[56:0]	Reserved
LFDSTrainingTimeoutErr	[56:0]	Reserved
LFDSFcinitTimeoutErr	[56:0]	Reserved
TwixDataLoss	[56:0]	Reserved

**MSR0000_0447...MSRC000_2123 [PCS_GMI Machine Check Miscellaneous 0]
(MCA::PCS::GMI::MCA_MISC0_PCS_GMI)**

Log miscellaneous information associated with errors.

_inst[GMICONTAINER[1:0]PCSGMI]_n[2,0]_aliasMSRLEGACY; MSR0000_0447

_ccd[1:0]_instGMICONTAINER12PCSGMI_n[3,1]_aliasMSRLEGACY; MSR0000_044B

_inst[GMICONTAINER[1:0]PCSGMI]_n[2,0]_aliasMSR; MSRC000_2113

_ccd[1:0]_instGMICONTAINER12PCSGMI_n[3,1]_aliasMSR; MSRC000_2123

Bits	Description
63	Valid. Reset: 1. 1=A valid CntP field is present in this register. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read-only.
62	CntP. Reset: 1. 1=A valid threshold counter is present. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read-only.
61	Locked. Reset: 0. 1=Writes to this register are ignored. This bit is set by BIOS to indicate that this register is not available for OS use. BIOS should set this bit if ThresholdIntType is set to SMI. AccessType: Core::X86::Msrr::HWCR[McStatusWrEn] ? Read-write : Read-only.
60	IntP. Reset: 1. 1=ThresholdIntType can be used to generate interrupts. 0=ThresholdIntType and interrupt generation are not supported. AccessType: (Core::X86::Msrr::HWCR[McStatusWrEn] !MCA::PCS::GMI::MCA_MISC0_PCS_GMI[Locked]) ? Read-write : Read-only.
59:56	Reserved.
55:52	LvtOffset. Reset: 0h. One per die. For error thresholding interrupts, specifies the address of the LVT entry in the APIC registers as follows: LVT address = (LvtOffset shifted left 4 bits) + 500h (see Core::X86::Apic::ExtendedInterruptLvtEntries). AccessType: (Core::X86::Msrr::HWCR[McStatusWrEn] !MCA::PCS::GMI::MCA_MISC0_PCS_GMI[Locked]) ? Read-write : Read-only.
51	CntEn. Reset: 0. 1=Count thresholding errors. AccessType: (Core::X86::Msrr::HWCR[McStatusWrEn] !MCA::PCS::GMI::MCA_MISC0_PCS_GMI[Locked]) ? Read-write : Read-only.
50:49	ThresholdIntType. Reset: Cold,0h. Specifies the type of interrupt signaled when Ovrflw is set and IntP==1. 00b = No interrupt. 01b = APIC based interrupt (see Core::X86::Msrr::McaIntrCfg[ThresholdLvtOffset]). 10b = SMI trigger event. 11b = Reserved. AccessType: (Core::X86::Msrr::HWCR[McStatusWrEn] !MCA::PCS::GMI::MCA_MISC0_PCS_GMI[Locked]) ? Read-write : Read-only.
48	Ovrflw. Reset: Cold,0. Set by hardware when ErrCnt transitions from FFEh to FFFh. When this field is set, ErrCnt no longer increments. When this bit is set, the interrupt selected by the ThresholdIntType field is generated. AccessType: (Core::X86::Msrr::HWCR[McStatusWrEn] !MCA::PCS::GMI::MCA_MISC0_PCS_GMI[Locked]) ? Read-write : Read-only.
47:44	Reserved.
43:32	ErrCnt. Reset: Cold,000h. This is written by software to set the starting value of the error counter. This is incremented by hardware when errors are logged. When this counter overflows, it stays at FFFh (no rollover). The threshold value, written by software, is (FFFh - the desired error count (the number of errors necessary in order for an interrupt to be taken)); the desired error count of 0 (a write value of FFFh) is not supported. AccessType: (Core::X86::Msrr::HWCR[McStatusWrEn] !MCA::PCS::GMI::MCA_MISC0_PCS_GMI[Locked]) ? Read-write : Read-only.
31:24	BlkPtr. Read-write. Reset: 00h. 00h=Extended MISC MSR block is not valid. 01h=Extended MSR block is valid.
23:0	Reserved.

**MSRC000_21[1...2]4 [PCS_GMI Machine Check Configuration]
(MCA::PCS::GMI::MCA_CONFIG_PCS_GMI)**

Reset: 0000_0002_0000_0125h.

Controls configuration of the associated machine check bank.

_inst[GMICONTAINER[1:0]PCSGMI]_n[2,0]_aliasMSR; MSRC000_2114

_ccd[1:0]_instGMICONTAINER12PCSGMI_n[3,1]_aliasMSR; MSRC000_2124

Bits	Description
63:39	Reserved.
38:37	DeferredIntType. Read-write. Reset: 0h. Specifies the type of interrupt signaled when a deferred error is logged. 00b = No interrupt. 01b = APIC based interrupt (see Core::X86::Msr::McaIntrCfg[DeferredLvtOffset]). 10b = SMI trigger event. 11b = Reserved.
36:35	Reserved.
34	LogDeferredInMcaStat. Read-write. Reset: 0. Init: BIOS,1. 1=Log deferred errors in MCA::PCS::GMI::MCA_STATUS_PCS_GMI and MCA::PCS::GMI::MCA_ADDR_PCS_GMI in addition to MCA::PCS::GMI::MCA_DESTAT_PCS_GMI and MCA::PCS::GMI::MCA_DEADDR_PCS_GMI. 0=Only log deferred errors in MCA::PCS::GMI::MCA_DESTAT_PCS_GMI and MCA::PCS::GMI::MCA_DEADDR_PCS_GMI. This bit does not affect logging of deferred errors in MCA::PCS::GMI::MCA_SYND_PCS_GMI, MCA::PCS::GMI::MCA_MISC0_PCS_GMI.
33	Reserved.
32	McaXEnable. Read-write. Reset: 0. Init: BIOS,1. Check: 1. 1=Software has acknowledged support for the MCAX feature set. 0=Software has not acknowledged support for the MCAX feature set. All uncorrected and fatal errors will cause an ErrorEvent packet to be generated. Deferred error interrupts are configured via Core::X86::Msr::McaIntrCfg.
31:9	Reserved.
8	McaLsbInStatusSupported. Read-only. Reset: 1. 1=MCA::PCS::GMI::MCA_CONFIG_PCS_GMI[McaLsbInStatusSupported] indicates that AddrLsb is located in McaStatus registers.
7:6	Reserved.
5	DeferredIntTypeSupported. Read-only. Reset: 1. 1=MCA::PCS::GMI::MCA_CONFIG_PCS_GMI[DeferredIntType] controls the type of interrupt generated on a deferred error. Deferred errors are supported in this bank only if MCA::PCS::GMI::MCA_CONFIG_PCS_GMI[DeferredErrorLoggingSupported]=1.
4:3	Reserved.
2	DeferredErrorLoggingSupported. Read-only. Reset: 1. 1=Deferred errors are supported in this MCA bank, and MCA::PCS::GMI::MCA_CONFIG_PCS_GMI[LogDeferredInMcaStat] controls the logging behavior of these errors. MCA::PCS::GMI::MCA_DESTAT_PCS_GMI and MCA::PCS::GMI::MCA_DEADDR_PCS_GMI are supported in this MCA bank. 0=Deferred errors are not supported in this bank.
1	Reserved.
0	McaX. Read-only. Reset: 1. 1=This bank provides Machine Check Architecture Extensions. Up to 4 additional MISC registers (MISC1-MISC4) are supported. MCA::PCS::GMI::MCA_MISC0_PCS_GMI[BlkPtr] indicates the presence of the additional MISC registers, but is not used to determine their MSR numbers. Deferred error interrupt type is specifiable by MCA bank. MCA::PCS::GMI::MCA_STATUS_PCS_GMI[TCC] is present.

MSRC000_21[1...2]5 [PCS_GMI IP Identification] (MCA::PCS::GMI::MCA_IPID_PCS_GMI)

Reset: 0000_0241_0000_0000h.

The MCA::PCS::GMI::MCA_IPID_PCS_GMI register is used by software to determine what IP type and revision is associated with the MCA bank.

_inst[GMICONTAINER[1:0]PCSGMI]_n[2,0]_aliasMSR; MSRC000_2115

_ccd[1:0]_instGMICONTAINER12PCSGMI_n[3,1]_aliasMSR; MSRC000_2125

Bits	Description
63:48	McaType. Read-only. Reset: 0000h. The McaType of the MCA bank within this IP.
47:44	InstanceIdHi. Read-write. Reset: 0h. The HI value instance ID of this IP. This is initialized to a unique ID per instance of this register.
43:32	HardwareID. Read-only. Reset: 241h. The Hardware ID of the IP associated with this MCA bank.
31:0	InstanceId. Read-write. Reset: 0000_0000h. The instance ID of this IP. This is initialized to a unique ID per instance of this register.
	Init: _ccd0_instGMICONTAINER12PCSGMI_n1_aliasMSR: 3070_9200h
	Init: _ccd1_instGMICONTAINER12PCSGMI_n3_aliasMSR: 3270_9200h
	Init: _instGMICONTAINER0PCSGMI_n0_aliasMSR: 1330_9200h
	Init: _instGMICONTAINER1PCSGMI_n2_aliasMSR: 1340_9200h

MSRC000_21[1...2]6 [PCS_GMI Machine Check Syndrome] (MCA::PCS::GMI::MCA_SYND_PCS_GMI)

Read-write, Volatile. Reset: Cold, 0000_0000_0000_0000h.

Logs physical location information associated with error in MCA::PCS::GMI::MCA_STATUS_PCS_GMI Thread 0

_inst[GMICONTAINER[1:0]PCSGMI]_n[2,0]_aliasMSR; MSRC000_2116

_ccd[1:0]_instGMICONTAINER12PCSGMI_n[3,1]_aliasMSR; MSRC000_2126

Bits	Description
63:32	Syndrome. Read-write, Volatile. Reset: Cold, 0000_0000h. Contains the syndrome, if any, associated with the error logged in MCA::PCS::GMI::MCA_STATUS_PCS_GMI. The low-order bit of the syndrome is stored in bit 0, and the syndrome has a length specified by MCA::PCS::GMI::MCA_SYND_PCS_GMI[Length]. The Syndrome field is only valid when MCA::PCS::GMI::MCA_SYND_PCS_GMI[Length] is not 0.
31:27	Reserved.
26:24	ErrorPriority. Read-write, Volatile. Reset: Cold, 0h. Encodes the priority of the error logged in MCA::PCS::GMI::MCA_SYND_PCS_GMI. 3'b000 = No error; 3'b001 = Reserved; 3'b010 = Corrected Error; 3'b011 = Deferred Error; 3'b100 = Uncorrected Error; 3'b101 = Fatal Error; all others reserved.
23:18	Length. Read-write, Volatile. Reset: Cold, 00h. Specifies the length in bits of the syndrome contained in MCA::PCS::GMI::MCA_SYND_PCS_GMI[Syndrome]. A value of 0 indicates that there is no valid syndrome in MCA::PCS::GMI::MCA_SYND_PCS_GMI. For example, a syndrome length of 9 means that MCA::PCS::GMI::MCA_SYND_PCS_GMI[Syndrome] bits [8:0] contains a valid syndrome.
17:0	ErrorInformation. Read-write, Volatile. Reset: Cold, 0_0000h. Contains error-specific information about the location of the error. Decoding is available in Table 84 [MCA_SYND_PCS_GMI].

Table 84: MCA_SYND_PCS_GMI

Error Type	Bits	Description
DataLossErr	[17:0]	Reserved
TrainingErr	[17:0]	Reserved
FlowCtrlAckErr_ReplayParityTwix	[17:0]	Reserved
RxFifoUnderflowErr	[17:0]	Reserved
RxFifoOverflowErr	[17:0]	Reserved
CRCErr	[17:0]	Reserved
BERExceededErr	[17:0]	Reserved
TxVcidDataErr_TxMetaDataErr_TxTwixFifoUnderflow	[17:0]	Reserved

ReplayBufParityErr	[17:0]	Reserved
DataParityErr_TxTwixOverflow	[17:0]	Reserved
ReplayFifoOverflowErr	[17:0]	Reserved
ReplaFifoUnderflowErr	[17:0]	Reserved
ElasticFifoOverflowErr	[17:0]	Reserved
DeskewErr	[17:0]	Reserved
FlowCtrlCRCErr_TwixOffline	[17:0]	Reserved
DataStartupLimitErr	[17:0]	Reserved
FCInitTimeoutErr	[17:0]	Reserved
RecoveryTimeoutErr	[17:0]	Reserved
ReadySerialTimeoutErr	[17:0]	Reserved
ReadySerialAttemptErr	[17:0]	Reserved
RecoveryAttemptErr	[17:0]	Reserved
RecoveryRelockAttemptErr	[17:0]	Reserved
ReplayAttemptErr	[17:0]	Reserved
SyncHdrErr_TwixRxBuff	[17:0]	Reserved
TxReplayTimeoutErr	[17:0]	Reserved
RxReplayTimeoutErr	[17:0]	Reserved
LinkSubTxTimeoutErr	[17:0]	Reserved
LinkSubRxTimeoutErr	[17:0]	Reserved
RxCMDPktErr	[17:0]	Reserved
LFDSSTrainingTimeoutErr	[17:0]	Reserved
LFDSFcinitTimeoutErr	[17:0]	Reserved
TwixDataLoss	[17:0]	Reserved

MSRC000_21[1...2]8 [PCS_GMI Machine Check Deferred Error Status] (MCA::PCS::GMI::MCA_DESTAT_PCS_GMI)

Reset: Cold,0000_0000_0000_0000h.

Holds status information for the first deferred error seen in this bank.

_inst[GMICONTAINER[1:0]PCSGMI]_n[2,0]_aliasMSR; MSRC000_2118

_ccd[1:0]_instGMICONTAINER12PCSGMI_n[3,1]_aliasMSR; MSRC000_2128

Bits	Description
63	Val. Read-write, Volatile. Reset: Cold,0. 1=A valid error has been detected (whether it is enabled or not).
62	Overflow. Read-write, Volatile. Reset: Cold,0. 1=An error was detected while the valid bit (Val) was set; at least one error was not logged. Overflow is set independently of whether the existing error is overwritten. (See the section on overwrite priorities.)
61:59	RESERV4. Read-write. Reset: Cold,0h.
58	AddrV. Read-write, Volatile. Reset: Cold,0. 1=MCA::PCS::GMI::MCA_DEADDR_PCS_GMI contains address information associated with the error.
57:54	RESERV3. Read-write. Reset: Cold,0h.
53	SyndV. Read-write, Volatile. Reset: Cold,0. 1=This error logged information in MCA::PCS::GMI::MCA_SYND_PCS_GMI. If MCA::PCS::GMI::MCA_SYND_PCS_GMI[ErrorPriority] is the same as the priority of the error in MCA::PCS::GMI::MCA_STATUS_PCS_GMI, then the information in MCA::PCS::GMI::MCA_SYND_PCS_GMI is associated with the error in MCA::PCS::GMI::MCA_DESTAT_PCS_GMI.
52:45	RESERV2. Read-write. Reset: Cold,00h.
44	Deferred. Read-write, Volatile. Reset: Cold,0. 1=A deferred error was created. A deferred error is the result of an uncorrectable data error which did not immediately cause a processor exception; poison is created and an exception is deferred until the poison data is consumed.
43:30	RESERV1. Read-write. Reset: Cold,0000h.
29:24	AddrLsb. Read-write, Volatile. Reset: Cold,00h. Specifies the least significant valid bit of the address contained in MCA::PCS::GMI::MCA_ADDR_PCS_GMI[ErrorAddr]. A value of 0 indicates that MCA::PCS::GMI::MCA_ADDR_PCS_GMI[55:0] contains a valid byte address. A value of 6 indicates that MCA::PCS::GMI::MCA_ADDR_PCS_GMI[55:6] contains a valid cache line address and that MCA::PCS::GMI::MCA_ADDR_PCS_GMI[5:0] are not part of the address and should be ignored by error handling software. A value of 12 indicates that MCA::PCS::GMI::MCA_ADDR_PCS_GMI[55:12] contain a valid 4KB memory page and that MCA::PCS::GMI::MCA_ADDR_PCS_GMI[11:0] should be ignored by error handling software.
23:22	RESERV0. Read-write. Reset: Cold,0h.
21:16	ErrorCodeExt. Read-write, Volatile. Reset: Cold,00h. Logs an extended error code when an error is detected. This model-specific field is used in conjunction with ErrorCode? to identify the error sub-type for root cause analysis.
15:0	ErrorCode. Read-write, Volatile. Reset: Cold,0000h. Error code for this error.

MSRC000_2129 [PCS_GMI Deferred Error Address] (MCA::PCS::GMI::MCA_DEADDR_PCS_GMI)

Read-only. Reset: Cold,0000_0000_0000_0000h.

The MCA::PCS::GMI::MCA_DEADDR_PCS_GMI register stores the address associated with the error in MCA::PCS::GMI::MCA_DESTAT_PCS_GMI. The register is only meaningful if MCA::PCS::GMI::MCA_DESTAT_PCS_GMI[Val]=1 and MCA::PCS::GMI::MCA_DESTAT_PCS_GMI[AddrV]=1. The lowest valid bit of the address is defined by MCA::PCS::GMI::MCA_DESTAT_PCS_GMI[AddrLsb].

_ccd[1:0]_instGMICONTAINER12PCSGMI_n[3,1]_aliasMSR; MSRC000_2129

Bits	Description
63:0	ErrorAddr. Read-only. Reset: Cold,0000_0000_0000_0000h. Contains the address, if any, associated with the error logged in MCA::PCS::GMI::MCA_DESTAT_PCS_GMI.

MSRC001_0411 [PCS_GMI Machine Check Control Mask] (MCA::PCS::GMI::MCA_CTL_MASK_PCS_GMI)

Read-write. Reset: 0000_0000_0000_0000h.

Inhibit detection of an error source.

_inst[GMICONTAINER[1:0]PCSGMI]_n[2,0]_aliasMSR; MSRC001_0411

Bits	Description
63:32	Reserved.
31	TwixDataLoss. Read-write. Reset: 0. For gmi3
30	LFDSFcinitTimeoutErr. Read-write. Reset: 0. For gmi3
29	LFDSTrainingTimeoutErr. Read-write. Reset: 0. For gmi3
28	RxCMDPktErr. Read-write. Reset: 0. RxCMDPktErr
27	LinkSubRxTimeoutErr. Read-write. Reset: 0. LinkSubRxTimeoutErr
26	LinkSubTxTimeoutErr. Read-write. Reset: 0. LinkSubTxTimeoutErr
25	RxReplayTimeoutErr. Read-write. Reset: 0. RxReplayTimeoutErr for xGMI
24	TxReplayTimeoutErr. Read-write. Reset: 0. TxReplayTimeoutErr for xGMI
23	SyncHdrErr_TwixRxBuff. Read-write. Reset: 0. SyncHdrErr for xGMI. TwixRxBuff for gmi3
22	ReplayAttemptErr. Read-write. Reset: 0. ReplayAttemptErr for xGMI
21	RecoveryRelockAttemptErr. Read-write. Reset: 0. RecoveryRelockAttemptErr
20	RecoveryAttemptErr. Read-write. Reset: 0. RecoveryAttemptErr
19	ReadySerialAttemptErr. Read-write. Reset: 0. ReadySerialAttemptErr
18	ReadySerialTimeoutErr. Read-write. Reset: 0. ReadySerialTimeoutErr
17	RecoveryTimeoutErr. Read-write. Reset: 0. RecoveryTimeoutErr
16	FCInitTimeoutErr. Read-write. Reset: 0. FCInitTimeoutErr
15	DataStartupLimitErr. Read-write. Reset: 0. DataStartupLimitErr
14	FlowCtrlCRCErr_TwixOffline. Read-write. Reset: 0. FlowCtrlCRCErr for xGMI. TwixOffline for gmi3
13	DeskewErr. Read-write. Reset: 0. DeskewErr
12	ElasticFifoOverflowErr. Read-write. Reset: 0. ElasticFifoOverflowErr
11	ReplaFifoUnderflowErr. Read-write. Reset: 0. ReplayFifoUnderflowErr
10	ReplayFifoOverflowErr. Read-write. Reset: 0. ReplayFifoOverflowErr
9	DataParityErr_TxTwixOverflow. Read-write. Reset: 0. DataParityErr for xGMI. TxTwixOverflow for gmi3
8	ReplayBufParityErr. Read-write. Reset: 0. ReplayBufParityErr
7	TxVcidDataErr_TxMetaDataErr_TxTwixFifoUnderflow. Read-write. Reset: 0. TxVcidDataErr for xGMI2. TXVcidDataErr for xGMI3. TxTwixFifoUnderflow for gmi3
6	BERExceededErr. Read-write. Reset: 0. BERExceededErr
5	CRCErr. Read-write. Reset: 0. CRCErr
4	RxFifoOverflowErr. Read-write. Reset: 0. RxFifoOverflowErr
3	RxFifoUnderflowErr. Read-write. Reset: 0. RxFifoUnderflowErr
2	FlowCtrlAckErr_ReplayParityTwix. Read-write. Reset: 0. FlowCtrlAckErr for xGMI. ReplayParityTwix for gmi3
1	TrainingErr. Read-write. Reset: 0. TrainingErr.
0	DataLossErr. Read-write. Reset: 0. DataLossErr

**MSRC001_0412 [PCS_GMI Machine Check Control Mask]
(MCA::PCS::GMI::MCA_CTL_MASK_PCS_GMI_1)**

Read-write. Reset: 0000_0000_0000_0000h.

Inhibit detection of an error source.

_ccd[1:0]_instGMICONTAINER12PCSGMI_n[3,1]_aliasMSR; MSRC001_0412

Bits	Description
63:32	Reserved.
31	TwixDataLoss. Read-write. Reset: 0. TwixDataLoss
30	LFDSFcinitTimeoutErr. Read-write. Reset: 0. LFDSFcinitTimeoutErr
29	LFDSTrainingTimeoutErr. Read-write. Reset: 0. LFDSTrainingTimeoutErr
28	RxCMDPktErr. Read-write. Reset: 0. RxCMDPktErr
27	LinkSubRxTimeoutErr. Read-write. Reset: 0. LinkSubRxTimeoutErr
26	LinkSubTxTimeoutErr. Read-write. Reset: 0. LinkSubTxTimeoutErr
25	RxLfdsFifoUnderflowErr. Read-write. Reset: 0. RxLfdsFifoUnderflowErr
24	RxLfdsFifoOverflowErr. Read-write. Reset: 0. RxLfdsFifoOverflowErr
23	TwixRxBuff. Read-write. Reset: 0. TwixRxBuff
22	DeskewAbortErr. Read-write. Reset: 0. DeskewAbortErr
21	RecoveryRelockAttemptErr. Read-write. Reset: 0. RecoveryRelockAttemptErr
20	RecoveryAttemptErr. Read-write. Reset: 0. RecoveryAttemptErr
19	ReadySerialAttemptErr. Read-write. Reset: 0. ReadySerialAttemptErr
18	ReadySerialTimeoutErr. Read-write. Reset: 0. ReadySerialTimeoutErr
17	RecoveryTimeoutErr. Read-write. Reset: 0. RecoveryTimeoutErr
16	FCInitTimeoutErr. Read-write. Reset: 0. FCInitTimeoutErr
15	DataStartupLimitErr. Read-write. Reset: 0. DataStartupLimitErr
14	TwixOffline. Read-write. Reset: 0. TwixOffline
13	DeskewErr. Read-write. Reset: 0. DeskewErr
12	ElasticFifoOverflowErr. Read-write. Reset: 0. ElasticFifoOverflowErr
11	ReplayFifoUnderflowErr. Read-write. Reset: 0. ReplayFifoUnderflowErr
10	ReplayFifoOverflowErr. Read-write. Reset: 0. ReplayFifoOverflowErr
9	TxTwixOverflow. Read-write. Reset: 0. TxTwixOverflow
8	ReplayBufParityErr. Read-write. Reset: 0. ReplayBufParityErr
7	TxTwixFifoUnderflow. Read-write. Reset: 0. TxTwixFifoUnderflow
6	BERExceededErr. Read-write. Reset: 0. BERExceededErr
5	CRCErr. Read-write. Reset: 0. CRCErr
4	RxFifoOverflowErr. Read-write. Reset: 0. RxFifoOverflowErr
3	RxFifoUnderflowErr. Read-write. Reset: 0. RxFifoUnderflowErr
2	ReplayParityTwix. Read-write. Reset: 0. ReplayParityTwix
1	TrainingErr. Read-write. Reset: 0. TrainingErr.
0	DataLossErr. Read-write. Reset: 0. DataLossErr

4 Advanced Platform Management Link (APML)

4.1 Overview

The Advanced Platform Management Link (APML) is a SMBus v2.0 compatible 2-wire processor slave interface. APML is also referred as the sideband interface (SBI).

APML is used to communicate with the Remote Management Interface (see SBI Remote Management Interface (SB-RMI) and SBI Temperature Sensor Interface (SB-TSI). For related specifications, see 1.2 [Reference Documents].

4.1.1 Definitions

Table 85: APML Definitions

Term	Description
ARA	Alert response address.
ARP	Address Resolution Protocol
EC	Embedded Controller.
KBC	Keyboard Controller.
Master or SMBus Master	The device that initiates and terminates all communication and drives the clock, SCL.
PEC	Packet error code.
POR	Power on reset.
RTS	Remote temperature sensor, typical examples are ADM1032, LM99, MAX6657, EMC1002.
SBI	Sideband interface.
SB-RMI	Remote Management interface.
Slave or SMBus slave	The slave cannot initiate SMBus communication and cannot drive the clock but can drive the data signal SDA and the alert signal ALERT_L.
TSI	Temperature sensor interface.

4.2 SBI Bus Characteristics

The SBI largely follows SMBus v2.0. This section describes the exceptions.

4.2.1 SMBus Protocol Support

The SBI follows SMBus protocol except:

- The processor does not implement SMBus master functionality.
- The SBI implements the Send Byte/Receive Byte, Read Byte/Write Byte, Block Read/Block Write and Block Write-Block Read Process Call SMBus protocols. The Send Byte/Receive Byte SMBus protocol is only supported by SB-TSI.
- Packet error checking (PEC) is not supported by SB-TSI.
- Address Resolution Protocol (ARP) is not implemented.
- Cumulative clock extensions are not enforced.

4.2.2 I2C Support

The processor supports higher I2C-defined speeds as specified in the Physical Layer Characteristics section. The processor supports the I2C master code transmission in order to reach the high-speed bus mode. Multiple SBI commands may be sent within a single high-speed mode session. Ten-bit addressing is not supported.

4.3 SBI Processor Information

4.3.1 SBI Processor Pins

Up to six processor pins are used for SBI support: two for data transfer, three for address determination and one for an interrupt output. Of the three address pins, one bit is socket_id used to determine which package is addressed. These pins do not have changeable pinstrap. The Serial Interface Clock (SIC) and Serial Interface Data (SID) pins function as the SMBus clock and data pins respectively. The SMBus alert pin (ALERT_L) is used to signal interrupts to the SMBus master.

4.3.1.1 Physical Layer Characteristics

The SIC and SID pins differ from the SMBus specification with regard to voltage. System board voltage translators are necessary to convert the SIC and SID pin voltage levels to that of the SMBus specification. SBI supports frequencies of 100 KHz, 400 KHz over SIC.

4.3.2 Processor States

SBI responds to SMBus traffic except when PWROK is de-asserted (and for a brief period after it is de-asserted). Access to internal processor state using SB-RMI is not supported under the following conditions:

- During cold and warm resets.
- During the APIC spin loop.

4.4 SBI Protocols

4.4.1 SBI Modified Block Write-Block Read Process Call

SBI uses a modified SMBus PEC-optional Block Write-Block Read Process Call protocol. The change from the SMBus protocol is support for an optional intermediate PEC byte and ACK after the ACK for Data Byte M. This PEC byte covers the data starting with the Slave Address through Data Byte M and is controlled by SBRMI::Control[PECEn]. This is the only modification to the standard SMBus PEC-optional Block Write-Block Read Process Call as defined by the SMBus Specification. The PEC byte after Data Byte N covers all previous bytes excluding the first PEC byte. Figure below shows the transmission protocol. Each byte in the protocol is sent with the most significant bit first (bit[7]). The master may reset the bus by holding the clock low for 25ms as specified by the SMBus Specification.

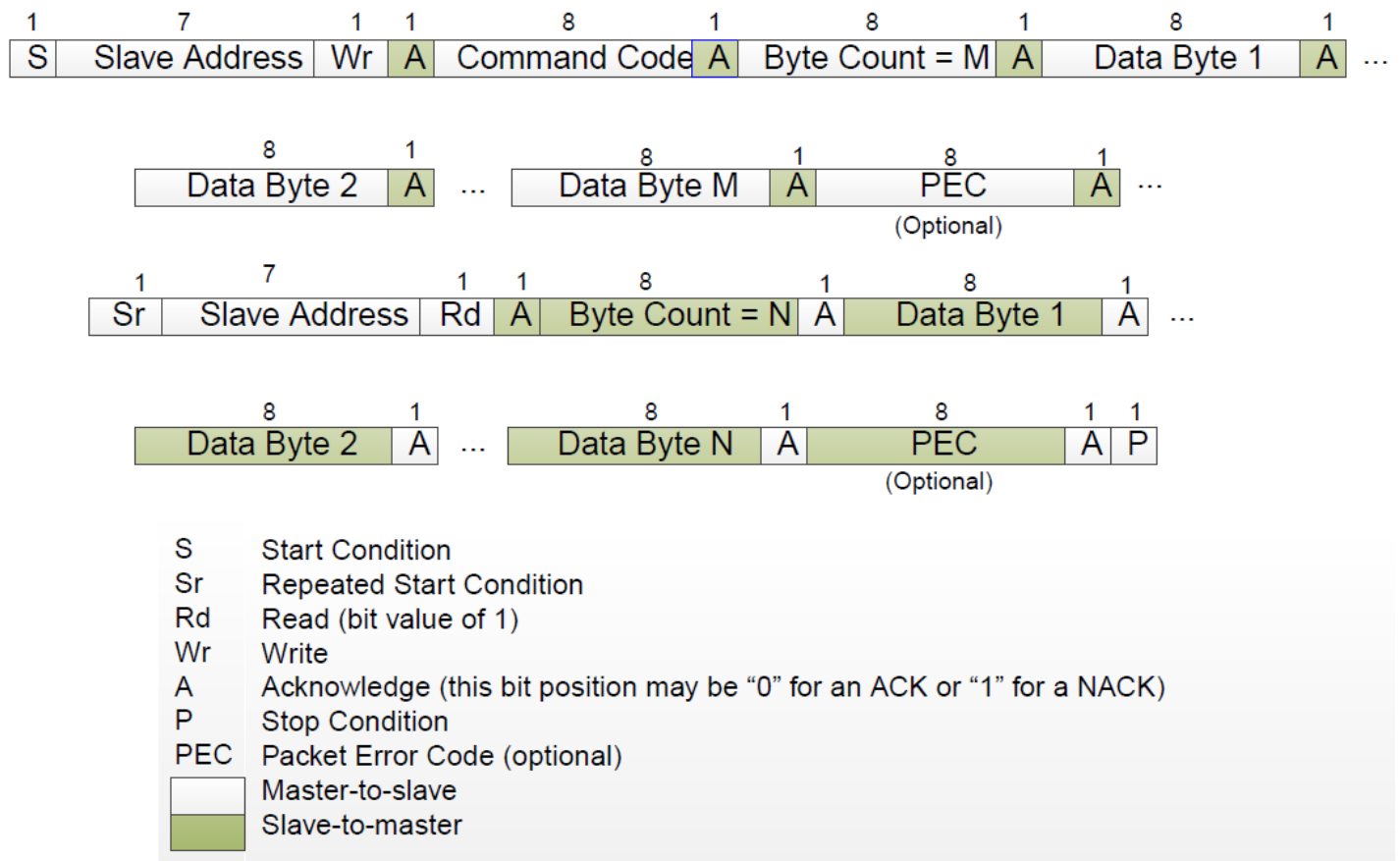


Figure 26: SBI Transmission Protocol

4.4.2 SBI Remote Management Interface (SB-RMI)

SB-RMI provides an interface for an external SMBus master that can be used to perform tasks such as monitoring the processor MCA registers, processor CPUID registers etc. SB-RMI supports signaling Alert_L when a MCE is received by any thread or when software sets SBRMI::Status[SwAlertSts]. Each package has an independent SMBUS slave port. See 4.5.1 [SBI SMBus Address].

Each package is required to contain the same number of logical threads. The SMBUS slave port attached to each package may access only the logical threads within the package. Core::X86::CpuId::SizeId identifies the number of logical threads available in a package.

4.4.2.1 SB-RMI Processor State Access

The SB-RMI Functions table describes the functions for accessing processor state. See the Processor Programming Reference of the processor family for additional information about the processor registers. MSR not listed in below table is not accessible, will get "Unsupported Command" status.

Table 86: SB-RMI Functions

Function	Description	Thread Specific
CPUID	Access to CPUID registers. General purpose registers are not altered unlike a	Y

	processor CUID instruction. Use Read CUID Command Protocol where CUID Function is placed into WrData[7:4] and register is placed in WrData[8]. Access is Read-only.	
MCA Registers	Register read command using the register address to access Core::X86::Msr::MCG_CAP determines the number of MCA banks. Use Read Processor Register Command Protocol where MSR address is placed into WrData[7:4]. Access is Read-only.	Y
DRAM Throttle	Register read or write command to access the DRAM Controller Command Throttle Register. The thread number field is not used for this request. Writes are uniformly applied to all DRAM Controller Command Throttle Register Instances within a package. Reads return Dram Controller Command Throttle Register instance 0. Access is Read-write.	N
Mailbox Service	Soft mailbox service request to firmware for power management purposes. Past implementations allowed for mailbox operations to X86 software. No usage models for communication with x86 software exists and x86 software messaging is not supported. Access is Read-write. See mailbox specific details.	N
Boot Status	Boot Status is placed in outbound message register SBRMI::MP0OutBndMsg. Access is Read-only.	N

4.4.2.1.1 SB-RMI Read Processor Register and Read CUID Commands

SB-RMI read processor register and read CUID commands are performed using the SBI Modified Block Write-Block Read Process Call. If an SMBus timeout occurs before the data is returned, a read data/status can be issued to read the data from the previous command. The previous command must be complete before a new command can be issued.

Table 87: SB-RMI Read Processor Register Command Protocol

Byte	Byte Name	Value	Notes
1	Slave Address	0111_XXX0b	Write Address.
2	Command	73h	Read CUID/Read Register Command Format.
3	WrDataLen	07h	7 Bytes.
4	WrData1	0Xh	Number of bytes to read from register. Valid values are 1 through 8.
5	WrData2	86h	Read Register command.
6	WrData3	XXXX_XXXXb	Bit[0] is Reserved. Bits[7:1] select the thread to address. 00h=Thread0. ... 7Fh=Thread127.
7	WrData4	XXh	Register Address[7:0] from the SB-RMI Functions table.
8	WrData5	XXh	Register Address[15:8] from the SB-RMI Functions table.
9	WrData6	XXh	Register Address[23:16] from the SB-RMI Functions table.
10	WrData7	XXh	Register Address[31:24] from the SB-RMI Functions table.
11	PEC	XXh	Optional PEC byte.
12	Slave Address	0111_XXX1b	Read Address.
13	RdDataLen	0Xh	Number of bytes returned = WrData1+1.

14	Status	XXh	Status Code.
15	RdData1	XXh	Register Data[7:0].
16	RdData2	XXh	Register Data[15:8]. Optional.
17	RdData3	XXh	Register Data[23:16].
18	RdData4	XXh	Register Data[31:24]. Optional.
19	RdData5	XXh	Register Data[39:32]. Optional.
20	RdData6	XXh	Register Data[47:40]. Optional.
21	RdData7	XXh	Register Data[55:48]. Optional.
22	RdData8	XXh	Register Data[63:56]. Optional.
23	PEC	XXh	Optional PEC byte.

Table 88: SB-RMI Read CPUID Command Protocol

Byte	Byte Name	Value	Notes
1	Slave Address	0111_XXX0b	Write Address.
2	Command	73h	Read CPUID/Read Register Command Format.
3	WrDataLen	08h	8 Bytes.
4	WrData1	08h	Number of CPUID bytes to read.
5	WrData2	91h	Read CPUID command.
6	WrData3	XXXX_XXXXb	Bit[0] is Reserved. Bits[7:1] select the thread to address. 00h=Thread0. ... 7Fh=Thread127.
7	WrData4	XXh	CPUID Function[7:0].
8	WrData5	XXh	CPUID Function[15:8].
9	WrData6	XXh	CPUID Function[23:16].
10	WrData7	XXh	CPUID Function[31:24].
11	WrData8	ECX[3:0]_000Xb	ECX[3:0] is the initial ECX value for extended CPUID operations. Must be 0h for non-extended operations. X: 0b=Return ebx:eax; 1b=Return edx:ecx.
12	PEC	XXh	Optional PEC byte.
13	Slave Address	0111_XXX1b	Read Address.
14	RdDataLen	09h	Number of bytes returned.
15	Status	XXh	Status Code.
16	RdData1	XXh	eax or ecx bits[7:0].
17	RdData2	XXh	eax or ecx bits[15:8].
18	RdData3	XXh	eax or ecx bits[23:16].
19	RdData4	XXh	eax or ecx bits[31:24].
20	RdData5	XXh	ebx or edx bits[7:0].
21	RdData6	XXh	ebx or edx bits[15:8].
22	RdData7	XXh	ebx or edx bits[23:16].
23	RdData8	XXh	ebx or edx bits[31:24].
24	PEC	XXh	Optional PEC byte.

Table 89: SB-RMI Read Data/Status Command Protocol

Byte	Byte Name	Value	Notes
1	Slave Address	0111_XXX0b	Write Address.
2	Command	72h	Read CPUID/Read Register Command Format.

3	WrDataLen	01h	1 byte of Write data.
4	WrData1	0Xh	Number of bytes to read from register. Valid values are 1 through 8.
5	PEC	XXh	Optional PEC byte.
6	Slave Address	0111_XXX1b	Read Address.
7	RdDataLen	0Xh	Number of bytes returned = WrData1 + 1.
8	Status	XXh	Status Code.
9	RdData1	XXh	Register Data[7:0]. Optional.
10	RdData2	XXh	Register Data[15:8]. Optional.
11	RdData3	XXh	Register Data[23:16]. Optional.
12	RdData4	XXh	Register Data[31:24]. Optional.
13	RdData5	XXh	Register Data[39:32]. Optional.
14	RdData6	XXh	Register Data[47:40]. Optional.
15	RdData7	XXh	Register Data[55:48]. Optional.
16	RdData8	XXh	Register Data[63:56]. Optional.
17	PEC	XXh	Optional PEC byte.

4.4.2.1.2 SB-RMI Write Processor Register Command

Writing processor registers from SB-RMI uses two SBI Modified Block Write-Block Read Process Call commands. The first command loads the address of the register to be written into the processor. The register address loaded by this command is stored on a per-thread basis. The second command writes the data to the processor register using the stored register address. The read data/status command can be used to determine that the command completed if a SMBus timeout occurs. The previous command must be complete before a new command can be issued. WrData Address ranges beyond 32 bits are ignored.

Write Register/Load Address command is only used for DRAM throttle feature for address C001_0079.

Table 90: SB-RMI Load Address Command Protocol

Byte	Byte Name	Value	Notes
1	Slave Address	0111_XXX0b	Write Address.
2	Command	71h	Write Register/Load Address Command Format.
3	WrDataLen	06h	6 bytes.
4	WrData1	81h	Load Address Command.
5	WrData2	XXXX_XXXXb	Bit[0] is Reserved. Bits[7:1] select the thread to address. 00h=Thread0. ... 7Fh=Thread127.
6	WrData3	XXh	Register Address[7:0] from SB-RMI Functions table.
7	WrData4	XXh	Register Address[15:8] from SB-RMI Functions table.
8	WrData5	XXh	Register Address[23:16] from SB-RMI Functions table.
9	WrData6	XXh	Register Address[31:24] from SB-RMI Functions table.
10	PEC	XXh	Optional PEC byte.
11	Slave Address	0111_XXX1b	Read Address.
12	RdDataLen	01h	Number of bytes returned.
13	Status	XXh	Status Code.
14	PEC	XXh	Optional PEC byte.

Table 91: SB-RMI Write Processor Register Command Protocol

Byte	Byte Name	Value	Notes
1	Slave Address	0111_XXX0b	Write Address.
2	Command	71h	Write Register/Load Address Command Format.
3	WrDataLen	0Xh	Total number of WrData bytes sent by the master. The total number of bytes written to the register (WrDataLen - 2) must match the size of the register that is being written or undefined data will be written into the register.
4	WrData1	87h	Write Register Command.
5	WrData2	XXXX_XXXXb	Bit[0] is Reserved. Bits[7:1] select the thread to address. 00h=Thread0. ... 7Fh=Thread127.
6	WrData3	XXh	Register Data[7:0].
7	WrData4	XXh	Register Data[15:8]. Optional.
8	WrData5	XXh	Register Data[23:16]. Optional.
9	WrData6	XXh	Register Data[31:24]. Optional.
10	WrData7	XXh	Register Data[39:32]. Optional.
11	WrData8	XXh	Register Data[47:40]. Optional.
12	WrData9	XXh	Register Data[55:48]. Optional.
13	WrData10	XXh	Register Data[63:56]. Optional.
14	PEC	XXh	Optional PEC byte.
7+WrDataLen	Slave Address	0111_XXX1b	Read Address.
8+WrDataLen	RdDataLen	01h	Number of bytes returned.
9+WrDataLen	Status	XXh	Status Code.
10+WrDataLen	PEC	XXh	Optional PEC byte.

4.4.2.1.3 SB-RMI Protocol Status Codes

The legal values for the Status byte of the SB-RMI processor state accesses are shown in the following table.

Table 92: SB-RMI Status Codes

Status Code	Name	Description
00h	Success	Command.
11h	Command Timeout	Command did not complete before an SMBus timeout occurred. This status code will never occur if (SBRMI_x01[TimeoutDis] == 1). MP has not sent the request to CPU/NB.
22h	Warm reset	A warm reset occurred during the transaction.
40h	Unknown Command Format	The value in Command Format field is not recognized.
41h	Invalid Read Length	The value in RdDataLen is less than 1 or greater than 32.
42h	Excessive Data Length	The sum of the RdDataLen and WrDataLen is greater than 32 and RdDataLen is greater than or equal to 1 and less than or equal to 32.
44h	Invalid thread	Invalid thread selected.
45h	Unsupported	Command not supported by the processor.

	Command	
81h	Command Aborted	The processor core targeted by the command could not start the command and was aborted by the processor.

4.4.2.2 SB-RMI Mailbox Service

SB-RMI supports soft mailbox service request to MP1 (power management firmware) through SBRMI inbound/outbound message registers. The message type is defined in the following table.

Table 93: SB-RMI Soft Mailbox Message

Command	Message	Description	Command Data In	Command Data Out
31h	WRITE_FAST_PPT_LIMIT	Set APU power limit for system power supply peak control.	[31:0]=fPPT in mW.	None
34h	WRITE_THERM_CTL_LIMIT	Set the thermal throttling limit.	[31:0]=Therm limit in degree Celsius.	None
35h	WRITE_VRM_VDD_CURRENT_LIMIT	Set VDDCR_VDD TDC.	[31:0]=VDD TDC in mA.	None
36h	WRITE_VRM_VDD_MAXIMUM_CURRENT_LIMIT	Set VDDCR_VDD EDC.	[31:0]=VDD EDC in mA.	None

4.4.2.2.1 SB-RMI Mailbox Sequence

The sequence is as follows:

1. The initiator (BMC) indicates that command is to be serviced by firmware by writing 80h to SBRMI::InBndMsg_inst7 (SBRMI_x3F). This register must be set to 80h after reset.
2. The initiator (BMC) writes the command to SBRMI::InBndMsg_inst0 (SBRMI_x38).
3. For Write operations or Read operations, which require additional addressing information as shown in Table 93 [SB-RMI Soft Mailbox Message] above, the initiator (BMC) writes Command Data In[31:0] to SBRMI::InBndMsg_inst[4:1] {SBRMI_x3C(MSB):SBRMI_x39(LSB)}.
4. The initiator (BMC) writes 01h to SBRMI::SoftwareInterrupt to notify firmware to perform the requested Read or Write command.
5. Firmware reads the message and performs the defined action.
6. Firmware writes the original command to outbound message register SBRMI::OutBndMsg_inst0 (SBRMI_x30).
7. Firmware writes SBRMI::Status[SwAlertSts] = 1 to generate an ALERT (if enabled) to initiator (BMC) to indicate completion of the requested command. Firmware must (if applicable) put the message data into the message registers SBRMI::OutBndMsg_inst[4:1] {SBRMI_x34(MSB):SBRMI_x31(LSB)}.
8. Firmware clears the interrupt on SBRMI::SoftwareInterrupt.
9. For a Read operation, the initiator (BMC) reads the firmware response Command Data Out[31:0] from SBRMI::OutBndMsg_inst[4:1] {SBRMI_x34(MSB):SBRMI_x31(LSB)}.
10. BMC must write 1'b1 to SBRMI::Status[SwAlertSts] to clear the ALERT to initiator (BMC). It is recommended to clear the ALERT upon completion of the current mailbox command.

Table 94: SB-RMI Soft Mailbox Error Code

Error Type	Description	Code
No error	Mailbox message command executed successfully without an error.	00h
Command Aborted or	Mailbox message command was aborted due to internal error.	01h

Parameter		
Unknown Command	Unknown mailbox message.	02h
Invalid Core	Invalid core is specified in mailbox message parameters.	03h

The mailbox error code is written by Firmware in SBRMI::OutBndMsg_inst7 (SBRMI_x37).

4.4.2.3 SB-RMI Boot code status

Boot code will dump the dynamic boot status into SBRMI::MP0OutBndMsg. BMC can then just read this status through SBI interface to determine progress through the boot flow.

4.4.2.4 SB-RMI Register Access

The SB-RMI registers can be read or written from the SMBus interface using the SMBus defined PEC-optional Read Byte and Write Byte protocols with the SB-RMI register number in the command byte or the PEC-optional Block Read and Block Write protocols with the first SB-RMI register number to be accessed in the command byte. Block Read/Write protocol access for SB-RMI registers is controlled by SBRMI::Control[BlkRWEn]. The SB-RMI interface supports Block Writes of up to 32 bytes, and Block Reads of up to 32 bytes as specified by SBRMI::ReadSize[RdSize]. Bytes are returned in ascending register order starting with the first SB-RMI register in the command byte.

4.4.2.4.1 SB-RMI Register Block Access

The following example shows a write from SBRMI_x18 to SBRMI_x1F using SMBus Block Write protocol with SBRMI::Control[BlkRWEn] set to 1.

Table 95: SB-RMI Register Block Write Protocol

Byte	Byte Name	Value	Notes
1	Slave Address	0111_XXX0b	Write Address.
2	Command	18h	Indicates starting register SBRMI_x18.
3	Byte Count	08h	Number of bytes to write.
4	Data Byte 1	00h	Write a value to SBRMI_x18h.
5	Data Byte 2	00h	Write a value to SBRMI_x19h.
6	Data Byte 3	00h	Write a value to SBRMI_x1Ah.
7	Data Byte 4	00h	Write a value to SBRMI_x1Bh.
8	Data Byte 5	00h	Write a value to SBRMI_x1Ch.
9	Data Byte 6	00h	Write a value to SBRMI_x1Dh.
10	Data Byte 7	00h	Write a value to SBRMI_x1Eh.
11	Data Byte 8	00h	Write a value to SBRMI_x1Fh.
12	PEC	XXh	Optional PEC byte.

The following example shows a read from SBRMI_x10 to SBRMI_x17 using SMBus Block Read protocol with SBRMI::Control[BlkRWEn] set to 1 and SBRMI::ReadSize[RdSize] set to 8.

Table 96: SB-RMI Register Block Read Protocol

Byte	Byte Name	Value	Notes
1	Slave Address	0111_XXX0b	Write Address.
2	Command	10h	Indicates starting register SBRMI_x10.
3	Slave Address	0111_XXX1b	Read Address.

4	Byte Count	08h	Number of bytes to read.
5	Data Byte 1	00h	Read a value from SBRMI_x10h.
6	Data Byte 2	00h	Read a value from SBRMI_x11h.
7	Data Byte 3	00h	Read a value from SBRMI_x12h.
8	Data Byte 4	00h	Read a value from SBRMI_x13h.
9	Data Byte 5	00h	Read a value from SBRMI_x14h.
10	Data Byte 6	00h	Read a value from SBRMI_x15h.
11	Data Byte 7	00h	Read a value from SBRMI_x16h.
12	Data Byte 8	00h	Read a value from SBRMI_x17h.
13	PEC	XXh	Optional PEC byte.

4.4.2.4.2 SB-RMI Register Byte Access

The following example shows a write to SBRMI_x03 using the SMBus Write Byte protocol with SBRMI::Control[BlkRWEn] set to 0.

Table 97: SB-RMI Register Write Byte Protocol

Byte	Byte Name	Value	Notes
1	Slave Address	0111_XXX0b	Write Address.
2	Command	03h	Indicates SB-RMI register 03.
3	Data Byte	04h	Write a value of 04h.
4	PEC	XXh	Optional PEC byte.

The following example shows a read from SBRMI_x03 using the SMBus Read Byte protocol with SBRMI::Control[BlkRWEn] set to 0.

Table 98: SB-RMI Register Read Byte Protocol

Byte	Byte Name	Value	Notes
1	Slave Address	0111_XXX0b	Write Address.
2	Command	03h	Indicates SB-RMI register 03.
3	Slave Address	0111_XXX1b	Read address.
4	Data Byte	04h	Value of SBRMI_x03h.
5	PEC	XXh	Optional PEC byte.

4.4.2.5 SB-RMI Alert

The processor alerts the SBI when a Machine Check Exception occurs within the system. The Machine Check Exception status is reflected in registers SBRMI_x01[F:0].

The processor alerts the SBI on system fatal error event. This status is reflected in SBRMI_x02[SwAlertSts]. To enable this functionality, SBRMI_x01[SwAlertMask] must be clear.

4.4.3 SBI Error Detection and Recovery

This section describes the various error detection and recovery methods that can be used on the SBI bus. The important item in providing a high reliability SBI connection is the ability to detect when an error occurs and to gracefully recover from that error. When the SBI connections are noisy, messages can become garbled which, in turn, may cause undefined behavior on the SBI bus. The most common noise sources are cross-talk and clock skew. Cross-talk results when the SBI

connections are routed too close to other signal carrying lines. Clock skew is usually a result of higher than expected capacitance, between the SBI signals (clock and / or data) and ground, which causes the master and slave devices to disagree on when data should be stable and when it is allowed to be changing.

4.4.3.1 Error Detection

SBI provides several methods of error detection: protocol ACK/NAK, packet error correction (PEC) fields, and timeouts. The ACK/NAK mechanism is always active in SBI, but the PEC and timeouts are optional.

4.4.3.1.1 ACK/NAK Mechanism

After each byte of an SBI message, the device receiving that byte must either acknowledge (ACK) that it received the byte correctly, or deny (NAK) that the byte was correctly received. This is most easily seen in the case of the address bytes which follow a START (or REPEATED START) sequence, but can be used anywhere in the message. In the case of an address byte, if a slave device recognizes the address, it will respond with an ACK and await the rest of the message. If a slave device does not recognize the message, it will respond with a NAK and ignore the rest of the message.

4.4.3.1.2 Packet Error Correction (PEC)

The RMI protocols allow for PEC bytes to be appended to messages. The sending side calculates the PEC, based on the data it intends to transmit, and appends it the transmitted data. The receiving side calculates the PEC based on the data it actually receives and compares that to the PEC it receives. If the two PECs do not match, an error has occurred and the message should be discarded. When a device detects a PEC mismatch, it should send a NAK in response to the PEC. No special programming is needed to enable the PEC on AMD devices. If the PEC is present on an incoming message, the device will verify the PEC and ACK or NAK as appropriate. The PEC is always calculated on outgoing messages. It is up to the bus master to request the PEC by sending clocks for that byte before sending either a NAK or a STOP sequence.

4.4.3.1.3 Bus Timeouts

Bus timeouts should be enabled to prevent a device waiting indefinitely on a message that may not be coming. Some timeouts are used to prevent the SBI bus from waiting for a response from a CPU that is in a power-saving idle mode. Other timeouts are used to allow the slave device to recognize that the bus master is attempting to reset all of the devices on the SBI bus. Either way, when a device recognizes a timeout, it should abort its current message transfer.

4.4.3.2 Error Recovery

The simplest form of error recovery is a retry. When the bus master detects an unexpected NAK, it should abort the current transfer and retry the message sequence. In some cases, however, a message can be so garbled that a simple retry is insufficient. This can occur, if there are multiple devices on the bus and a garbled address byte has caused the wrong slave device to be selected. That slave device may even continue to transmit during the retry. In those cases, it will be necessary to force a reset of all devices on the SBI bus, before retrying the message transfer.

4.4.3.2.1 SBI Bus Reset

The bus master can hold the clock low for a period longer the standard timeout in order to force slave devices off the bus (see docSMB section 3.1.1.3 of the System Management Bus (SMBus) Specification, version 2.0). All SBI slave devices are required to reset their communications if another device holds the clock line low for longer than TTimeout, min (25 milliseconds). The devices are required to complete their reset within TTimeout, max (35 milliseconds). SBI bus masters should use the extended timeout to force a reset of all slave devices if a simple retry does not remove an error condition.

4.5 SBI Physical Interface

4.5.1 SBI SMBus Address

The SMBus address is really 7 bits. Some vendors and the SMBus specification show the address as 8 bits: bits[7:1] as the left-justified address, and bit[0] as the Read/Write flag, where 0 indicates a Write and 1 indicates a Read. Some vendors use only the 7 bits to describe the address.

4.5.2 SBI Bus Timing

SBI supports 100KHz standard-mode and 400 KHz fast-mode I2C operation. Refer to the standard-mode and fast-mode timing parameters in the I2C specification.

4.6 SB-RMI Registers

Reads to unimplemented registers return 00h. Writes to unimplemented registers are discarded.

SBRMIx00 [Revision] (SBRMI::Revision)	
Read-only. Reset: 10h.	
Bits	Description
7:0	Revision: SB-RMI revision. Read-only. Reset: 10h. This field specifies the APML specification revision that the product is compliant to. 0x10=1.0x Revision.
SBRMIx01 [Control] (SBRMI::Control)	
Read-write. Reset: 01h.	
Bits	Description
7	PECEn: packet error checking enable. Read-write. Reset: 0. This only controls the intermediate PEC of the SBI Modified Block Write-Block Read Process Call. 0=Intermediate PEC is disabled. 1=Intermediate PEC is enabled.
6:5	Reserved.
4	SwAlertMask: software alert mask. Read-write. Reset: 0. 0=Alert_L signaling is enabled when SBRMI_x02SwAlertSts is set. 1=Alert_L signaling is disabled when SBRMI_x02SwAlertSts is set.
3	BlkRWEn: block read/write enable. Read-write. Reset: 0. Controls Block Read/Write access to register ranges SBRMI_x[4F:10] and SBRMI_x[9F:80]. 0=SMBus accesses can only use the Byte Read/Write protocol. 1=SMBus accesses can only use the Block Read/Write protocol. NOTE: All other register ranges only support Byte Read/Write access, independent of the state of the BlkRWEn control bit.
2	TimeoutDis: SB-RMI timeout disable. Read-write. Reset: 0. 1=SMBus defined timeouts are disabled. If the SB-TSI interface is also in use, SMBus timeouts should be enabled or disabled in a consistent manner on both interfaces. The SB-TSI timeout setting is used by SB-RMI until the SMBus interface can determine which interface is targeted by the transaction.
1	AraDis: SB-RMI ARA disable. Read-write. Reset: 0. 1=Sending of an ARA response is disabled. 0=Sending of an ARA response is enabled.
0	AlertMask: SB-RMI alert mask. Read-write. Reset: 1. Read-write; set-by-hardware if AraDis=0 and a successful ARA is sent. 1=Alert_L signaling disabled. 0=Alert_L is asserted if any unmasked event is present in the [The Alert Status Registers] SBRMI_x1[F:0], or if SBRMI_x02[SwAlertSts] == 1 and SwAlertMask == 0.

SBRMIx02 [Status] (SBRMI::Status)

Reset: 00h.

Bits	Description
7:2	Reserved.
1	SwAlertSts: SB-RMI software alert status. Read-write, Volatile. Reset: 0. Write-one-to-clear from the SMBus interface; Read-write from the processor. Set by firmware as a result of a Machine Check Exception prior to the MCE related warm reset. Set by firmware to indicate the completion of a mailbox operation.
0	AlertSts: SB-RMI alert status. Read-only, Volatile. Reset: 0. Read-only. 1=Alert event present in SBRMI::AlertStatus.

SBRMIx03 [Read Size] (SBRMI::ReadSize)

Read-write. Reset: 01h.

This register specifies the number of bytes to return when using the block read protocol to read SBRMI_x[4F:10] and SBRMI_x[90:80].

Bits	Description								
7:6	Reserved.								
5:0	RdSize: read size. Read-write. Reset: 01h. Specifies the number of bytes to return when using the block read protocol.								
Valid Values:									
	<table> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>00h</td><td>Reserved.</td></tr> <tr> <td>20h-01h</td><td><Value> bytes.</td></tr> <tr> <td>3Fh-21h</td><td>Reserved.</td></tr> </table>	Value	Description	00h	Reserved.	20h-01h	<Value> bytes.	3Fh-21h	Reserved.
Value	Description								
00h	Reserved.								
20h-01h	<Value> bytes.								
3Fh-21h	Reserved.								

SBRMIx0[4...9] [Thread Enable Status] (SBRMI::ThreadEnableStatus)

Read-only.

_inst[3:0]; SBRMIx[09,08,05,04]

Bits	Description															
7:0	threadEnStat: thread enable status. Read-only.															
	Description: 1=Thread is enabled.															
	<table><tr><td>Offset[7:0]</td><td>inst</td><td>Description</td></tr><tr><td>04h</td><td>0</td><td>Threads[7:0].</td></tr><tr><td>05h</td><td>1</td><td>Threads[15:8].</td></tr><tr><td>08h</td><td>2</td><td>Threads[23:16].</td></tr><tr><td>09h</td><td>3</td><td>Threads[31:24].</td></tr></table>	Offset[7:0]	inst	Description	04h	0	Threads[7:0].	05h	1	Threads[15:8].	08h	2	Threads[23:16].	09h	3	Threads[31:24].
	Offset[7:0]	inst	Description													
	04h	0	Threads[7:0].													
	05h	1	Threads[15:8].													
	08h	2	Threads[23:16].													
09h	3	Threads[31:24].														

SBRMIx1[0...F] [Alert Status] (SBRMI::AlertStatus)

Read,Write-1-to-clear,Volatile.

_inst[15:0]; SBRMIx1[F:0]

Bits	Description		
7:4	Reserved.		
3:0	MceStat: MCE status. Read,Write-1-to-clear,Volatile.		
	Description: Bit vector for threads. 1=MCE occurred for thread. Set by hardware.		
	Offset[7:0]	inst	Description
	10h	0	Threads[48,32,16,0].
	11h	1	Threads[49,33,17,1].
	12h	2	Threads[50,34,18,2].
	13h	3	Threads[51,35,19,3].
	14h	4	Threads[52,36,20,4].
	15h	5	Threads[53,37,21,5].
	16h	6	Threads[54,38,22,6].
	17h	7	Threads[55,39,23,7].
	18h	8	Threads[56,40,24,8].
	19h	9	Threads[57,41,25,9].
	1Ah	10	Threads[58,42,26,10].
	1Bh	11	Threads[59,43,27,11].
	1Ch	12	Threads[60,44,28,12].
	1Dh	13	Threads[61,45,29,13].
1Eh	14	Threads[62,46,30,14].	
1Fh	15	Threads[63,47,31,15].	

SBRMIx2[0...F] [Alert Mask] (SBRMI::AlertMask)

Read-write.

_inst[15:0]; SBRMIx2[F:0]

Bits	Description																																																			
7:4	Reserved.																																																			
3:0	MceAlertMsk: MCE alert mask. Read-write. Description: Bit vector for threads. 1=Alert signaling disabled for corresponding SBRMI::AlertStatus[MceStat] for thread. <table><tr><th>Offset[7:0]</th><th>inst</th><th>Description</th></tr><tr><td>20h</td><td>0</td><td>Threads[48,32,16,0].</td></tr><tr><td>21h</td><td>1</td><td>Threads[49,33,17,1].</td></tr><tr><td>22h</td><td>2</td><td>Threads[50,34,18,2].</td></tr><tr><td>23h</td><td>3</td><td>Threads[51,35,19,3].</td></tr><tr><td>24h</td><td>4</td><td>Threads[52,36,20,4].</td></tr><tr><td>25h</td><td>5</td><td>Threads[53,37,21,5].</td></tr><tr><td>26h</td><td>6</td><td>Threads[54,38,22,6].</td></tr><tr><td>27h</td><td>7</td><td>Threads[55,39,23,7].</td></tr><tr><td>28h</td><td>8</td><td>Threads[56,40,24,8].</td></tr><tr><td>29h</td><td>9</td><td>Threads[57,41,25,9].</td></tr><tr><td>2Ah</td><td>10</td><td>Threads[58,42,26,10].</td></tr><tr><td>2Bh</td><td>11</td><td>Threads[59,43,27,11].</td></tr><tr><td>2Ch</td><td>12</td><td>Threads[60,44,28,12].</td></tr><tr><td>2Dh</td><td>13</td><td>Threads[61,45,29,13].</td></tr><tr><td>2Eh</td><td>14</td><td>Threads[62,46,30,14].</td></tr><tr><td>2Fh</td><td>15</td><td>Threads[63,47,31,15].</td></tr></table>	Offset[7:0]	inst	Description	20h	0	Threads[48,32,16,0].	21h	1	Threads[49,33,17,1].	22h	2	Threads[50,34,18,2].	23h	3	Threads[51,35,19,3].	24h	4	Threads[52,36,20,4].	25h	5	Threads[53,37,21,5].	26h	6	Threads[54,38,22,6].	27h	7	Threads[55,39,23,7].	28h	8	Threads[56,40,24,8].	29h	9	Threads[57,41,25,9].	2Ah	10	Threads[58,42,26,10].	2Bh	11	Threads[59,43,27,11].	2Ch	12	Threads[60,44,28,12].	2Dh	13	Threads[61,45,29,13].	2Eh	14	Threads[62,46,30,14].	2Fh	15	Threads[63,47,31,15].
Offset[7:0]	inst	Description																																																		
20h	0	Threads[48,32,16,0].																																																		
21h	1	Threads[49,33,17,1].																																																		
22h	2	Threads[50,34,18,2].																																																		
23h	3	Threads[51,35,19,3].																																																		
24h	4	Threads[52,36,20,4].																																																		
25h	5	Threads[53,37,21,5].																																																		
26h	6	Threads[54,38,22,6].																																																		
27h	7	Threads[55,39,23,7].																																																		
28h	8	Threads[56,40,24,8].																																																		
29h	9	Threads[57,41,25,9].																																																		
2Ah	10	Threads[58,42,26,10].																																																		
2Bh	11	Threads[59,43,27,11].																																																		
2Ch	12	Threads[60,44,28,12].																																																		
2Dh	13	Threads[61,45,29,13].																																																		
2Eh	14	Threads[62,46,30,14].																																																		
2Fh	15	Threads[63,47,31,15].																																																		

SBRMIx3[0...7] [Out-Bound Message] (SBRMI::OutBndMsg)

Read-write. Reset: 00h.

_inst[7:0]; SBRMIx3[7:0]

Bits	Description
7:0	OutBndMsg: outbound message data. Read-write. Reset: 00h.
	Description: Read-write from the processor; Read-only from the SMBus interface.
	Usage convention is:
	<ul style="list-style-type: none">• SBRMI::OutBndMsg_inst0 is command copied by firmware from SBRMI::InBndMsg_inst0.• SBRMI::OutBndMsg_inst[4:1] are 32-bit data.• SBRMI::OutBndMsg_inst[6:5] are Reserved.• SBRMI::OutBndMsg_inst[7] contains Mailbox Error Code, per Table 94 [SB-RMI Soft Mailbox Error Code]

Offset[7:0]	inst	Description
30h	0	Outbound message 0.
31h	1	Outbound message 1.
32h	2	Outbound message 2.
33h	3	Outbound message 3.
34h	4	Outbound message 4.
35h	5	Outbound message 5.
36h	6	Outbound message 6.
37h	7	Outbound message 7.

SBRMIx3[8...F] [In-Bound Message] (SBRMI::InBndMsg)

Read-write. Reset: 00h.

_inst[7:0]; SBRMIx3[F:8]

Bits	Description																											
7:0	InBndMsg: inbound message data. Read-write. Reset: 00h.																											
	Description: Read-write from the SMBus interface; Read-only from the processor. These registers are used for communicating 32-bit messages from BMC to firmware.																											
	Usage convention is:																											
	<ul style="list-style-type: none">• SBRMI::InBndMsg_inst0 is command.• SBRMI::InBndMsg_inst[4:1] are 32-bit data.• SBRMI::InBndMsg_inst[6:5] are Reserved.• SBRMI::InBndMsg_inst7: Bit[7] Must be 1'b1 to send message to firmware.																											
	<table><tr><th>Offset[7:0]</th><th>inst</th><th>Description</th></tr><tr><td>38h</td><td>0</td><td>Inbound message 0.</td></tr><tr><td>39h</td><td>1</td><td>Inbound message 1.</td></tr><tr><td>3Ah</td><td>2</td><td>Inbound message 2.</td></tr><tr><td>3Bh</td><td>3</td><td>Inbound message 3.</td></tr><tr><td>3Ch</td><td>4</td><td>Inbound message 4.</td></tr><tr><td>3Dh</td><td>5</td><td>Inbound message 5.</td></tr><tr><td>3Eh</td><td>6</td><td>Inbound message 6.</td></tr><tr><td>3Fh</td><td>7</td><td>Inbound message 7.</td></tr></table>	Offset[7:0]	inst	Description	38h	0	Inbound message 0.	39h	1	Inbound message 1.	3Ah	2	Inbound message 2.	3Bh	3	Inbound message 3.	3Ch	4	Inbound message 4.	3Dh	5	Inbound message 5.	3Eh	6	Inbound message 6.	3Fh	7	Inbound message 7.
	Offset[7:0]	inst	Description																									
	38h	0	Inbound message 0.																									
	39h	1	Inbound message 1.																									
	3Ah	2	Inbound message 2.																									
	3Bh	3	Inbound message 3.																									
3Ch	4	Inbound message 4.																										
3Dh	5	Inbound message 5.																										
3Eh	6	Inbound message 6.																										
3Fh	7	Inbound message 7.																										

SBRMIx40 [Software Interrupt] (SBRMI::SoftwareInterrupt)

Read,Write-1-only. Reset: 00h.

This register is used by the SMBus master to generate an interrupt to the processor to indicate that a message is available.

Bits	Description
7:1	Reserved.
0	SwInt: firmware interrupt. Read,Write-1-only. Reset: 0. Read,Write-1-only from the SMBus interface; Read,Write-1-to-clear from firmware. 1=Indicates a firmware mailbox service request.

SBRMIx41 [Thread Number] (SBRMI::ThreadNumber)

Read-write. Reset: 00h.

This register indicates the maximum number of threads present.

Bits	Description
7:0	threadNum: thread number. Read-write. Reset: 00h. Read-only from the SMBus interface. Specifies the maximum number of threads present. Format is [6:1] number of threads – 40h and range of available threads 40h – 01h. Firmware loads the initial value based on the maximum number of threads available after any fused off or soft-down-coring is complete.

SBRMIx8[0...7] [MP0 Out-Bound Message] (SBRMI::MP0OutBndMsg)

Read-write. Reset: 00h.

_inst[7:0]; SBRMIx8[7:0]

Bits	Description	
7:0	MP0OutBndMsg: outbound message data. Read-write. Reset: 00h. Description: Read-write from the processor; Read-only from the SMBus interface. These registers are used for sending messages from PSP firmware running on the MP0 to the SMBus master. MP0 boot status is dynamically written to this register during the boot process.	
	Offset[7:0]	Description
	80h	MP0 Outbound message 0.
	81h	MP0 Outbound message 1.
	82h	MP0 Outbound message 2.
	83h	MP0 Outbound message 3.
	84h	MP0 Outbound message 4.
	85h	MP0 Outbound message 5.
	86h	MP0 Outbound message 6.
	87h	MP0 Outbound message 7.

5 SB Temperature Sensor Interface (SB-TSI)

5.1 Overview

The SBI temperature sensor interface (SB-TSI) is an emulation of the software and physical interface of a typical 8-pin remote temperature sensor (RTS), see Figure 27 [RTS Thermal Management Example]. The goal is to resemble a typical RTS so that KBC or BMC firmware requires minimal changes for future AMD products, see Figure 28 [SB-TSI Thermal Management Example]. SB-TSI supports the SMBus protocols that typical RTS supports.

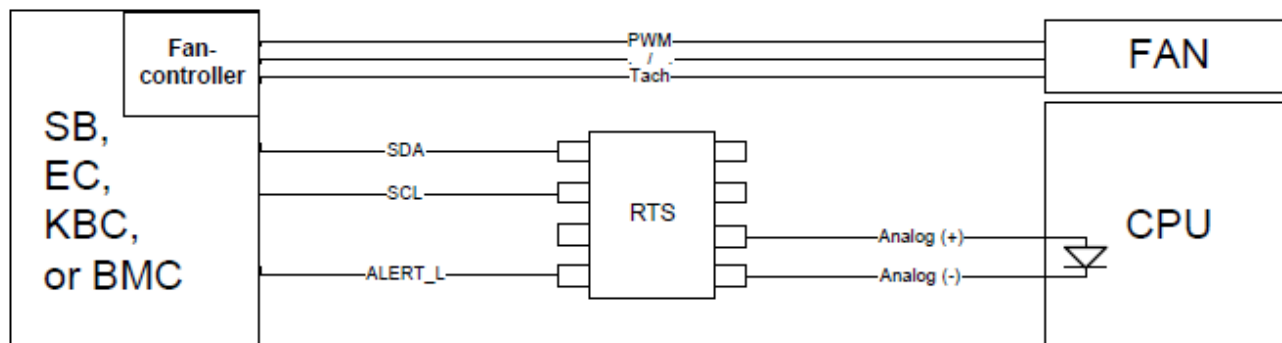


Figure 27: RTS Thermal Management Example

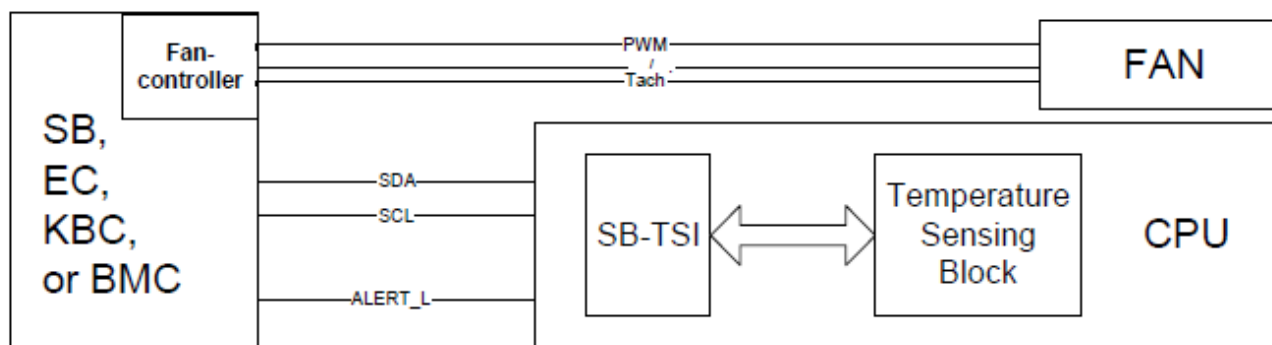


Figure 28: SB-TSI Thermal Management Example

Refer to the following external sources for additional information.

- System Management Bus (SMBus) specification. See docSMB.
- I2C-bus Specification and User Manual, Revision 03. See docI2C.

5.1.1 Definitions

Table 99: SB-TSI Definitions

Term	Description
BMC	Base management controller.
TCC	Temperature calculation circuit.
Tctl	Processor temperature control value.
TSM	Temperature sensor macro.
SB-TSI	Sideband Internal Temperature Sensor Interface. See APML.

5.2 SB-TSI Protocol

The SB-TSI largely follows SMBus v2.0 specification except:

- The combined-format repeated start sequence is not supported in standard-mode and fast-mode. The response of the processor's SB-TSI to the sequence is undefined.
- Only 7-bit SMBus addresses are supported.
- SB-TSI implements the Send/Receive Byte and Read/Write Byte protocols.
- SB-TSI registers can only be written by using a Write byte command.
- Address Resolution Protocol (ARP) is not supported.
- Packet Error Checking (PEC) is not supported.
- The usage of unsupported protocols may lead to an undefined bus condition.
- To release the bus from an undefined condition and to reset the SB-TSI slave, the bus master must hold the clock low for a duration of time that is longer than Ttimeout.max, as specified for SMBus. The time-out needs to be enabled by SBTSI::TimeoutConfig[TimeoutEn] = 1.

5.2.1 SB-TSI Send/Receive Byte Protocol

A SMBus master can Read SB-TSI registers by issuing a send byte command with the address of the register to be read as the data byte followed by a receive byte command.

5.2.1.1 SB-TSI Address Pointer

The SB-TSI controller has an internal address pointer that is updated when a register is accessed using a Read or Write byte command or when a send byte command is received. This address pointer is used to determine the address of the register being read when a receive byte command is processed by the controller.

5.2.2 SB-TSI Read/Write Byte Protocol

An SMBus master can Read or Write SB-TSI registers by issuing a Read or a Write byte command with the address of the register to be read or written in the command code field.

5.2.3 Alert Behavior

The ALERT_L pin is asserted if (SBTSI::Status[TempHighAlert] || SBTSI::Status[TempLowAlert]) && ~SBTSI::Config[AlertMask] as shown in Figure 3. The following registers also affect temperature alert behavior.

- SBTSI::Config[AraDis]: Disables ARA response.
- SBTSI::UpdateRate[UpRate]: Specifies rate at which temperature thresholds are checked.
- {SBTSI::HiTempInt[HiTempInt], SBTSI::HiTempDec[HiTempDec]}: Sets high temperature threshold.
- {SBTSI::LoTempInt[LoTempInt], SBTSI::LoTempDec[LoTempDec]}: Sets low temperature threshold.
- SBTSI::AlertThreshold[AlertThr]: Specifies number of consecutive temperature samples to assert an alert.
- SBTSI::AlertConfig[AlertCompEn]: Specifies ALERT_L pin to be in latched or comparator mode. Affects ARA.

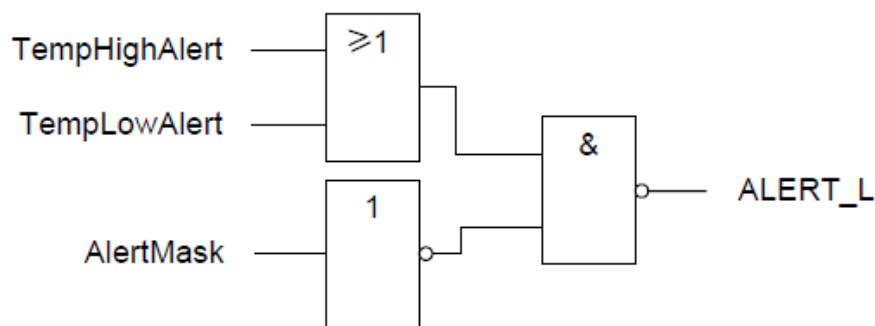


Figure 29: Alert Assertion Diagram

5.2.4 Atomic Read Mechanism

To ensure that the two required Reads (integer and decimal) for reading the CPU temperature are always originated from one temperature value, atomic reading procedures are required. SB-TSI offers functions to maintain atomicity between the temperature integer and decimal bytes.

[The SB-TSI Configuration Register] SBTSI::Config[ReadOrder] specifies the order for reading integer and decimal part of the CPU temperature value for atomic CPU temperature Reads. If SBTSI::Config[ReadOrder] is 0, then a Read of the integer part (SBTSI::CpuTempInt) of the CPU temperature triggers a latch of the decimal part (SBTSI::CpuTempDec) until the next Read of the integer part. This latch syncs the decimal part with the integer part. The integer part is continuously updated.

If SBTSI::Config[ReadOrder] is 1, then the Read order to ensure atomicity is Reversed, i.e., decimal part = first, integer part = second.

If it is not possible to ensure a dedicated Read order as described above, the Run/Stop bit ([The SB-TSI Configuration Register] SBTSI::Config[RunStop]) may be used to provide atomicity of reading the CPU temperature. If this bit is 0, the CPU temperature registers are updated continuously. If it is 1, they get frozen and always deliver their last value on Read requests.

- Set SBTSI::Config[RunStop].
- Read the integer (SBTSI::CpuTempInt) or the decimal (SBTSI::CpuTempDec) part of the CPU temperature.
- Read the remaining part of the CPU temperature.
- Clear SBTSI::Config[RunStop].

5.2.5 SB-TSI Temperature and Threshold Encodings

SB-TSI CPU temperature readings and limit registers encode the temperature in increments of 0.125 from 0 to 255.875. The high byte represents the integer portion of the temperature from 0 to 255. One increment in the high byte is equivalent to a step of one. The upper three bits of the low byte represent the decimal portion of the temperature. One increment of these bits is equivalent to a step of 0.125.

Table 100: SB-TSI CPU Temperature and Threshold Encoding Examples

Temperature	Temperature High Byte SBTSI::CpuTempInt[CpuTempInt] SBTSI::HiTempInt[HiTempInt]	Temperature Low Byte SBTSI::CpuTempDec[CpuTempDec] SBTSI::HiTempDec[HiTempDec]
-------------	---	--

	SBTSI::LoTempInt[LoTempInt]	SBTSI::LoTempDec[LoTempDec]
0.000 °C	0000_0000b	0000_0000b
1.000 °C	0000_0001b	0000_0000b
25.125 °C	0001_1001b	0010_0000b
50.875 °C	0011_0010b	1110_0000b
90.000 °C	0101_1010b	0000_0000b

5.2.6 SB-TSI Temperature Offset Encoding

By default, SBTISI::CpuTempInt and SBTISI::CpuTempDec provide Tctl from the processor. The temperature offset registers allow the system to adjust the SB-TSI temperature from Tctl.

The SB-TSI temperature offset registers use a different encoding in order to provide negative temperature values. SBTISI::CpuTempOffInt[CpuTempOffInt] and SBTISI::CpuTempOffDec[CpuTempOffDec] form an 11-bit, 2's complement value representing the temperature offset. The high byte encodes the integer portion of the temperature and the upper three bits of the low byte represent the fractional portion of the temperature offset. One increment of these bits is equivalent to a step of 0.125 °C. After reset the offset is always set to 0 °C. Software needs to adjust the offset to the appropriate level.

Table 101: SB-TSI Temperature Offset Encoding Examples

Temperature	Temperature High Byte SBTSI::CpuTempOffInt[CpuTempOffInt]	Temperature Low Byte SBTSI::CpuTempOffDec[CpuTempOffDec]
-10.375 °C	1111_0101b	1010_0000b
-0.250 °C	1111_1111b	1100_0000b
0.000 °C	0000_0000b	0000_0000b
0.875 °C	0000_0000b	1110_0000b
10.000 °C	0000_1010b	0000_0000b

5.3 SB-TSI Physical Interface

This chapter describes the physical interface of the SB-TSI.

5.3.1 SB-TSI SMBus Address

The SMBus address is really 7 bits. Some vendors and the SMBus specification show the address as 8 bits: bits[7:1] as the left-justified address, and bit[0] as the Read/Write flag, where 0 indicates a Write and 1 indicates a Read. Some vendors use only the 7 bits to describe the address. The addresses can vary with address select pins.

Table 102: SB-TSI Address Encodings

Socket ID	SB-TSI Address
0b	98h for 8-bit or 4Ch for 7-bit.
1b	90h for 8-bit or 48h for 7-bit.

5.3.2 SB-TSI Bus Timing

SB-TSI supports standard-mode (100 kHz) and fast-mode (400 kHz) according to the I2C-bus Specification and User Manual.

5.3.3 SB-TSI Bus Electrical Parameters

SB-TSI conforms to most of the I2C fast-mode electrical parameters. See the Electrical Data Sheet for the processor family for electrical parameters.

5.3.4 Pass-FET Option

The KBC may not have the capability to directly interface to SB-TSI. Pass FETs may be used to create two SMBus segments, as shown in the following diagram.

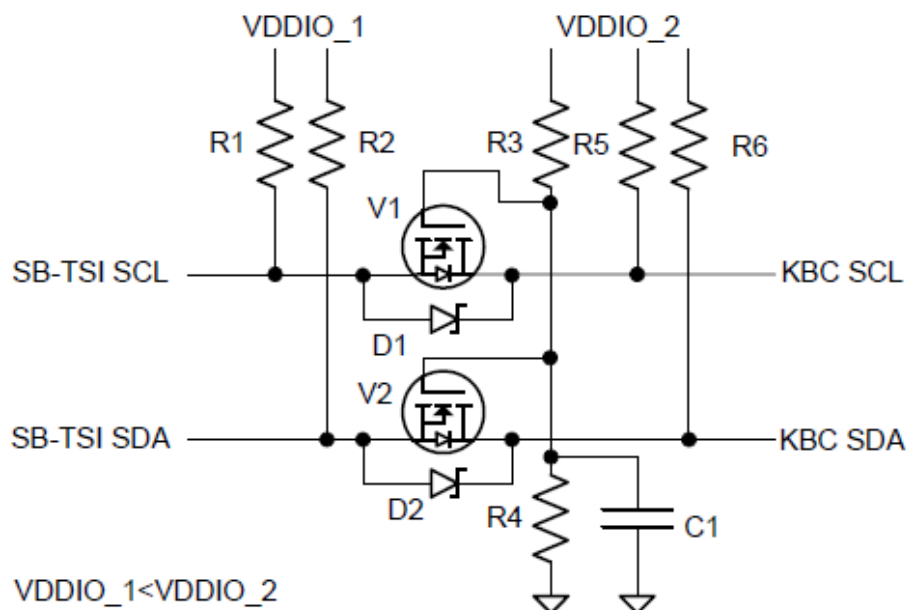


Figure 30: Pass FET Implementation

Notes:

- SCL and SDA pull-up resistors (R5 and R6, respectively) are the normal pull-up resistors for an SMBus segment and are not part of the translation circuit. They are shown for completeness.
- The gates of the FETs are tied to a voltage approximately V_{gs} above the lower rail voltage. A resistive divider is shown, but a convenient power rail would do nicely.
- Care must be taken to install the FETs so that any body diode does not conduct.
- The key requirement is that the high side drive low enough to register as a low on the low side. (High side $V_{ol} < V_{il}$ on low side).

5.4 SB-TSI Registers

Reads to unimplemented registers return 00h. Writes to unimplemented registers are discarded.

SBTSIx01 [CPU Integer Temperature] (SBTSI::CpuTempInt)

Read-only.

The CPU temperature is calculated by adding the CPU temperature offset (SBTSI::CpuTempOffInt, SBTSI::CpuTempOffDec) to the processor control temperature (Tctl). SBTSI::CpuTempInt and SBTSI::CpuTempDec combine to return the CPU temperature. For the temperature encoding, see 5.2.5 [SB-TSI Temperature and Threshold Encodings]

Bits	Description
7:0	CpuTempInt: integer CPU temperature value. Read-only. Reset: Cold,XXh. This field returns the integer portion of the CPU temperature.

SBTSIx02 [SB-TSI Status] (SBTSI::Status)

Read-only, Volatile.

If SBTSI::AlertConfig[AlertCompEn] == 0, the temperature alert is latched high until the alert is Read. If SBTSI::AlertConfig[AlertCompEn] == 1, the alert is cleared when the temperature does not meet the threshold conditions for temperature and number of samples. See 5.2.3 [Alert Behavior].

Bits	Description
7:5	Reserved.
4	TempHighAlert: temperature high alert. Read-only, Volatile. Reset: Cold,X. 1=Indicates that the CPU temperature is greater than or equal to the high temperature threshold (SBTSI::HiTempInt, SBTSI::HiTempDec) for SBTSI::AlertThreshold[AlertThr] consecutive samples. 0=Indicates that the CPU temperature is less than the high temperature threshold (SBTSI::HiTempInt, SBTSI::HiTempDec) for SBTSI::AlertThreshold[AlertThr] samples and SBTSI::AlertConfig[AlertCompEn] == 1. Hardware will clear this bit when Read if SBTSI::AlertConfig[AlertCompEn] == 0.
3	TempLowAlert: temperature low alert. Read-only, Volatile. Reset: Cold,X. 1=Indicates that the CPU temperature is less than or equal to the low temperature threshold (SBTSI::LoTempInt, SBTSI::LoTempDec) for SBTSI::AlertThreshold[AlertThr] consecutive samples. 0=Indicates the CPU temperature is greater than the low temperature threshold (SBTSI::LoTempInt, SBTSI::LoTempDec) for SBTSI::AlertThreshold[AlertThr] samples and SBTSI::AlertConfig[AlertCompEn] == 1. Hardware will clear this bit when Read if SBTSI::AlertConfig[AlertCompEn] == 0.
2:0	Reserved.

SBTSIx03 [SB-TSI Configuration] (SBTSI::Config)

Reset: Cold,00h.

The bits in this register are Read-only and can be written by Writing to the corresponding bits in SBTSI::ConfigWr. See 5.2.3 [Alert Behavior] and 5.2.4 [Atomic Read Mechanism].

Bits	Description
7	AlertMask: alert mask. Read-only, Volatile. Reset: Cold,0. 0=ALERT_L pin enabled. 1=ALERT_L pin disabled and does not assert. IF (SBTSI::Config[AraDis] == 0) THEN Read-only; set-by-hardware. ELSE Read-only ENDIF. Hardware sets this bit if SBTSI::Config[AraDis] == 0, either SBTSI::Status[TempHighAlert] == 1 or SBTSI::Status[TempLowAlert] == 1, and a successful ARA is sent.
6	RunStop: run stop. Read-only. Reset: Cold,0. 0=Updates to SBTSI::CpuTempInt and SBTSI::CpuTempDec and the alert comparisons are enabled; Alert history counters (specified by SBTSI::AlertThreshold[AlertThr]) and the corresponding timer (specified by SBTSI::UpdateRate[UpRate]) continue to update. 1=Updates to SBTSI::CpuTempInt and SBTSI::CpuTempDec and the alert comparisons are disabled; Alert history counters (specified by SBTSI::AlertThreshold[AlertThr]) and the corresponding timer (specified by SBTSI::UpdateRate[UpRate]) are stopped. See 5.2.4 [Atomic Read Mechanism] for further details.
5	ReadOrder: atomic read order. Read-only. Reset: Cold,0. 0=Reading SBTSI::CpuTempInt causes the state of SBTSI::CpuTempDec to be latched. 1=Reading SBTSI::CpuTempDec causes the state of SBTSI::CpuTempInt to be latched. See 5.2.4 [Atomic Read Mechanism] for further details.
4:2	Reserved.
1	AraDis: ARA disable. Read-only. Reset: Cold,0. Read-only. 1=ARA response disabled.
0	Reserved.

SBTSIx04 [Update Rate] (SBTSI::UpdateRate)

Read-write. Reset: Cold,08h.

Bits	Description
7:0	UpRate: update rate. Read-write. Reset: Cold,08h. This field specifies the rate at which CPU temperature is compared against the temperature thresholds to determine if an alert event has occurred. Write access causes a reset of the alert history counters (specified by SBTSI::AlertThreshold[AlertThr]) and the corresponding timer (specified by SBTSI::UpdateRate[UpRate]).
ValidValues:	
Value	Description
00h	0.0625 Hz
01h	0.125 Hz
02h	0.25 Hz
03h	0.5 Hz
04h	1 Hz
05h	2 Hz
06h	4 Hz
07h	8 Hz
08h	16 Hz
09h	32 Hz
0Ah	64 Hz
FFh-0Bh	Reserved.

SBTSIx07 [High Temperature Integer Threshold] (SBTSI::HiTempInt)

Read-write. Reset: Cold,46h.

The high temperature threshold specifies the CPU temperature that causes ALERT_L to assert if the CPU temperature is greater than or equal to the threshold. SBTSI::HiTempInt and SBTSI::HiTempDec combine to specify the high temperature threshold. See 5.2.5 [SB-TSI Temperature and Threshold Encodings]. Reset value equals 70 °C. Write access causes a reset of the alert history counters (specified by SBTSI::AlertThreshold[AlertThr]) and the corresponding timer (specified by SBTSI::UpdateRate[UpRate]). See 5.2.3 [Alert Behavior].

Bits	Description
7:0	HiTempInt: high temperature integer threshold. Read-write. Reset: Cold,46h. This field specifies the integer portion of the high temperature threshold.

SBTSIx08 [Low Temperature Integer Threshold] (SBTSI::LoTempInt)

Read-write. Reset: Cold,00h.

The low temperature threshold specifies the CPU temperature that causes ALERT_L to assert if the CPU temperature is less than or equal to the threshold. SBTSI::LoTempInt and SBTSI::LoTempDec combine to specify the low temperature threshold. See 5.2.5 [SB-TSI Temperature and Threshold Encodings]. Write access causes a reset of the alert history counters (specified by SBTSI::AlertThreshold[AlertThr]) and the corresponding timer (specified by SBTSI::UpdateRate[UpRate]). See 5.2.3 [Alert Behavior].

Bits	Description
7:0	LoTempInt: low temperature integer threshold. Read-write. Reset: Cold,00h. This field specifies the integer portion of the low temperature threshold.

SBTSIx09 [SB-TSI Configuration Write] (SBTSI::ConfigWr)

Read-write. Reset: Cold,00h.

This register provides write access to SBTSI::Config.

Bits	Description
7	AlertMask: alert mask. Read-write. Reset: Cold,0. See SBTSI::Config[AlertMask].
6	RunStop: run stop. Read-write. Reset: Cold,0. See SBTSI::Config[RunStop].
5	ReadOrder: atomic read order. Read-write. Reset: Cold,0. See SBTSI::Config[ReadOrder].
4:2	Reserved.
1	AraDis: ARA disable. Read-write. Reset: Cold,0. See SBTSI::Config[AraDis].
0	Reserved.

SBTSIx10 [CPU Decimal Temperature] (SBTSI::CpuTempDec)

Read-only.

See SBTSI::CpuTempInt.

Bits	Description
7:5	CpuTempDec: decimal CPU temperature value. Read-only. Reset: Cold,XXXb. Read-only. This field returns the decimal portion of the CPU temperature.
4:0	Reserved.

SBTSIx11 [CPU Temperature Offset High Byte] (SBTSI::CpuTempOffInt)

Read-write. Reset: Cold,00h.

SBTSI::CpuTempOffInt and SBTSI::CpuTempOffDec combine to specify the CPU temperature offset. See 5.2.6 [SB-TSI Temperature Offset Encoding] for encoding details.

Bits	Description
7:0	CpuTempOffInt: CPU temperature integer offset. Read-write. Reset: Cold,00h. This field specifies the integer portion of the CPU temperature offset added to Tctl to calculate the CPU temperature. Write access causes a reset of the alert history counters (specified by SBTSI::AlertThreshold[AlertThr]) and the corresponding timer (specified by SBTSI::UpdateRate[UpRate]).

SBTSIx12 [CPU Temperature Decimal Offset] (SBTSI::CpuTempOffDec)

Read-write. Reset: Cold,00h.

See SBTSI::CpuTempOffInt.

Bits	Description
7:5	CpuTempOffDec: CPU temperature decimal offset. Read-write. Reset: Cold,0h. This field specifies the decimal/fractional portion of the CPU temperature offset added to Tctl to calculate the CPU temperature. Write access causes a reset of the alert history counters (specified by SBTSI::AlertThreshold[AlertThr]) and the corresponding timer (specified by SBTSI::UpdateRate[UpRate]).
4:0	Reserved.

SBTSIx13 [High Temperature Decimal Threshold] (SBTSI::HiTempDec)

Read-write. Reset: Cold,00h.

See SBTSI::HiTempInt.

Bits	Description
7:5	HiTempDec: high temperature decimal threshold. Read-write. Reset: Cold,0h. This field specifies the decimal portion of the high temperature threshold.
4:0	Reserved.

SBTSIx14 [Low Temperature Decimal Threshold] (SBTSI::LoTempDec)

Read-write. Reset: Cold,00h.

See SBTSI::LoTempInt.

Bits	Description
7:5	LoTempDec: low temperature decimal threshold. Read-write. Reset: Cold,0h. This field specifies the decimal portion of the low temperature threshold.
4:0	Reserved.

SBTSIx22 [Timeout Configuration] (SBTSI::TimeoutConfig)

Read-write. Reset: Cold,80h.

Bits	Description
7	TimeoutEn: SMBus timeout enable. Read-write. Reset: Cold,1. 0=SMBus defined timeout support disabled. 1=SMBus defined timeout support enabled. SMBus timeout enable.
6:0	Reserved.

SBTSIx32 [Alert Threshold Register] (SBTSI::AlertThreshold)

Read-write. Reset: Cold,00h.

See 5.2.3 [Alert Behavior].

Bits	Description
7:3	Reserved.
2:0	AlertThr: alert threshold. Read-write. Reset: Cold,0h. Specifies the number of consecutive CPU temperature samples for which a temperature alert condition needs to remain valid before the corresponding alert bit is set. For SBTSI::AlertConfig[AlertCompEn] == 1, it specifies the number of consecutive CPU temperature samples for which a temperature alert condition need to remain not valid before the corresponding alert bit gets cleared. Write access resets the alert history counters (specified by SBTSI::AlertThreshold[AlertThr]) and the corresponding timer (specified by SBTSI::UpdateRate[UpRate]). Details in SBTSI::Status.
ValidValues:	
Value	Description
0h	1 Sample
6h-1h	<Value+1> Samples
7h	8 Samples

SBTSIxBF [Alert Configuration] (SBTSI::AlertConfig)

Read-write.

Bits	Description
7:1	Reserved.
0	AlertCompEn: alert comparator mode enable. Read-write. Reset: Cold,X. 0=SBTSI::Status[TempHighAlert] and SBTSI::Status[TempLowAlert] are Read to clear. 1=SBTSI::Status[TempHighAlert] and SBTSI::Status[TempLowAlert] are Read-only; ARA response disabled. Write access does not change the alert history counters (specified by SBTSI::AlertThreshold[AlertThr]) or the corresponding timer (specified by SBTSI::UpdateRate[UpRate]). See SBTSI::Status.

SBTSIxFE [Manufacture ID] (SBTSI::ManId)

Read-only. Reset: Cold,00h.

Bits	Description
7:1	Reserved.
0	ManId: Manufacture ID. Read-only. Reset: Cold,0. Returns the AMD manufacture ID.

SBTSIxFF [Revision] (SBTSI::Revision)

Read-only. Reset: Cold,04h.

Bits	Description
7:0	Revision: SB-TSI revision. Read-only. Reset: Cold,04h. Specifies the SBI temperature sensor interface revision.

List of Namespaces

Namespace	Heading(s)
Core::X86::Apic	2.1.10.2.2 [Local APIC Registers]
Core::X86::Cpuid	2.1.11.1 [CPUID Instruction Functions]
Core::X86::Msr	2.1.12.1 [MSRs - MSR0000_xxxx] 2.1.12.2 [MSRs - MSRC000_xxxx] 2.1.12.3 [MSRs - MSRC001_0xxx] 2.1.12.4 [MSRs - MSRC001_1xxx]
Core::X86::Pmc::Core	2.1.13.3 [Large Increment per Cycle Events] 2.1.13.4.1 [Floating-Point (FP) Events] 2.1.13.4.2 [Load/Store (LS) Events] 2.1.13.4.3 [Instruction Cache (IC) and Branch Prediction (BP) Events] 2.1.13.4.4 [DE Events] 2.1.13.4.5 [EX (SC) Events]
Core::X86::Pmc::L2	2.1.13.4.6 [L2 Cache Events]
Core::X86::Pmc::L3	2.1.13.5.1 [L3 Cache PMC Events]
Core::X86::Smm	2.1.10.1.6 [System Management State]
IO	2.1.6 [PCI Configuration Legacy Access]
L3::L3CRB	2.2.1 [L3 MSR Registers]
L3::L3CT	2.2.2 [L3 Clocks and Test (CT) MSR Registers.]
MCA::CS	3.2.5.8 [CS]
MCA::DE	3.2.5.4 [DE]
MCA::EX	3.2.5.5 [EX]
MCA::FP	3.2.5.6 [FP]
MCA::IF	3.2.5.2 [IF]
MCA::KPX::GMI	3.2.5.15 [KPX GMI]
MCA::KPX::SERDES	3.2.5.14 [KPX SERDES]
MCA::L2	3.2.5.3 [L2]
MCA::L3	3.2.5.7 [L3]
MCA::LS	3.2.5.1 [LS]
MCA::MP5	3.2.5.12 [MP5]
MCA::NBIO	3.2.5.13 [NBIO]
MCA::PB	3.2.5.11 [PB]
MCA::PCS::GMI	3.2.5.16 [PCS GMI]
MCA::PIE	3.2.5.9 [PIE]
MCA::UMC	3.2.5.10 [UMC]

SBRMI	4.6 [SB-RMI Registers]
SBTSI	5.4 [SB-TSI Registers]

List of Definitions

ABS: ABS(integer expression): Remove sign from signed value.

AGESA™: AMD Generic Encapsulated Software Architecture.

AM5: Desktop, single socket. For client desktop platform (LGA) with DDR5. AM5 = (Core::X86::CpuId::BrandId[PkgType] == 00h).

AP: Applications Processor.

APML: Advanced Platform Management Link.

ARA: Alert response address.

ARP: Address Resolution Protocol

BAR: The BAR, or base address register, physical register mnemonic format is of the form PREFIXxZZZ. PREFIX is an all capital letter name that connotes the BAR to which the offset is added to get the physical address of the operation. ZZZ is the offset.

BCD: Binary Coded Decimal number format.

BCS: Base Configuration Space.

BIST: Built-In Self-Test. Hardware within the processor that generates test patterns and verifies that they are stored correctly (in the case of memories) or received without error (in the case of links).

BMC: Base management controller.

Boot VID: Boot Voltage ID. This is the VDD and VDDNB voltage level that the processor requests from the external voltage regulator during the initial phase of the cold boot sequence.

BSC: Boot strap core. Core 0 of the BSP.

BSP: Boot strap processor.

C-states: These are ACPI defined core power states. C0 is operational. All other C-states are low-power states in which the processor is not executing code. See docACPI.

Canonical-address: An address in which the state of the most-significant implemented bit is duplicated in all the remaining higher-order bits, up to bit[63].

CCX: Core Complex where more than one core shares L3 resources.

CEIL: CEIL(real expression): Rounds real number up to nearest integer.

CMP: Specifies the core number.

COF: Current operating frequency of a given clock domain.

Cold reset: PWROK is de-asserted and RESET_L is asserted.

Configurable: Indicates that the access type is configurable as described by the documentation.

CoreCOF: Core current operating frequency in MHz. CoreCOF = (Core::X86::Msrr::PStateDef[CpuFid[7:0]]/Core::X86::Msrr::PStateDef[CpuFidId]) * 200. A nominal frequency reduction can occur if spread spectrum clocking is enabled.

COUNT: COUNT(integer expression): Returns the number of binary 1's in the integer.

CpuCoreNum: Specifies the core number.

CPUID: The CPUID, or x86 processor identification state, physical register mnemonic format is of the form CPUID FnXXXX_XXXX_EiX[_xYYY], where XXXX_XXXX is the hex value in the EAX and YYY is the hex value in ECX.

DID: Divisor Identifier. Specifies the post-PLL divisor used to reduce the COF.

docACPI: Advanced Configuration and Power Interface (ACPI) Specification. <http://www.acpi.info>.

docAPM1: AMD64 Architecture Programmer's Manual Volume 1: Application Programming, order# 24592.

docAPM2: AMD64 Architecture Programmer's Manual Volume 2: System Programming, order# 24593.

docAPM3: AMD64 Architecture Programmer's Manual Volume 3: Instruction-Set Reference, order# 24594.

docAPM4: AMD64 Architecture Programmer's Manual Volume 4: 128-Bit and 256-Bit Media Instructions, order# 26568.

docAPM5: AMD64 Architecture Programmer's Manual Volume 5: 64-Bit Media and x87 Floating-Point Instructions, order# 26569.

docASF: Alert Standard Format Specification. <http://dmtf.org/standards/asf>.

docATA: AT Attachment with Packet Interface. <http://www.t13.org>.

docDP: VESA DisplayPort Standard. <http://www.vesa.org/vesa-standards>.

docI2C: I2C Bus Specification. http://www.nxp.com/documents/user_manual/UM10204.pdf

docIOMMU: AMD I/O Virtualization Technology Specification, order# 48882.

docJEDEC: JEDEC Standards. <http://www.jedec.org>.

docPCIe: PCI Express® Specification. <http://www.pcisig.org>.

docPCILb: PCI Local Bus Specification. <http://www.pcisig.org>.

docRevG: Revision Guide for AMD Family 19h Models 60h-6Fh Processors

docSATA: Serial ATA Specification. <http://www.sata-io.org>.

docSDHC: Secure Digital Host Controller Standard Specification. <https://www.sdcard.org>.

docUSB: Universal Serial Bus Specification. <http://www.usb.org>.

Doubleword: A 32-bit value.

DW: Doubleword.

EC: Embedded Controller.

ECS: Extended Configuration Space.

Error-on-read: Error occurs on read.

Error-on-write: Error occurs on write.

Error-on-write-0: Error occurs on bitwise write of 0.

Error-on-write-1: Error occurs on bitwise write of 1.

FCH: The integrated platform subsystem that contains the IO interfaces and bridges them to the system BIOS. Previously included in the Southbridge.

FID: Frequency Identifier. Specifies the PLL frequency multiplier for a given clock domain.

FL1: Notebook and mobile workstations. FL1 = (Core::X86::CpuId::BrandId[PkgType] == 01h).

FLOOR: FLOOR(integer expression): Rounds real number down to nearest integer.

GT/s: Giga-Transfers per second.

HWPF: Hardware Prefetcher.

IBS: Instruction based sampling.

IFCM: Isochronous flow-control mode, as defined in the link specification.

Inaccessible: Not readable or writable (e.g., Hide ? Inaccessible : Read-Write).

IO configuration: Access to configuration space through IO ports CF8h and CFCh.

IORR: IO range register.

KBC: Keyboard Controller.

L1 cache: The level 1 caches (instruction cache and the data cache).

L2 cache: The level 2 caches.

L3: Level 3 Cache. The L3 term is also in Addrmaps to enumerate CCX units.

L3 cache: Level 3 Cache.

Linear (virtual) address: The address generated by a core after the segment is applied.

LINT: Local interrupt.

Logical address: The address generated by a core before the segment is applied.

logical mnemonic: The register mnemonic format that describes the register functionally, what namespace to which the register belongs, a name for the register that connotes its function, and optionally, named parameters that indicate the different function of each instance (e.g., Link::Phy::PciDevVendIDF3). See 1.4.3.1 [Logical Mnemonic].

LRL: Least recently used.

LVT: Local vector table. A collection of APIC registers that define interrupts for local events (e.g., APIC[530:500] [Extended Interrupt [3:0] Local Vector Table]).

Macro-op: The front-end of the pipeline breaks instructions into macro-ops and transfers (dispatches) them to the back-end of the pipeline for scheduling and execution. See Software Optimization Guide.

Master abort: This is a PCI-defined term that is applied to transactions on other than PCI buses. It indicates that the transaction is terminated without affecting the intended target; Reads return all 1s; Writes are discarded; the master abort error code is returned in the response, if applicable; master abort error bits are set if applicable.

Master or SMBus Master: The device that initiates and terminates all communication and drives the clock, SCL.

MAX: MAX(integer expression list): Picks maximum integer or real value of comma separated list.

MB: Megabyte; 1024 KB.

MCA: Machine Check Architecture.

MCAX: Machine Check Architecture eXTensions.

MergeEvent: A PMC event that is capable of counter increments greater than 15, thus requiring merging a pair of even/odd performance monitors.

Micro-op: Processor schedulers break down macro-ops into sequences of even simpler instructions called micro-ops, each of which specifies a single primitive operation. See Software Optimization Guide.

MIN: MIN(integer expression list): Picks minimum integer or real value of comma separated list.

MMIO: Memory-Mapped Input-Output range. This is physical address space that is mapped to the IO functions such as the IO links or MMIO configuration.

MMIO configuration: Access to configuration space through memory space.

MSR: The MSR, or x86 model specific register, physical register mnemonic format is of the form MSRXXXX_XXXX, where XXXX_XXXX is the hexadecimal MSR number. This space is accessed through x86 defined RDMSR and WRMSR instructions.

MTRR: Memory-type range register. The MTRRs specify the type of memory associated with various memory ranges.

NBC: NBC=(CUID Fn00000001_EBX[LocalApicId[3:0]] == 0). Node Base Core. The lowest numbered core in the node.

NTA: Non-Temporal Access.

OW: Octword. An 128-bit value.

P-state: Performance state.

PCICFG: The PCICFG, or PCI defined configuration space, physical register mnemonic format is of the form DXFYxZZZ. X specifies the hexadecimal device number (this may be 1 or 2 digits). Y specifies the function number. ZZZ specifies the hexadecimal byte address (This may be 2 or 3 digits. e.g., D18F3x40 specifies the register at device 18h, function 3, and address 40h).

PCIe®: PCI Express.

PCS: Physical Coding Sublayer.

PEC: Packet error code.

physical mnemonic: The register mnemonic that is formed based on the physical address used to access the register (e.g., D18F3x00). See 1.4.3.2 [Physical Mnemonic].

PMC: The PMC, or x86 performance monitor counter, physical register mnemonic format is any of the forms {PMCxXXX, L2IPMCxXXX, NBPMCxXXX}, where XXX is the performance monitor select.

POR: Power on reset.

POW: POW(base, exponent): POW(x,y) returns the value x to the power of y.

PPIN: Protected Processor Inventory Number.

Processor: System on Chip (SoC) covered by this PPR. See 1.8 [Processor Overview].

PTE: Page table entry.

QW: Quadword. A 64-bit value.

RAS: Reliability, availability and serviceability (industry term). See 3.1 [Machine Check Architecture].

REFCLK: Reference clock. Refers to the clock frequency (100 MHz) or the clock period (10 ns) depending on the context used.

register instance parameter specifier: A register instance parameter specifier is of the form _register parameter name[register parameter value list] (e.g., The register instance parameter specifier _dct[1:0] has a register parameter name of dct (The DCT PHY instance name) and a register parameter value list of "1:0" or 2 instances of DCT PHY).

register instance specifier: The register instance specifier exists when there is more than one instance for a register. The register instance specifier consists of one or more register instance parameter specifier (e.g., The register instance specifier _dct[1:0]_chiplet[BCST,3:0]_pad[BCST,11:0] consists of 3 register instance parameter specifiers, _dct[1:0], _chiplet[BCST,3:0], and _pad[BCST,11:0]).

register name: A name that connotes the function of the register.

register namespace: A namespace for which the register name must be unique. A register namespace indicates to which IP it belongs and an IP may have multiple namespaces. A namespace is a string that supports a list of "::" separated names. The convention is for the list of names to be hierarchical, with the most significant name first and the least significant name last (e.g., Link::Phy::Rx is the RX component in the Link PHY).

register parameter name: A register parameter name is the name of the number of instances at some level of the logical hierarchy (e.g., The register parameter name dct specifies how many instances of the DCT PHY exist).

register parameter value list: The register parameter value list is the logical name for each instance of the register parameter name (e.g., For _dct[1:0], there are 2 DCT PHY instances, with the logical names 0 and 1, but it should be noted that the logical names 0 and 1 can correspond to physical values other than 0 and 1). It is the purpose of the AddressMappingTable to map these register parameter values to physical address values for the register.

Reserved-write-as-0: Reads are undefined. Must always write 0.

Reserved-write-as-1: Reads are undefined. Must always write 1.

ROUND: ROUND(real expression): Rounds to the nearest integer; halfway

rounds away from zero.

RTS: Remote temperature sensor, typical examples are ADM1032, LM99, MAX6657, EMC1002.

SB-RMI: Remote Management interface.

SB-TSI: Sideband Internal Temperature Sensor Interface. See APML.

SBI: Sideband interface.

Shutdown: A state in which the affected core waits for either INIT, RESET, or NMI. When shutdown state is entered, a shutdown special cycle is sent on the IO links.

Slave or SMBus slave: The slave cannot initiate SMBus communication and cannot drive the clock but can drive the data signal SDA and the alert signal ALERT_L.

SMAF: System Management Action Field. This is the code passed from the SMC to the processors in STPCLK assertion messages.

SMI: System management interrupt.

SMM: System Management Mode.

SMT: Simultaneous multithreading. See

Core::X86::CpuId::CoreId[ThreadsPerCore].

Speculative event: A performance monitor event counter that counts all occurrences of the event even if the event occurs during speculative code execution.

SSC: Spread Spectrum Clocking.

SVM: Secure virtual machine.

TCC: Temperature calculation circuit.

Tctl: Processor temperature control value.

TDC: Thermal Design Current.

TDP: Thermal Designer Power. A power consumption parameter that is used in conjunction with thermal specifications to design appropriate cooling solutions for the processor.

Thread: One architectural context for instruction execution.

TOM2: Top of extended Memory.

TSI: Temperature sensor interface.

TSM: Temperature sensor macro.

UMI: Unified Media Interface. The link between the processor and the FCH.

UNIT: UNIT(register field reference): Input operand is a register field reference that contains a valid values table that defines a value with a unit (e.g., clocks, ns, ms, etc.). This function takes the value in the register field and returns the value associated with the unit (e.g., If the field had a valid value definition where 1010b was defined as 5 ns). Then if the field had the value of 1010b, then UNIT() would return the value 5.

Unpredictable: The behavior of both reads and writes is unpredictable.

VID: Voltage level identifier.

Volatile: Indicates that a register field value may be modified by hardware, firmware, or microcode when fetching the first instruction and/or might have read or write side effects. No read may depend on the results of a previous read and no write may be omitted based on the value of a previous read or write. Not volatile indicates that software may service a read from the results of a previous read and that a write may be dropped if it's value matches the value previously read or written.

Warm reset: RESET_L is asserted only (while PWROK stays high).

WDT: Watchdog timer. A timer that detects activity and triggers an error if a specified period of time expires without the activity.

WRIG: Writes Ignored.

Write-0-only: Writing a 0 clears to a 0; Writing a 1 has no effect. If not associated with Read, then reads are undefined.

Write-1-only: Writing a 1 sets to a 1; Writing a 0 has no effect. If not associated with Read, then reads are undefined.

Write-1-to-clear: Writing a 1 clears to a 0; Writing a 0 has no effect. If not associated with Read, then reads are undefined.

Write-once: Capable of being written once; all subsequent writes have no effect. If not associated with Read, then reads are undefined.

X2APICEN: x2 APIC is enabled. X2APICEN =

(Core::X86::Msr::APIC_BAR[ApicEn] && Core::X86::Msr::APIC_BAR[x2ApicEn]).

XBAR: Cross bar; command packet switch.

Memory Map - MSR

Physical Mnemonic	Namespace
0000_0000h...0000_0001h	MCA::LS
0000_0010h...0000_02FFh	Core::X86::Msr
0000_0400h...0000_0403h	MCA::LS
0000_0404h...0000_0407h	MCA::IF
0000_0408h...0000_040Bh	MCA::L2
0000_040Ch...0000_040Fh	MCA::DE
0000_0414h...0000_0417h	MCA::EX
0000_0418h...0000_041Bh	MCA::FP
0000_041Ch...0000_043Bh	MCA::L3
0000_043Ch...0000_043Fh	MCA::MP5
0000_0440h...0000_0443h	MCA::PB
0000_0444h...0000_044Bh	MCA::PCS::GMI
0000_044Ch...0000_0453h	MCA::KPX::GMI
0000_0454h...0000_045Bh	MCA::UMC
0000_045Ch...0000_0463h	MCA::CS
0000_0464h...0000_0467h	MCA::NBIO
0000_0470h...0000_0473h	MCA::PIE
0000_0474h...0000_047Bh	MCA::KPX::SERDES
0000_06A0h...0000_0853h	Core::X86::Msr
00000C81	L3::L3CRB
0000_0C8Dh...0000_0C8Fh	Core::X86::Msr
0000_0C90h...0000_0C9Fh	L3::L3CRB
0000_0DA0h...C000_010Fh	Core::X86::Msr
C000_0200h...C000_028Fh	L3::L3CRB
C000_0300h...C000_0410h	Core::X86::Msr
C000_2000h...C000_2009h	MCA::LS
C000_2010h...C000_2016h	MCA::IF
C000_2020h...C000_2029h	MCA::L2
C000_2030h...C000_2036h	MCA::DE
C000_2050h...C000_2056h	MCA::EX
C000_2060h...C000_2066h	MCA::FP
C000_2070h...C000_20E9h	MCA::L3
C000_20F0h...C000_20F6h	MCA::MP5
C000_2100h...C000_2106h	MCA::PB
C000_2110h...C000_2129h	MCA::PCS::GMI
C000_2130h...C000_2149h	MCA::KPX::GMI
C000_2150h...C000_216Fh	MCA::UMC
C000_2170h...C000_2189h	MCA::CS
C000_2190h...C000_2198h	MCA::NBIO
C000_21C0h...C000_21C9h	MCA::PIE
C000_21D0h...C000_21E8h	MCA::KPX::SERDES
C001_0000h...C001_0230h	Core::X86::Msr
C0010231	L3::L3CRB
C0010232	Core::X86::Msr
C0010233	L3::L3CRB
C0010234	Core::X86::Msr
C0010235	L3::L3CRB

C0010236	Core::X86::Msr
C0010237	L3::L3CRB
C0010238	Core::X86::Msr
C0010239	L3::L3CRB
C001023A	Core::X86::Msr
C001023B	L3::L3CRB
C001_0240h...C001_025Fh	Core::X86::Msr
C0010299	L3::L3CT
C001029A	Core::X86::Msr
C001029B	L3::L3CT
C001_02B0h...C001_031Fh	Core::X86::Msr
C0010400	MCA::LS
C0010401	MCA::IF
C0010402	MCA::L2
C0010403	MCA::DE
C0010405	MCA::EX
C0010406	MCA::FP
C001_0407h...C001_040Eh	MCA::L3
C001040F	MCA::MP5
C0010410	MCA::PB
C001_0411h...C001_0412h	MCA::PCS::GMI
C001_0413h...C001_0414h	MCA::KPX::GMI
C001_0415h...C001_0416h	MCA::UMC
C001_0417h...C001_0418h	MCA::CS
C0010419	MCA::NBIO
C001041C	MCA::PIE
C001_041Dh...C001_041Eh	MCA::KPX::SERDES
C001_0800h...C001_103Ch	Core::X86::Msr
C001_1095h...C001_109Ah	L3::L3CRB

Memory Map - SMN

Physical Mnemonic	Namespace
20350400: L3CRB00x000004A0...x000004C8	L3::L3CRB
20B50400: L3CRB10x000004A0...x000004C8	L3::L3CRB