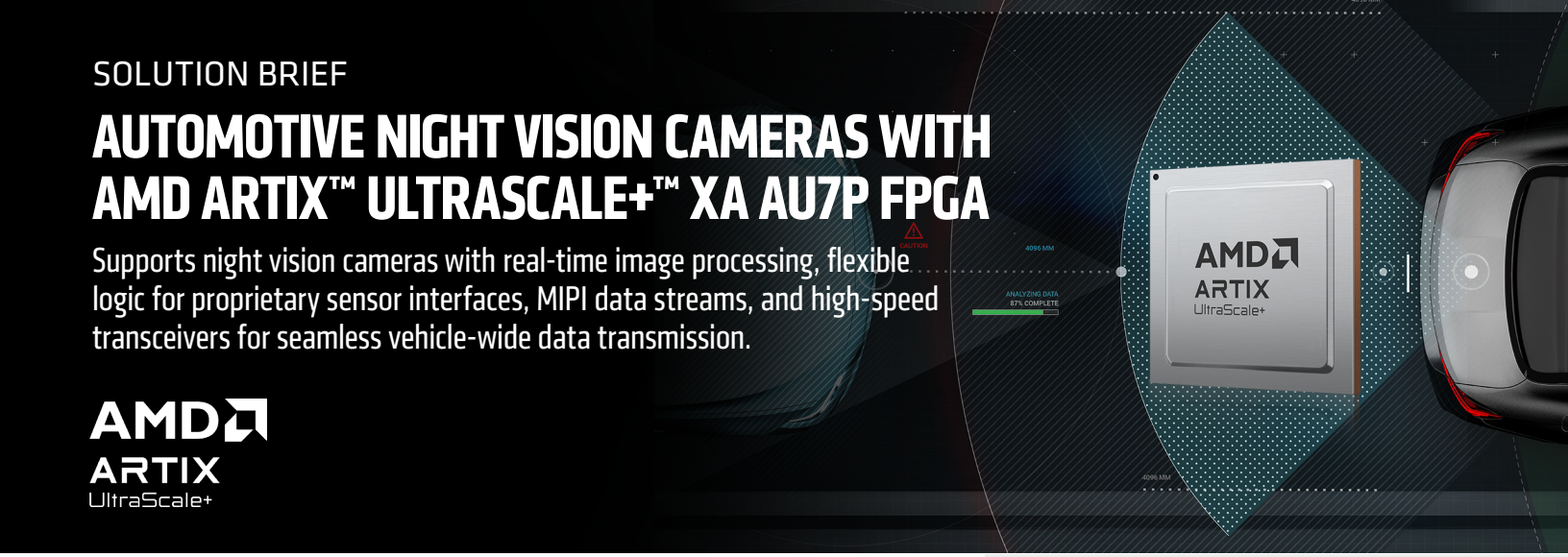
SOLUTION BRIEF

AUTOMOTIVE NIGHT VISION CAMERAS WITH AMD ARTIX™ ULTRASCALE+™ XA AU7P FPGA

Supports night vision cameras with real-time image processing, flexible logic for proprietary sensor interfaces, MIPI data streams, and high-speed transceivers for seamless vehicle-wide data transmission.



OVERVIEW

The AMD Artix™ UltraScale+™ XA AU7P FPGA offers a compact, power-efficient, and cost-optimized solution for night vision cameras in ADAS and autonomous vehicles. Its innovative architecture and advanced peripherals deliver exceptional performance per watt to support long-wave infrared (LWIR) cameras, vital for enhancing Automatic Emergency Braking (AEB) and pedestrian detection.

LWIR cameras detect heat signatures of pedestrians, animals, and objects in low visibility. A 2024 U.S. Department of Transportation mandate requires AEB systems with night functionality in all new vehicles by 2029, propelling the adoption of advanced sensing technologies. The expected rise of L4 vehicles and robotaxis in the 2030s will further boost demand for automotive LWIR cameras.

The 9x9 mm Artix UltraScale+ XA AU7P FPGA meets stringent automotive LWIR requirements with an automotive-grade package, AEC-Q00 qualification, and ISO 26262 ASIL-B certification. Leveraging the AMD LUT6 architecture and superior thermal resistance, it delivers exceptional efficiency, making the XA AU7P FPGA the premier choice for advanced night vision cameras.

KEY BENEFITS

HIGH COMPUTE TO OPTIMAL COST & POWER
Optimized performance per watt, delivering exceptional compute density in a cost-effective package.

FLEXIBILITY
Seamless integration with diverse sensor interfaces, ISP pipelines, and ADAS data types.

STATE OF THE ART FUNCTIONAL SAFETY
Certified to ISO 26262 ASIL-B standards, ensuring reliable operation in critical automotive systems.

SECURITY
Features multi-level protection with RSA-2048 authentication, NIST-certified AES-GCM decryption, and anti-tamper capabilities. Other features include CNSA 2.0 PQC & certified secure boot.

HIGHLIGHTS

ADVANCED DSP COMPUTE FOR IMAGE SENSOR PROCESSING

- 216 DSP slices support real-time pixel correction and image enhancement for LWIR sensor data.
- Optimized for fixed- and floating-point computation.

HIGH I/O BANDWIDTH AND COMPUTE FOR VEHICLE-WIDE COMMUNICATION

- AMD Artix UltraScale+ FPGAs offer up to 1.8X higher F_{MAX} compared to Lattice 16 nm solutions, enabling faster real-time image processing.[1]
- 2.5 Gb/s MIPI performance supports the latest sensor technologies.
- The 16 Gb/s line rate enables high-speed data transfer from LWIR sensors to ADAS systems with optimal signal integrity.

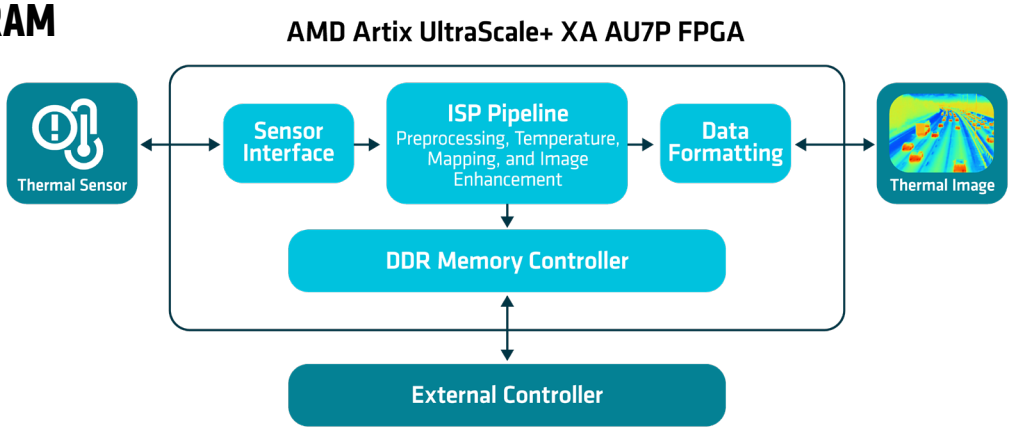
AUTOMOTIVE-GRADE CHIPSCALE PACKAGE FOR SPACE-CONSTRAINED CAMERAS

- Ultra-compact 9x9 mm form factor fits into space-limited camera housings.
- Chipscale packaging enhances signal density, reliability, and electrical performance for edge sensors.

LOW-POWER FOR ACCURATE THERMAL SENSING

- AMD UltraScale+ devices offer up to 46% lower total power compared to Lattice Nexus.[2]
- AMD packages offer up to 34% lower junction-to-ambient thermal dissipation compared to equivalent Lattice device packages,[3] allowing simplified thermal management in LWIR camera housings.
- AMD Artix UltraScale+ low-voltage, low-speed grade devices enable reduction in static and dynamic power.

BLOCK DIAGRAM



FEATURES

AMD ARTIX ULTRASCALE+ XA FPGA HIGHLIGHTS	
ENHANCED & OPTIMIZED PROGRAMMABLE LOGIC ARCHITECTURE	• Up to 40% lower utilization with LUT6 architecture over LUT4[4] • Voltage scaling to tune power and performance on the same device • Enhanced CLB/LUTs, routing, and ASIC-class clocking for high utilization
HIGH-PERFORMANCE TRANSCEIVERS	• Minimum of 12 Gb/s and up to 16 Gb/s transceiver line rates • Power-optimized architecture vs. Artix 7 FPGAs • Single oscillator for fabric and SerDes eliminates extra clocking components
EXCEPTIONAL DSP COMPUTE	• Highest performance in a cost-optimized AMD FPGA • Up to 1,860 GOP/s, 620 GFLOPs (FP32) in the largest device
SAFETY AND MULTI-LEVEL SECURITY FEATURES	• RSA-4096 authentication to verify design source • NIST AES-CGM decryption approved, for faster configuration • Permanent tamper penalty to prevent adversaries from accessing security features • Security monitoring IP to adapt to security threats across the product lifecycle
OUTSTANDING MIPI AND LVDS PERFORMANCE	• Up to 2500 Mb/s MIPI and LVDS performance • Support for advanced vision sensors (MIPI, SLVS-EC)
ANALOG MIXED-SIGNAL MONITORING BLOCK	• Voltage, current, and temperature tracking for safe, secure, and reliable operation • Helps meet requirements for key standards: FIPS 140-2, IEC 61508, and ISO26262 • Allows for integration of low-amplitude sensors
ROBUST AUTOMOTIVE IP PORTFOLIO	• SEM-IP • CAN/CAN-FD • MIPI Controller • Ethernet IP • Video Processing IP: scalers, frame capture, color space converters, ISP, etc. • DSP IP: FFT and assorted functions

NEXT STEPS

- Explore a full list of **Automotive IP** offered through AMD & partners
- Learn more about the **automotive-grade AMD Artix™ UltraScale+™ portfolio**
- Learn more about **AMD competitive advantages** over other offerings in the market

ENDNOTES

1. Based on AMD analysis in July 2024, calculating F_{MAX} ratios averaged over 30 open-core designs for (16 nm) AMD Artix UltraScale+ AU7P FPGA, compared to the (16 nm) Lattice Avant E70 FPGA, at the respective highest speed grades. Results will vary based on architecture, device, speed grade, package size, design, configuration, and other factors. (AUS-010)
2. Based on AMD testing in July 2024, performed in AMD Power Estimation Tools (XPE_2019_1_2 for 28 nm node size and PDM_2024.1 for 16 nm node size), and Lattice Radiant Power Estimation Tool 2024.1, to measure the power consumption of the AMD Spartan UltraScale+ FPGAs versus the Lattice Nexus platform. Total Power results include fabric power and HDIO only. Stated results assume a normalized max ambient temperature of 100°C. Actual performance, power consumption, and/or power savings will vary based on device, customer design specifications, system configuration, and other factors. (SUS-014)
3. Based on July 2024 AMD analysis of published data sheets using standard JESD51 definition for θJa versus equivalent Lattice packages. Stated results are provisional and will vary based on architecture, package size, speed grade, device, design, configuration, and other factors. (COP-002)
4. Based on AMD testing in July 2024, measuring the utilization scores of the LUT6 architecture-based AMD Artix 7 A100T (28 nm) and Artix UltraScale+ AU7P (16 nm) versus the LUT4 architecture-based Lattice Nexus MachXO5 25 (28 nm) and Lattice Avant E70 (16 nm) devices, measured on AMD Vivado 2024.1 and Lattice Radiant 2024.1, respectively, at various speed grades, averaged over 30 open-core designs. Results will vary based on architecture, device, speed grade, package size, design, configuration, and other factors. (COP-001)

DISCLAIMERS

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