SOLUTION BRIEF

INDUSTRIAL AUTOMATION FIELD EQUIPMENT WITH AMD COST-OPTIMIZED DEVICES

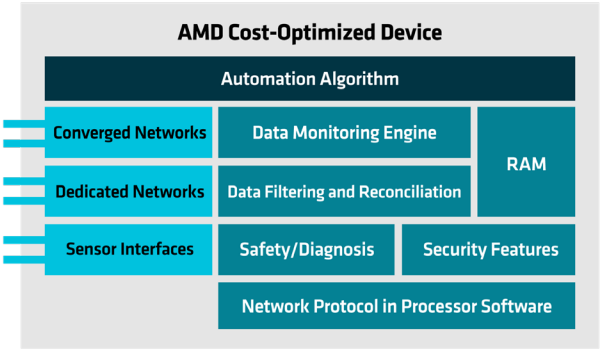
AMD
together we advance_

OVERVIEW

The automation of industrial processes is key to increasing productivity in the factory. While experience with a specific process is critical in implementing effective automation, the underlying technology defines how far automation can evolve. The following elements are key factors in maximizing productivity through automation:

- **Connectivity:** Multi-networked operation for access to maximum momentary and historical information
- **Memory:** Capability to store streams of information locally
- **Real-time data monitoring, filtering, reconciliation:** Local data processing engines
- **Functional safety:** Diagnostic coverage with integrated monitors and custom function in logic. Certified systematic capability.
- **Security features:** Anti-Tamper, Information Assurance, Supply-Chain Assurance to help protect automation in the field from attacks

AMD cost-optimized devices integrate all functions in a platform concept. Programmability adds flexibility for continuous improvements of automation algorithms over the lifetime and allows the operator to increase productivity more and more without changing hardware.



HIGHLIGHTS

AMD COST-OPTIMIZED DEVICES OFFER SIGNIFICANT BENEFITS OVER COMPETING SOLUTIONS

- Leading integration scale with 40% better utilization using LUT6 vs. competing LUT4 architecture[1]
- An average 1.8X higher F_{MAX} using the same 16 nm process node at the highest speed grades[2]
- Up to 46% lower total power consumption using LUT6 architecture and advanced packaging vs. competing LUT4 architecture[3]
- Certified Safety design flow
- AMD LogiCORE™ IP Catalog

KEY BENEFITS

SCALABILTY

- Wide range of available densities
- Scalable integrated memory
- High programmable I/O count
- Migration path from FPGA to SoC

SAFETY CERTIFICATION

- Annual design flow audits
- Certified systematic capability
- Tools for failure rate analysis

SECURITY FEATURES

- Authentication and encryption
- System monitors
- Secure provisioning
- Post Quantum Cryptography (PQC)

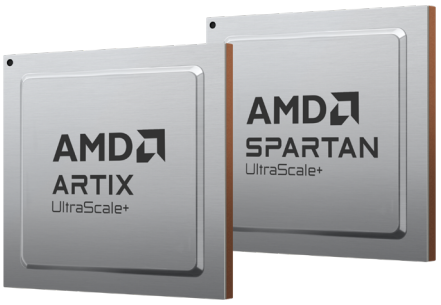
LONG LIFECYCLE

- At least 15+ years availability
- In-field updates
- Easy migration between families

INTELLIGENT AND CONNECTED FIELD EQUIPMENT

DIFFERENTIATORS

ADAPTIVE TECHNOLOGY HIGHLIGHTS	
SCALABLE DATA ACQUISITION	• Programmable I/Os • Ethernet, Industrial Networking, TSN* • High-Speed Transceivers
ADAPTABLE FOR BROWNFIELD	• Connects to both new and legacy industrial equipment • High number 3.3V capable ports (Spartan™ UltraScale+™ FPGAs)
READY FOR UPCOMING SECURITY STANDARDS	• Post-Quantum Crypto for Secure Boot • User accessible security resources • TRNG and PUF
HIGH COMPUTE PERFORMANCE	• Scalable compute performance with AMD MicroBlaze™ V (RISC-V soft core) processor • Integrated memory controller and interfaces to LPDDR4 and LPDDR3*



* In select devices

TARGET APPLICATIONS

SMART SENSOR

- Flexible interfacing to all types of sensing equipment via fieldbuses, industrial Ethernet, image sensor interfaces, SPI, I^2C, and AD converters
- Real-time behavior for processing of cyclic information from sensors
- Processing of received data with algorithms in programmable logic
- Connection to a superordinated IP network using Ethernet
- Integration of building blocks using a common design flow with AMD tools

HIGH-PERFORMANCE SAFE CONTROL OF ACTUATORS

- Deterministic control loops for inverters in fast programmable logic and 1.8X higher clock frequency[2]
- Scalable for multiple connected actuators
- Improved diagnostic coverage with isolated monitoring using the AMD Isolation Design Flow (IDF)
- Comprehensive user guide, tools, and safety manual on the web-based AMD Safety Lounge (requires purchasing of Functional Safety Package)
- Fast time to market with the AMD safety certified design flow

DATA COLLECTION AND FORWARDING IN INDUSTRIAL IOT

- On device RAM in different densities as block RAM, UltraRAM, or distributed RAM
- MicroBlaze V controller and application processor with RISC-V ISA
- AMD Time Sensitive Networking (TSN) Subsystem on Artix™ UltraScale+ FPGAs
- Security features to help ensure genuine programming files and protect intellectual property
- Out-of-the-box solution with AMD Vivado™ Design Suite for superior timing closure,[4] even for complex processing tasks

IP

KEY INTELLECTUAL PROPERTY		PROVIDED BY
TSN ENDPOINT SUBSYSTEM	• The Time Sensitive Networking LogiCore IP from AMD allows to connect the processing system of AMD SoCs directly to TSN infrastructure	**AMD**
MANAGED / UNMANAGED ETHERNET SWITCH	• Switches build Ethernet Infrastructure with a scalable number of ports. Interface speeds up to 10 Gb/s are possible	**SOC-E**
INDUSTRIAL NETWORKING	• Profinet, EtherNet/IP with integrated MicroBlaze processor for a networking solution with deterministic performance by design	**SOFTING**

FEATURES

PLATFORM HIGHLIGHTS	
SPARTAN ULTRASCALE+ FPGA	• Highest I/O-to-logic-cell ratio with high number of 3.3V capable ports[5] • Integrated DDR Memory Controller* • Compliant PCIe® Gen4* • Lower density devices for power-constrained applications
ARTIX ULTRASCALE+ FPGA	• Transceivers with up to 16 Gb/s • Very small form factor InFO and CSP packages available • Massive DSP bandwidth, up to 1.8 TeraMACs • Time Sensitive Networking IP from AMD

* In select devices

NEXT STEPS

- Explore a full list of **Industrial IP** offered through AMD & partners
- Learn more about **AMD Spartan UltraScale+ FPGAs**
- Learn more about **AMD Artix UltraScale+ FPGAs**
- Learn more about **AMD competitive advantages** over other offerings in the market

ENDNOTES

1. Based on AMD testing in July 2024, measuring the utilization scores of the LUT6 architecture-based AMD Artix 7 A100T (28 nm) and Artix UltraScale+ AU7P (16 nm) versus the LUT4 architecture-based Lattice Nexus MachXO5 25 (28 nm) and Lattice Avant E70 (16 nm) devices, measured on AMD Vivado 2024.1 and Lattice Radiant 2024.1, respectively, at various speed grades, averaged over 30 open-core designs. Results will vary based on architecture, device, speed grade, package size, design, configuration, and other factors. (COP-001)
2. Based on AMD analysis in July 2024, calculating F_{MAX} ratios averaged over 30 open-core designs for (16 nm) AMD Artix UltraScale+ AU7P FPGA, compared to the (16 nm) Lattice Avant E70 FPGA, at the respective highest speed grades. Results will vary based on architecture, device, speed grade, package size, design, configuration, and other factors. (AUS-010)
3. Based on AMD testing in July 2024, performed in AMD Power Estimation Tools (XPE_2019_1_2 for 28 nm and PDM_2024.1 for 16 nm), and Lattice Radiant Power Estimation Tool 2024.1, to measure the power consumption of the Spartan UltraScale+ 35P, 50P, and 100P FPGAs versus Lattice MachXO5-NX 25, CertusPro-NX50, and MachXO5-NX 100T FPGAs at HP speed grade. Total Power results include fabric power and HDIO only. Stated results assume a normalized max ambient temperature of 100°C and a 40% utilization advantage for LUT6, when selecting competitive devices for comparison. Results are subject to change when products are released in market and will vary based on architecture, package size, speed grade, device, design, configuration, and other factors. (SUS-014)
4. Based on AMD place-and-route testing in September 2024, using 26 open-core designs compiled with Vivado 2024.1 and Lattice Radiant Software 2024.1 in default mode, with the Artix UltraScale+ AU10P device vs. Lattice Mach LFMXO5 device @ 150 MHz F_{MAX} target; and Kintex UltraScale+ KU5P device vs. Lattice Avant E70 device @ 200 MHz F_{MAX} target. P&R performance will vary based on device, design, configuration, and other factors. (VIV-011)
5. Highest I/O-per-logic-cell is based on an AMD internal analysis of the product data sheet for AMD Spartan UltraScale+ SU10P FPGA and the published product data sheets for the comparable competitive FPGAs with a 28 nm and lower node-size, from Efinix, Intel, Lattice, and Microchip. Cost reduction per I/O is based on AMD list prices for the AMD Spartan UltraScale+ SU10P versus Spartan 7 7S50, as of February 2024, for designs requiring at least 200 GPIO. (SUS-011)

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