SOLUTION BRIEF

AMD CPU AND FPGA INTEGRATION FOR SERVER I/O

ENABLING GPU AND CPU I/O EXPANSION AND SECURITY

AMD
together we advance_

OVERVIEW

The data center server market is becoming increasingly competitive. Server manufacturers have access to the same underlying compute technologies, meaning performance is a table stake. To differentiate and win in the market, ODMs and OEMs are being driven to integrate increasingly advanced features. Capabilities like advanced security, real-time monitoring, networking, power efficiency, and more are becoming critical to purchasing decisions. The vast majority of servers today rely on FPGAs to orchestrate this differentiation, adding intelligence to host processor motherboards (HPM) and server control modules (SCM). AMD Spartan™ UltraScale+™ FPGAs enable next-generation server designs through state-of-the-art security with post-quantum cryptography, the industry's highest ratio of I/O to programmable logic,[1] and integration with AMD EPYC™ Server CPUs.

HIGHLIGHTS

FAST TIME TO MARKET WITH A PROVEN CPU + FPGA SOLUTION

- Reduce OpEx and mitigate schedule risk by leveraging AMD EPYC HPM and SCM reference platforms, designed using Spartan 7 and Spartan UltraScale+ FPGAs
- Simplify support by working with a single vendor across CPU and FPGAs
- Push-button FPGA timing closure with industry-leading development environment[2] and a two-speed-grade performance advantage[3]

DESIGN WITH STATE-OF-THE-ART SECURITY

- PQC FPGA secure boot to ensure authenticity of HPM, SCMs, and BMC programmable devices
- Programmable logic access to hard silicon security resources for secure storage and PFR use-cases, including TRNG, PUF, LMS, and more

ADVANCED CONNECTIVITY AND SCALABLE PORTFOLIO

- Industry's highest ratio of I/O-to-logic with rich 3.3V I/O support[1]
- Over 50 cost-optimized devices to enable selection of the ideal device
- Options for PCIe®-attach board control
- Proven reliability with 7 Series and UltraScale+ portfolios

KEY BENEFITS

PART OF AMD EPYC PROCESSOR REFERENCE DESIGN

- Design for Spartan UltraScale+ FPGAs and AMD EPYC host processor
- Low-risk path to motherboard implementation
- AMD technical support across products

I/O EFFICIENCY

- Aggregates low-speed signaling protocols
- Support for I2C /SMBus, GPIO, and UART
- Minimizes I/O pins for component connectivity
- Board real estate savings

INTEROPERABILITY & OPEN STANDARDS

- Open Compute Platform (OCP) compliant
- IP tested to latest specifications
- LTPI IP available
- Targets multiple vendor x86 platforms

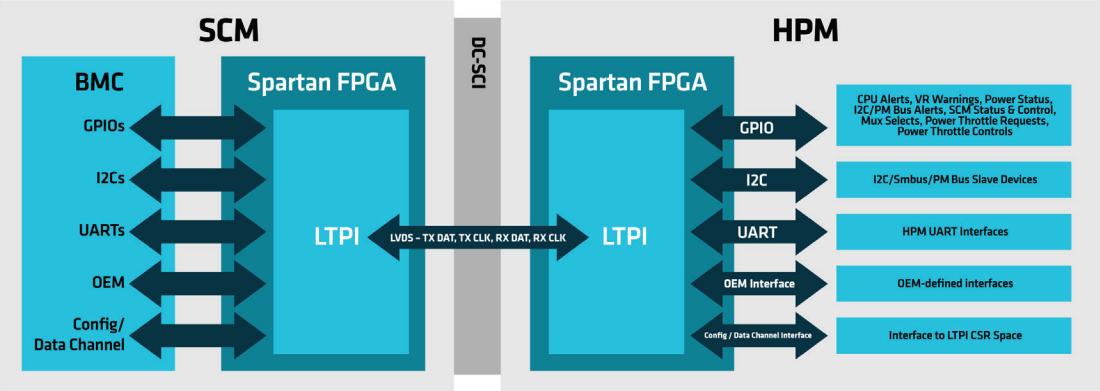
FPGA HARDWARE FLEXIBILITY

- Efficient use of fabric resources
- Field upgradeable for new standards
- Adapt quickly with broad IP catalog

INTEGRATE ADDITIONAL FUNCTIONALITY

- Power monitoring and control
- System reset and bring-up logic
- Hot-plug logic
- I/O expanders for CPU and BMC

EXAMPLE SERVER I/O BLOCK DIAGRAM



COMPETITIVE ADVANTAGES

AMD SPARTAN ULTRASCALE+ FPGA	
SERVER REFERENCE DESIGN SUPPORT	• AMD-supported reference design including AMD CPUs and FPGAs • Proven interoperability • Single vendor support • Access to Devhub and server architecture
FLEXIBLE I/O	• Industry highest I/O-to-logic-cell ratio[1] • Up to 572 I/O on a single FPGA • Multiple voltage ranges (1.5V – 3.3V) • Multiple I/O types supporting diverse set of standard interfaces • Flexible clocking
SECURITY	• Platform Management Controller (PMC) with dedicated security resources • PQC Secure Boot of FPGA image • User access to PMC enables use of security resources post-boot for secure storage and HWRoT use-cases • True Random Number Generator (TRNG) and Physical Unclonable Function (PUF)
POWER/PERFORMANCE ADVANTAGE	• Up to 46% lower power leveraging 16 nm FinFET and super packaging technology[4] • Two-speed-grade performance advantage[3] • Push-button timing closure for typical board control designs

NEXT STEPS

- Learn more about **AMD competitive advantages** over other offerings in the market
- For information on Spartan UltraScale+ FPGA silicon and eval board, contact your local sales representative or email **dc-inquiries@amd.com**.

ENDNOTES

1. Based on AMD internal analysis December 2023, comparing the total I/O-to-logic-cell ratio for AMD Spartan UltraScale+ FPGAs to previous generations of AMD cost-optimized FPGAs. (SUS-001)
2. Based on AMD place-and-route testing in September 2024, using 26 open-core designs compiled with AMD Vivado 2024.1 and Lattice Radiant Software 2024.1 in default mode, with the AMD Artix UltraScale+ AU10P device vs. Lattice Mach LFMXO5 device @ 150 MHz F_{MAX} target; and AMD Kintex UltraScale+ KU5P device vs. Lattice Avant E70 device @ 200 MHz F_{MAX} target. P&R performance will vary based on device, design, configuration, and other factors. (VIV-011)
3. Based on AMD analysis in July 2024, calculating the F_{MAX} yields for all available speed grades for the (16 nm) AMD Artix UltraScale+ AU7P and the (16 nm) Lattice Avant E70. Actual results will vary based on architecture, device, speed grade, package size, design, configuration, and other factors. (AUS-009)
4. Based on AMD testing in July 2024, performed in AMD Power Estimation Tools (XPE_2019_1_2 for 28 nm and PDM_2024.1 for 16 nm), and Lattice Radiant Power Estimation Tool 2024.1, to measure the power consumption of the AMD Spartan UltraScale+ 35P, 50P, and 100P FPGAs versus Lattice MachXO5-NX 25, CertusPro-NX50, and MachXO5-NX 100T FPGAs at HP speed grade. Total Power results include fabric power and HDIO only. Stated results assume a normalized max ambient temperature of 100°C and a 40% utilization advantage for LUT6, when selecting competitive devices for comparison. Results are subject to change when products are released in market and will vary based on architecture, package size, speed grade, device, design, configuration, and other factors. (SUS-014)

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