5 REASONS TO CHOOSE AMD COST-OPTIMIZED FPGAs FOR YOUR NEXT DESIGN

At a glance

Unlock efficiency today and into the future with the utilization, performance, and package advantages of the AMD Cost-Optimized Portfolio of FPGAs and adaptive SoCs—available at price points that balance feature set and affordability.

1 OPTIMIZE LUT UTILIZATION AND DO MORE WITH LESS

Great designs start with a great architecture: The LUT6 architecture of AMD UltraScale+™ and 7 Series devices provides a 40% average utilization advantage over the legacy LUT4 architecture used by Lattice Semiconductor.[1]

2 MAXIMIZE EFFICIENCY WITH A TWO-SPEED-GRADE PERFORMANCE ADVANTAGE

The slowest AMD Artix™ UltraScale+ speed grade (-1L) outpaces Lattice's fastest Avant speed grade (-9 HV) by up to 31%, resulting in a two-speed-grade advantage.[2] Pinning fastest to fastest, AMD excels with up to a 1.8X higher F_{MAX} advantage.[3]

3 ENHANCE THERMAL DISSIPATION WITH ADVANCED PACKAGING

Minimize the temperature of devices under load to reduce static power consumption and simplify product design. The advanced packages of AMD cost-optimized FPGAs and adaptive SoCs provide 34% lower thermal resistance on average than equivalent Lattice device packages.[4]

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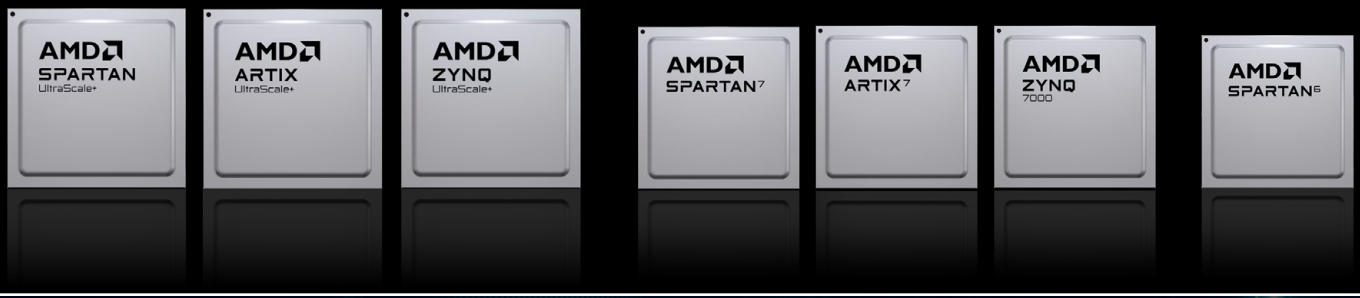
4 REDUCE POWER CONSUMPTION

The lower static and dynamic power usage of AMD cost-optimized devices supports smaller,[5] cooler[6] products. AMD Spartan™ UltraScale+ FPGAs offer up to 36% lower total power consumption than comparable Lattice Nexus platform FPGAs[7]—and up to 46% lower total power consumption for high-performance designs.[8]

5 DESIGN WITH THE FUTURE OF CONNECTIVITY IN MIND

Extend the lifespan of your designs with fast, up-to-date, broad connectivity. AMD device options within the Cost-Optimized Portfolio include support for 3.2G MIPI D-PHY and PCIe® Gen4-compliant interfaces, along with hardened LPDDR4x/LPDDR5 memory controllers.



IMPROVE YOUR COST-SENSITIVE DESIGNS, *NOW AND TOMORROW*

Explore the AMD Cost-Optimized Portfolio of FPGAs and adaptive SoCs.

Learn more about how AMD and Lattice devices compare.

1. Based on AMD testing in July 2024, measuring the utilization scores of the LUT6 architecture-based AMD Artix™ 7 A100T (28 nm) and Artix UltraScale+™ AU7P (16 nm) vs. the LUT4 architecture-based Lattice Nexus Mach X05 25 (28 nm) and Lattice Avant E70 (16 nm) devices, measured on AMD Vivado™ 2024.1 and Lattice Radiant 2024.1, respectively, at various speed grades, averaged over 30 open-core designs. Results will vary based on architecture, device, speed grade, package size, design, configuration, and other factors. (COP-001)
2. Based on AMD analysis in July 2024, calculating the F_{MAX} yields for all available speed grades for the (16 nm) AMD Artix™ UltraScale+™ AU7P and the (16 nm) Lattice Avant E70. Actual results will vary based on architecture, device, speed grade, package size, design, configuration, and other factors. (AUS-009)
3. Based on AMD analysis in July 2024, calculating F_{MAX} ratios averaged over 30 open-core designs for (16 nm) AMD Artix™ UltraScale+™ AU7P FPGA, compared to the (16 nm) Lattice Avant E70 FPGA, at the respective highest speed grades. Results will vary based on architecture, device, speed grade, package size, design, configuration, and other factors. (AUS-010)
4. Based on July 2024 AMD analysis of published data sheets using standard JESD51 definition for θJa versus equivalent Lattice packages. Stated results are provisional and will vary based on architecture, package size, speed grade, device, design, configuration, and other factors. (COP-002)
5. See note 1 above.
6. See note 4 above.
7. Based on AMD testing in July 2024, performed in AMD Power Estimation Tools (XPE_2019_1_2 for 28 nm and PDM_2024.1 for 16 nm), and Lattice Radiant Power Estimation Tool 2024.1, measuring the power consumption of the AMD Spartan™ UltraScale+™ 35P, 50P, and 100P FPGAs vs. Lattice Mach X05-NX 25, CertusPro-NX 50, and Mach X05-NX 100T FPGAs at LP speed grade. Total Power results include fabric power and HDIO only. Stated results assume a normalized max ambient temperature of 100°C and a 40% utilization advantage for LUT6 when selecting competitive devices for comparison. Results are subject to change when products are released in market and will vary based on architecture, package size, speed grade, device, design, configuration, and other factors. (SUS-013)
8. Based on AMD testing in July 2024, performed in AMD Power Estimation Tools (XPE_2019_1_2 for 28 nm and PDM_2024.1 for 16 nm), and Lattice Radiant Power Estimation Tool 2024.1, to measure the power consumption of the AMD Spartan™ UltraScale+™ 35P, 50P, and 100P FPGAs vs. Lattice Mach X05-NX 25, CertusPro-NX50, and Mach X05-NX 100T FPGAs at HP speed grade. Total Power results include fabric power and HDIO only. Stated results assume a normalized max ambient temperature of 100°C and a 40% utilization advantage for LUT6, when selecting competitive devices for comparison. Results are subject to change when products are released in market and will vary based on architecture, package size, speed grade, device, design, configuration, and other factors. (SUS-014)

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