

## SOLUTION BRIEF

# HIGH THROUGHPUT WAFER TEST AND PERFORMANCE-OPTIMIZED INSTRUMENTATION SOLUTIONS POWERED BY AMD KINTEX™ ULTRASCALE+™ GEN 2 FPGAs



together we advance\_

## OVERVIEW

AMD Kintex™ UltraScale+™ Gen 2 devices enable Instrumentation solutions and Semiconductor Automated Test Equipment (Semi-ATE) with integrated LPDDR4X/5/5X controller support, PCIe® Gen4 connectivity, and essential flexible I/O. Test requirements continue to quickly evolve driven by increasing device complexity, tighter wafer-level test constraints and rising cost, and pressure to reduce the solutions power envelope. Kintex UltraScale+ Gen 2 devices provide the scalability and flexibility to match the needs of system on chip (SoC) wafer testers, memory testers, and low-cost instrumentation.

## TARGET APPLICATIONS

### SYSTEM ON CHIP WAFER TESTERS

For SoC test applications, the combination of high bandwidth, rich I/O resources, low power consumption, and small footprint provides a strong advantage. More bandwidth enables increased DUT parallelism with faster data offload from the probe head. Hard high-speed transceivers allow probe cards and load boards to aggregate multiple high-speed lanes, enabling parallel DUT testing and higher site counts per insertion. Flexible I/O supports the large signal counts required for SoC validation and characterization. Together, these features reduce test times with increased test throughput and system efficiency.

### LOW-COST INSTRUMENTATION

The low power and small form factor allow equipment manufacturers to shrink system size, with package sizes as small as 25 mm x 25mm, while maintaining high performance. The hard IP for memory controllers and 100G Ethernet MACs (including FEC) reduces power versus soft IP implementation. Up to 1,872 DSP slices and 225K LUTs integrated DSP compute enables real-time data processing and analysis directly at the instrument, improving measurement responsiveness and throughput. MIPI D-PHY support allows the FPGA to drive high-quality, low-cost displays. LPDDR4X/5/5X memory for fast data access, ensures the platform is both performance-scalable and future-ready.

## KEY BENEFITS

### MEMORY SOLUTIONS TO SCALE AND LAST

- On-chip memory enables compact instruments with scalable performance
- Support for LPDDR4X/5/5X extends test solution lifecycles

### SYSTEM-WIDE CONNECTIVITY TO SCALE TEST COVERAGE AND FLEXIBILITY

- Maximize connectivity throughout the test system with up to 396 I/Os supporting 1600 Mb/s LVDS and 120 HDIO up to 3.3V

### REAL-TIME DATA PROCESSING TO ACCELERATE TEST THROUGHPUT AND INSIGHT

- Up to 1,872 DSP48E2 blocks for signal processing and data compute ready for complex signal processing and data analytics

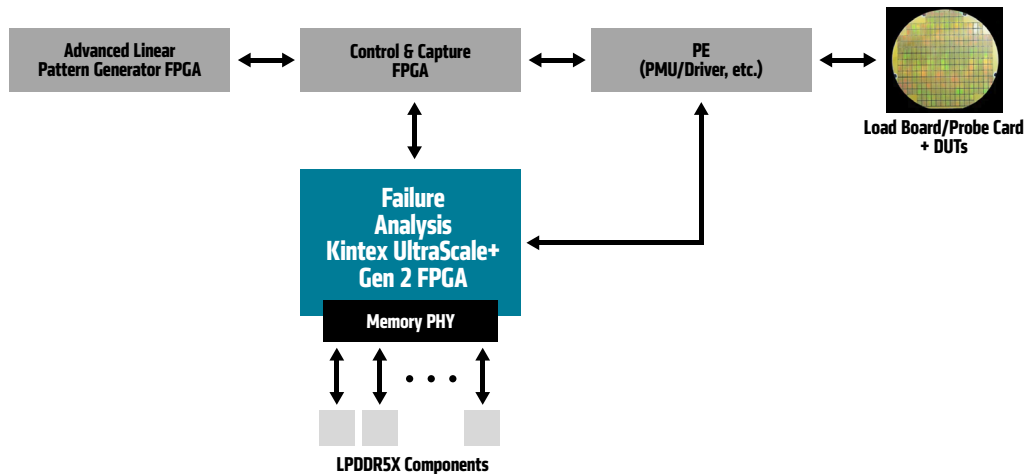


# TARGET APPLICATIONS

## MEMORY TESTERS

In memory test applications, high memory bandwidth and I/O capabilities directly translate to higher DUT counts and support for increasingly complex signaling. Kintex UltraScale+ Gen 2 FPGAs support external LPDDR4X/5/5X, dense on-chip memory, and high I/O density for LVDS and LVCMOS allows the device to meet demanding data-movement requirements while maintaining an efficient power envelope. The compact form factor and dedicated hard IP combined reduce the system thermal and power levels. This reduces thermal load on the DUT head, enabling the FPGA to be placed in typical system configurations directly at the test head or near the DUT. This placement enhances timing accuracy and enables high-performance pattern generation, timing generation, and data aggregation. LPDDR5X support further enables lower-cost system designs and extends solution lifecycles.

## MEMORY TESTER APPLICATION



PLATFORM HIGHLIGHTS	
TEST THROUGHPUT & DUT PARALLELISM	<ul style="list-style-type: none"> <li>Up to 51 Mb on-chip memory enables high-performing local intelligence</li> <li>Up to six 4266 Mb/s controllers with total aggregate bandwidth of 819.2 Gb/s LPDDR4X/5/5X</li> <li>XP5IO enables 4266 Mb/s memory and 3200 Mb/s MIPI D-PHY interfaces</li> </ul>
FLEXIBLE CONNECTIVITY	<ul style="list-style-type: none"> <li>Up to 516 total I/Os with 396 XP5IO operating at 1600 Mb/s LVDS</li> <li>High density I/O (HDIO) provides flexibility with support up to 3.3V</li> </ul>
POWER-OPTIMIZED ARCHITECTURE	<ul style="list-style-type: none"> <li>Dedicated hard IP for memory controllers and 100G Ethernet MACs (including FEC) that may reduce system-level power compared to soft IP approaches</li> <li>Support for LPDDR4X/5/5X versus DDR4 reduces system power</li> </ul>

## NEXT STEPS

- For more information on AMD Kintex UltraScale+ Gen 2 FPGAs, visit [www.amd.com/kintex-ultrascale-plus-gen2](http://www.amd.com/kintex-ultrascale-plus-gen2)
- For more information on AMD Test & Measurement solutions, visit [www.amd.com/en/solutions/test-and-measurement.html](http://www.amd.com/en/solutions/test-and-measurement.html)
- For more information on AMD Semiconductor Automated Test Equipment, visit [www.amd.com/en/solutions/test-and-measurement/semiconductor-automated-test-equipment.html](http://www.amd.com/en/solutions/test-and-measurement/semiconductor-automated-test-equipment.html)
- For more information on AMD Instrumentation solutions, visit [www.amd.com/en/solutions/test-and-measurement/instrumentation.html](http://www.amd.com/en/solutions/test-and-measurement/instrumentation.html)

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