RF Beamforming in XQR Versal™ Adaptive SoCs Using Adaptive Intelligent Engines

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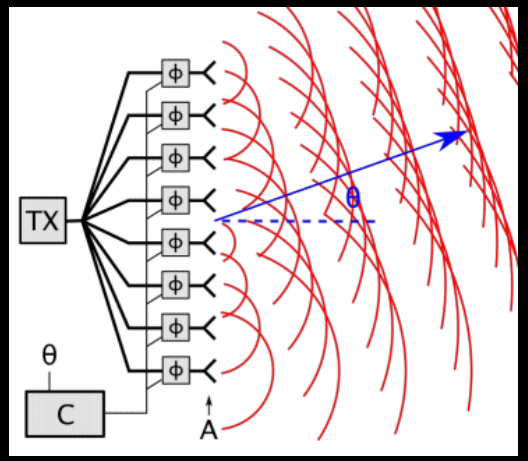
Agenda

- Beamforming
  - Background and introduction
- Example of beamforming in a reconfigurable platform
  - Overview of mathematical implementation of beamforming algorithm
  - Implementation in Adaptive Intelligent Engines
  - Performance and utilization example
- AMD XQR Versal™ Adaptive SoC product information
  - Features and benefits
  - Qualification and availability
  - Radiation effects
- Questions and answers

Beamforming – Background Information

- Basic concepts of beamforming – also called Spatial Filtering
  - RX beamforming uses differences in time-of-arrival (phase difference) of a signal at multiple independent antenna elements to filter out unwanted signals and noise, and allow lower power transmission from the signal of interest
  - TX beamforming uses multiple independent antenna elements to set up interference patterns that are constructive at the intended recipient, improving signal to noise ratio and allowing lower power transmission

- Applicable to many types of systems which operate by propagation of waves –
  RF communications, radar, acoustic, sonar, laser and optical



Phased Array Antenna
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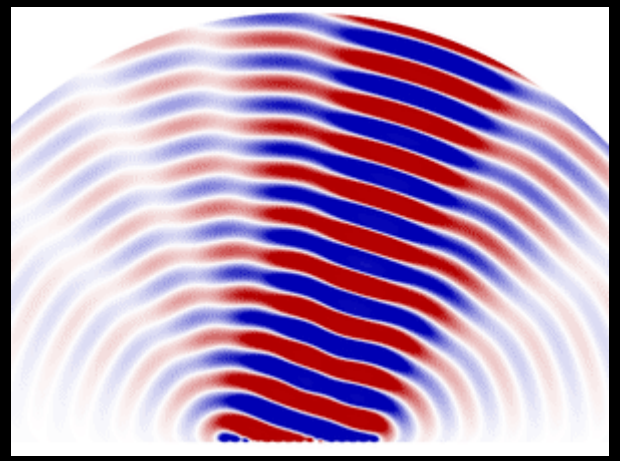
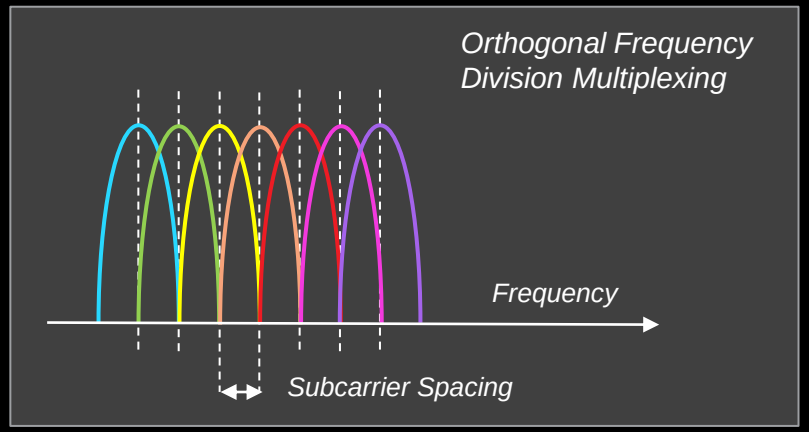
Screenshot from
https://upload.wikimedia.org/wikipedia/commons/4/4a/Phased_array_animation_with_arrow_10frames_371x400px_100ms.gif



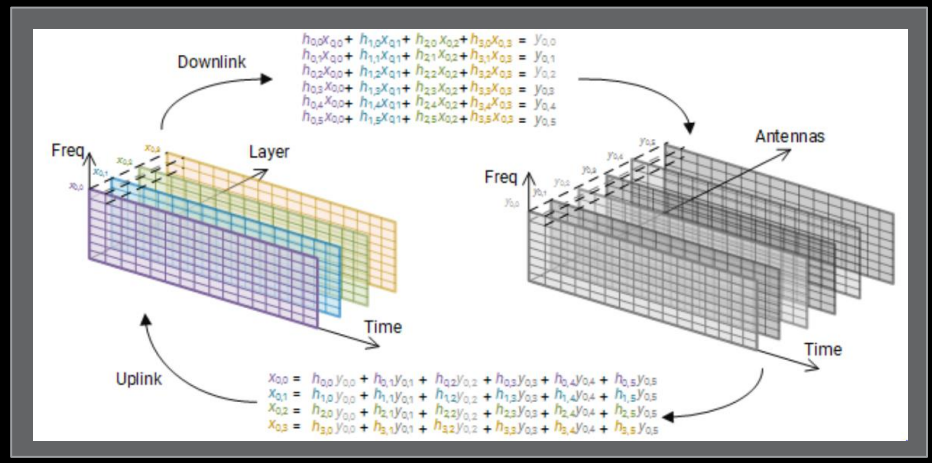
Phased Array with 11 Emitters Spaced 1/4 Wavelength Apart
Credit David Jessop, Licensed under Creative Commons
Screenshot from https://upload.wikimedia.org/wikipedia/commons/1/1e/Phasearray.gif

Example Design

- Our example design is a 5G cellular communications beamformer incorporating OFDMA
  - Orthogonal Frequency Division Multiple Access is a modulation scheme using multiple subcarriers, with frequency separation specifically chosen to minimize interference between subcarriers



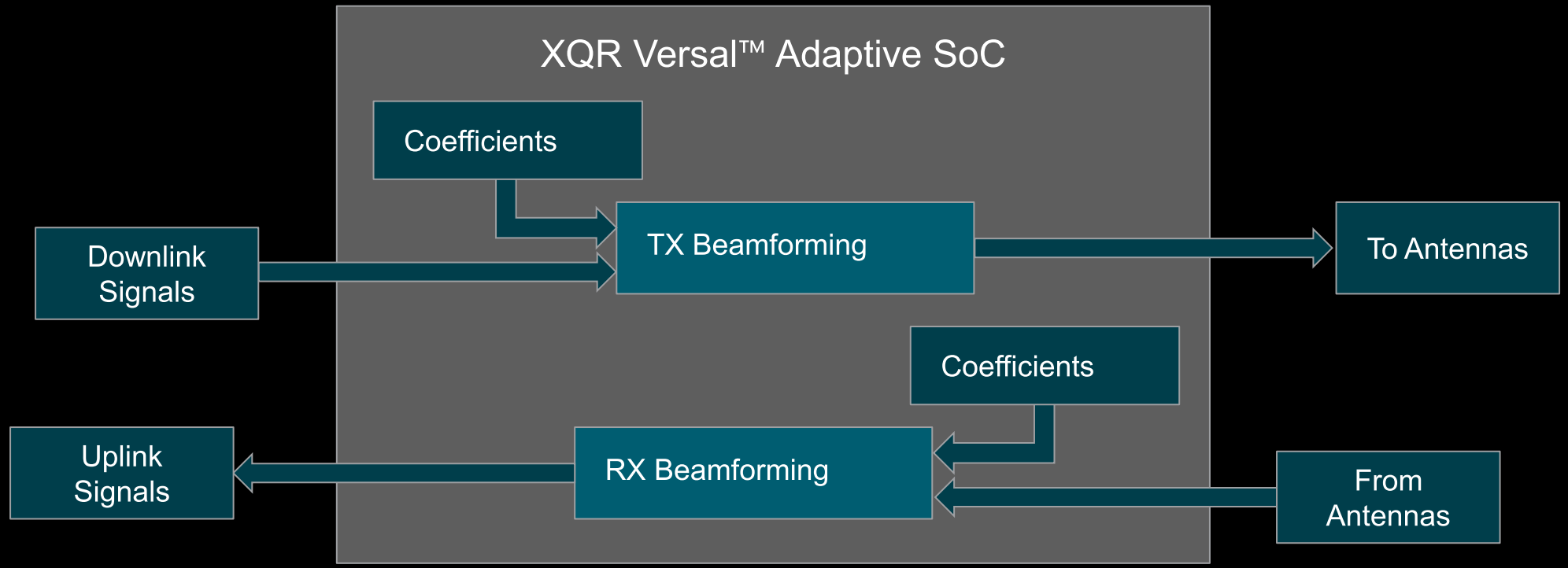
- Our example has MIMO (multiple input, multiple output) in which all 64 antenna elements receive or transmit multiple signals
  - MIMO dramatically expands the number of devices a given antenna array can communicate with
  - At any point in time, the beamforming input comprises a two-dimensional matrix of complex values representing subcarrier and signal layer
  - Complex matrix multiplication applies beamforming weights to determine signal amplitude sent to each antenna



- The principals of beamforming are universal and can be applied to a wide variety of RF space applications

System Block Diagram

- Massive MIMO with 64 antenna elements (8 x 8 array)
- 100MHz subcarrier bandwidth
- 32 downlink / transmit layers and 32 uplink / receive layers



Beamforming Formulation – Transmit / Downlink

- Transmit signal on each antenna is a weighted summation of the layers
  - L = number of subcarriers sharing same coefficient matrix H
  - M = number of layers / streams
  - N = number of antennas
  - B = occupied bandwidth
  - $[\ ]^T$ is vector transpose operation

- Vector of layers on subcarrier k is $X_k = [x_{k,0}, x_{k,1}, x_{k,2} \ldots . , x_{k,M-1}]^T$

- Vector of frequency domain transmit signal on the antennas is $Y_k = [y_{k,0}, y_{k,1}, y_{k,2} \ldots . , y_{k,N-1}]^T$

- Beamforming can be formulated as a matrix multiplication
  $[Y_k, Y_{k+1}, \ldots , Y_{k+L-1}]_{N \times L} = H_{N \times M} \cdot [X_k, X_{k+1}, \ldots , X_{k+L-1}]_{M \times L}$

- Requires N × M × B complex multiplication and accumulation operations (CMACs)

Beamforming Formulation – Receive / Uplink

- Receive signal on each antenna is a weighted summation of the layers
  - L = number of subcarriers sharing same coefficient matrix H
  - M = number of layers / streams
  - N = number of antennas
  - B = occupied bandwidth
  - $[\ ]^T$ is vector transpose operation
- Vector of layers on subcarrier k is $X_k = [x_{k,0}, x_{k,1}, x_{k,2} \ldots, x_{k,M-1}]^T$
- Vector of frequency domain receive signal on the antennas is $Y_k = [y_{k,0}, y_{k,1}, y_{k,2} \ldots, y_{k,N-1}]^T$
- Beamforming can be formulated as a matrix multiplication
  $[X_k, X_{k+1}, \ldots, X_{k+L-1}]_{M\times L} = H_{M\times N} \cdot [Y_k, Y_{k+1}, \ldots, Y_{k+L-1}]_{N\times L}$
- Requires N × M × B complex multiplication and accumulation operations (CMACs)

Computation Requirements

- With 100 MHz bandwidth, 64 antennas, and 32 layers, downlink beamforming requires 100,000,000 × 64 × 32 = 204,800,000,000 CMACs per second, 204.8 GCMAC/s

- Options for implementation

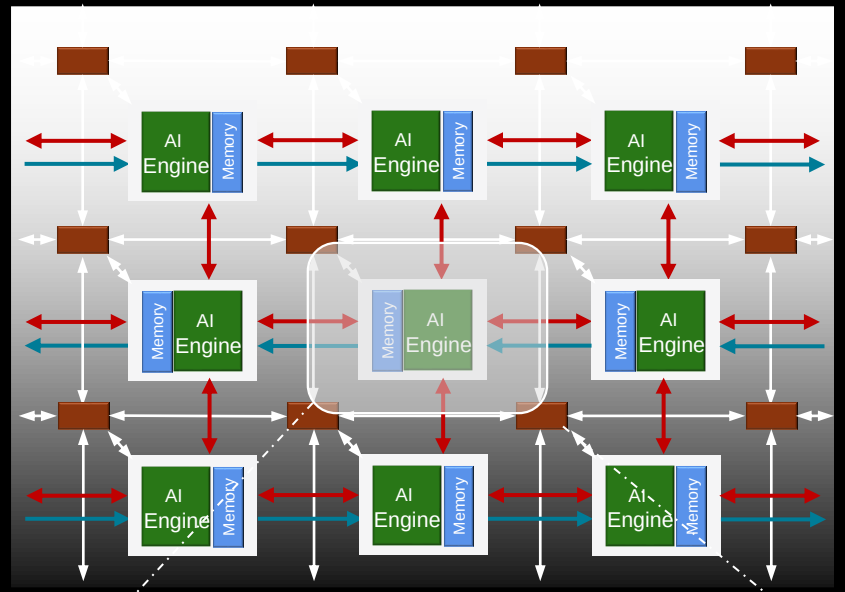
  - DSP blocks (DSP58)
    - With 400 MHz clock, two DSP58 can compute 400,000,000 CMACs per second
    - Requires 1,024 DSP58 blocks to achieve 204.8 GCMAC/s in each direction – 2,048 DSP58 blocks total

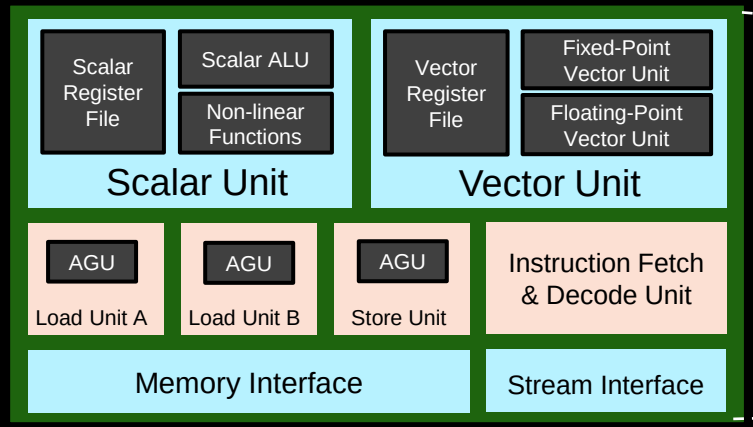
  - AI Engines
    - One AI Engine can compute 6,400,000,000 CMACs per second (at 80% runtime ratio) with 1 GHz clock
    - Requires 32 AI Engines to achieve 204.8 GCMAC/s in each direction – 64 AI Engines total

- Advantage of using AI Engines
  - More efficient use of device resources
  - AI Engines are software programmable
  - Modifications to design can be made in hours, not weeks

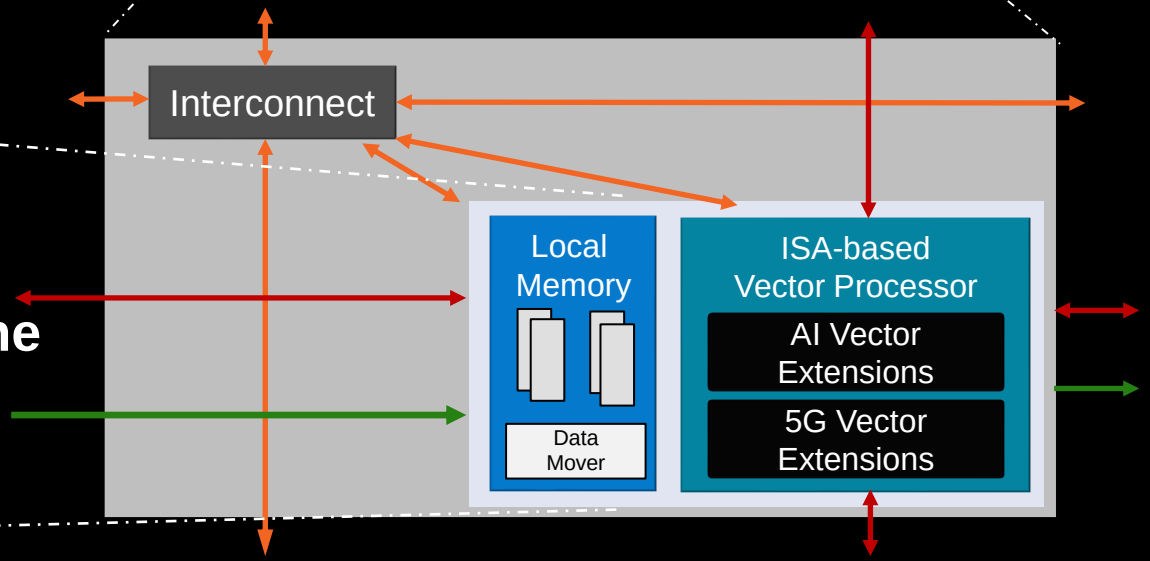
Versal™ Adaptive SoC AI Engine

- Each AI Engine consists of
  - 512-bit SIMD (single instruction, multiple data) vector units, both fixed-point and floating-point
  - 16 KB program memory
  - 32-bit scalar RISC processor
  - 256-bit load (x2) and store units with individual address generation units (AGUs)
- Capable of 32GMACs/second
- Software programmable



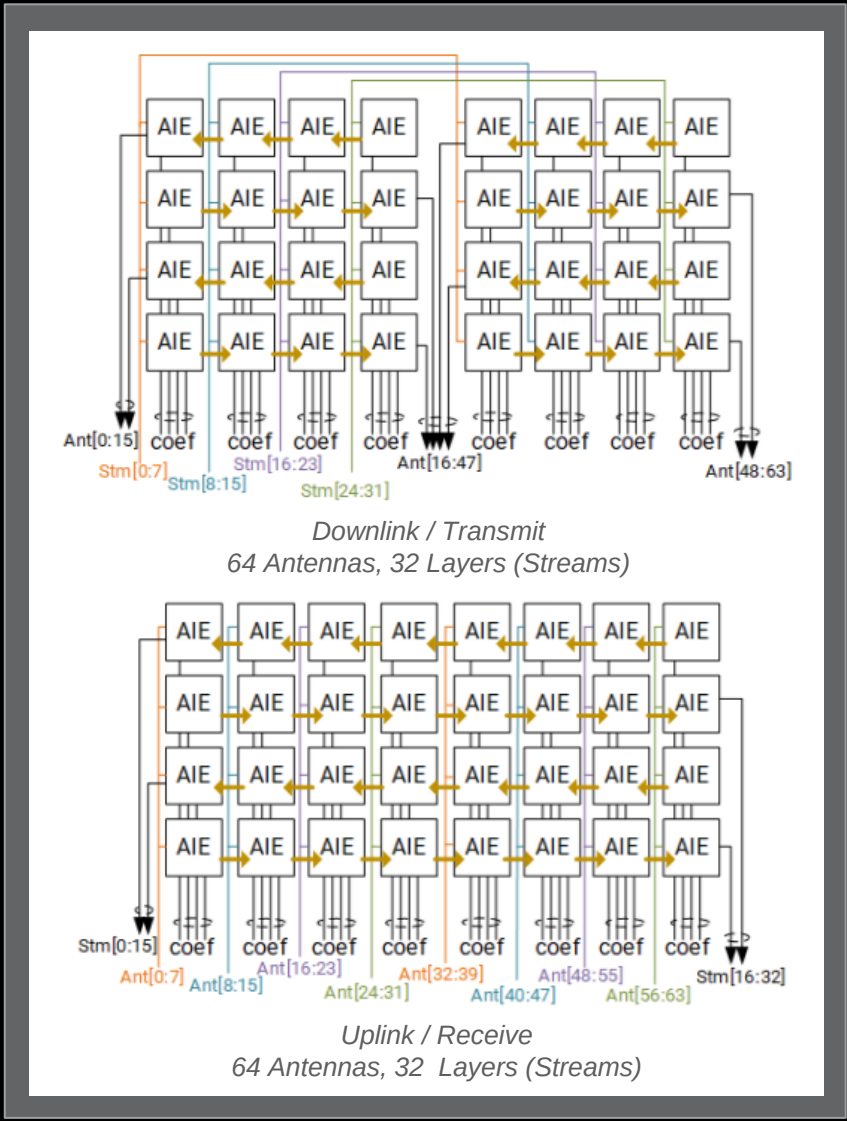


AI Engine



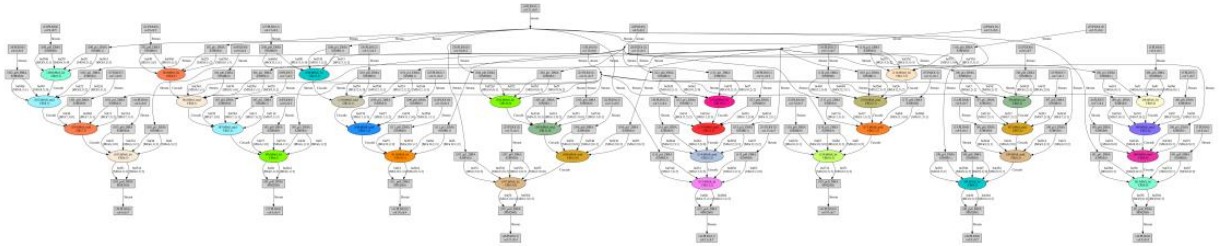
Implementing Beamforming in AI Engines

- The beamforming multiplications must be partitioned to fit into the architecture of the AI Engines
  - Multiple rows of AI Engines are used, with each AI Engine performing one partition of the overall matrix multiplication
  - Within each row, the cascading bus connects the accumulation register of one AI Engine to the next in the row
  - The final AI Engine in each row writes its portion of the output matrix into its local memory
  - Programmable logic fabric provides the input data from local memory and retrieves the results from the AI Engine
- For this design, the optimum decomposition is 8 rows each comprising 4 AI Engine tiles for both downlink and uplink

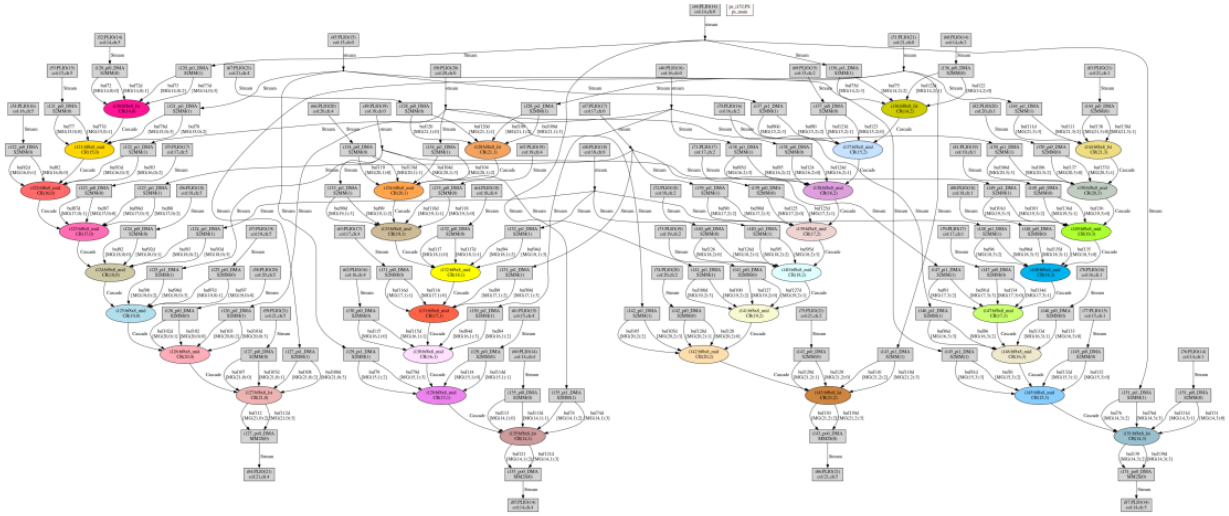


Compilation Results

- AMD Vivado™ tools compile the design and generate block diagram
  - Each colored bubble represents an AI Engine
  - Gray boxes represent DMAs and memories
  - DMA, AXI switches, PL-AIE interfaces are automatically configured



Downlink / Transmit
64 Antennas, 32 Layers (Streams)



Uplink / Receive
64 Antennas, 32 Layers (Streams)

XQR Versal™ Adaptive SoC VC1902 Product Table

		XQRVC1902-1MSBVSRA2197 (AI Core)
Intelligent Engines	AI Engine Tiles	400 (AIE)
	AI Engine Data Memory (Mb)	100
	AI-ML Shared Memory (Mb)	-
	DSP Engines	1,968
Adaptable Engines	System Logic Cells (K)	1,968
	LUTs	899,840
	NoC Master/NoC Slave Ports	28
	Distributed RAM (Mb)	27
Memory	Total Block RAM (Mb)	34
	UltraRAM (Mb)	130
	Accelerator RAM (Mb)	-
	Total PL Memory (Mb)	191
	DDR Memory Controllers	4
	DDR Bus Width	256
Scalar Engines	Application Processing Unit	Dual-core Arm® Cortex®-A72, 48KB/32KB L1 Cache w/ECC 1 MB L2 Cache w/ECC
	Real-time Processing Unit	Dual-core Arm Cortex-R5F, 32KB/32KB L1 Cache, and 256KB TCM w/ECC
	Memory	256KB On-Chip Memory w/ECC
	Connectivity	Ethernet (x2); UART (x2); CAN-FD (x2) USB 2.0 (x1); SPI (x2); I2C (x2)
Serial Transceivers	GTx Transceivers	44 GTY (26.5625 Gb/s)
Integrated Protocol IP	CCIX & PCIe® w/DMA (CPM)	1 x Gen4x8, CCIX
	PCI Express	4 x Gen4x8
	Multirate Ethernet MAC	4
	Platform Management Controller	Boot, Security, Safety, Monitoring, High-Speed Debug, SEU Mitigation (XilSEM)
Package	Ruggedized Organic BGA	VSRA2197, 45mm x 45mm, 0.92mm pitch
I/O		648 XPIO, 44 HDIO, 78 MIO, 44 GTY
Radiation Single Event Effects (SEE)	Proton and Heavy-Ion Testing Ongoing in 2023	NO SEL, 100% Correctable SEUs, Ultra-low SEFI

XQRVC1902 B qual completed 6/2022

Versal™ Adaptive SoC Class B Qualification Summary

- AMD has successfully completed our Class B qualification for the Versal XQRVC1902 device

Stress Test	MIL-STD-883 JEDEC reference	Conditions	Duration / Sample Size	Results
Prod. Burn-in	TM 1015	Dynamic, Tj = 125°C Vccmax	160 hrs.	Passed
Group A	TM 5005	Functional, AC and DC Parameters Test at -55°C, 25°C and 125°C	Test at -55°C, 25°C and 125°C	Passed
Group B	Various JEDEC	Assembly Monitors	✓	Passed
Group C[2]	TM 1005	Tj = 125°C, Vccmax	2 lots, 90 units total - 1000 hours 1 lot, 45 units - 6000 hours	Passed
HTS[1]	TM 1008	Ta = 150°C	1000 hours 3 lots, 75 units total	Passed
THB[1]	JESD22-A101	85°C / 85% RH, Vccmax	1000 hours 3 lots, 75 units total	Passed
Temp Cycle[1]	TM 1010	B: -55°C / 125°C	1000 cycles 3 lots, 75 units total	Passed
Group D[1]	TM 5005	Sub-Groups 1,3,4,5	3 lots, 15 units / subgroup	Passed

(1) Units submitted to MSL-4 preconditioning prior to stressing

Versal™ Adaptive SoC Radiation Effects Summary

	Protons (2 – 105 MeV) Low Earth Orbit, 500 km, 20° inclination			Heavy-ions (1 - 80 MeV·cm²/mg) Geosynchronous Earth Orbit			TID (gamma)
	CRAM SEU (upset/bit/day)	SEL	SEFI (events/device/year)	CRAM SEU (upset/bit/day)	SEL	SEFI (events/device/year)	
Observed Rates	**3.5x10^{-9}**	**ZERO** events observed	PS: **1.3** XilSEM: **ZERO** AIE, GT CY2023-24	**6.5x10^{-12}**	**ZERO** events observed	PS: 0.16 and XilSEM: 4.9x10^{-3} AIE, GT CY2023-24	**PASS 120 KRad(Si)**
Comments	Proton energy: 64-400MeV Environment: 1x10^{12} p/cm^2 at 125°C			Ion Energy: 1-80 MeV·cm^2/mg Environment: 1x10^7 per ion/cm^2 at 125°C			<18 Krad/min

Estimates based on CREME96 AP8-Max; 500km and GEO models

- DUTs: Versal 7nm VC1902, 20 parts from 5 wafer lots to account for lot-to-lot variation
- ZERO SEL events in maximum V_{CC} and junction temperature conditions at LET up to 80 MeV·cm^2/mg
- ZERO uncorrectable Configuration RAM (CRAM) events in LEO and GEO
  - Configuration RAM protected by EDAC and interleaving
- Robust XilSEM internal scrubber SEFI rate may eliminate need for on-board scrubber in space flight
  - Reference AMD / Xilinx user guides UG643 and PG352 for XilSEM scrubbing operation and cycle time
- AMD has published Versal SEE results at SEE/MAPLD 2022, NSREC 2022 and 2023, RADECS 2022 and 2023
  - Check AMD / Xilinx Space Lounge for new reports, links to conference papers and updated content

Conclusion

- Digital beamforming is a critical capability for space-based communications, radar and spectrum analysis
- High-throughput SIMD vector processors provide a software-programmable method of implementing the complex matrix multiplication needed for beamforming and other forms of RF signal processing
- AI Engines in AMD Versal™ Adaptive SoC devices allow major design changes to be implemented with minimal timing closure delays, saving significant design cycle time compared to changes in RTL
- For further information, consult AMD application note and reference design XAPP1352, "Beamforming Implementation on AI Engine"

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Timelines, roadmaps, and/or product release dates shown in these slides are plans only and subject to change.

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