PRODUCT BRIEF

# Versal™ Prime Series

## Optimized for Connectivity, Inline Acceleration, and Diverse Workloads

## OVERVIEW

The Versal Prime series is the foundational Versal adaptive SoC series, offering a diverse selection of devices with broad applicability across multiple markets. The Prime series is a highly integrated, multicore, heterogeneous compute platform that delivers breakthrough performance for a wide range of applications, including data center networking, storage, and wired communications, by enabling low-latency inline acceleration in devices optimized for connectivity.

Versal Prime devices feature an extensive software programmable silicon infrastructure of optimized IP cores, including a programmable network on chip (NoC), memory controllers, PCIe® and CCIX controllers, and 100G multirate Ethernet cores. This integrated infrastructure significantly reduces the need for soft IP implementations in the Adaptable Engines, resulting in smaller designs and faster place-and-route, simplifying development and increasing productivity.

With the Vivado™ Design Suite, the Vitis™ unified software development platform, IP, and libraries, any developer designing systems with the Versal Prime series has a comprehensive set of development tools they can leverage to customize their adaptive computing solutions.

## HIGHLIGHTS

### Hardened Infrastructure for Performance and Increased Design Productivity

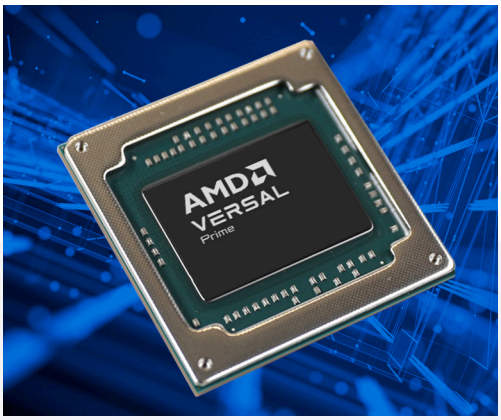
- Multi-terabit programmable NoC connecting the heterogeneous compute engines and the integrated IP cores
- Simplified kernel and IP replacement in Adaptable Engines
- Shell architecture available at boot for dedicated connectivity and increased system-level performance

### Optimized for Inline Acceleration

- Adaptable Engines for custom computational blocks with hardware-level performance
- Enhanced DSP Engines with support for new operations and data types
- Scalar Engines for complex OS-supported applications and real-time, low-latency applications
- Dynamic Function eXchange (DFX) for dynamic workload provisioning

### Next-Generation I/O and Connectivity IP

- 32G NRZ and 58G PAM4 transceivers for high bandwidth network connectivity
- 100G multirate Ethernet cores supporting various Ethernet configurations
- Integrated PCIe Gen4 and Gen5 for maximum CPU-to-accelerator bandwidth
- High-performance GPIO for versatile connectivity




## TARGET APPLICATIONS

### Data Center

- Storage Acceleration
- Network Acceleration

### Wired Communications

- xHaul Gateway
- Passive Optical Networks
- Optical Transport Networks

### Aerospace

- Avionics Control

### Test and Measurement

- Communication Tester

### Broadcast and Pro A/V

- Broadcast Switches

### Healthcare and Medical

- Medical Imaging

## FEATURES

| FEATURES OVERVIEW | |
|---|---|
| Scalar Engines | > Complex algorithm processing and decision-making tasks<br>> Dual-core Arm® Cortex®-A72 application processing unit<br>> Dual-core Arm Cortex-R5F real-time processing unit |
| Platform Management Controller | > Boot & configuration and advanced power & thermal management<br>> Security, safety, and reliability enclave<br>> Integrated platform interfaces & high-speed debug |
| Adaptable Engines | > Re-architected for higher compute capacity and less global routing<br>> High bandwidth, low latency data movement between engines and I/O<br>> Dynamic Function eXchange (DFX) for dynamic workload provisioning |
| Intelligent Engines | > Enhanced DSP Engines (DSP58) with support for new operations and data types including single and half-precision floating point<br>> Backwards compatibility to UltraScale+™ DSP48s |
| Programmable Network on Chip | > High bandwidth programmable multi-terabit NoC<br>> Streamlined programming experience with tools to manage quality of service<br>> Simplifies kernel and IP placement in Adaptable Engines and reduces soft logic needed for connectivity |
| Shell Architecture | > Prebuilt software programmable silicon infrastructure and system connectivity<br>> Turn-key, pre-engineered performance while simplifying timing closure and reducing device congestion |
| 32G NRZ & 58G PAM4 Transceivers | > Rearchitected low latency 32G NRZ GTY and GTYP transceivers<br>> 58G PAM4 GTM transceivers for maximum network connectivity |
| Integrated blocks for PCIe Gen4 and Gen5 with DMA and CCIX | > High bandwidth CPU-to-accelerator connectivity for next-generation systems<br>> Hardened, queue-based DMA engines for data center applications<br>> Symmetric/asymmetric access to memory with cache coherent interconnect for accelerators |
| Integrated 100G Multirate Ethernet Cores | > Scalable Ethernet IP to maximize throughput while maintaining flexibility<br>> Multirate: 1x100GE, 2x50GE, 1x40GE, 4x25GE, and 4x10GE<br>> Optional built-in RS-FEC / Firecode FEC and IEEE 1588 hardware timestamping |
| Integrated DDR Memory Controller | > High bandwidth DDR4 and LPDDR4 support<br>> Optimized for both linear and random traffic |

## TAKE THE NEXT STEP

For more information about the AMD Versal Prime series, visit https://www.xilinx.com/versal-prime.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