

AMD VERSAL™ PREMIUM SERIES GEN 2 CXL® UNLOCKS MORE MEMORY

SOLUTION BRIEF



OVERVIEW

AMD Versal™ Premium Series Gen 2 adaptive SoCs are a versatile and configurable platform, offering a comprehensive CXL® 3.1 subsystem. These adaptive SoCs are designed to cater to a wide spectrum of CXL applications, varying from simple to complex use cases. Whether you are an advanced adaptive SoC developer or a beginner getting started with CXL, Versal Premium Series Gen 2 provides a flexible CXL 3.1 subsystem that is ideal for memory expansion, memory pooling, and memory acceleration applications.

INTRODUCTION TO CXL

Compute Express Link® (CXL) is a new high-speed interconnect technology developed by a consortium of industry leaders. It aims to bridge the gap between CPUs, GPUs, and other high-performance accelerators, enabling them to work together more efficiently in a unified memory space. CXL achieves this by providing a high-bandwidth, low-latency, memory-centric, and cache-coherent interface that allows devices to share data and memory across the interconnect.

CXL MEMORY EXPANSION

Data generation and processing continue to surge globally along with the proliferation of advanced technologies such as artificial intelligence and machine learning. As a result, the demand for increased memory capacity during computation has become an even more pressing need. FPGA system designers face memory challenges similar to those in typical processor-based designs. As such, customers can add more memory to their FPGA through the CXL 3.1 subsystem with the Versal Premium Series Gen 2 – the first in the Versal portfolio to offer this CXL memory expansion capability.

CXL NEAR MEMORY COMPUTATION

The current landscape of computation has ushered in a new era that requires a substantial amount of memory-intensive operations. As the need for such computational tasks continues to rise, there is increasing interest and drive from industry professionals to move certain memory-intensive operations closer to the memory, in an effort to improve system performance while reducing power consumption. The Versal Premium Series Gen 2 adaptive SoC has emerged as an ideal platform for near-memory processing applications, where designers can make use of the CXL interface to move preprocessed and postprocessed data more efficiently across memory space.



MORE CAPACITY, MORE BANDWIDTH¹

KEY BENEFITS

- Designed for CXL Compliance
- Improves System Performance
- Flexible & Configurable

KEY CAPABILITY

- CXL 3.1 Hardware-Based Subsystem
- CXL Memory Expansion
- CXL Near Memory Computation

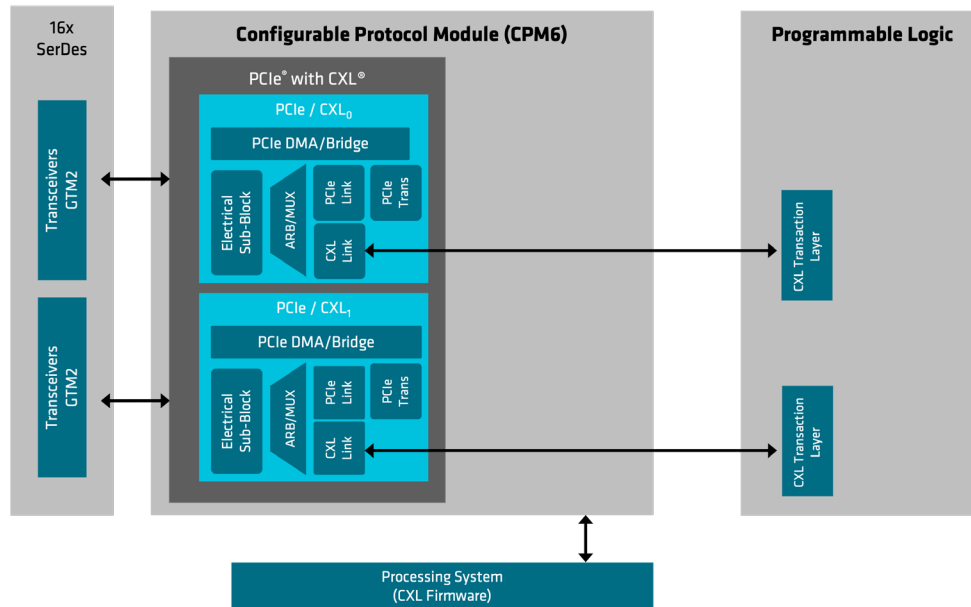
KEY FEATURES

- CXL 1.1, 2.0, and 3.1
- Max Link Rate: 64 GT/s (PAM4)
- 2 x CXL Controllers
- 16 PCIe/CXL Lanes (2 x 8)
- CXL.io Support
- CXL.mem Support
- CXL.cache Support
- End Point Mode: Type-3/2/1
- Host Mode: Type-3
- Customer Example Designs (CED)

CXL 3.1 SUBSYSTEM FEATURE OVERVIEW

The Versal Premium Series Gen 2 CXL subsystem comprises of four major components: GTM2 transceiver, configurable protocol module 6 (CPM6) controller, CXL transaction layer IP, and CXL firmware. System architects can choose to use the entire CXL subsystem or part of the subsystem with their own configuration and customization. The CXL subsystem supports both CXL end point mode and CXL host mode.

VERSAL PREMIUM SERIES GEN 2 CXL SUBSYSTEM



GT M2 TRANSCEIVER

- PCIe® Physical Layer
- Gen1 to Gen6 Support (NRZ and PAM4)

CXL TRANSACTION LAYER IP

- Available through Vivado™ LogiCORE™ IP catalog
- Configurable for Type-3, Type-2, and Type-1

CPM6 CONTROLLER

- CXL 1.1/2.0/3.1 Alternate Protocol Negotiation
- 68B and 256B FLIT
- CPM6 CXL Arbiter & Multiplexer (ArbMux)
- CPM6 Data Link Layer (DLL)

CXL FIRMWARE

- C-source Code Available
- Initialization & Configure. Runtime Management

NEXT STEPS

For more information on Versal Premium Series Gen 2 devices, visit www.amd.com/versal-premium-gen2

ENDNOTES

1. Based on AMD internal analysis of the total memory bandwidth (CXL 3.1 and LPDDR5X memory components) available with AMD Versal Premium Series Gen 2 devices vs. the same devices with LPDDR5X memory alone. Memory bandwidth will vary based on system configuration and other factors. (VER-059)

DISCLAIMERS

The information contained herein is for informational purposes only and is subject to change without notice. While every precaution has been taken in the preparation of this document, it may contain technical inaccuracies, omissions and typographical errors, and AMD is under no obligation to update or otherwise correct this information. Advanced Micro Devices, Inc. makes no representations or warranties with respect to the accuracy or completeness of the contents of this document, and assumes no liability of any kind, including the implied warranties of noninfringement, merchantability or fitness for particular purposes, with respect to the operation or use of AMD hardware, software or other products described herein. No license, including implied or arising by estoppel, to any intellectual property rights is granted by this document. Terms and limitations applicable to the purchase or use of AMD's products are as set forth in a signed agreement between the parties or in AMD's Standard Terms and Conditions of Sale. GD-18u

COPYRIGHT NOTICE

© 2024 Advanced Micro Devices, Inc. All rights reserved. AMD, the AMD Arrow logo, LogiCORE, Versal, Vivado, and other designated brands included herein are trademarks of Advanced Micro Devices, Inc. CXL is a trademark of Compute Express Link Consortium, Inc. PCIe and PCI Express are trademarks of PCI-SIG and used under license. Other product names used in this publication are for identification purposes only and may be trademarks of their respective owners. PID3004992