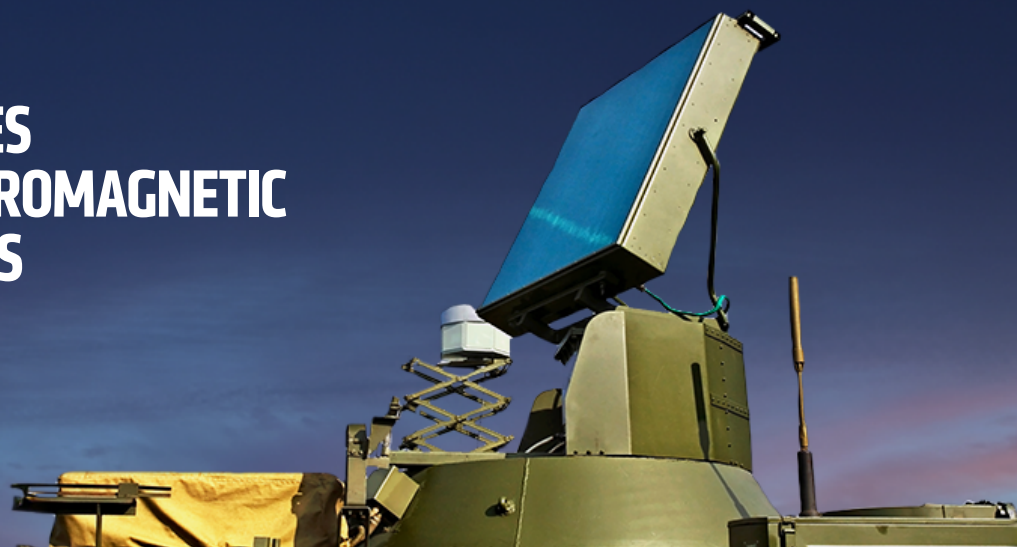
AMD VERSAL™ RF SERIES FOR ADVANCING ELECTROMAGNETIC SPECTRUM OPERATIONS

SOLUTION BRIEF

AMD
together we advance_



OVERVIEW

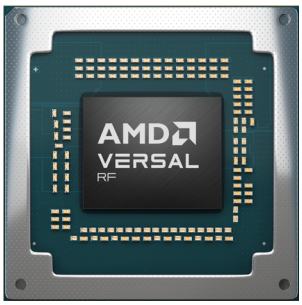
Electromagnetic Spectrum Operations (EMSO) are becoming increasingly more challenging as the spectrum becomes more congested and contested. To operate successfully in this environment, systems must be enabled with the signal processing power to analyze a broad RF spectrum, applying state-of-the-art techniques, and with the flexibility to adapt to evolving requirements.

The AMD Versal™ RF Series offers a solution to this challenge with enhanced signal processing performance per watt, as well as wideband data converters for improved frequency agility.

Building on the legacy of the AMD Zynq™ UltraScale+™ RFSoC, as well as the innovative Versal architecture, the Versal RF Series integrates wideband RF data converters, dedicated signal processing functions (for FFTs, polyphase channelizers, and LDPC decoders), real-time and application Arm® processor cores, vector processing engines, hard memory controllers, and programmable logic integrated within a single silicon die. This integration provides a single-chip, low-latency solution for a wide range of EMSO applications in a smaller size and low-power envelope suitable for 3U or even smaller form factors.

3X RF Input/Output Frequency

compared to previous generation[2] with 18 GHz of BW



HIGHLIGHTS

REDUCED SWAP THROUGH HARD DSP IP FUNCTIONS

- Up to 80% reduction in dynamic power with hard logic[1] for FFT/iFFT, channelizer, digital filter, and LDPC decoder IP
- 4 GSPS throughput FFT/iFFT sub-block, 8-pt to 4k-pt hard IP instance for a total of 240 GOPs/FFT IP instance
- LDPC decoder supporting LDPC decoding for DVB-S2/X, 5G, WiFi, and DOCSIS

EXTENDED RF BANDWIDTH AND SAMPLING RATES COMPARED TO PRIOR AMD GENERATION

- 18 GHz of input bandwidth offers 3X input frequency improvement[2]
- 32 GSPS RF-ADC sample rate offers 6.4X increase in the maximum RF-ADC sample rate[2]
- 16 GSPS RF-DAC sample rate offers 1.6X increase in the maximum RF-DAC sample rate[2]

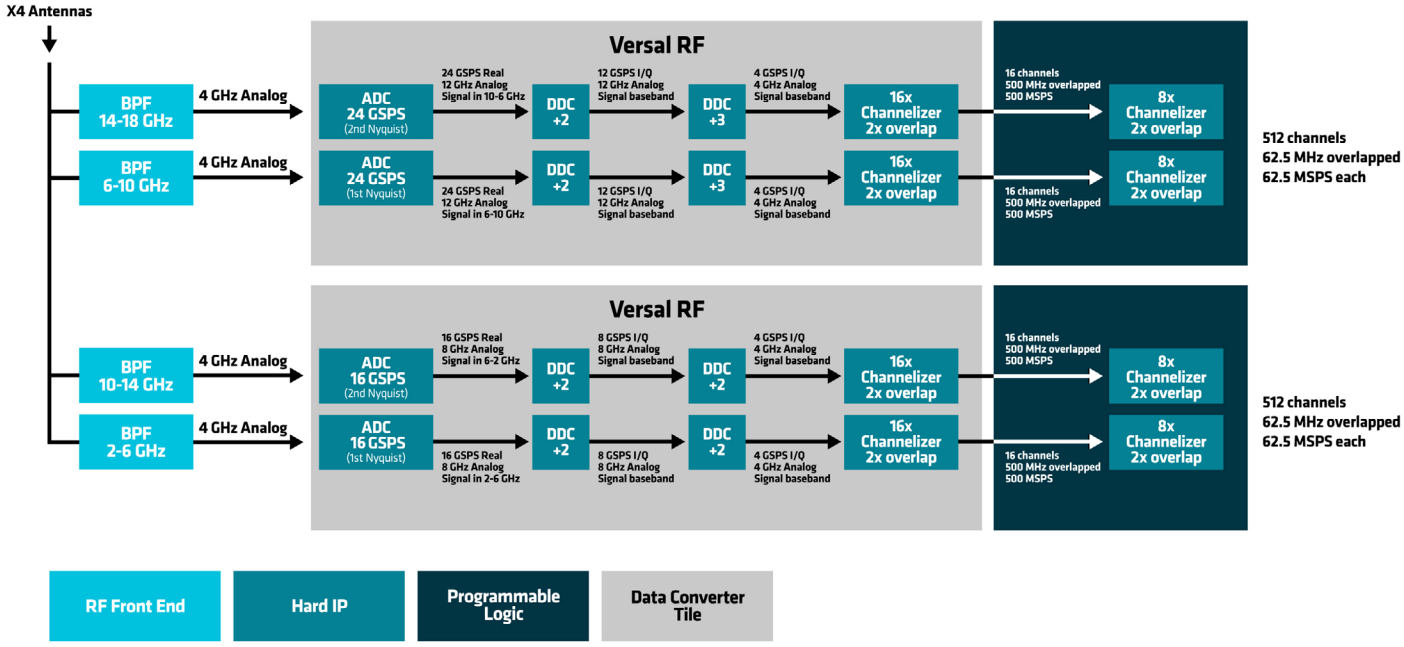
INCREASED COMPUTE DENSITY FOR RF SIGNAL PROCESSING

- Up to 19X the DSP compute compared to the previous generation[3]
- Up to 11X more DSP compute per GHz of Nyquist observable bandwidth compared to previous generation[4]
- Up to 3X more compute vs. the largest Intel® Agilex 9 Series Direct RF-Series device in a comparable package size[5]

TARGET APPLICATIONS

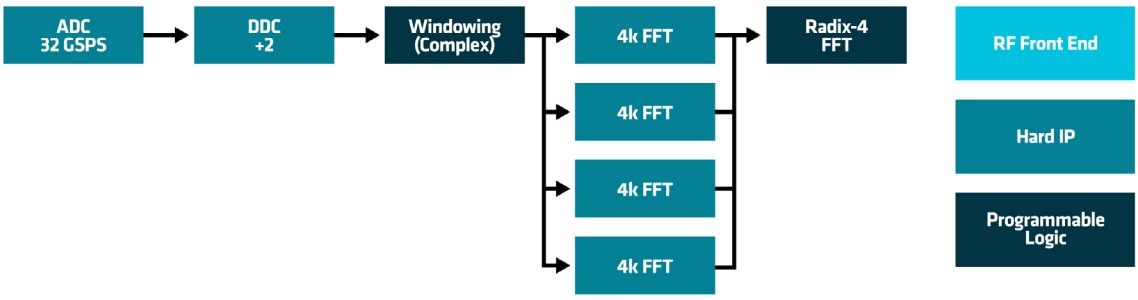
WIDEBAND-SPECTRUM VISIBILITY

- 18 GHz of analog bandwidth provides direct sampling of X and Ku bands
- 32 GSPS data converters capture large swaths of bandwidth
- Monolithic integration means the full sample rate can be directly connected to the signal processing IP
- Hard channelizers can separate wideband channels into narrowband processing channels



HARD IP FOR SPECTRUM ANALYSIS

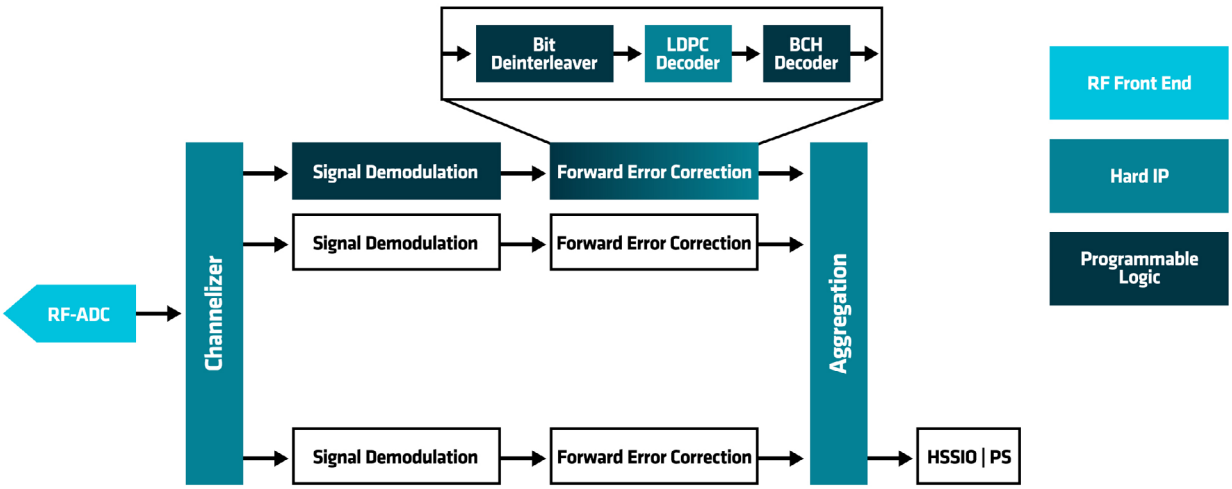
- FFT blocks support 8 to 4k-point FFT at 4 GSPS
- First- and second-stage polyphase channelizer IP cores can separate an 8 GSPS channel into sixty-four 62.5 MSPS channels
- Channelizers and FFTs can be cascaded for larger sizes
- Two digital down converters per RF-ADC
- Two digital up converters per RF-DAC



CONFIGURABLE LDPC DECODER

- Multiple gigabit soft-decision LDPC decoding with either offset or scaled min-sum node updates
- Layered decoding architecture supports range of QC codes with submatrix size <= 384 and weight <= 2
- 6-bit LLR input with 2 fractional bits and 4-bit configurable offset or scaling parameter per layer
- Preset configurations for 5G New Radio (NR), DVB-S2/X (SATCOM), DOCSIS 4.0, and WiFi (802.11) codes
- Supports on-the-fly code changes on a frame-by-frame basis for VCM/ACM applications
- Multiple channels can share a single hard block instance
- **Throughput:**
  - 5GNR = 7.7 Gb/s @ 8 iterations
  - DVB-S2 = 4 Gb/s @ 8 iterations
  - DVB-S2X = 3.7 Gb/s @ 8 iterations

SATACOM DVB-S2/X Receiver Processing Chain



NEXT STEPS

For more information on Versal RF Series, visit: **www.amd.com/versal-rf**
Visit the AMD Aerospace and Defense page at: **https://www.amd.com/en/solutions/aerospace-and-defense.html**

ENDNOTES

1. Based on an AMD engineering projection of hard IP power values, November 2024. AMD Power Design Manager (2023.2.2) used to determine total power of soft logic, based on Vivado 2023.2.2 IP catalog. (VER-074)
2. Based on AMD internal analysis in October 2024, of data sheet specifications for input frequency, max bandwidth, RF-ADC and RF-DAC electrical characteristics, and the maximum RF-ADC and RF-DAC sample rates of the AMD Versal RF devices, compared to the data sheet specifications of the AMD Zynq UltraScale+ RFSoC Gen 3 (prior generation) devices. Actual results may vary based on configuration, device, design, and other factors. (VER-067)
3. Based on AMD internal analysis to calculate the theoretical DSP compute (including hard IP, AI Engines, and DSP) in channelizer mode offered by the Versal RF Series devices versus the published DSP compute of the previous-generation Zynq UltraScale+ RFSoC Gen 3, as of September 2024. Actual results will vary based on configuration, device, design, and other factors. (RF-ADCs and RF-DACs combined) (VER-068)
4. Based on AMD internal analysis to calculate the theoretical DSP compute per GHz of Nyquist observable bandwidth (RF-ADCs and RF-DACs combined) in channelizer mode, of the Versal RF Series devices and of the previous-generation Zynq UltraScale+ RFSoC Gen 3, as of September 2024. Actual results will vary based on configuration, device, design, and other factors. (VER-081)
5. Based on an AMD internal analysis comparing the theoretical processing capability (including hard IP, AI Engines, and DSP) of the Versal RF VR19xx devices versus the largest Intel Agilex 9 Direct RF-Series ARGW027 device. Results may vary based on device, configuration, design, and other factors. (VER-071)

DISCLAIMERS

COPYRIGHT NOTICE