AMD
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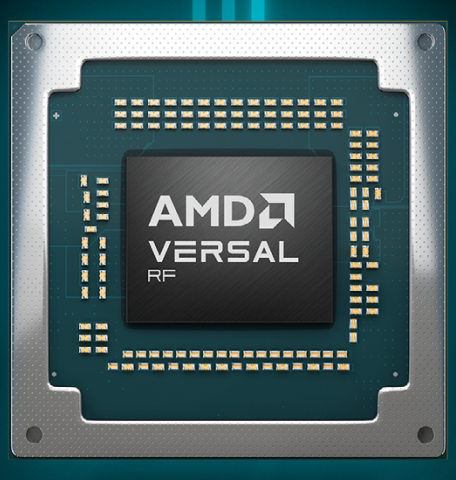
LEAP AHEAD
WITH HIGH-PERFORMANCE RF CONVERTERS AND MORE DSP COMPUTE

Next-generation RF systems for aerospace and defense, SATCOM, and test and measurement just got easier. Introducing the **AMD Versal™ RF Series adaptive SoC**, with the highest-resolution RF-sampling ADCs, programmable logic, and hard DSP compute IP on a single chip.[1]



MASSIVE DSP COMPUTE

SWaP OPTIMIZATION

WIDEBAND SPECTRUM OBSERVABILITY

Up to **19X** more DSP compute compared to previous-generation devices[2]

Up to **7.5X** increase in operations per watt with hard FFT/iFFT IP blocks[3]

Up to **80** tera operations per second (TOPS) of digital signal processing (DSP) compute[5]

Performance and efficiency—all in one chip

Up to **80%** lower dynamic power consumption in dedicated DSP IP cores[4]

14-bit signal resolution RF-ADC and RF-DAC converters with calibration

Up to eight **32 GSPS** sample rate RF-ADCs in a single package

Built for advanced RF systems

ANALYZE WIDER OBSERVABLE BANDWIDTH

Enable precise, flexible, and fast signal analysis with a high sample rate and resolution.

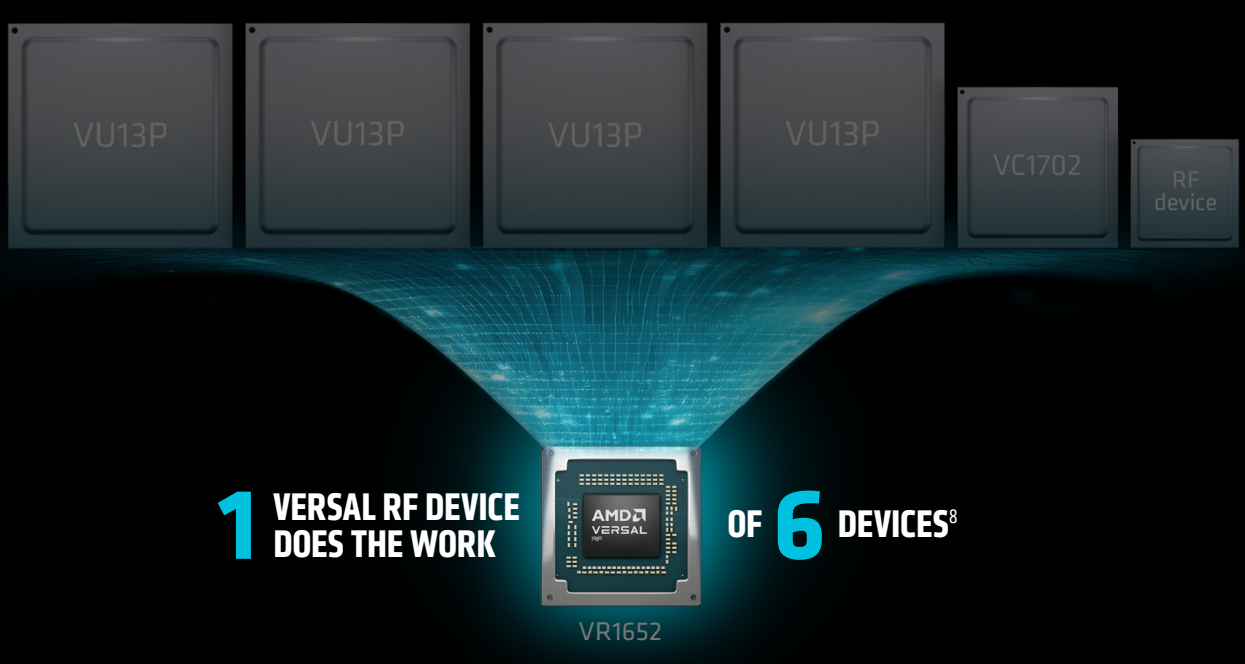
MEET DEMANDING COMPUTE NEEDS EFFICIENTLY

Hard DSP IP blocks reduce the need for soft logic.

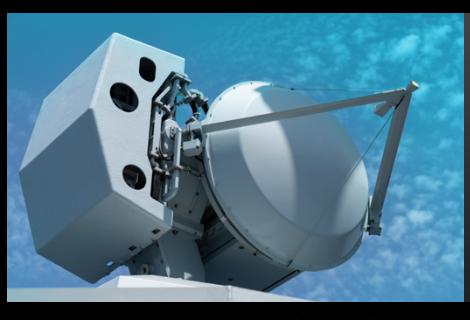
REDUCE POWER CONSUMPTION AND OVERALL FOOTPRINT

Count on one highly integrated solution optimized for size, weight, and power (SWaP).

Get more compute at lower power[6,7]



1 VERSAL RF DEVICE DOES THE WORK OF 6 DEVICES[8]



Develop accurate and fast RF applications

Signals intelligence (SIGINT), electromagnetic spectrum operations (EMSO), and phased-array radar

High-speed RF testers and oscilloscopes, and spectrum analyzers

AMD VERSAL™ RF ADAPTIVE SoCs

Gain flexibility and performance for RF signal processing workloads today and in the future.

Learn More

1. Based on an AMD internal analysis, comparing the RF-ADC sample rate (GSPS) specification of the Versal RF VR1652 and VR1952 devices versus the published specifications of the Intel Agilex 9 Direct RF-Series AGRW014 and AGRW027 FPGAs and the pre-release design specifications of the ADI Apollo AD9084 and AD9088 devices. (VER-075)
2. Based on an AMD internal analysis to calculate the theoretical DSP compute (including hard IP, AI Engines, and DSP) in channelizer mode offered by the Versal RF Series devices versus the published DSP compute of the previous-generation AMD Zynq™ UltraScale+™ RFSoC Gen 3, as of September 2024. Actual results will vary based on configuration, device, design, and other factors. (VER-068)
3. Based on an AMD internal analysis to calculate the theoretical DSP compute (including hard IP, AIEs, and DSPs) offered by the Versal RF VR16xx devices, and on AMD engineering projections in November 2024 using the hard IP functions in Versal RF Series devices to measure dynamic power versus the total power calculation of an AMD soft logic implementation, as measured with AMD Power Design Manager (2023.2.2), based on the AMD Vivado™ 2023.2.2 IP catalog. (VER-083)
4. Based on an AMD engineering projection of hard IP power values, November 2024. AMD Power Design Manager (2023.2.2) used to determine total power of soft logic, based on the Vivado 2023.2.2 IP catalog. (VER-074)
5. Tera Operations per Second (TOPS) for a Versal RF Series device is the maximum number of operations per second that can be executed in an optimal scenario and may not be typical. TOPS will vary based on device, design, configuration, and other factors. (VER-084)
6. See note 2 above.
7. See note 4 above.
8. Based on an AMD internal analysis in November 2024 comparing the amount of DSP processing, AI Engine compute, and RF sampling converter capabilities offered by one (1) Versal RF Series VR1652 device (single chip) versus that of four (4) AMD Virtex™ UltraScale+ VU13P devices + one (1) Versal AI Core VC1702 device + one (1) ADI discrete AD9084 RF converter. Results will vary based on device, design, configuration, and other factors. (VER-077)

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