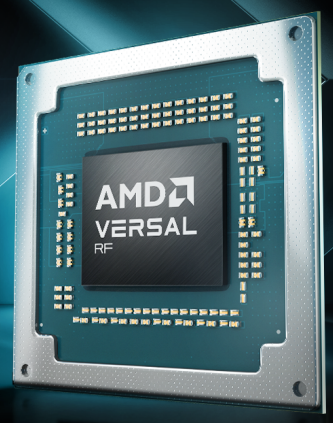
AMD VERSAL™ RF SERIES

Wideband Spectrum. Massive DSP Compute. Single Chip.

PRODUCT BRIEF

AMD
together we advance_



OVERVIEW

AMD Versal™ RF Series adaptive SoCs provide direct wideband digital sampling into the Ku band in a size, weight, and power (SWaP) optimized single-chip solution with massive digital signal processing (DSP) capability for low-latency signal characterization at the edge.

The wide bandwidth, high sample rate, and high-resolution needs of modern applications require more DSP resources than traditional FPGA architectures. Versal RF Series devices provide these resources in a heterogeneous compute solution consisting of hard IP blocks, AI Engines (AIE), and traditional DSP and programmable logic with up to 80 TOPS of compute in a single chip.[1] By distributing the processing across DSPs, AIEs, and hard IP blocks, the Versal RF Series allows the customer to trade flexibility for performance to meet their needs.

The Versal RF Series' 14-bit (with calibration), 32 GSPS RF-ADC is the highest resolution RF-ADC monolithically integrated with adaptable logic.[2] To rival the compute of the Versal RF Series, a comparable competitor's solution would require additional FPGA resources, tripling the package area.[3] By taking advantage of hard IP blocks for signal processing, customers can realize up to 80% dynamic power savings over a soft implementation.[4] For customers with restrictive SWaP considerations who cannot sacrifice performance, the Versal RF Series offers an ideal solution.

KEY APPLICATIONS

AEROSPACE AND DEFENSE

- Electromagnetic Spectrum Operations (EMSO)
- Radar Systems
- MilCom

TEST AND MEASUREMENT

- High-Speed, Multi-Channel Testers
- Wideband Spectrum Analysis
- Oscilloscopes
- Wireless 6G Testers

WIRELESS

- Pre-6G Systems

HIGHLIGHTS

PRECISE, WIDEBAND SIGNAL CHARACTERIZATION

- Up to eight 14-bit (with calibration), 32 GSPS RF-ADCs with hard DUC and DDC IP enable fast, high resolution, flexible, wide-spectrum characterization
- 18 GHz I/O instantaneous bandwidth enables a wider input frequency pipe
- Up to sixteen 14-bit (with calibration), 16 GSPS RF-DACs provide RF transmit functions

MASSIVE DSP COMPUTE

- Signal processing functions are implemented in hard IP cores
  - FFT/iFFT, channelizer, polyphase arbitrary resampler, LDPC decoder: including DVB-S2/S2X
- AIE tiles and DSP58 Engines combine with hard IP blocks, providing up to 80 TOPS of compute[1]
- Massive DSP compute from hard IP blocks enables a single-device solution

SIZE, WEIGHT, AND POWER (SWAP) OPTIMIZED

- Hard IP blocks reduce dynamic power consumption by up to 80% over soft IP implementation[4]
- Monolithic implementation reduces area and power of analog – digital interface
- Smaller thermal load reduces system-level size and weight

FEATURES	HIGHLIGHTS
DIRECT RF-ADCS	• RF input frequency up to 18 GHz • 14-bit resolution with calibration • 8 GSPS and 32 GSPS RF-ADC tiles • Fast frequency hopping in mixers • Low-latency mode • Up to 80X decimation • Optional 8 GSPS hard IP channelizer block • RF-ADC samples can be directly connected to PL at full throughput and lowest latency
DIRECT RF-DACS	• RF output frequency up to 18 GHz • 14-bit resolution with calibration • 16 GSPS sample rate • Fast frequency hopping in mixers • Low-latency mode • Up to 160X interpolation • Optional 8/16 GSPS hard IP inverse channelizer block • RF-DAC samples can be directly connected to PL at full throughput and lowest latency
HARD FFT/IFFT IP	• Maximum throughput per unit 8 samples/cycle (4 GSPS) • VR16xx combined FFT throughput 112 GSPS • VR19xx combined FFT throughput up to 160 GSPS • Point size & FFT/iFFT change on-the-fly on a block basis
HARD CHANNELIZER (ANALYZER) / INVERSE CHANNELIZER (SYNTHESIZER) IP	• 1 GSPS native rate • Full-rate programmable 64-tap prototype filter • Can be configured as 8 channel polyphase; 8 complex or 16 real taps per channel • Ability to use as reverse channelizer (synthesizer)
LDPC DECODER	• LDPC decode only (no LDPC encode or turbo decode) • Support added for DVB-S2/X LDPC codes • Integrated support for 5GNR (no PL resources required) • Available on the VR16xx devices only, not available on the VR19xx devices
AI ENGINES AND DSP ENGINES	• 32 16-bit GMACs per AIE @ 1.3 GHz • DSP Engines for diverse workloads
PROCESSING SYSTEM (PS) OF INTEGRATED CPUS	• Dual-core Arm® Cortex®-A72 application processing unit for Linux®-class operating systems • Dual-core Arm Cortex-R5F real-time processing unit for low latency and determinism • Platform management for quick boot, power & thermal management, and safety & security enclave
DDR5/LPDDR5X MEMORY CONTROLLERS	• Support for DDR5 @ 6400 Mb/s and LPDDR5X @ 8533 Mb/s • Up to 136.5 GB/s memory bandwidth in the largest devices • Flexible pin planning – swap hard controller pins to support other interfaces
PROGRAMMABLE LOGIC (PL)	• Low-latency, deterministic, parallel processing • Fully customizable to enable differentiated, proprietary algorithms • Field-upgradeable: Adaptable to changing conditions and evolving workloads
PROGRAMMABLE I/O	• New high-performance X5IO support DDR5/LPDDR5X, LVDS, and other standards • MIPI C-PHY support (4.5 GSPS) to complement 4.5 Gb/s D-PHY support • HDIO and MIO support lower speeds and logic levels up to 3.3V

NEXT STEPS

For more information on Versal RF Series devices, visit **www.amd.com/versal-rf**

ENDNOTES

1. Tera operations per second (TOPS) for an AMD Versal RF Series device is the maximum number of operations per second that can be executed in an optimal scenario and may not be typical. TOPS will vary based on device, design, configuration, and other factors. (VER-084)
2. Based on an AMD internal analysis, comparing the RF-ADC sample rate (GSPS) specification of the Versal RF VR1652 and VR1952 devices versus the published specifications of the Intel Agilex 9 Direct RF-Series AGRW014 and AGRW027 FPGAs and the pre-release design specifications of the ADI Apollo AD9084 and AD9088 devices. (VER-075)
3. Based on an AMD internal analysis (including hard IP, AIEs, and DSPs) to calculate the OPS offered by one (1) Versal RF VR1952 device versus OPS offered by one (1) Intel Agilex Direct RF-Series AGRW027 FPGA and two (2) Intel Agilex 7 Series AGI027 FPGAs. Results may vary based on device, configuration, design, and other factors. (VER-069)
4. Based on AMD engineering projections in November 2024, using the hard IP functions in Versal RF Series devices to measure dynamic power vs. the total power calculation of an AMD soft logic implementation, as measured with AMD Power Design Manager (2023.2.2), based on AMD Vivado 2023.2.2 IP catalog. (VER-080)

DISCLAIMERS

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