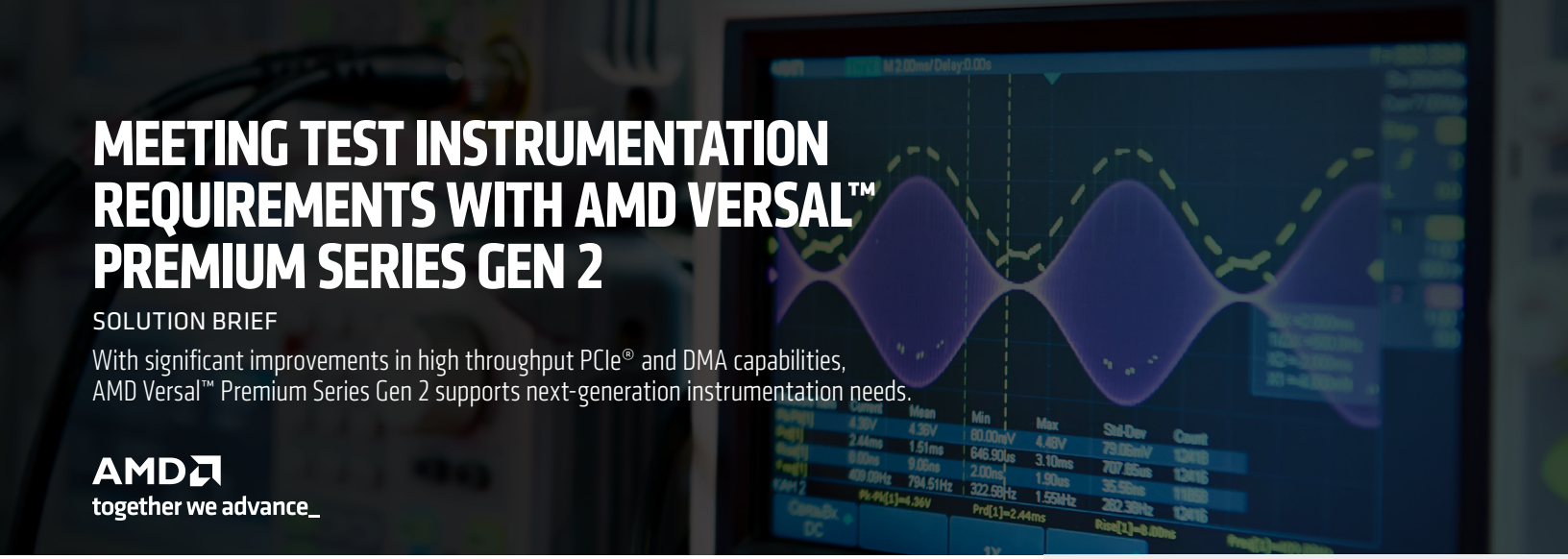

MEETING TEST INSTRUMENTATION REQUIREMENTS WITH AMD VERSAL™ PREMIUM SERIES GEN 2

SOLUTION BRIEF

With significant improvements in high throughput PCIe® and DMA capabilities, AMD Versal™ Premium Series Gen 2 supports next-generation instrumentation needs.

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OVERVIEW

Next-generation instrumentation equipment such as scopes, analyzers, signal-sources, and generators support host-to-device, device-to-host, and peer-to-peer communication across different types of end points. With this level of connectivity, there is a need for high I/O bandwidth across PCIe® backplanes to support increased channel bandwidth and channel count. With more channels and higher sample rates preferred by testers, higher DSP compute density is required. These requirements drive the need for higher memory bandwidth to support different types of memory devices such as DDR, LPDDR5X, and LPCAMM.

AMD Versal™ Premium Series Gen 2 devices address these next-generation instrumentation requirements with upgraded transceivers, high memory bandwidth, and multi-protocol transceiver support. Versal Premium Series Gen 2 devices offer the industry's first adaptive SoCs and FPGAs with an integrated block for PCIe Gen6 and CXL® 3.1.[1] These high throughput PCIe and CXL interfaces enable the demanding data transfer needs for instrumentation solutions.

KEY BENEFITS

UPGRADED TRANSCEIVERS

Next-generation transceivers supporting NRZ and PAM4 standards

HIGH MEMORY BANDWIDTH

Support for up to 273 GB/s external memory bandwidth with LPDDR5X-8533

HIGH DSP COMPUTE DENSITY

Higher DSP-to-logic ratio compared to 1st Gen Versal Premium Series devices

COMPACT FORM FACTOR

Enables smaller form factor testers, with package sizes as small as 35x35 mm

HIGHLIGHTS

ENHANCED TRANSCEIVER CAPABILITY

- Transceivers with broad protocol coverage from 1.25G – 128 Gb/s line rates*
- The Versal Premium Series Gen 2 2VP3602 device offers 2X more total transceiver bandwidth vs. the competition[2]
- NRZ and PAM4 encoding with efficiency up to 7pJ/bit with NRZ 1.15 GB to 56 GB and 56G to 128G PAM4

HIGH THROUGHPUT PCIE AND DMA BANDWIDTH

- Support for 2 PCIe Gen6x8 controllers with endpoint, root-port, and peer-to-peer modes
- Hard DMA engines provide up to 128 GB/s transfer throughput*
- GT-Direct Mode for CPM to bypass integrated block for PCIe for direct transceiver fabric access

HIGH DSP-LOGIC RATIO

- Scalable device family with LUT capacity ranging from 600k LUTs to 1.5M LUTs
- Increased DSP capability in Versal Premium Series Gen 2 devices enables more data processing—with 1.2-1.9X more DSP-to-logic ratio than the previous generation of Versal Premium Series devices[3]

MEMORY CAPABILITY

- Versal Premium Series Gen 2 offers the fastest connectivity to LPDDR5X memory (at up to 8533 Mb/s)[4]

** Data is preliminary and subject to change. (VER-063)*

TARGET APPLICATIONS

SCOPES, ANALYZERS, SIGNAL SOURCES, AND GENERATORS

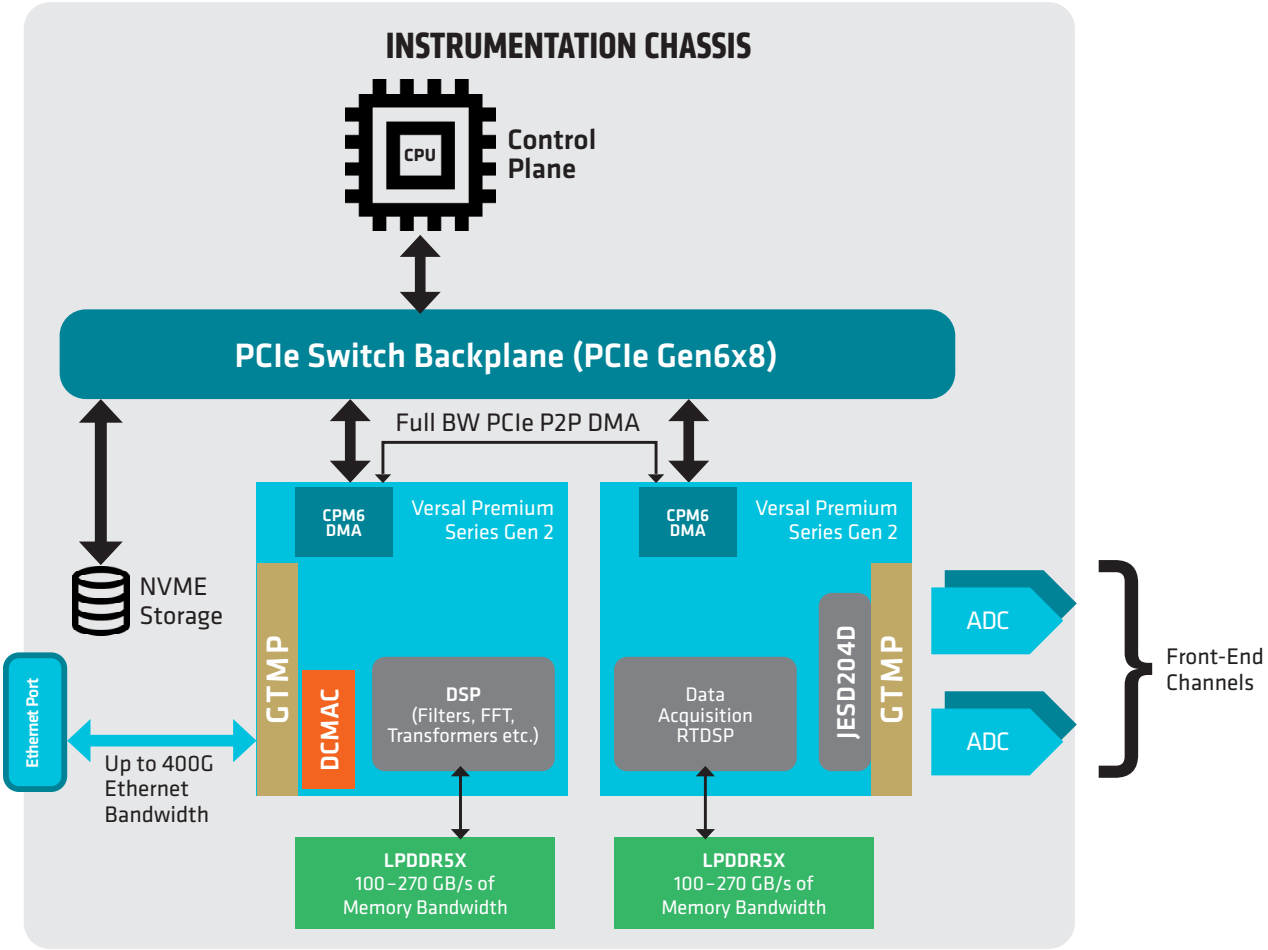
Instrumentation equipment is composed of scopes, analyzers, signal sources, and generators. The next-generation scopes and analyzers need massive memory and I/O bandwidth for interfacing with data acquisition and DACs. The next-generation equipment requires support for upcoming JESD204D standards based on PAM4. With these higher sample rates, there is higher demand for DSP capabilities.

Versal Premium Series Gen 2 addresses next-generation instrumentation with the following features:

- Transceivers up to 128 GB line rate*
- Support for up to 273 GB/s external memory bandwidth with LPDDR5X-8533
- Support for integrated interface for PCIe Gen6 for high throughput connectivity to instrument backplane
- Higher DSP-to-logic ratio, significantly increasing the DSP capability compared to first generation devices[3]
- Capability for devices to connect to CXL memory expander modules for greater memory bandwidth than an LPDDR5X memory interface alone

** Data is preliminary and subject to change. (VER-063)*

INSTRUMENTATION APPLICATION



FEATURES

FEATURE	HIGHLIGHTS
PROCESSING SYSTEM	• Complex algorithm processing and decision-making tasks • Dual-core Arm® Cortex®-A72 application processing unit • Dual-core Arm Cortex-R5F real-time processing unit
DSP ENGINES	• DSP-rich architecture with up to 7,616 DSP58 Engines • Wide range of modes supporting fixed and floating point data types suitable for DSP and ML applications
PCIe INTERFACES	• Up to 2 Tb/s aggregate bandwidth across 16 lanes (two x8 links) operating at 64 Gb/s per lane • Enhanced security features with Integrity and Data Encryption (IDE) support in hard IP
DEDICATED MEMORY CONTROLLERS	• Supports DDR5 up to 6400 Mb/s and LPDDR5X up to 8533 Mb/s • Hard inline ECC and encryption for data integrity and security
CONNECTIVITY IP	• Up to 3.1 Tb/s of scalable Ethernet throughput • Multirate: 400/200/100/50/40/25/10G • Multi-standard: FlexE, Flex-O, eCPRI, FCoE, and OTN
GTM2 TRANSCEIVERS	• Low-latency monolithic transceiver architecture • Supports PAM4 and NRZ encoding • 1.25-128 Gb/s data rate per channel[5]

NEXT STEPS

For more information on Versal Premium Series Gen 2 devices, visit **www.amd.com/versal-premium-gen2**
For more information on Test and Measurement, visit **www.amd.com/en/solutions/test-and-measurement.html**

ENDNOTES

1. Based on an AMD internal analysis of AMD Versal Premium Series Gen 2 devices with CXL 3.1 and PCIe 6.0 vs. comparable competitive devices without CXL 3.1 and/or with PCIe Gen 4/5, as of July 2024. (VER-055)
2. Based on AMD internal analysis of the AMD Versal Premium Series Gen 2 devices vs. published specifications of comparable competitive devices in the fastest speed grade. Actual total transceiver bandwidth will vary based on system configuration and other factors. (VER-060)
3. Based on AMD internal analysis of AMD Versal Premium Series Gen 2 devices vs. previous generation Versal Premium Series devices, as of July 2024. Actual DSP-to-logic ratio will vary based on system configuration and other factors. (VER-061)
4. Based on AMD internal analysis of Versal Premium Series Gen 2 device DDR/LPDDR memory interface specifications vs. comparable competitive devices, as of July 2024. Actual performance will vary based on system configuration and other factors. (VER-058)
5. Data is preliminary and subject to change. (VER-063)

DISCLAIMERS

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