AMD VERSAL™ PREMIUM SERIES GEN 2: FASTER DATA FLOW, UNLOCKED INSIGHTS

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OVERVIEW

AMD Versal™ Premium Series Gen 2 offers new levels of memory and data bandwidth with CXL® 3.1, PCIe® Gen6, and DDR5/LPDDR5X interfacing capabilities, tailored to fit the application requirements of today's and tomorrow's data center, communications, test & measurement, and aerospace & defense data-intensive applications. AMD Versal Premium Series Gen 2 speeds up data flow[1,2] and reduces memory bottlenecks,[3] allowing data-intensive applications to be accelerated and insights to be unlocked.

As a heterogeneous compute platform, Versal Premium Series Gen 2 is engineered to help users reach high levels of acceleration for a wide range of compute-intensive workloads by providing high compute density, custom memory hierarchy, and DSP Engine resources.

With the AMD Vivado™ Design Suite and the AMD Vitis™ unified software development platform, Versal Premium Series Gen 2 offers a complete solution stack for hardware and software developers to maximize productivity.

HIGHLIGHTS

ACCELERATE HOST CONNECTIVITY

- Industry's first adaptive SoCs and FPGAs with an integrated block for PCIe Gen6 and CXL 3.1[4]
- Hard IP for CXL 3.1 provides memory coherency, supports memory pooling, and enables heterogeneous compute
- Double bandwidth per lane with PCIe Gen6 (compared to prior-gen Versal series with PCIe Gen5)[2]

UNLOCK MORE MEMORY FASTER

- Ultra-fast enhanced DDR memory connectivity with support for LPDDR5X up to 8533 Mb/s and DDR5 up to 6400 Mb/s
- Additional memory and memory bandwidth by interfacing to CXL memory expansion modules
- Utilize memory more efficiently and eliminate stranded memory with memory pooling and support for Multi-Headed Single Logic Device (MH-SLD) use cases

STRENGTHEN DATA SECURITY

- Offers more secure data transfers available with PCIe Integrity and Data Encryption (IDE) in hard IP[5]
- Helps secure data storage with inline encryption built into integrated memory interface controllers

KEY APPLICATIONS

DATA CENTER
- Compute Acceleration
- Custom Networking
- Computational Storage

TEST & MEASUREMENT
- Protocol Analyzers
- Wireless Testers
- Network Testers

COMMUNICATIONS
- 5G & 6G Wireless
- Data Center Interconnect
- Security Appliance

AEROSPACE & DEFENSE
- Avionics
- Radar
- Cognitive Radio/SDR

FEATURES

FEATURE	HIGHLIGHTS
PROCESSING SYSTEM	• Complex algorithm processing and decision-making tasks • Dual-core Arm® Cortex®-A72 application processing unit • Dual-core Arm Cortex-R5F real-time processing unit
PLATFORM MANAGEMENT CONTROLLER	• Boot, configuration, and advanced power & thermal management • Security, safety, and reliability enclave • Integrated platform interfaces and high-speed debug
PROGRAMMABLE LOGIC	• High-bandwidth, low-latency compute and data movement • Programmable memory hierarchy for optimal compute efficiency
DSP ENGINES	• DSP-rich architecture with up to 7,616 DSP58 Engines • Wide range of modes supporting fixed and floating point data types suitable for DSP and ML applications
PROGRAMMABLE NETWORK ON CHIP	• High-bandwidth multi-terabit NoC for reliable QoS • Programmable framework memory-mapped access to all resources • Easy IP and kernel placement
ON-CHIP MEMORY	• Up to 281 Mb of tightly coupled memory for performance, power, and latency • Up to 59 TB/s of on-chip memory bandwidth
GTM2 TRANSCEIVERS	• Low-latency monolithic transceiver architecture • Supports PAM4 and NRZ encoding • 1.25-128 Gb/s data rate per channel*
PCIE GEN 6	• Up to 2 Tb/s aggregate bandwidth across 16 lanes (two x8 links) operating at 64 Gb/s per lane • Enhanced security features, with Integrity and Data Encryption (IDE) support in hard IP
CXL 3.1	• Up to 2 Tb/s bandwidth on a memory coherent link • Supports memory pooling and Multi-Head Single-Logic Device (MH-SLD) use cases • Connects to CXL memory expander modules for greater bandwidth than LPDDR5X memory alone, with 1.9-2.9X more total bandwidth[3]
INTEGRATED 600G ETHERNET AND 100G MULTIRATE ETHERNET CORES	• Up to 3.1 Tb/s of scalable Ethernet throughput • Multirate: 400/200/100/50/40/25/10G • Multi-standard: FlexE, Flex-O, eCPRI, FCoE, and OTN
400G HIGH-SPEED CRYPTO ENGINES	• AES-GCM-256/128 engines • Up to 800 Gb/s of line rate encryption throughput • 400G of MACsec, IPsec, and bulk encryption per engine
DEDICATED MEMORY CONTROLLERS	• Supports DDR5 up to 6400 Mb/s and LPDDR5X up to 8533 Mb/s • Hard inline ECC and encryption for data integrity and security
LDPC DECODER	• Provides high throughput LDPC soft-decision decoding • Efficient solution for error correction in communications and storage applications

* Data is preliminary and subject to change. (VER-063)

NEXT STEPS

For more information on Versal Premium Series Gen 2 devices, visit **www.amd.com/versal-premium-gen2**

ENDNOTES

1. Based on an AMD internal analysis of AMD Versal Premium Series Gen 2 devices with CXL 3.1 vs. comparable competitive device(s) with CXL 2.0, as of July 2024. Actual line rate speed will vary based on system configuration and other factors. (VER-056)

2. Based on an AMD internal analysis of the AMD Versal Premium Series Gen 2 devices with PCIe Gen6 vs. comparable competitive and prior generation AMD Versal Premium Series devices with PCIe Gen4/5, as of July 2024. Actual line rate speeds will vary based on system configuration and other factors. (VER-057)

3. Based on AMD internal analysis of the total memory bandwidth (CXL 3.1 and LPDDR5X memory components) available with AMD Versal Premium Series Gen 2 devices vs. the same devices with LPDDR5X memory alone. Memory bandwidth will vary based on system configuration and other factors. (VER-059)

4. Based on an AMD internal analysis of AMD Versal Premium Series Gen 2 devices with CXL 3.1 and PCIe 6.0 vs. comparable competitive devices without CXL 3.1 and/or with PCIe Gen 4/5, as of July 2024. (VER-055)

5. Based on AMD internal analysis in October 2024, AMD Versal Premium Series Gen 2 devices include the PCIe Integrity and Data Encryption feature, while the competition does not. (VER-064)

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