Designing With The AMD MicroBlaze™ V Processor for The AMD Spartan™ Ultrascale+™ FPGA

AMD
together we advance_

AMD MicroBlaze™ V Soft Processor

AXI Interconnect

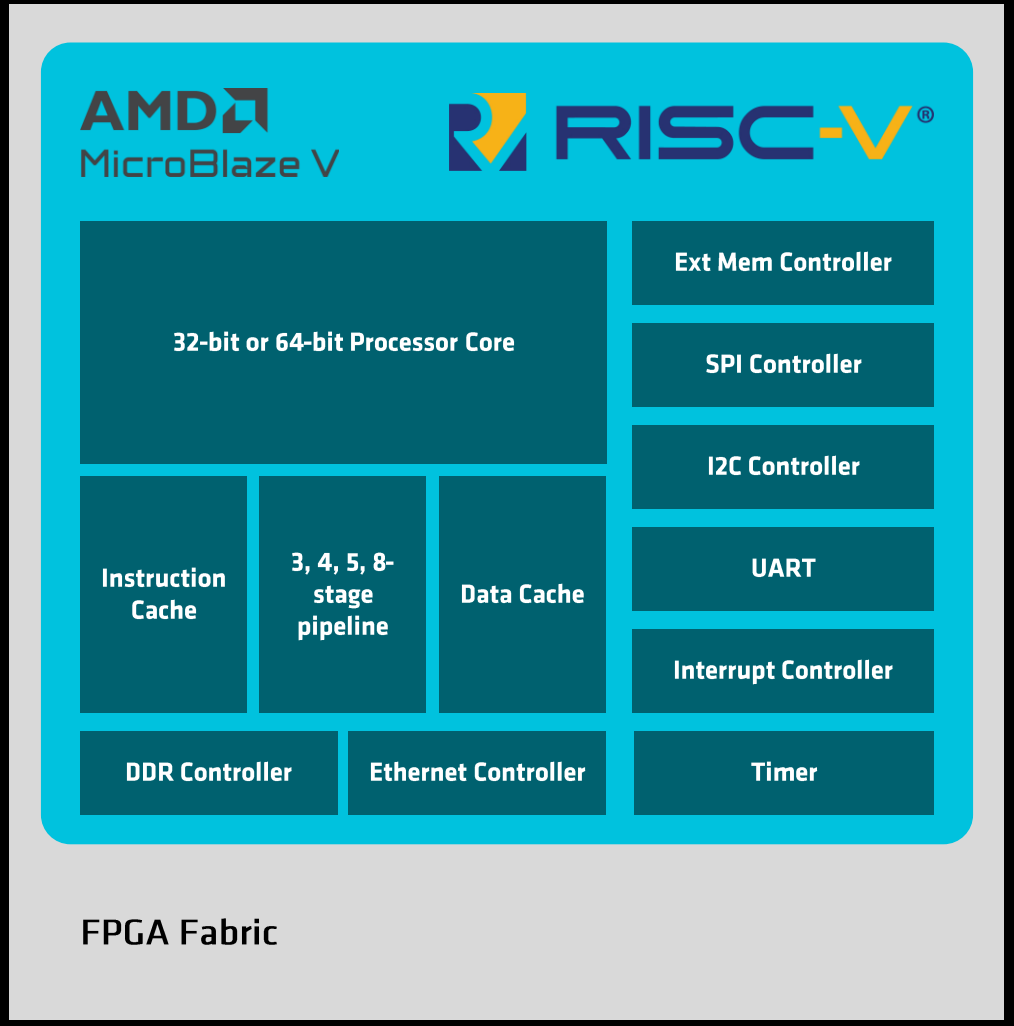
- Plug-and-play design integration
- Extensive soft IP peripherals

RISC-V Extension Support

- Support for extensions: M, A, F, D, C, Zb[abcs], Zicsr, Zifencei, Zicbom

Area & Performance Tuning

- Configurable pipeline length
- Optional instruction and data caches



Lockstep Capable

- Tamper resistance
- Fault protection

Triple Modular Redundant (TMR) Capable

- Single event upset (SEU) mitigation
- Voter circuit

Predefined Configurations

- Microcontroller: Area optimal
- Real-Time: RTOS support with soft DDR controller and cache

File Flow Tools Window Help Quick Access

AMD Vivado ML Edition

Quick Start

Create Project >
Open Project >
Open Example Project >

Tasks

Manage IP >
Open Hardware Manager >
Vivado Store >

Learning Center

Documentation and Tutorials >
Quick Take Videos >
What's New in 2025.1 >

Recent Projects

mbv_demo
/group/techsup/anusnand/mbv/project

counter
/group/techsup/anusnand/counter_demo/project

Tcl Console

```
start_gui
```

Type a Tcl command here

Additional Resources

UG1629:

MicroBlaze V Processor Reference Guide

PG428: :

MicroBlaze Debug Module V LogiCORE™ IP Product Guide

WP469:

Using MicroBlaze to Accelerate Cost-Sensitive Embedded System Development

UG1711:

MicroBlaze V Processor Embedded Design User Guide

PG112:

LMB BRAM Interface Controller LogiCORE IP Product Guide

GitHub:

Vivado-Design-Tutorials/Designing_in_IPI

XD131:

Programming an Embedded MicroBlaze™ Processor Tutorial

XMP507:

MicroBlaze V Processor Quick Start Guide for Vitis™ Unified 2024.1

PG268:

Triple Modular Redundancy (TMR) LogiCORE IP Product Guide

GitHub:

Embedded-Design-Tutorials/Programming an Embedded MicroBlaze V Processor

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