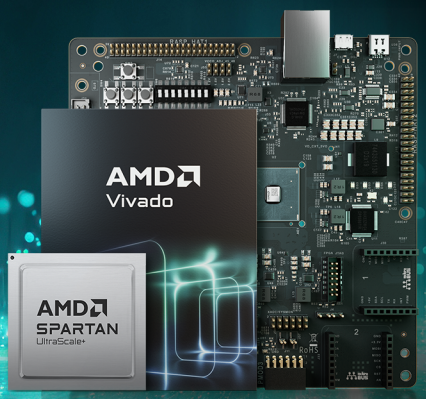
SOLUTION BRIEF

AMD FPGA & ADAPTIVE SoC IP

BROAD SELECTION OF IP TO ACCELERATE DESIGN CYCLES

AMD
together we advance_



OVERVIEW

Accelerate your design cycles with a robust, production-ready portfolio of nearly 400 IP cores. AMD provides an unmatched breadth of foundational building blocks and application-specific subsystems, each rigorously verified and optimized for AMD FPGA and adaptive SoC architectures.

Whether working on vision pipelines or high-speed connectivity, the IP portfolio scales across device families and design requirements. Leveraging RTL and IP integrator flows within the AMD Vivado™ Design Suite, developers can rapidly assemble, validate, and deploy systems that differentiate on application value.

HIGHLIGHTS

BROAD SELECTION OF IP FOR EVERY APPLICATION

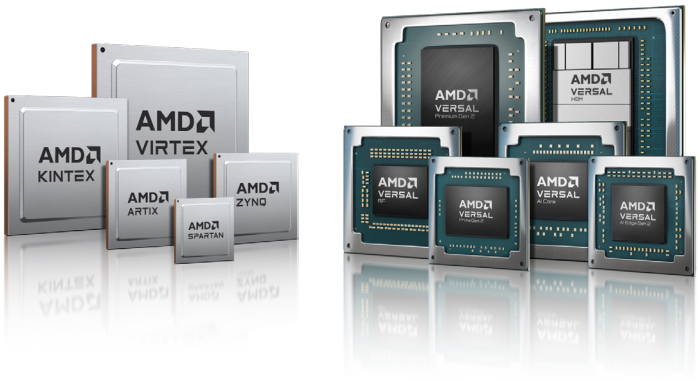
- From building block IP to production-grade, complex subsystems
- Hard and soft IP optimized across AMD silicon architectures

RIGOROUS VALIDATION AND LONG-TERM SUPPORT

- IP RTL verification and randomized regression testing
- Full-system, use-case validation and compliance coverage
- Long-term technical support

STREAMLINED INTEGRATION INTO YOUR DEVELOPMENT PROCESS

- Open standards and AXI-based design flows
- RTL and IP Integrator supported design flows
- Examples, software drivers, and comprehensive documentation



IP PORTFOLIO HIGHLIGHTS

FOUNDATIONAL ELEMENTS

- I/O interfaces and high-speed serial
- Building blocks, clocking & reset functions
- Debug & verification IP
- Soft Error Mitigation

MEMORY SOLUTIONS

- External memory interfaces & controllers
- Block memory and FIFO generators
- UltraRAM, MPRAM, CAM, CDCAM

MULTIMEDIA & VIDEO

- Video codec and processing
- Audio
- Video connectivity

INTERFACES & INTERCONNECT

- AXI infrastructure, peripherals, and NoC
- Data converters
- PCI Express®, Ethernet, and serial interfaces
- Storage

EMBEDDED PROCESSORS

- AMD MicroBlaze™ soft processors
- RISC-V based architecture support
- Integrated Arm® processing systems

DSP & MATH FUNCTIONS

- Core arithmetic building blocks
- Error correction subsystems

MARKET-SPECIFIC

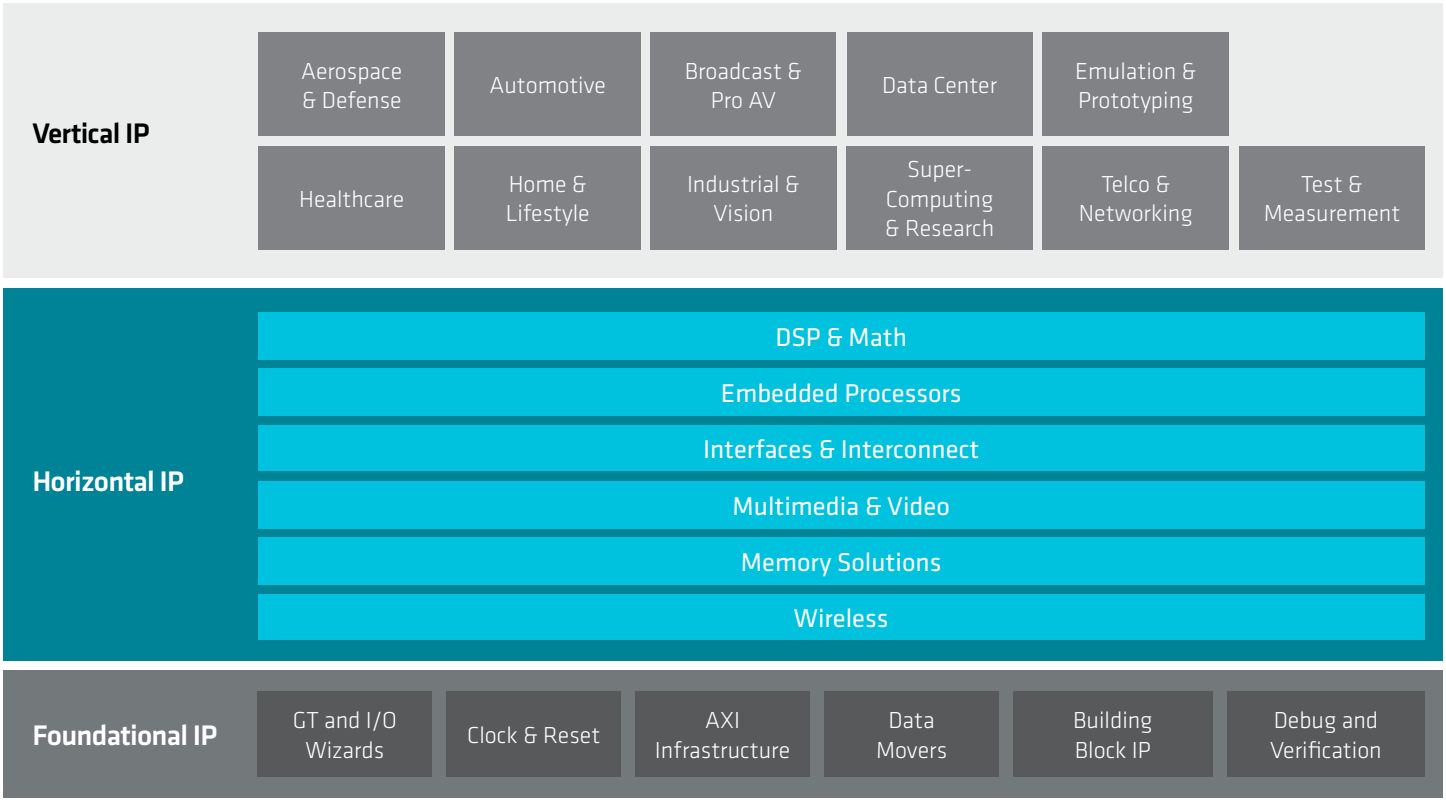
- Aerospace & Defense
- Automotive
- Broadcast & Pro AV
- Healthcare
- Industrial and Vision
- Telco & Networking
- And More ...

BROAD SELECTION OF IP FOR EVERY APPLICATION

The AMD IP catalog spans hundreds of pre-verified cores that support functions essential to embedded system development: high-speed connectivity, DSP and math functions, memory interfaces, multimedia processing and connectivity, and wireless applications. These cores are architected for optimal performance across device families, enabling developers to streamline design cycles and scale to next-generation projects. IP can be accessed directly through the Vivado Design Suite and is available through both RTL-level and IP Integrator block-based design flows.

Platform-level design starts with selecting the right device—balancing programmable logic and hard IP for ASIC-class performance/watt of critical functions—then layering in proven soft IP to streamline the rest. This approach enables faster integration and more time to focus on application-level differentiation.

NEARLY 400 CORES AVAILABLE IN THE AMD IP CATALOG



RIGOROUS VALIDATION AND LONG-TERM SUPPORT

Each AMD IP core is verified using industry-standard methodologies—including randomized regression testing, protocol and compliance checks, and system-level validation—to ensure correctness across a wide range of configurations. This includes static timing analysis, DRC checks, bitstream/Programmable Device Image (PDI) generation, and testing the IP in full use-case systems. Combined with robust documentation, examples, software drivers, and long-term technical support, AMD provides a suite of resources to streamline IP integration into any design.

STREAMLINED INTEGRATION INTO YOUR DEVELOPMENT PROCESS

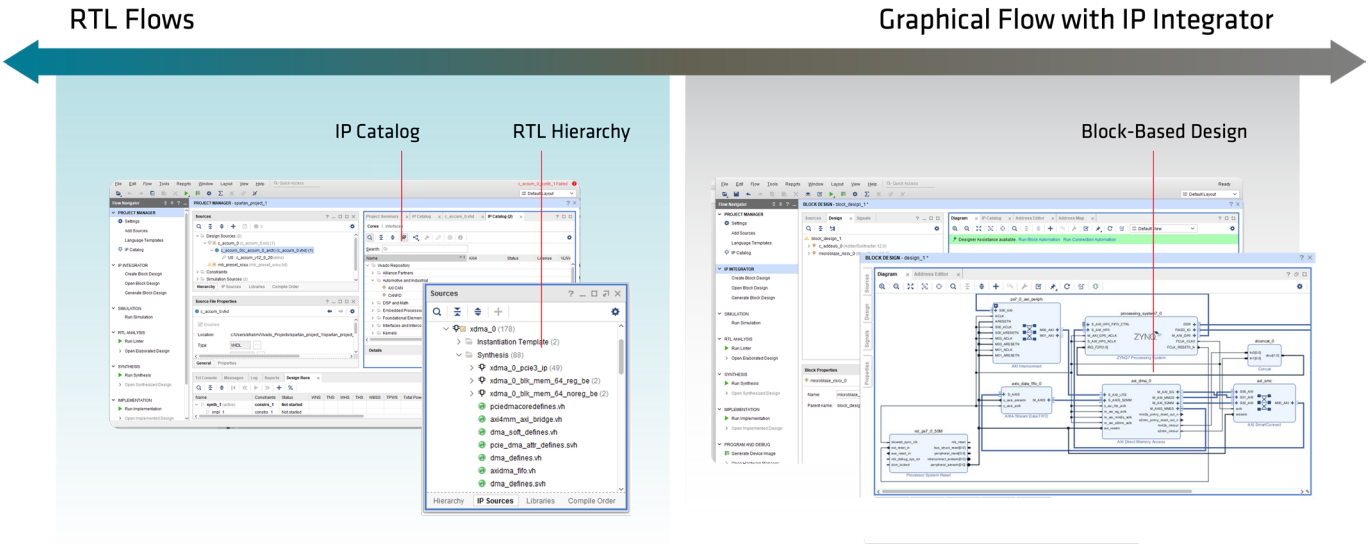
Accelerate IP integration with the AMD Vivado™ Design Suite, which supports both RTL-based and block-based design flows, each streamlining IP assembly based on preference.

In Vivado IP integrator, designers can drag and drop IP blocks, configure them through guided wizards, and rely on the Vivado tools to handle address mapping and connectivity to AXI interfaces. The result is correct-by-construction integration—enforced through real-time design rule checks (DRCs), interface validation, and automated parameter propagation.

For developers using RTL flows, IP cores are instantiated directly in code—allowing for greater control over hierarchy, connectivity, and integration with custom scripts and version-controlled environments. This approach can be preferable for complex designs where fine-grained control is required.

To support both workflows, AMD provides reference designs, detailed documentation, and software drivers specific to AMD architectures, ensuring teams can evaluate, integrate, and deploy with confidence.

FLEXIBLE IP INTEGRATION METHODOLOGIES



NEXT STEPS

- Learn more about AMD and Partner IP at **Intellectual Property**
- Download **AMD Vivado™ Design Suite** to start designing with IP in either RTL or IP Integrator flows