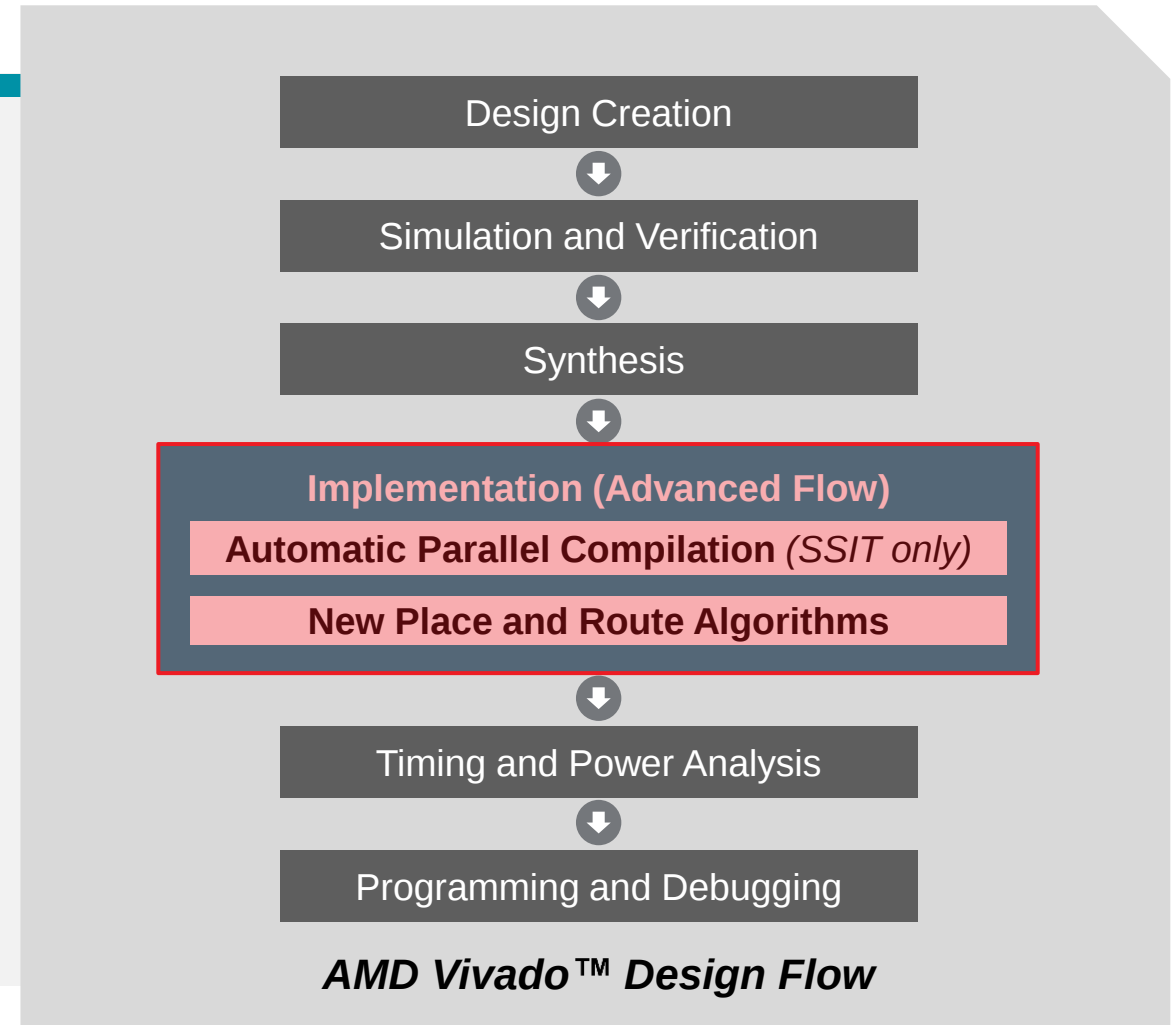




Migrating Pre-2024.2 AMD Versal™ Adaptive SoC Design Projects to Vivado 2024.2

AMD Vivado™ Design Suite Tool Flow With “Advanced Flow”

- AMD Versal™ devices have significantly higher logic density compared to AMD UltraScale+™ devices
- Complex Versal™ designs lead to significantly longer compilation times
- Essential to control compile time, design closure, and congestion as designs become more complex



Automatic Partitioning for Parallel Processing

Partitioning & Floorplanning

Automatic partitioning based on design hierarchy, resource usage, and connections between hierarchical blocks



Global Placement

Evaluates timing impact and reduces routing congestion



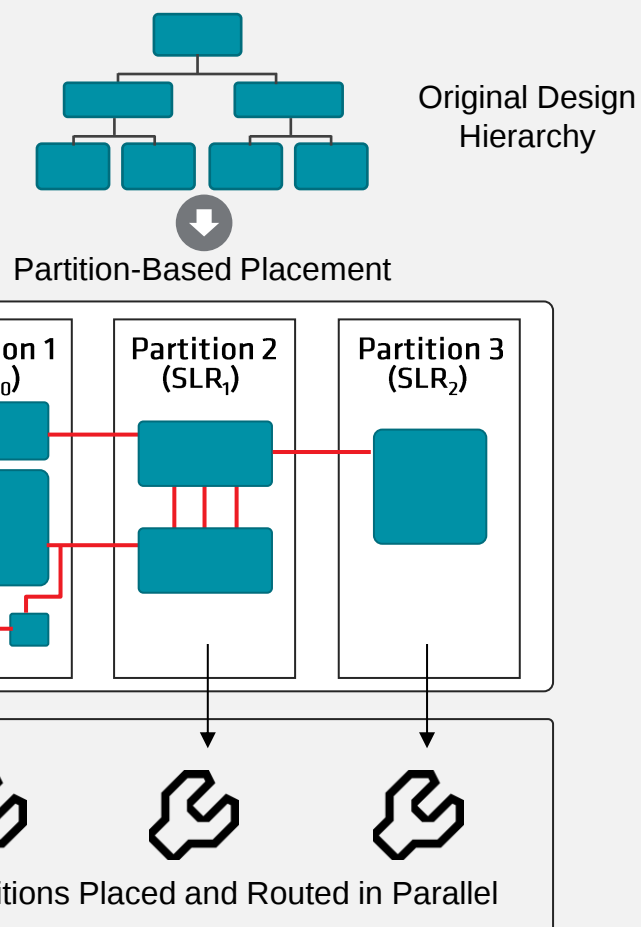
Detailed Placement & Post-Place Optimizer

Ensures optimal logic density and overall performance



Routing

Routing of partitions in parallel, fast timing convergence



“Advanced Flow” Reduces Congestion for Faster Design Closure

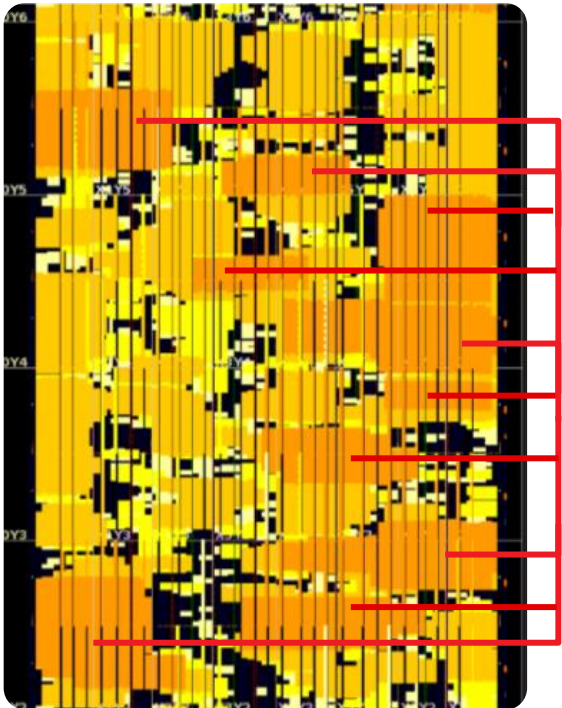
Congestion: High utilization of routing resources in certain areas; can potentially lead to difficult timing closure

Standard Flow
AMD Vivado™ Design Suite
2024.1 Release

*Design taken as-is, no
additional optimization settings*

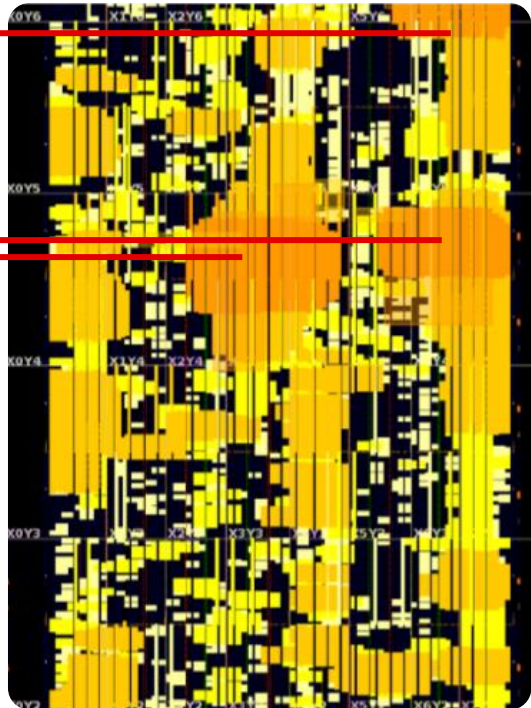
Advanced Flow
Vivado Design Suite
2024.2 Release or Later

Congestion Level ¹	
0	
1	
2	
3	
4	
5	
6	
7	
8	



Many High
Congestion Regions

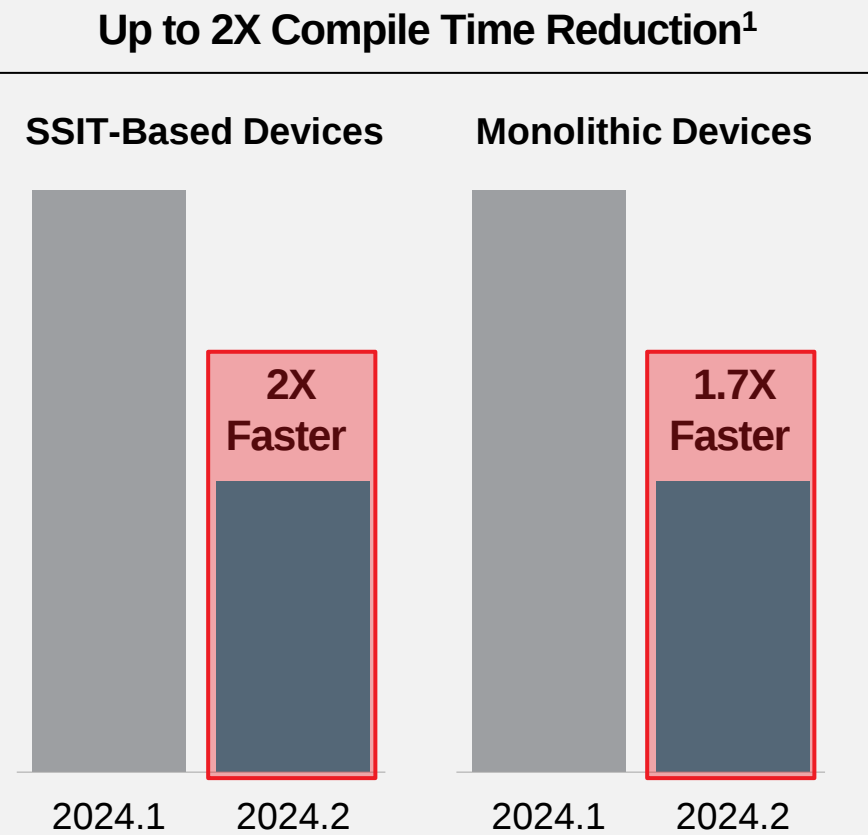
Fewer High
Congestion Regions



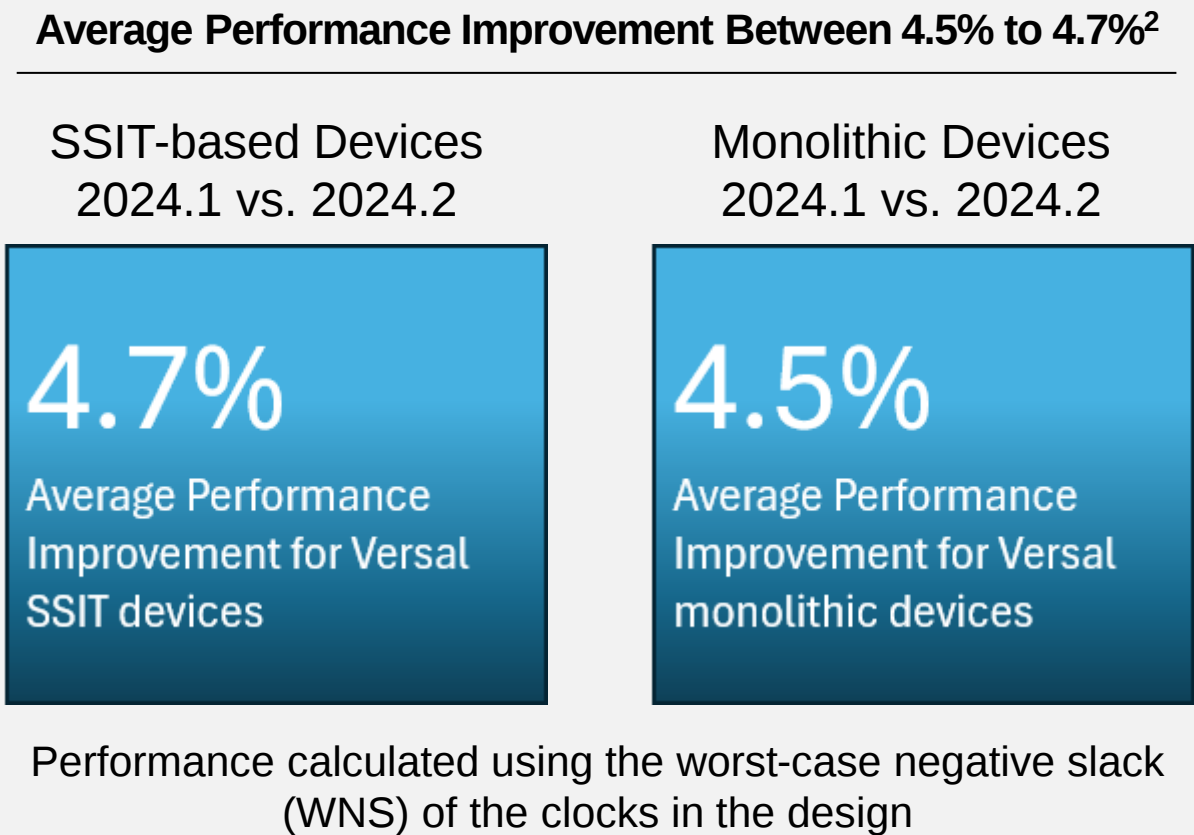
Less Congestion Gives Placer More Room to Optimize for F_{MAX}

Source: AMD, March 2025
1: See [Versal Adaptive SoC System Integration and Validation Methodology Guide \(UG1388\): Congestion Level Ranges](#) for details on congestion levels and definitions

Compile Time Reduction & Performance Improvement with Advanced Flow for AMD Versal™ Devices



1: See Endnotes VIV-010, VIV-011



2: See Endnotes VIV-013, VIV-014

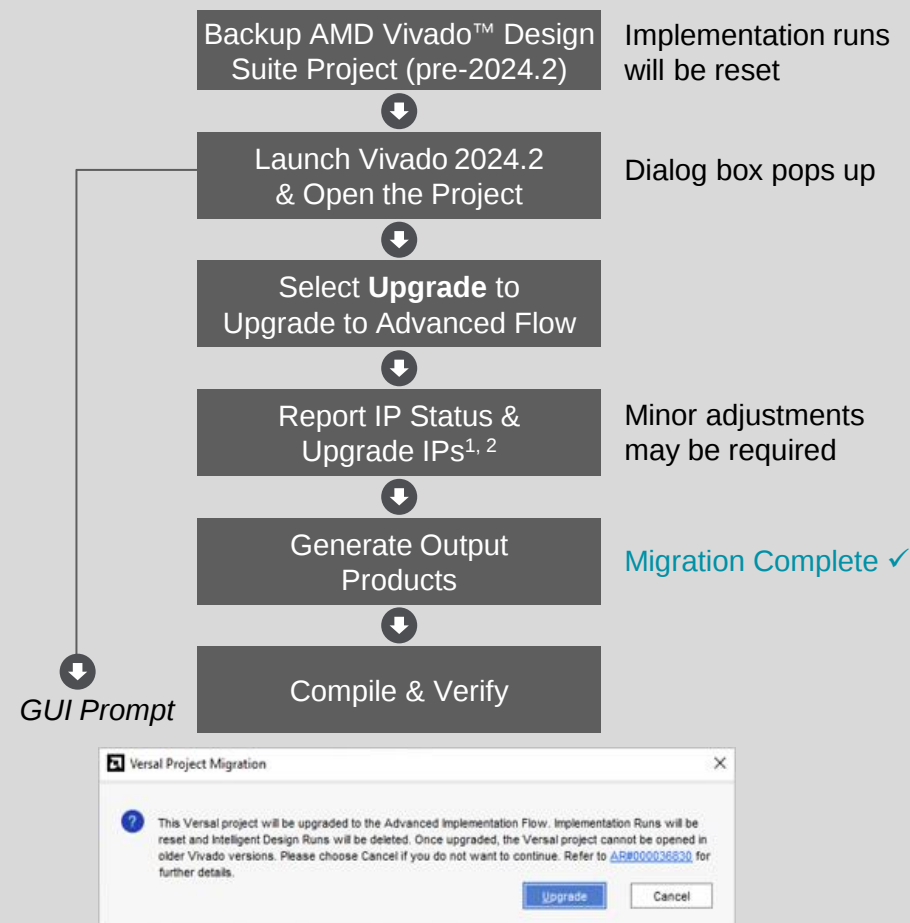
Migrating AMD Vivado™ Design Suite Projects to the Advanced Flow

For New AMD Versal™ Adaptive SoC Projects

- Default flow
- Automated, no additional steps or licenses required
- Cannot go back to earlier AMD Vivado Design Suite (pre-2024.2)

Certain features not yet supported as of 2024.2¹

- Intelligent Design Runs (IDR)
- Incremental implementation flows
- Additional power optimization settings



1: Not necessary to upgrade all IP immediately; see [UG896: Designing with IP](#) (sections [Upgrading IP](#) & [Selectively Upgrading IP](#)); also [Managing Vivado IP Version Upgrades](#) video

2: Refer to release notes of latest release for updated feature support

Summary & Key Benefits

01

Advanced Flow: New AMD Vivado™ Design Suite place and route feature set for AMD Versal™ devices in 2024.2

02

Advanced Flow offers faster compilation and reduces congestion

03

Migrating a design to use Advanced Flow in Vivado Design Suite 2024.2 version is irreversible

04

Pre-2024.2 implemented design runs cannot be opened or reused in the 2024.2 release

05

Synthesis runs and pre-place checkpoints created between 2021.1 and 2024.2 are compatible

06

Advanced Flow place and route algorithms enable higher productivity with more turns per day

Endnotes

- VIV-011: *Up to 2X compile time reduction for Versal adaptive SoC SSIT devices*
Based on a single-test scenario performed by AMD in December 2024, measuring the average compile times (hours/minutes) over 124 designs targeting Versal Stacked Silicon Interconnect (SSI) technology devices using Vivado Design Suite 2024.2 vs. Vivado Design Suite 2024.1. Compile time results will vary based on device, design, configuration, and other factors. (VIV-011).
- VIV-010: *Up to 1.7X compile time reduction for monolithic Versal adaptive SoC devices*
Based on a single-test scenario performed by AMD in December 2024, with measuring the average compile times (hours/minutes) over 151 designs targeting Versal monolithic devices using Vivado Design Suite 2024.2 vs. Vivado Design Suite 2024.1. Compile time results will vary based on device, design, configuration, and other factors. (VIV-010)
- VIV-014: *Up to 4.7% performance (F_{MAX}) improvement for Versal adaptive SoC SSIT devices* Based
on AMD worst negative slack performance testing in April 2025, using Vivado Design Suite 2024.2 vs. 2024.1. Stated results are a geomean average over 125 SSI designs. Results may vary based on device, design, configuration, software, and other factors. (VIV-014)
- VIV-013: *Up to 4.5% performance (F_{max}) improvement for monolithic Versal adaptive SoC devices*
Based on AMD worst negative slack performance testing in April 2025, using Vivado Design Suite 2024.2 vs. 2024.1. Stated results are a geomean average over 153 monolithic designs. Results may vary based on device, design, configuration, software, and other factors. (VIV-013)

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