Reducing Clock Skew in AMD Versal™ Devices

AMD
together we advance_

Agenda

- **Enhancement in AMD Versal™ Clocking Architecture**
- Basic Deskew in AMD Versal Devices
- Calibrated Deskew in AMD Versal SSIT Devices
- Summary

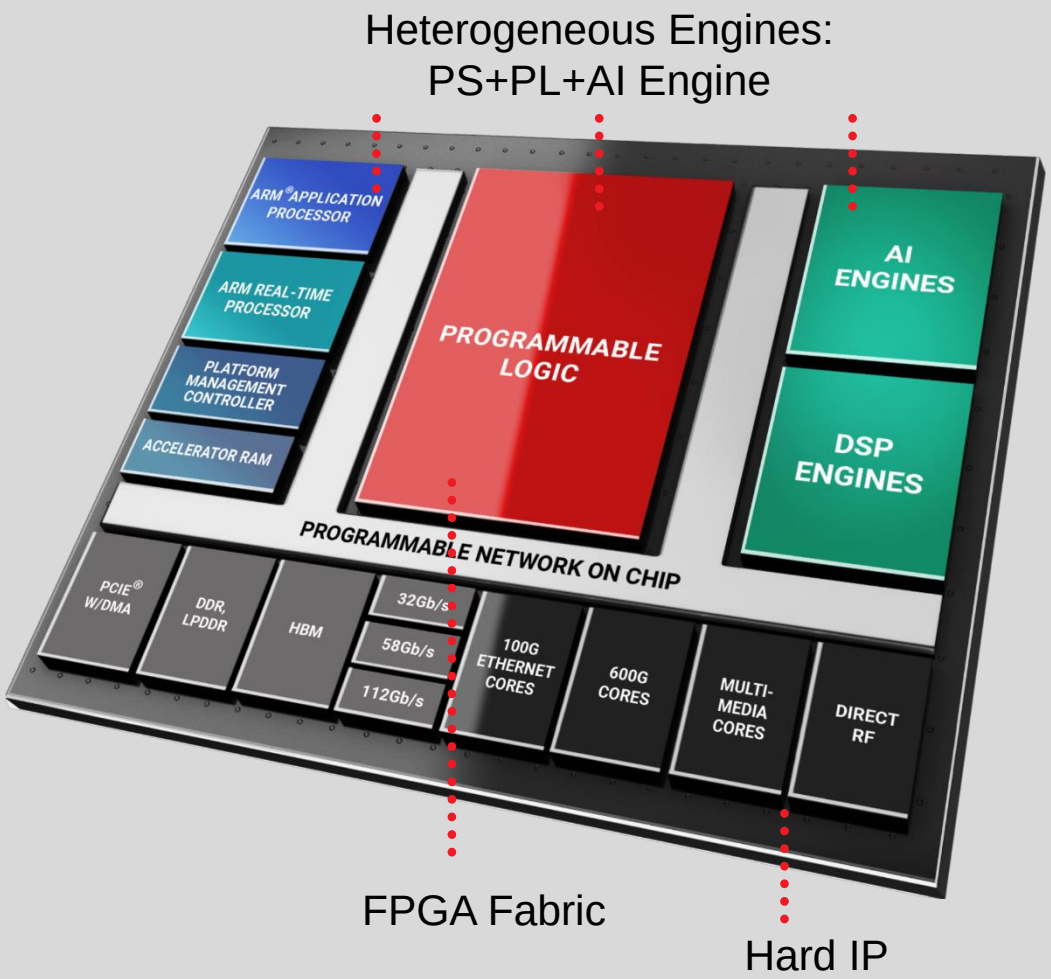
AMD Versal™ Adaptive SoCs: Heterogeneous Acceleration with Hard IP

Heterogeneous Acceleration
Diverse compute engines

Breakthrough Integration of Hard IP
ASIC perf/watt for bandwidth-intensive functions

FPGA Fabric for Differentiation
Hardware adaptable for custom algorithms

Traditional Timing Closure Techniques Still Apply to FPGA Fabric with AMD Vivado™ Design Suite



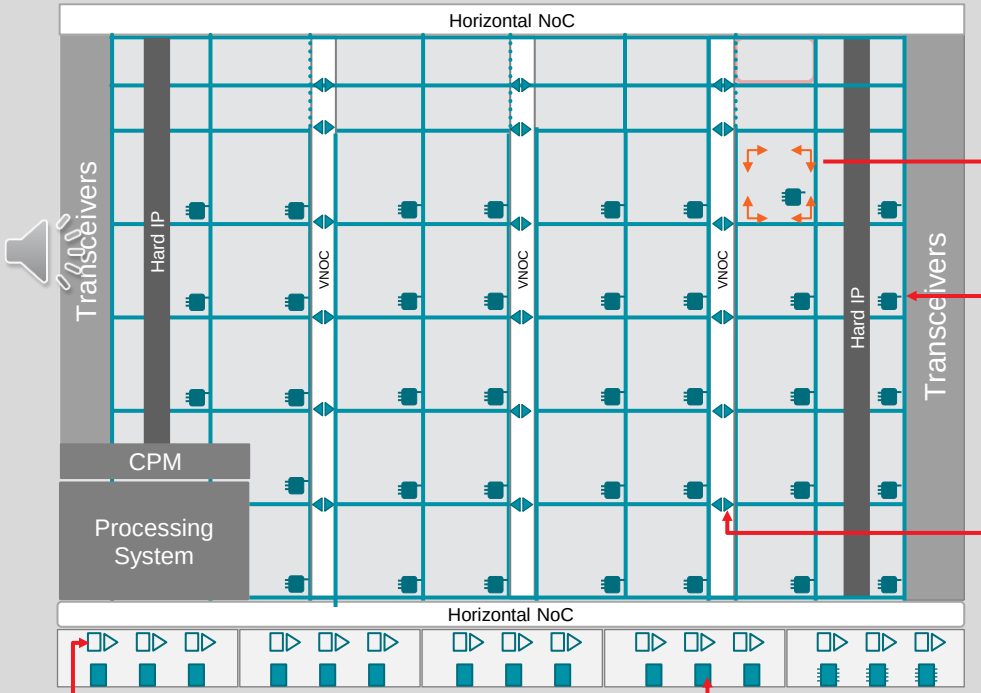
AMD Versal™ Clocking Architecture Enhancements

To minimize skew and maximize performance

- **Similar segmented clock network**
  Similar clocking elements (e.g., MMCM, XPLL)
- **BUFG_Fabric for High Fanout Nets**
  Fast access from fabric to clock networks
- **Multi-Clock Buffer (MBUFG) reduces skew for CDCs**
  Dedicated clock divider near fabric
- **Flexible Clock Trees for Targeted Skew Reduction**
  More balanced skew across super logic regions (SLRs) and intra-SLR
- **Calibrated Deskew for Multi-SLR Devices**
  Calibrates programmable delay at device startup

AMD Versal™ Clocking Architecture

Breadth of Enhancements to Reduce Skew for F_{MAX}



AMD Versal™ Architecture Clock Routing & Distribution

Purpose: Route a clock from BUFG to a central point, aka “clock root”

Clock Region & HCS

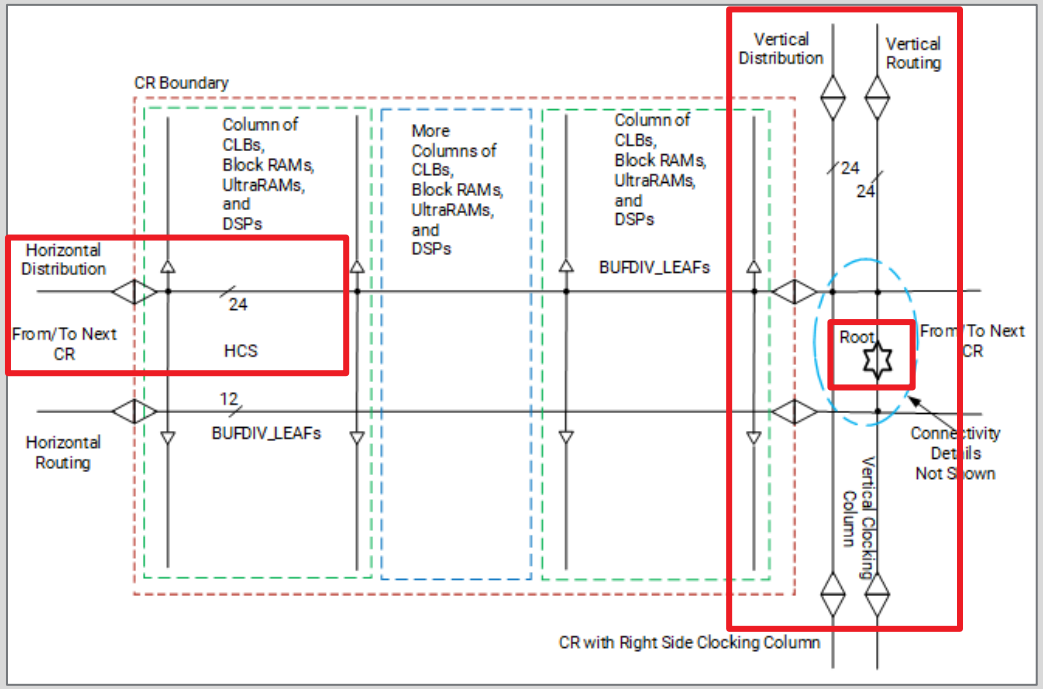
- Clocking architecture composed of blocks of clock regions (CR)
- Horizontal clock spine (HCS) runs horizontally in the center of each row of CRs and GTs

Clock Routing

- Clock root can be next to any CR in device
- Clock travels vertically and then horizontally using clock routing tracks
- 12 horizontal, 24 vertical routing tracks

Clock Distribution

- Distribution tracks move the root for all the loads at a specific location for improved localized skew
- Clocking columns drive vertical routing & distribution tracks through delay lines
- 24 horizontal, 24 vertical distribution

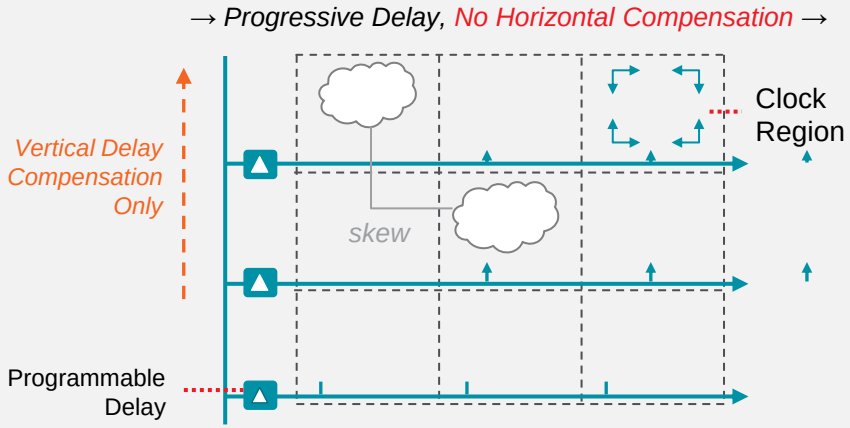


Vertical H Tree Clock Distribution for Enhanced Deskew

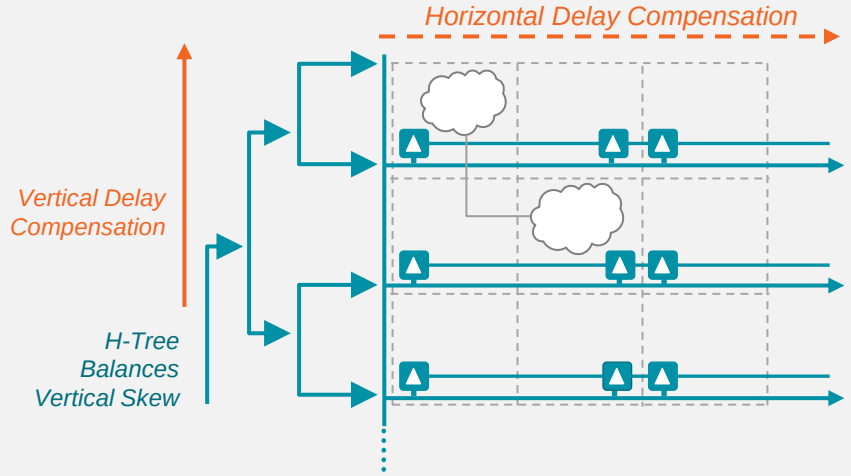
AMD Versal™ clocking architecture topology is segmented similar to AMD UltraScale+™ clocking

- Employs new Vertical H tree to minimize clock skew in vertical and horizontal direction (driven by vertical routing)
- Ensures entry to vertical clock routing happens at the center of the tree to minimize the insertion delay
- Purpose: Route a clock from BUFG to a central point, aka “clock root”
- **Benefits:** Improves localized skew, balances delay lines, reduces clock insertion delay, and flexibility

UltraScale+ Device Clocking



Versal Device Clocking



Review clock utilization reports to understand resource usage

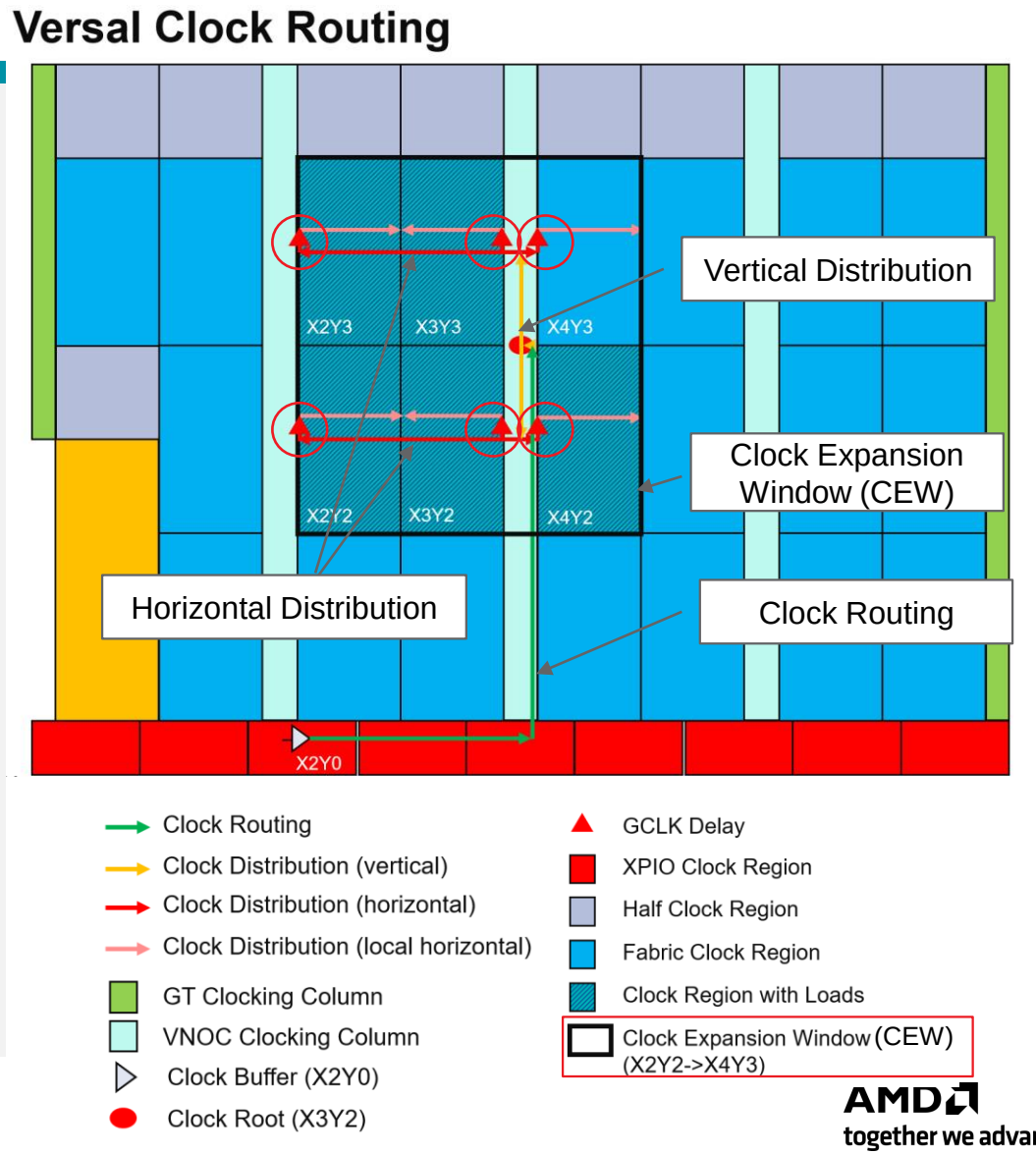
AMD Versal™ Architecture Clock Routing and Deskew Settings

AMD Vivado™ Design Suite implementation tries to minimize worst negative slack (WNS)—not the clock skew

To reduce clock skew, use:

- **Basic Deskew** – Leverages new AMD Versal™ architecture clock routing
  - Best for lower insertion delay. Typical usage:
    - Small clock trees, like in I/O interfaces
    - Minimizing inter-clock skew for sync CDC paths using parallel BUFG
  - Less restrictive on clock root placement

- **Calibrated Deskew** – Used in Versal SSIT devices
  - Additional programmable delays calibrated at device startup
  - Decreases skew between clock regions horizontally
  - Decreases skew between clock regions vertically
  - Decreases skew between SLRs for higher crossing F_{MAX}



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Basic Deskew Using Vertical H Tree

- Skew greatly impacts large devices with high F_{MAX}
- Basic deskew feature leverages new AMD Versal™ device clock routing

Typical usage: Paths with lower insertion delay - small clock trees, CDC paths

Clock tree types for different QoR areas: 3 deskew templates available[1]

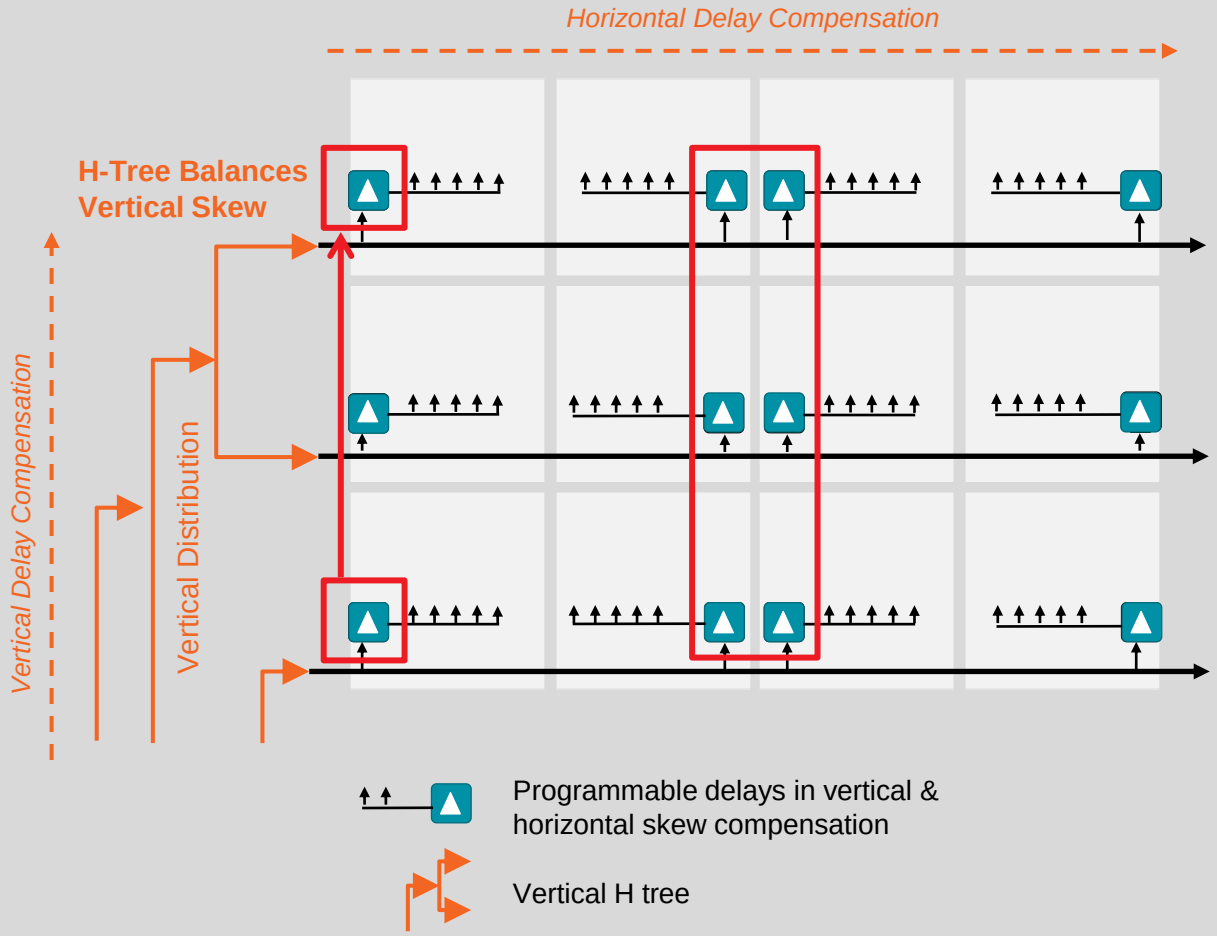
Inter-SLR	Intra-SLR	Balanced
Prioritize SLR crossings (at the expense of Intra-SLR)	Prioritize PL within SLRs (at the expense of Inter-SLR)	Optimal balance of inter- and intra-SLR skew (default)

1: Refer to UG1388: *AMD Versal Adaptive SoC Integration and Validation Methodology Guide*: *Applying Common Techniques for Reducing Clock Skew*

Basic Deskew Using Vertical H Tree: Visual Representation

- Delay lines can now compensate in both the vertical and horizontal direction
- Vertical H-tree: Removes transistor/wire delay mismatch in vertical direction and reduces total prog delay needed
- Horizontal compensation still suffers from transistor/wire delay mismatch

See AM003: *"AMD Versal™ Adaptive SoC Clocking Resources Architecture"* for details



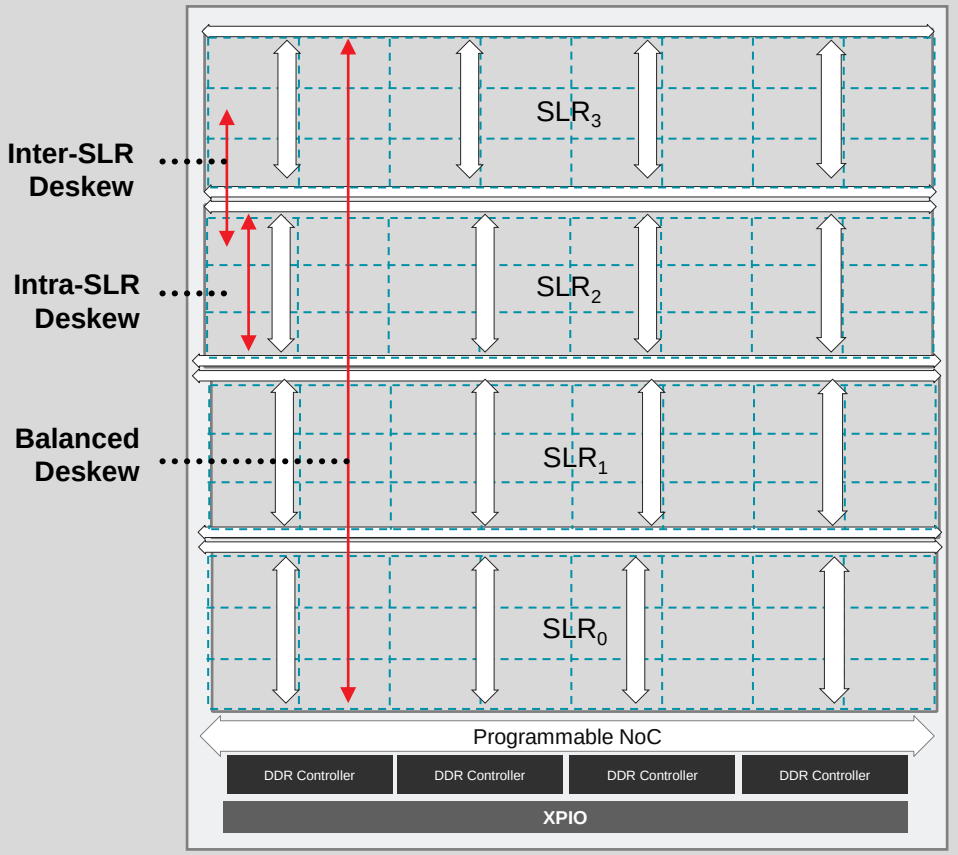
Selecting the Optimal V-Tree Clock Configuration

V-trees are optimized for a specific goal

V-Tree Type	Optimization Criteria
Balanced	Minimize skew across SLRs (default)
Inter-SLR	Maximize SLR crossing performance
Intra-SLR	Minimize skew within an SLR

- Balanced V-tree provides the best performance for the majority of designs
- Inter-SLR provides best SLR crossing performance for USER_SLL_REG FD-FD paths
- Intra-SLR minimizes skew within SLR clock region rows

- Can select *globally* or *on a per clock net basis*:
  - Globally: `place_design -clock_vtree_type < interSLR | intraSLR | balanced >`
  - Per clock: `set_property USER_CLOCK_VTREE_TYPE < interSLR | intraSLR | balanced > [get_nets …]`



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Calibrated Deskew (CDS) Feature for AMD Versal™ SSIT Devices

Large AMD Versal™ devices struggles with metal vs transistor delay mismatch even after basic deskew mechanism

AMD Versal SSIT devices use a calibrated skew compensation system to minimize both local and global skew

- Global clock calibration executed while the part is powered up

Calibrated Deskew

- Adaptive mesh network for clock distribution
- Occurs in vertical and horizontal direction and across SLRs

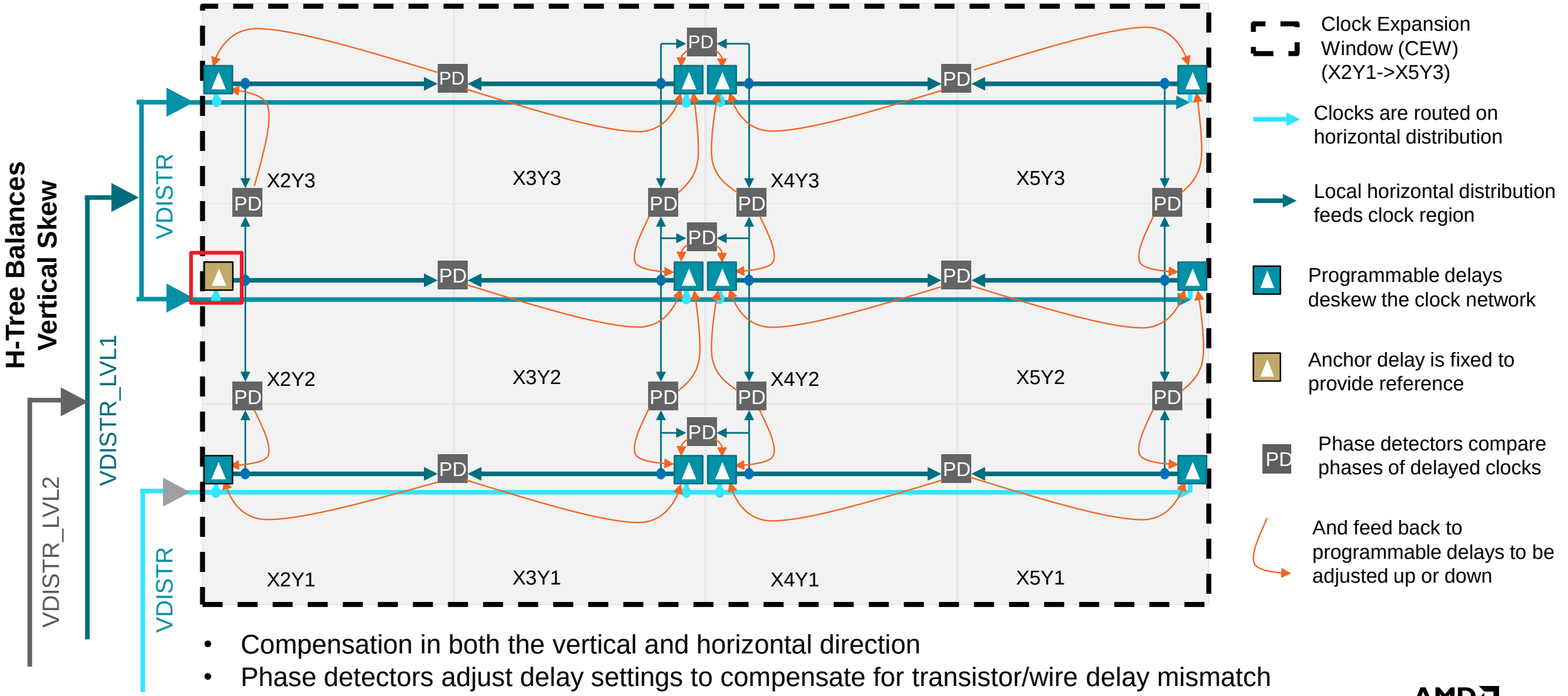
How Calibrated Deskew Works?

- Phase detectors compare clock phases
- Programmable delays adjusted based on feedback
- Operates vertically and horizontally
- Enable calibrated deskew using `set_property GCLK_DESKEW CALIBRATED [get_nets <clock_net>]`

Benefits

- Minimizes skew across clock networks
- Optimizes intra-SLR paths and inter-SLR crossings
- Improves QoR over V-tree topology

Calibrated Deskew: Visual Representation



- Compensation in both the vertical and horizontal direction
- Phase detectors adjust delay settings to compensate for transistor/wire delay mismatch
- Adaptive deskew mesh network then converges on an optimal solution in real time

When to Use & When to Avoid Calibrated Deskew

GENERAL GUIDANCE

Calibrated deskew is *not enabled* by default

Always implement the design, check timing report, and look for the critical paths and SLR performance

A powerful feature, but if used incorrectly can be ineffective or degrade performance

Use Calibrated Deskew

- If the critical paths show large clock skew
- If the SLR crossing performance needs to be maximized
- If an MBUFG is used for sync CDC
- For large SSIT devices
- For designs that have:
  - Clock running over 350 MHz
  - Many clock loads spanning all SLRs

Avoid Using Calibrated Deskew

- If parallel BUFGs are used for sync CDC
- If the BUFG_FABRIC drives the high fanout control signals
- If fabric to XPIO paths are used (I/O paths)
- For GT column V-trees and VNOC far left & far right columns
- For smaller size devices
- For designs that have inter-clock timing paths

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Summary

01 AMD Versal™ architecture employs both vertical and horizontal clock skew compensation for clock routing

02 Basic deskew feature in AMD Versal™ devices supports three user selectable v-tree clock configurations types:

- Balanced – Minimize skew across SLRs (default)
- Inter-SLR – Maximize SLR crossing performance
- Intra-SLR – Minimize skew within SLRs

03 Calibrated deskew mechanism minimizes both local and global skew, improving F_{MAX} for intra-SLR and inter-SLR paths in Versal SSIT Devices

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