
TOOLS, IP, AND SOLUTIONS FOR COST-OPTIMIZED FPGAS
AMD
together we advance_

INDUSTRY CHALLENGES WITH FRAGMENTED TOOL FLOWS

Time to Design Closure

- Meeting F_{MAX} target can be unpredictable
- Varying levels of tool optimization features
- Implementation flows spanning multiple tools can cause delays

Developer Efficiency

- Fragmented flow left for user to maintain
- Limited automation across entire flow

Learning Curve

- New training per tool
- Varying levels of learning resources
- Multiple sources of technical support

AMD VIVADO™ DESIGN SUITE FOR STREAMLINED DESIGN CYCLES

Design Entry

- Import RTL and/or GUI-based IP Integration
- High-level design w/structured C++ or MATLAB®

Simulation & Verification

- Behavioral (RTL) or gate-level (post-synthesis)
- AMD Vivado™ simulator (no-cost) & 3rd party simulator support

Implementation

- Native RTL synthesis integrated with P&R
- Guided flows and ML-based algorithms for QoR

Debug

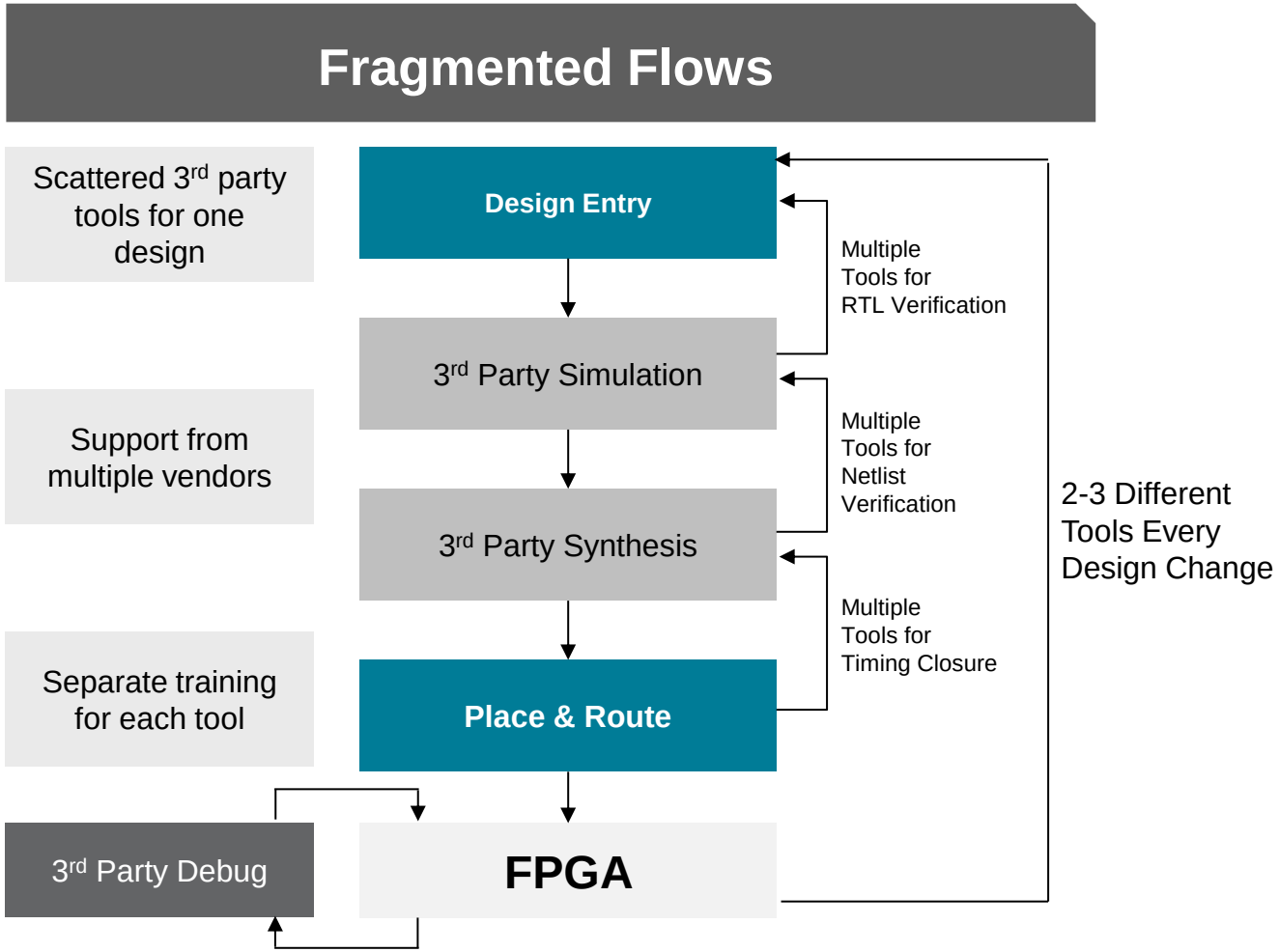
- Integrated Logic Analyzer (ILA) IP (ChipScope)
- Integrated with P&R for fast iterations

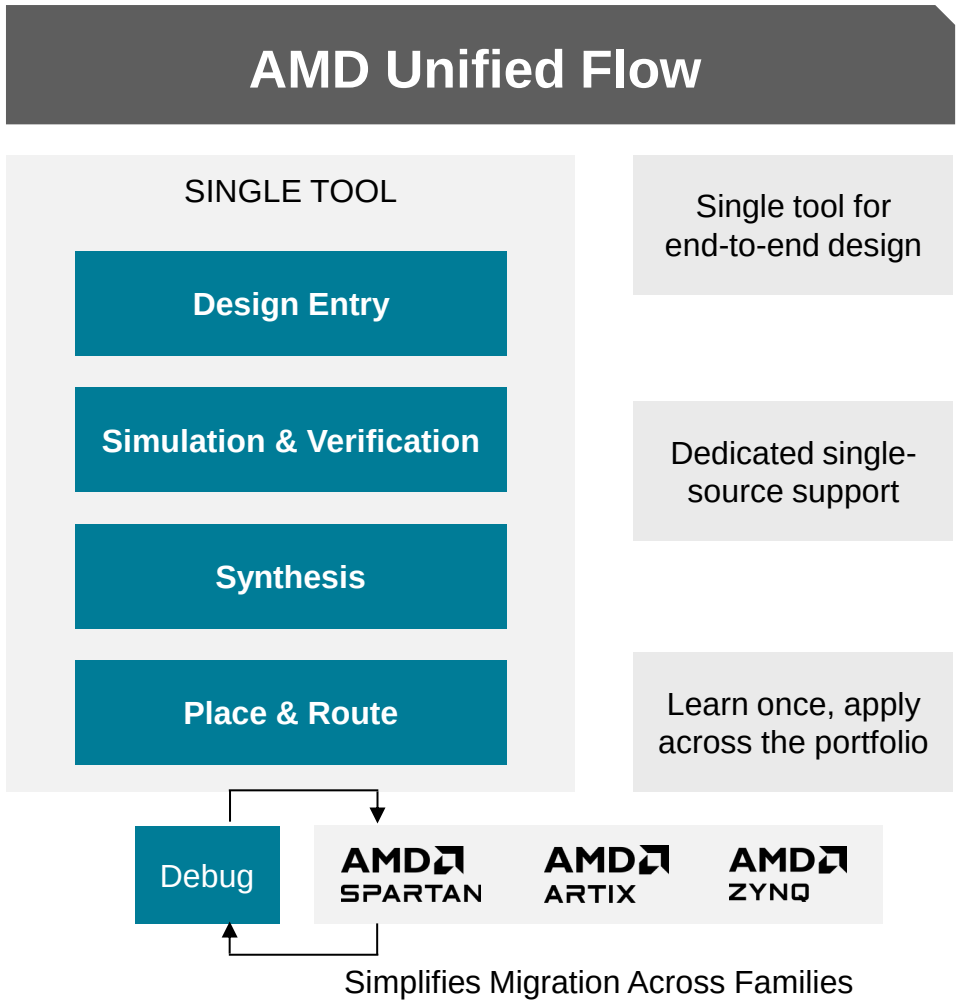
AMD Vivado

AMD SPARTAN | AMD ARTIX | AMD ZYNQ

Free Standard Edition

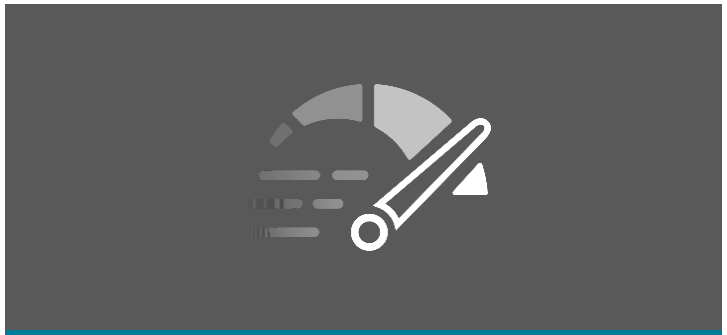
BENEFITS OF A UNIFIED VS. FRAGMENTED FLOW





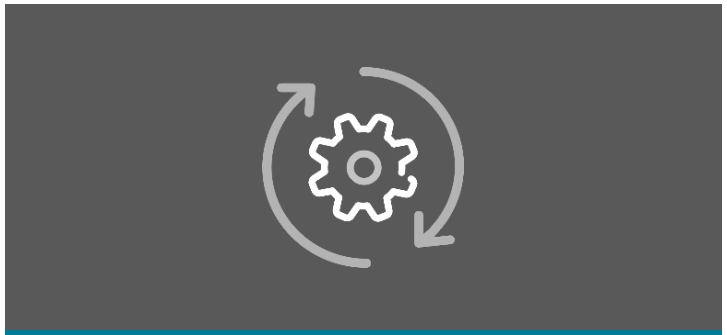
AMD VIVADO™ ADVANCED FEATURES TO ACCELERATE PRODUCTIVITY

Integrated Flow Across Cost-Optimized Portfolio



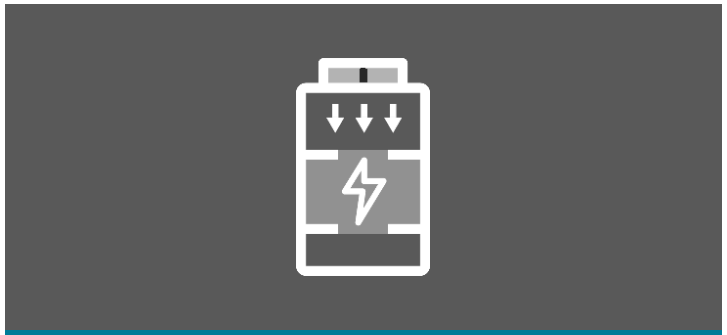
Meet Target F_{MAX}

- Tool recommendations for timing closure
- ML-based implementation algorithms



Fast Design Iterations

- Incremental compile flows
- Ease-of-use features at every stage of the flow



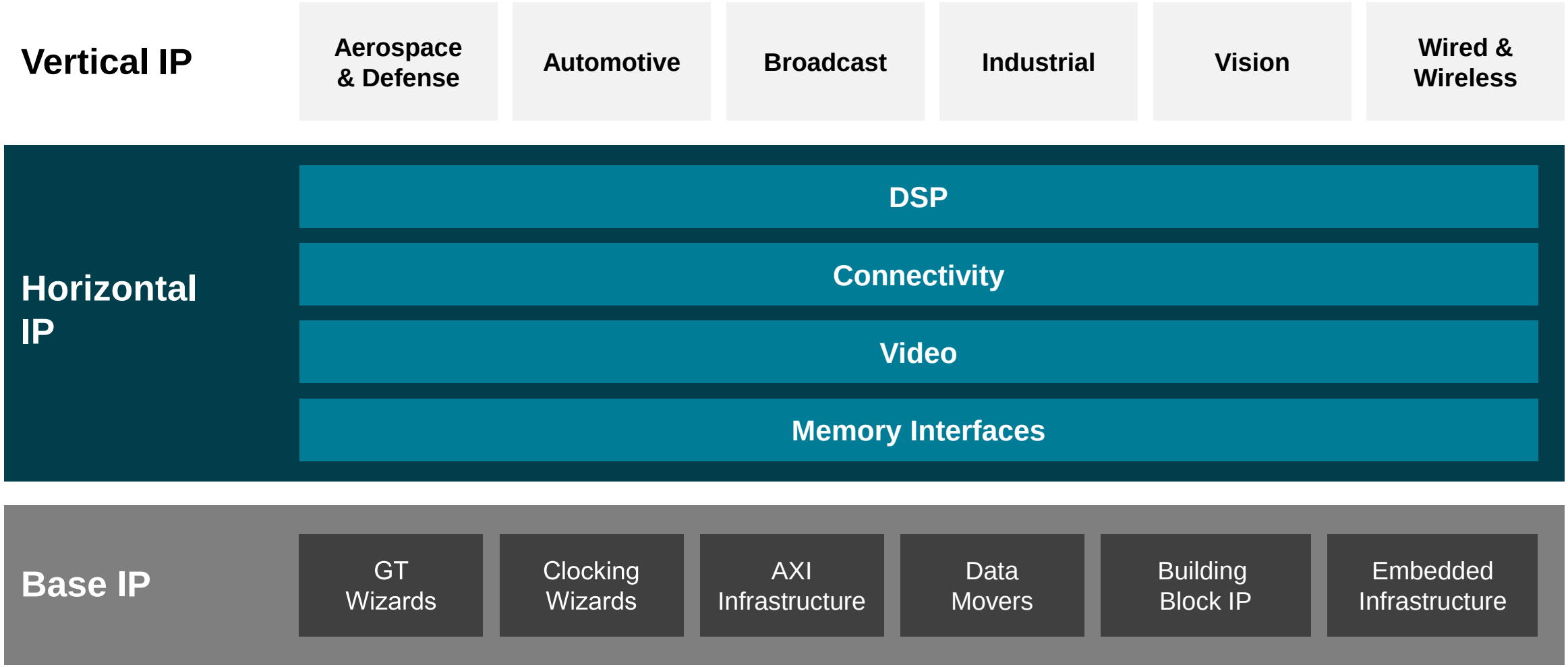
Accurate Power Estimation

- Holistic system-level power budgeting & thermal design
- Informed device selection

STARTS WITH DESIGN ENTRY

LARGE IP CATALOG TO ACCELERATE THE DESIGN PHASE

OVER 500 CORES



HIGH-LEVEL SYNTHESIS WITH C/C++ FOR HIGHER LEVELS OF ABSTRACTION

- Design in structured C/C++ → synthesizable libraries → RTL for implementation in hardware
- AMD Vivado™ RTL synthesis under the hood
- Ideal for algorithmic development or production IP with moderate QoR requirements

DESIGNING WITH MATHWORKS MATLAB OR SIMULINK

- Design with MATLAB® or Simulink® → synthesizable libraries → RTL for implementation in hardware
- AMD Vivado™ RTL synthesis under the hood
- Ideal for fast Proof of Concepts for algorithms

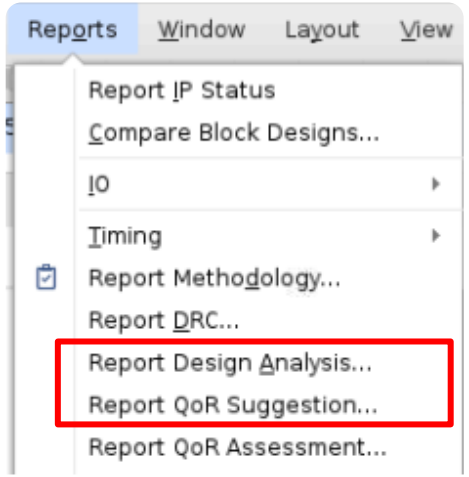
MEET TARGET F_{MAX}

DESIGN ANALYSIS & STRATEGY RECOMMENDATIONS TO MEET TARGET F_{MAX}

RQA

Report QoR Assessment

- Scores the design, predicts likelihood of meeting F_{MAX}
- Flags issues that impact performance
- Done post-synthesis or at any stage of implementation flow



Implementation **fail**

Timing **fail**

Timing **difficult**

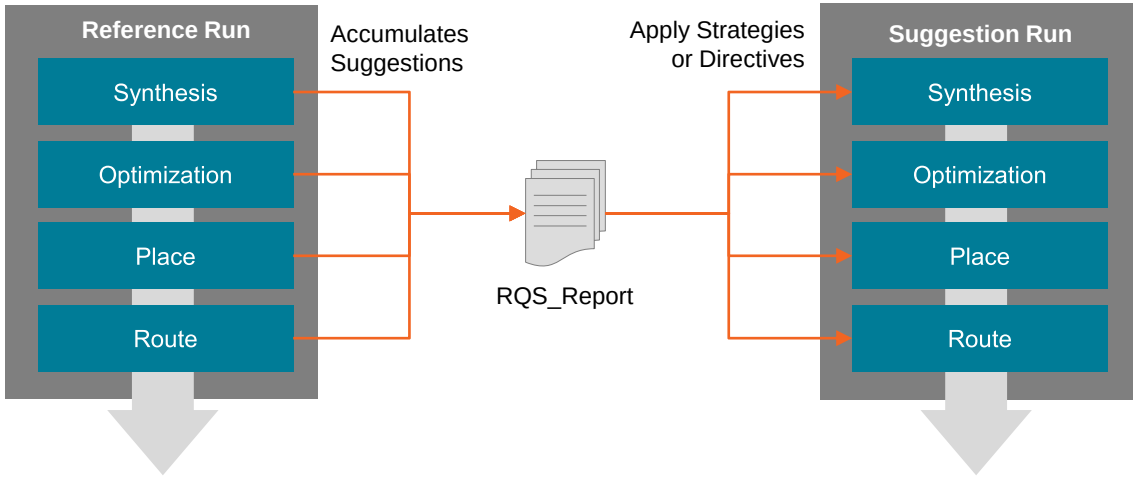
Timing **fair**

Timing **easy** to meet

RQS

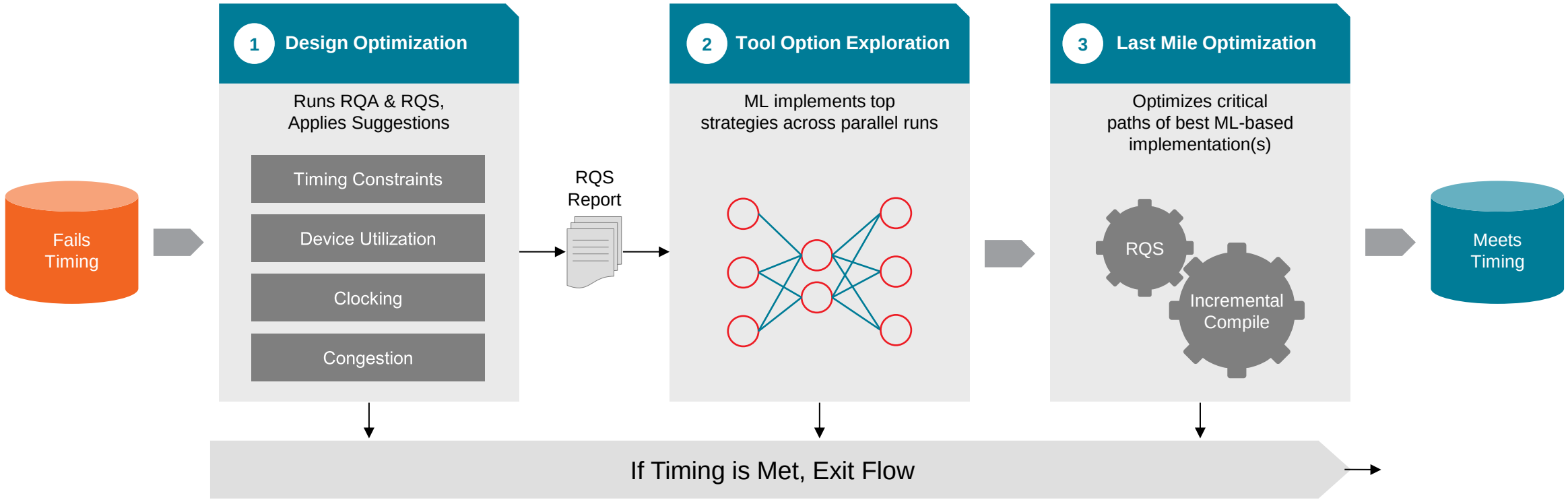
Report QoR Suggestions

- Suggests compile strategies or directives to improve F_{MAX}
- Analyzes design at different stages of implementation flow
- RQS improves RQA score



INTELLIGENT DESIGN RUNS: ML-BASED IMPLEMENTATION ALGORITHMS

- The **Intelligent Design Run (IDR)** flow provides automated timing closure, leveraging RQA and RQS
- Uses machine learning to estimate delays & congestion, then recommends constraints to improve timing
- ML strategies implement tool options and directives across multiple runs

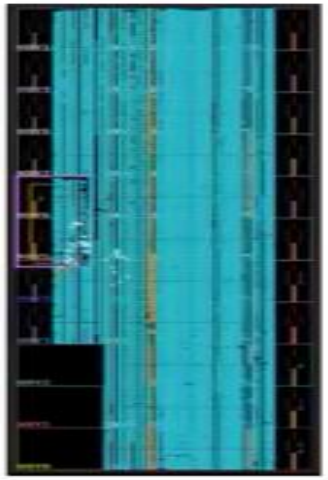


FAST DESIGN ITERATION

ABSTRACT SHELL FOR OPTIMAL COMPILE TIME

- Fast place-and-route compile times on incremental design changes
- Leverages Dynamic Function eXchange (‘partial reconfiguration’) technology
- User designates portion of design (“Reconfigurable Partition”) to be modified, e.g., frequently updated IP
- AMD Vivado™ tools will only recompile the module and minimal boundary interface → **Abstract Shell**
- Ideal for team-based design, the need (e.g., distribute partitions among designers)

First Implementation
Full



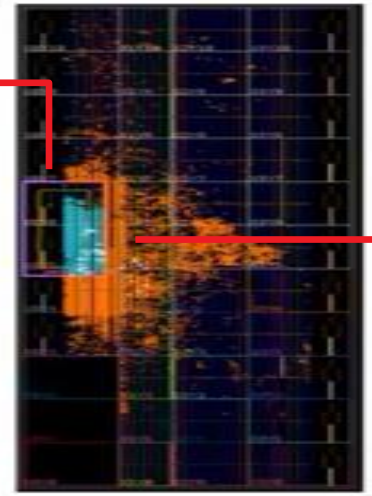
Designate Reconfigurable Partition

Designate Reconfigurable Partition

Design Change *(within Partition)*

Second Implementation
Re-Compiles Partition and “Abstract Shell” Only

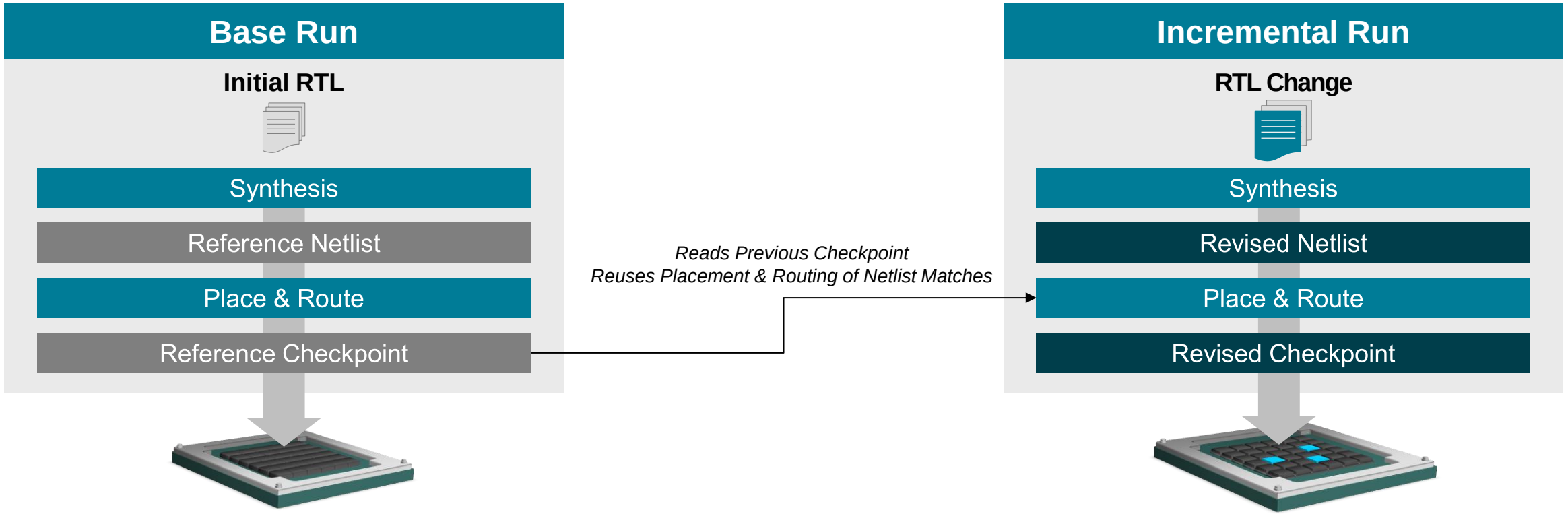
Reconfigurable Partition



Abstract Shell *(Minimal interface around RP)*

INCREMENTAL COMPILE

- Speeds up compile time by reusing synthesis and P&R data from base run
- Good for small changes, e.g., < 5% of design (e.g., minor updates, RTL bug fixes, adding debug cores)
- Helps ensure timing closure of previous run is maintained



ACCURATE POWER ESTIMATES

POWER DESIGN MANAGER

Early Power Estimates

- Allows for optimal device selection to meet thermal & power req's
- Estimates power, explore tradeoffs before design and implementation

Accurate Power Estimates

- Up-to-date power characterization models
- IP wizards for granular, accurate power for hard and soft IP

Explore Power Management Techniques

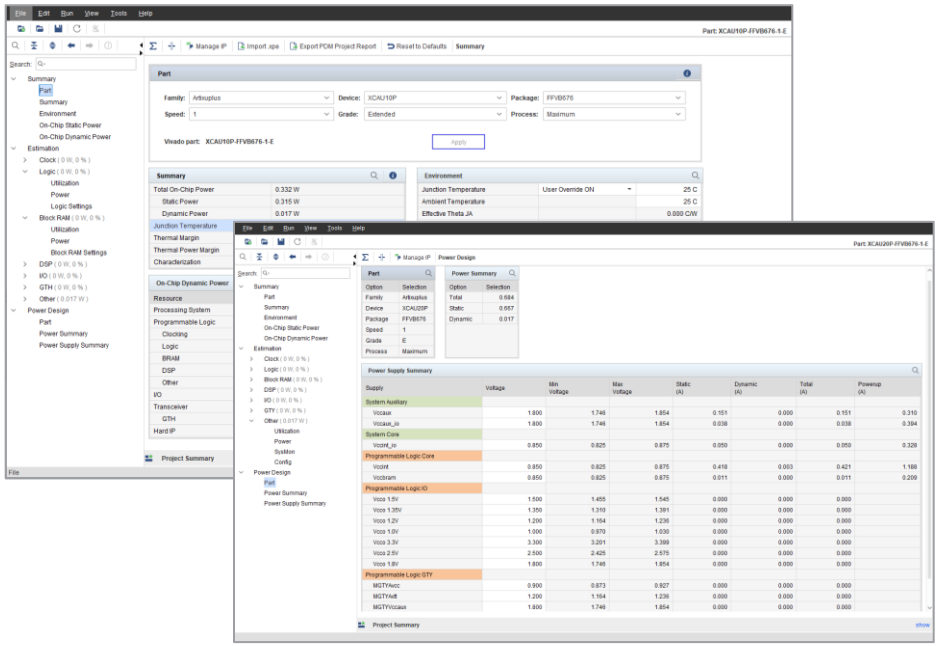
- Clock Gating, Logic Gating
- Frequency Scaling

XPE (Xilinx Power Estimator) vs. PDM Support

- 7 Series devices supported by XPE only (no PDM)
- XPE still supported for AMD Artix UltraScale+ for Zynq UltraScale+
- PDM Supports AMD UltraScale+ devices or later

AMD
Power Design Manager

Stand-Alone Tool, License-Free
does not require any other software



GETTING STARTED AND KEY TAKE-AWAYS

AVAILABLE AMD VIVADO™ RESOURCES

Collateral & Docs

- UltraFast™ Methodology Guide
- UltraFast Quick Reference Guide
- Timing Closure Quick Reference Guide
- Intelligent Design Runs White Paper
- Abstract Shell White Paper
- Abstract Shell Case Study
- And more . . .

Videos & Tutorials

- Design Flow Tutorial (UG888)
- Logic Simulation Tutorial (UG937)
- UltraFast Methodology Checklist
- Vivado IP Flow
- Designing with IP Integrator
- Introduction to Clock Constraints
- Abstract Shell
- Logic Debug in Vivado
- Intro to Power Design Manager
- And more …

On-Demand Courses

- Designing with Vivado Part 1
- Designing with Vivado Part 2
- Designing with Vivado Part 3
- Designing with Vivado Part 4
- Design Closure Techniques
- Designing with IP Integrator
- Dynamic Function Exchange

Support Forums

- Installation & Licensing
- Design Entry & IP Flows
- Simulation & Verification
- Synthesis
- Implementation
- Timing & Constraints
- Debug & Tools
- Advanced Flows

Live Training From Partners

Coaching Service Partners

Download Vivado™ Design Suite at www.amd.com/vivado

Faster Development and Trusted Results

Integrated Tool Flow Across Cost-Optimized Portfolio

AMD SPARTAN | AMD ARTIX | AMD ZYNQ

Trusted QoR Results

- Meet F_{MAX} quickly with advanced flows
- Fast iterations for timing closure
- ML algorithms for advanced techniques

Developer Efficiency

- 100+ Soft IPs to jumpstart design
- High-levels of abstraction
- Fast compile times and iterations
- Accurate and early power estimation

Rapid Learning Curve

- Library of collateral, videos, & courses
- Example designs and trainings
- Single source for technical support

DISCLAIMER AND ATTRIBUTIONS

DISCLAIMER

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