# Conquer Complexity with AMD Spartan™ UltraScale+™ FPGAs

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**October 23, 2024**

AMD
together we advance_

# Agenda

1. AMD Cost-Optimized Portfolio Overview
2. AMD Spartan™ UltraScale+™ FPGA Family
3. Simplify Your Design with Vivado
4. Design Once with Long Lifecycle
5. Application Examples
6. Timelines & Next Steps

# AMD Cost-Optimized Portfolio Applications

## 4K Broadcast


## 3D Immersive Audio

## AI-Enabled ADAS

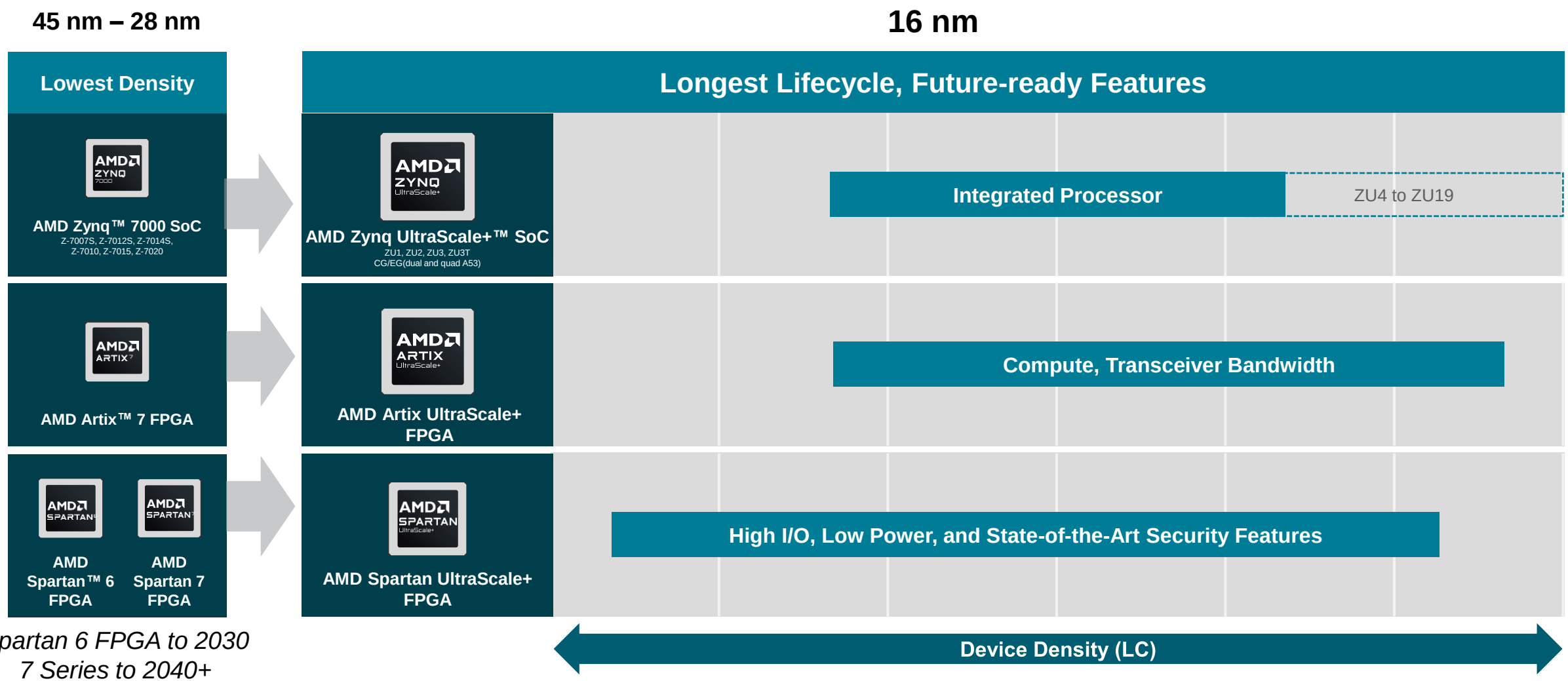
## LiDAR Platforms

## Medical Imaging

## Robotics


## Video Collaboration

# BROAD AMD PORTFOLIO TO ADDRESS DIVERSE NEEDS




*Spartan 6 FPGA to 2030*
*7 Series to 2040+*
*UltraScale+ to 2045+*

# AMD Spartan™ Ultrascale+™ FPGA

# AMD SPARTAN™ ULTRASCALE+™ FPGA

## High I/O, Low Power & State-of-the-Art Security Features

- Industry's highest I/O to logic cell ratio ≤28nm, enabling cost reduction for I/O-intensive applications
- Up to 30% power reduction[1] with 16 nm FinFET & power efficiency via hardened DDR and PCIe®
- Most security features in AMD Cost-Optimized Portfolio, NIST approved Post-Quantum Cryptography


## Accelerate Time to Market with Proven Design Tools

- Tools leadership since 2012 with AMD Vivado™ Design Suite
- One tool covering simulation to verification for entire FPGA portfolio[2]

## Design Once with a Trusted Supplier

- Nearly 40 years in the FPGA market & billions of devices shipped
- >15 years product lifecycle and in-field upgradeability for maximum design longevity

See Endnotes SUS-001, SUS-002, SUS-003, SUS-011
[1]AMD Projection
[2]Starting at 28 nm

# AMD SPARTAN™ ULTRASCALE+™ FPGA: OPTIMIZED FOR THE EDGE

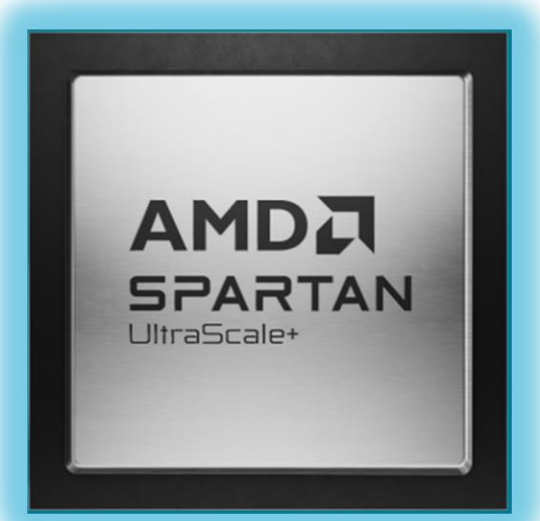
## Proven 16 nm Technology

**Low Power**
- 16 nm FinFET & hard DDR, PCIe®

**Block RAM and UltraRAM**
- Up to 26 Mb of on-chip memory

**Transceivers and PCIe®**
- Up to 8 GTH with 16.3 Gb/s
- PCIe® Gen4 x8

**Digital Signal Processing**
- Up to 384 DSP48E2 blocks
- Floating / fixed point support




## Future-Ready Capabilities

**Flexible I/O Interfaces**
- Up to 572 I/Os, 3.3V support
- 3.2G MIPI D-PHY

**State-of-the-Art Security**
- Post-Quantum Crypto (PQC) ready
- PPK/SPK, TRNG, PUF

**Hard Memory Controller**
- LPDDR4x/5 up to 4266 Mb/s
- First UltraScale+ with LPDDR5

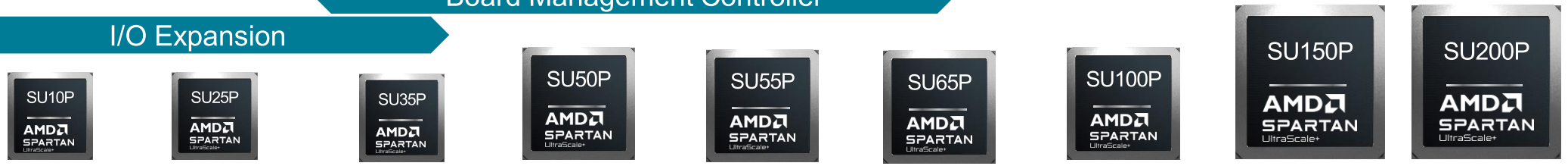
**Small Form Factor**
- CSP and BGA packages
- As small as 10x10 mm

# AMD SPARTAN™ ULTRASCALE+™ FAMILY PRODUCT TABLE

Edge Sensing and Control

Board Management Controller

I/O Expansion

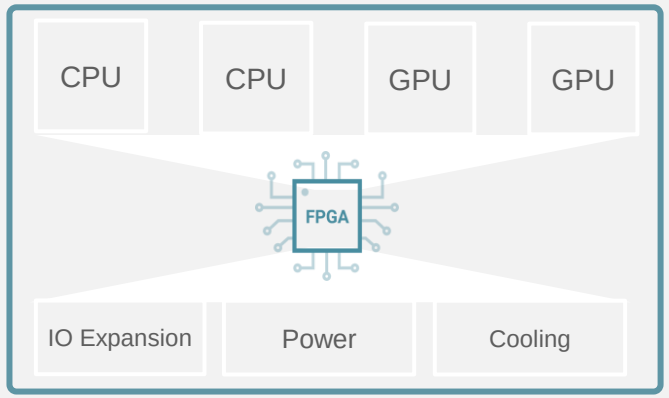



| Device | SU10P | SU25P | SU35P | SU50P | SU55P | SU65P | SU100P | SU150P | SU200P |
|---|---|---|---|---|---|---|---|---|---|
| LUTs (K) | 5 | 10 | 16 | 24 | 24 | 30 | 46 | 63 | 100 |
| Logic Cells (K) | 11 | 22 | 36 | 52 | 52 | 65 | 100 | 137 | 218 |
| Max. Total I/O | 304 | 304 | 304 | 388 | 352 | 478 | 478 | 572 | 572 |
| I/O to LC Ratio | 27 | 13 | 8 | 7 | 6 | 7 | 4 | 4 | 2 |
| Total On-chip Memory (Mb) | 1.77 | 1.84 | 1.93 | 2.91 | 2.91 | 4.31 | 5.89 | 11.65 | 26.79 |
| Hard IP (DDRMC / PCIe®) | - | - | - | - | 2 / - | 2 / 1 | 2 / 1 | 2 / 2 | 2 / 2 |
| # GTH Transceiver | - | - | - | - | - | 4 | 4 | 8 | 8 |
| Smallest Package | 10x10 | 10x10 | 10x10 | 12x12 | 12x12 | 12x12 | 12x12 | 23x23 | 23x23 |

# DESIGNED TO FACILITATE EFFECTIVE INTERFACING

## Highest I/O to Logic Cell Ratio

I/O Expansion & Baseboard Management Controller (BMC)



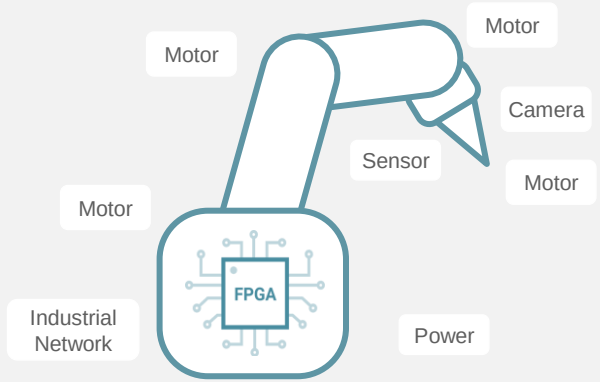

Datacenter BMC

2.4X I/O to LC ratio vs. AMD Artix™ 7 FPGA

3.5X I/O to LC ratio vs. AMD Spartan™ 7 FPGA

## Increased Connectivity and Flexibility

Any-to-Any Connectivity for Edge Sensing and Control




Industrial Robotics

2.5X Transceiver Bandwidth vs. AMD Artix 7 FPGA

4X MIPI Bandwidth vs. AMD Spartan 7 / Artix 7 FPGAs

**Industry's highest I/O to Logic Cell Ratio for 28nm and newer FPGAs**

See Endnotes SUS-001, SUS-011

# AMD SPARTAN™ ULTRASCALE+™ FPGA INTERFACES ARE THE FASTEST IN COP

| Feature | AMD Spartan™ 6 FPGA | Spartan 7 FPGA | AMD Artix™ 7 FPGA | Artix UltraScale+™ FPGA | Spartan UltraScale+ FPGA |
|---|---|---|---|---|---|
| **MIPI (Mbps)** | 800 | 800 | 800 | 1500 | 3200 |
| **MIPI DPHY** | Requires external resistor network | | | Native | Native |
| **DDR*** | DDR2-800 (Hard MC) | DDR3-800 (Soft MC) | DDR3-800 (Soft MC) | DDR4-1866 (Soft MC) | DDR4-2400 (Soft MC) and LPDDR4x/5-4266 (Hard MC) |
| **Transceiver Speed (Gbps)** | 3.2 | - | 6.6 | 16.3 | 16.3 |
| **PCI Express®** | Gen1 x1 (Soft IP with external PHY) | Gen1 x1 (Soft IP with external PHY) | Gen2 x4 (Hard IP) | Gen4 x8 (Hard IP) | Gen4 x8 (Hard IP) |

* DDR and LVDS are based on -2 speed grades

# COMPREHENSIVE I/O CAPABILITIES

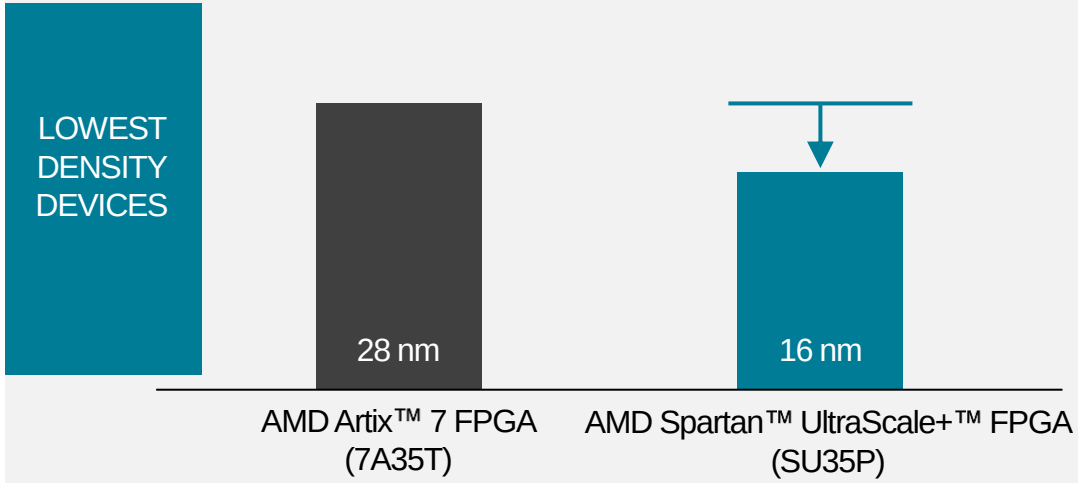
| | HDIO | HPIO | XPIO | XP5IO |
|---|---|---|---|---|
| **AMD Spartan™ US+ FPGA** | ✓ | ✓ | x | ✓ |
| **AMD UltraScale+™ FPGA** | ✓ | ✓ | x | x |
| **AMD Versal™ Adaptive SoC** | ✓ | x | ✓ | x |
| **Bank Size** | 42/84 pin | 52 pin | 54 pin | 66 pin |
| **Total IO Pin Count** | 100 – 336 | 52 - 104 | 30 – 2064 (SSIT) | 0 - 132 |
| **Voltages** | 1.2v – 3.3v | 1.2v – 1.8v | 0.6v – 1.5v | 0.5v – 1.5v |
| **Max Data Rate*** | 250 Mb/s | 1600 Mb/s | 1800 Mb/s | 1800 Mb/s |
| **Key Features** | Higher Voltage Range | High speed IO features (e.g. Delay, serialization, termination) | High speed IO features (e.g. Delay, serialization, termination) | Highest speed IO features (e.g. Delay, serialization, termination) |

*Non-memory, Non MIPI performance

# LOW POWER: 16 NM FINFET AND HARDENED INTERFACE IP

## UP TO 30% LOWER TOTAL POWER[1] WITH 16 NM FABRIC

Static & Dynamic Power @ 80% Utilization, 200 MHz

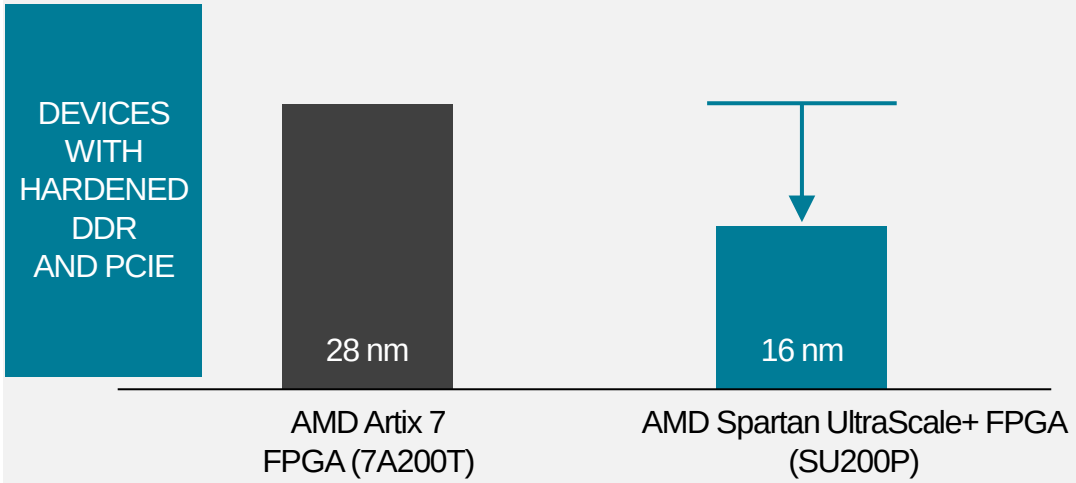



Up to 1.9X Fabric Performance[1]

Up to 1.2X Total I/O

## UP TO 60% LOWER POWER INTERFACING[1]

Total Device Power Normalized to PCIe® and DDR Bandwidth




5X Memory Controller Bandwidth

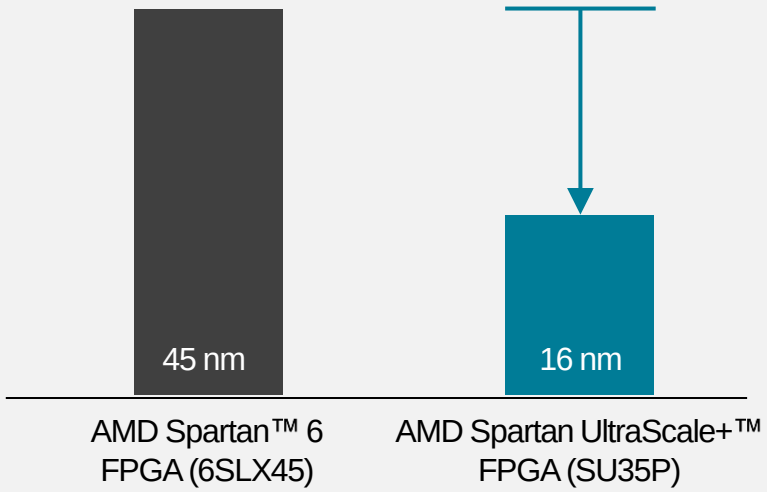
4X PCIe Bandwidth

See Endnotes SUS-003, SUS-004, SUS-005 , SUS-006, SUS-007, SUS-008
1: AMD Projection

# ADVANTAGES FOR EXISTING SPARTAN 6 CUSTOMERS

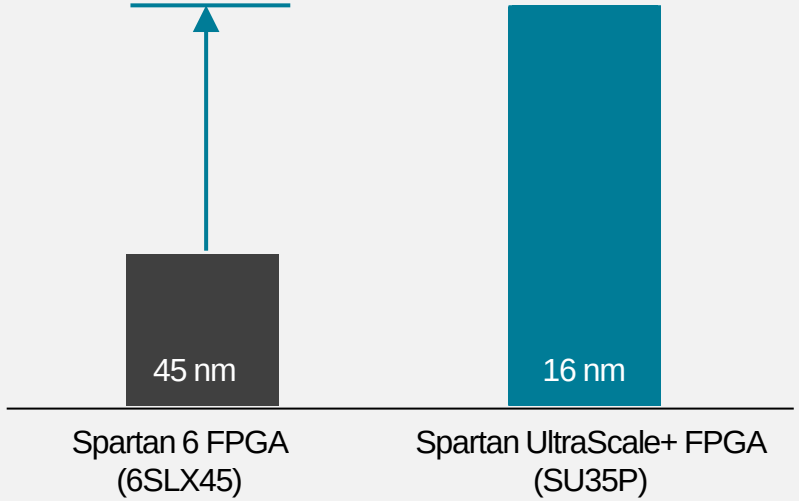
## Up to 60% Lower Total Power[1]

Static & Dynamic Power @ 80% Utilization, 200 MHz, TJ 85 °C




## Up to 2.6X Performance per Watt[1]

Fmax Per Total Power @ 80% Utilization, 200 MHz , TJ 85 °C




See Endnotes SUS-012, SUS-013
1: AMD Projection

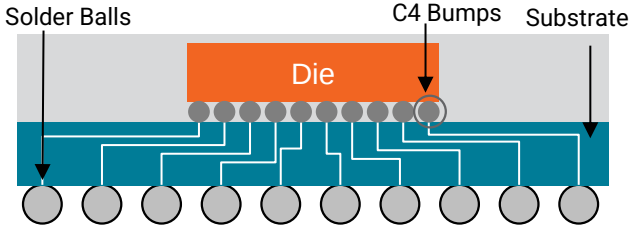
# MINIMIZING FOOTPRINT WITH ADVANCED PACKAGING

Small Form Factor
Up to 70% less PCB area

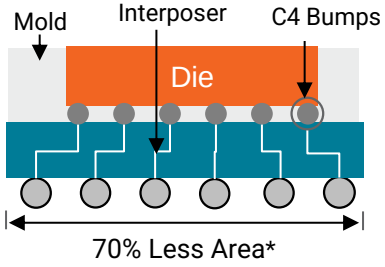
Improved Thermal Dissipation
Low power and simplified mechanicals

| Device | Chip Scale Package | | | Integrated Fan Out Package | | |
|---|---|---|---|---|---|---|
| Size (mm) | 9x9 | 10x10 | 12x12 | 11.5x9.5 | 9.5x15 | 9.5x16 |
| AU7P | ✓ | | | | | |
| AU10P | | | | ✓ | | |
| AU15P | | | | ✓ | | |
| SU10P | | ✓ | ✓ | | | |
| SU25P | | ✓ | ✓ | | | |
| SU35P | | ✓ | ✓ | | | |
| ZU1 | | | | | ✓ | |
| ZU2 | | | | | | ✓ |
| ZU3 | | | | | | ✓ |

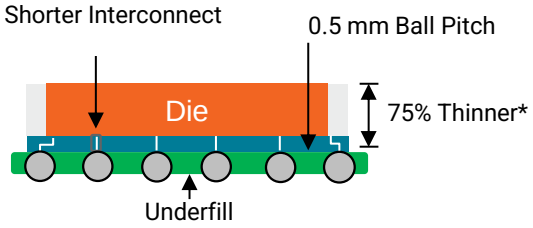
## Standard BGA Package




## Chip Scale Package




## InFO Package




See Endnotes AUS-007, ZUS-007

# OPTIMIZING FOR COST BY SIZING DOWN

## Cost Reduction for I/O Intensive Applications

AMD Spartan™ 7
FPGA Design
210 GPIO


Spartan UltraScale+™
FPGA Design
220 GPIO

## Cost Reduction via Hardened Memory Controllers

AMD Artix™ 7
FPGA Design
50K LC User Logic
+
30K LC Soft DDR
Memory Controller


Spartan UltraScale+
FPGA Design
50K LC User Logic
+
**Hardened LPDDR5**
**Memory Controller**



See Endnotes SUS-009, SUS-010

# STATE-OF-THE-ART SECURITY FEATURES

## Protect Your IP

- PQC with NIST-approved algorithms
- AES-GCM for secure configuration
- PUF for unique device identification and improved physical security

## Prevent Tampering

- Customizable Tamper Responses incl. permanent penalty to protect the device against misuse
- DPA countermeasures for side-channel attacks

## Maximize Uptime

- Enhanced SEU performance for increased reliability
- In-field temperature and voltage monitoring

**AMD Spartan™ UltraScale+™ FPGAs have the most security features in the Cost-Optimized Portfolio**

See Endnotes SUS-002

# MAINTAINING SECURITY PRIOR TO OPERATION

| PASSIVE FEATURES | AMD Spartan™ 6 FPGA | AMD 7 Series FPGAs and Adaptive SoCs | AMD UltraScale+™ FPGAs and Adaptive SoCs | AMD Spartan UltraScale+ FPGA |
|---|---|---|---|---|
| • Confidentiality w/ AES-256 (eFUSE) | ✓ | ✓ | ✓ GCM | ✓ GCM |
| • Secure Configuration of PL – RISC V Root of Trust | ✓ | ✓ | ✓ | ✓ |
| • Hardened Readback Disable | ✓ | ✓ | ✓ | ✓ |
| • Symmetric Key Authentication | | ✓ | ✓ | ✓ |
| • Public Key (Asymmetric) Authentication | | | ✓ | ✓ |
| • DPA Resistant | | | ✓ | ✓ |
| • Black / Obfuscated Key Load | | | | ✓ |
| • Post-Quantum Cryptography (PQC) | | | | ✓ |
| • Primary/Secondary Public Key Cryptography | | | | ✓ |


**Upgraded Pre-configuration Security Features (Before Booting Bitstream)**

# MAINTAINING SECURITY DURING OPERATION

| ACTIVE FEATURES | AMD Spartan™ 6 FPGA | AMD 7 Series FPGAs and Adaptive SoCs | AMD UltraScale+™ FPGAs and Adaptive SoCs | AMD Spartan UltraScale+ FPGA |
|---|---|---|---|---|
| • Single Event Upset (SEU) Checking | ✓ | ✓ | ✓ | ✓ |
| • JTAG Disable/Monitor (BSCAN) | ✓ | ✓ | ✓ | ✓ |
| • Unique Identifier (Device DNA) | ✓ | ✓ | ✓ | ✓ |
| • Unique Identifier (User eFUSE) | | ✓ | ✓ | ✓ |
| • On-chip Temperature/Voltage Monitors | | ✓ | ✓ | ✓ |
| • PROGRAM_B Intercept | | ✓ | ✓ | ✓ |
| • Tamper Event Logging | | | ✓ | ✓ |
| • Permanent JTAG Disable | | | ✓ | ✓ |
| • Permanent Decryptor Disable | | | ✓ | ✓ |
| • Permanent Tamper Penalty | | | ✓ | ✓ |
| • Physical Unclonable Function (PUF) | | | | ✓ |
| • True Random Number Generator (TRNG) | | | | ✓ |

**Upgraded Post-configuration Security Features (After Booting Bitstream)**

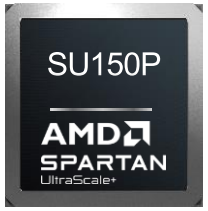
# IMPROVED CONFIGURATION WITH AMD SPARTAN™ ULTRASCALE+™ FPGA

| Design Priority | Configuration Mode | AMD Spartan™ 6 FPGAs | AMD 7 Series FPGAs | AMD Kintex™ & Virtex™ UltraScale™ FPGAs Artix™, Kintex, & Virtex UltraScale+™ FPGAs | Spartan UltraScale+ FPGAs |
|---|---|---|---|---|---|
| Minimum Cost with no flash | Slave Serial (x1) | Yes | Yes | Yes | Yes |
| | Slave SelectMAP (x8, x16, x32) | Yes (x8, x16) | Yes | Yes | Yes |
| | JTAG (x1) | Yes | Yes | Yes | Yes |
| Increasing Performance with serial NOR flash | Master SPI/QSPI (x1, x2, x4) | Yes | Yes | Yes | Yes |
| | Master Dual QSPI (x8) | No | No | Yes | No |
| | Master OSPI (x8) | No | No | No | Yes |

**Increased System Performance with Octal SPI for Flash Configuration**

# AMD SPARTAN™ ULTRASCALE+™ FPGA VS. ARTIX™ ULTRASCALE+ FPGA

AMD Artix™ UltraScale+™ FPGA




| Device | SU10P | SU25P | SU35P | SU50P | SU55P | SU65P | SU100P | SU150P | SU200P |
|---|---|---|---|---|---|---|---|---|---|
| Logic Cells (K) | 11 | 22 | 36 | 52 | 52 | 65 | 100 | 137 | 218 |
| Max. Total I/O | 304 | 304 | 304 | 388 | 352 | 478 | 478 | 572 | 572 |
| I/O to LC Ratio | 27 | 13 | 8 | 7 | 6 | 7 | 4 | 4 | 2 |
| Total On-chip Memory (Mb) | 1.77 | 1.84 | 1.93 | 2.91 | 2.91 | 4.31 | 5.89 | 11.65 | 26.79 |
| Hard IP (DDRMC / PCIe®) | - | - | - | - | 2 / - | 2 / 1 | 2 / 1 | 2 / 2 | 2 / 2 |
| # GTH Transceiver | - | - | - | - | - | 4 | 4 | 8 | 8 |
| Smallest Package | 10x10 | 10x10 | 10x10 | 12x12 | 12x12 | 12x12 | 12x12 | 23x23 | 23x23 |

# AMD SPARTAN™ ULTRASCALE+™ FPGA VS. ARTIX™ ULTRASCALE+ FPGA

AMD SPARTAN UltraScale+

Lower Densities

| Overlapping Logic Density | | | |
|---|---|---|---|
| 60-80K LC | 100K LC | 150K LC | 200K LC |
| SU65P | SU100P | SU150P | SU200P |
| Hard Memory Controller LPDDR4x/5 | | | |
| Security Upgrades | | | |
| 1x PCIe® Gen4x4 | | 2x PCIe® Gen4x4 or 1x Gen4x8 | |
| 3.2G MIPI | | | |
| Higher 3.3V to Logic Cell Ratio | | | |
| AU7P | AU10P | AU15P | AU20P |
| | > 8 GTH/GTY Transceivers | | |
| 9x9mm Pkg | InFO for Best Thermal Dissipation | | |
| 1x PCIe® Gen3x4 | 1x PCIe® Gen4x8 | | 1x PCIe® Gen3x8 |
| Higher DSP to Logic Cell Ratio | | | |

AMD ARTIX UltraScale+

*Higher Densities*

# LEADERSHIP IN TOOLS WITH AMD VIVADO™ Design TOOLS

# ACCELERATE TTM WITH PROVEN VIVADO™ DESIGN TOOLS

## Industry Challenges

### Learning Curve

### Developer Efficiency

### Trusted Results

## AMD Approach

- Single tool supporting entire portfolio[1]
- >100 Soft IPs in catalog
- Example designs and trainings

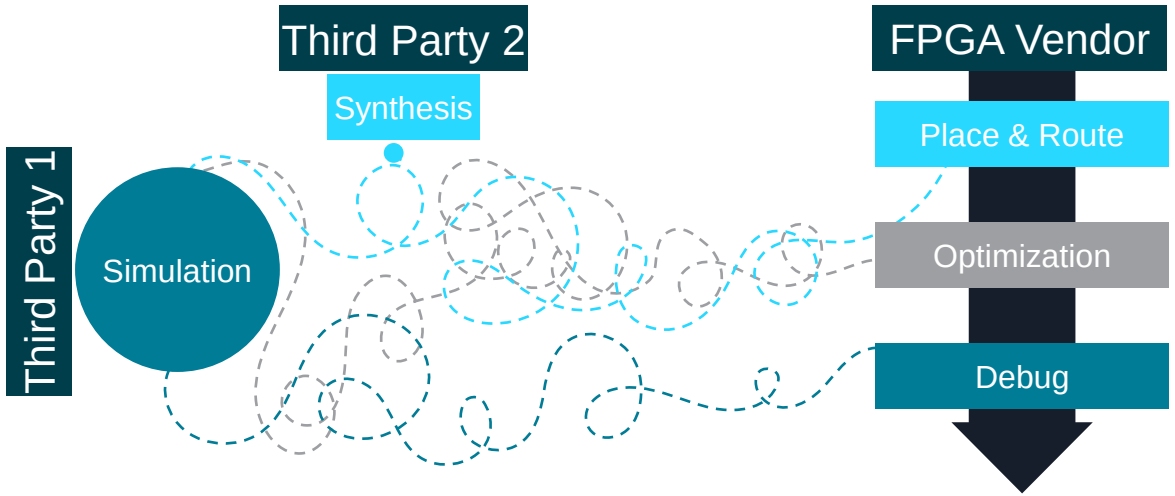
- Single tool for the entire design cycle
- Fast design iterations
- Worldwide technical support

- Proven performance over PVT
- Advanced design analysis
- Functional safety certified

1. Starting at 28 nm

# ONE TOOL: LESS COMPLEXITY FROM SIMULATION TO DEBUG

## STATUS QUO - FRAGMENTED FLOW

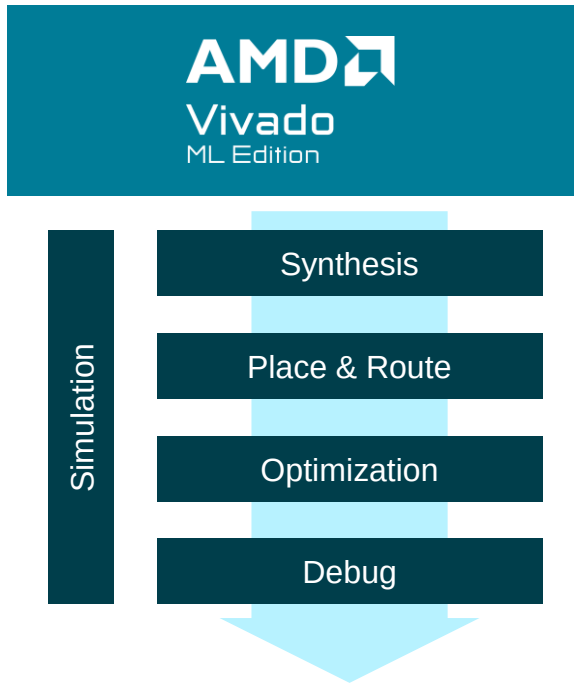



Scattered 3rd party tools for one design

Requires support from multiple vendors

Each tool, a separate training

## AMD APPROACH - UNIFIED FLOW




Single tool for end-to-end design

Dedicated single-source support

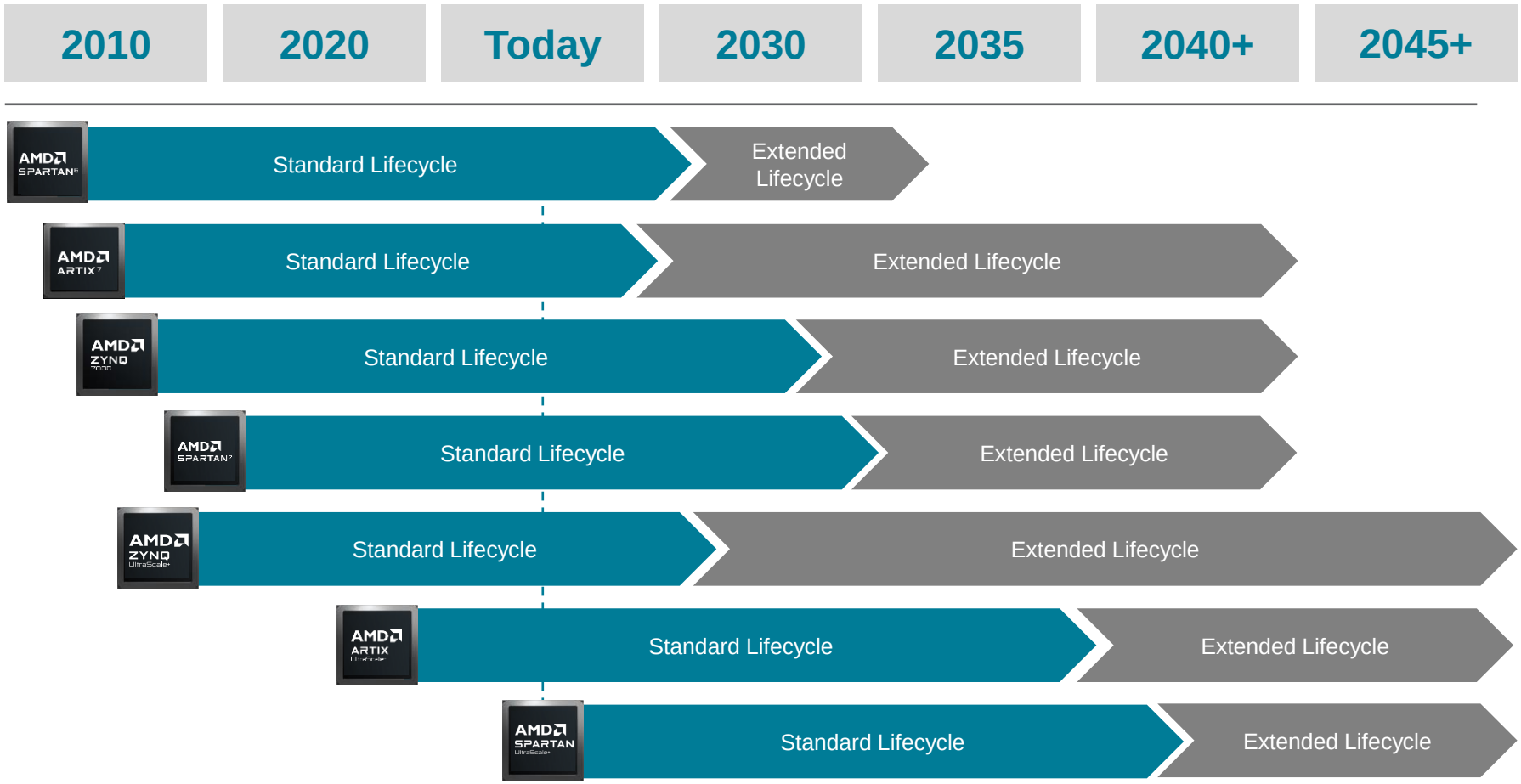
Learn once, apply many

# TRUSTED COP FPGA PROVIDER WITH PROVEN PRODUCT LIFECYCLES

# LONG-TERM INVESTMENT IN COST-OPTIMIZED PORTFOLIO

**Worldwide sales from AMD and authorized distributors**

**Over 15 years of life-time FPGA/ adaptive SoC support**




Roadmap subject to change

# APPLICATION EXAMPLES

# AMD SPARTAN™ ULTRASCALE+™ FPGA APPLICATION EXAMPLES

## Industrial

- Factory Automation, Robotics
- IIoT Gateways & Edge Appliances
- Smart City, Smart Grid
- HMI and Machine Vision

## Medical

- Smart Patient Monitor
- Ultrasound, CT/MRI Scan
- Multi-Stream Endoscopy
- Robot-Assisted Surgery

## Comms

- 4G and 5G Wireless Infrastructure
- Board Controller
- Access Network and Connectivity

## Data Center

- Board Management Controller
- Compute Acceleration
- Network Acceleration
- Hyperscale Storage

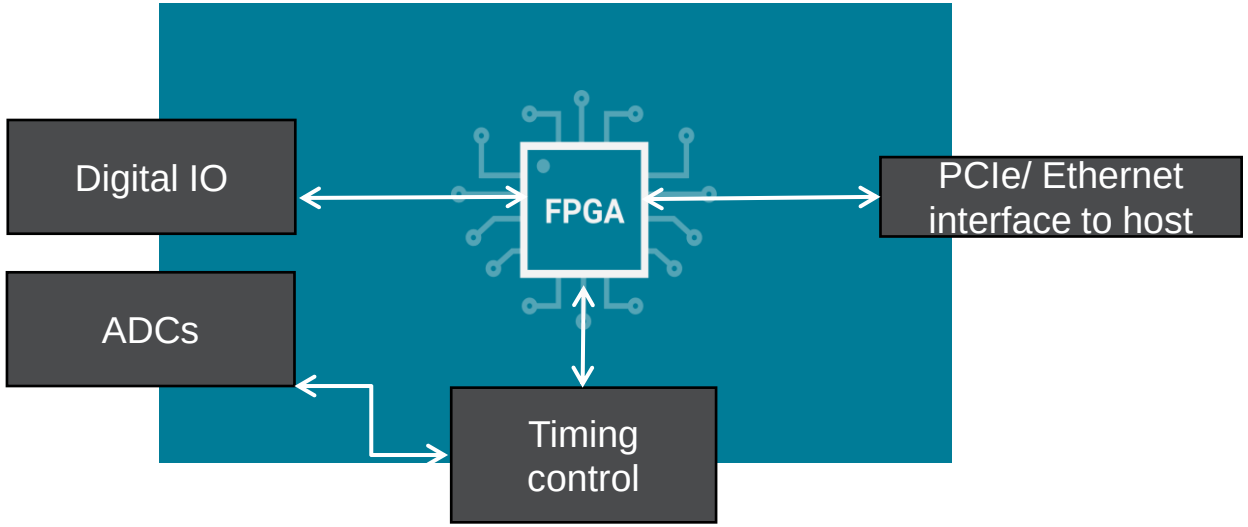
## AV and Broadcast

- Professional AV (Streaming, LED Walls, KVM, and Pro Audio)
- Broadcast (Switchers/Routers, Video Processing, Cameras)

## Test and Measurement

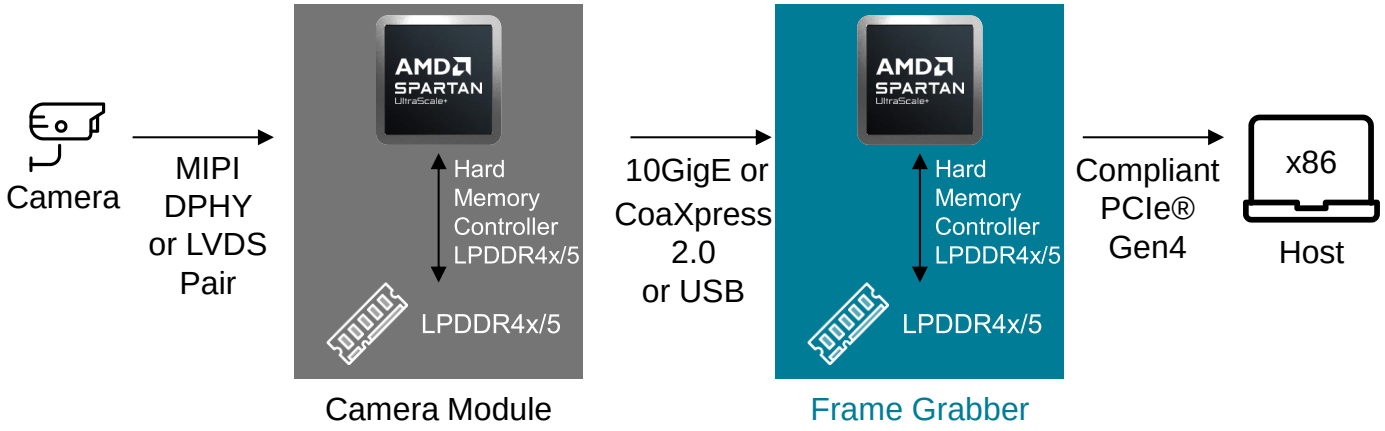
- Semiconductor ATE
- T&M Instrumentation
- Wired & Wireless Testers

# VERSATILE DATA ACQUISITION AND EDGE PROCESSING



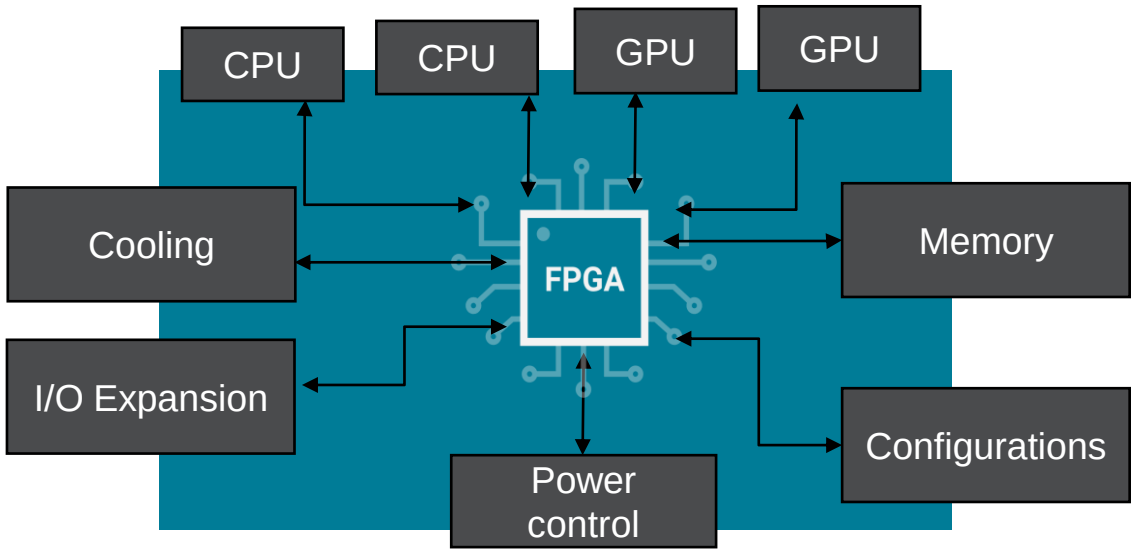

| Data Acquisition Application Requirements | Spartan™ UltraScale+™ FPGA Capabilities |
|---|---|
| Parallelization and independent real-time monitoring for sensor aggregation | PL Architecture with up to 572 flexible I/Os supporting LVDS for ADC interface. |
| Efficient processing at the edge | Combination of 26.79Mb on-chip memory and DSP slices for FFT |
| Interface to the host processing system | Rich AMD IP portfolio including PCIe and Ethernet scalable networking |
| Maintain low power profile and protect data | Its low-power consumption, and advanced security features |

# MACHINE VISION AND VIDEO CAPTURE CARDS




| Machine Vision Application Requirements | Spartan™ UltraScale+™ FPGA Capabilities |
|---|---|
| High-performance I/O for >20 MP image sensor | HPIO, XP5IO and 3.3V I/O with SLVS-EC high-speed sensor support (40G bandwidth), LVDS, and 3.2G MIPI |
| Real-time transfer and high-efficiency storage | PCIe® Gen4 and hard memory controllers LPDDR4x/5 to transfer and store high-quality baseband video. |
| Standards for 10GigE Vision, CoaXpress 2.0 and PCIe | AMD and partner soft IP for many vision standards. |

# DATA CENTER SERVER I/O AND BOARD MANAGEMENT CONTROLLER




| BMC Application Requirements | Spartan™ UltraScale+™ FPGA Capabilities |
|---|---|
| Space constrained and low power requirement | FPGA can provide power management solutions and small form factor for entire BMC on a single chip |
| Monitor voltages and temperature, adjust fans and thermal solutions, emergency shut down if necessary | Flexible I/Os, diverse peripherals and internal Sysmon allow the FPGA to monitor external and internal events |
| Allow fast reporting back to the data center | Reference design as a general board-management controller supporting various communication standard protocols |
| Enable remote upgrade the firmware | Sophisticated configuration methods allows fail safe upgrade |

# GETTING STARTED AND NEXT STEPS

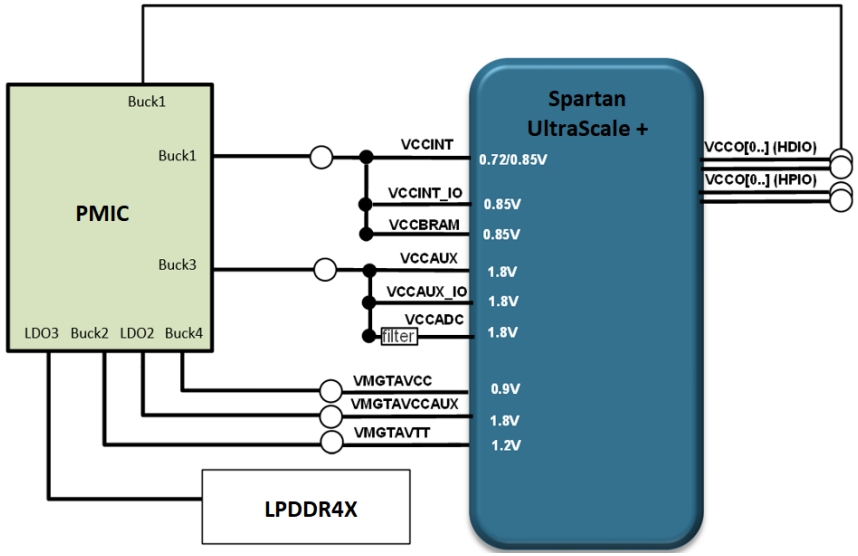
# GETTING STARTED MILESTONES AND AVAILABLE ASSETS

| Product Launch (March'24) | Early Access Program (NOW) | Production (Mid'25) |
|---|---|---|
| • Adaptive Computing Blog | • Overview Datasheet | • Silicon Production Shipping |
| • Infographic & Listicle | • Architecture Manuals | • Tools Production Support |
| • COP Portfolio eBook | • Mechanical Drawings and Pinouts | • Evaluation Kits Shipping |
| • Product & Solution Briefs | • AC/DC Switching Characteristics | |
| • Product Webpage | • Power Delivery Solution | |
| • UltraScale Architecture & Product Data Sheet | • Tools Early Access | |

# START WORKING ON POWER DELIVERY SOLUTIONS

## Strategic Power Partnerships

- Power reference designs to springboard your solution
- Design for low cost, low BOM & high channel integration
- High frequency switching regulators to reduce inductor size
- Single PMIC solutions
- Telemetry enabled power management for battery power applications




## PDM Power Design Tab Support

- Dynamic decoupling capacitor calculations and recommended P/Ns
- Power rail consolidation images & power sequencing diagrams
- Simplified power specification details based on user requirement
- Step load estimations calculated on dynamic currents

**Power Rail Characteristics**

| Supply | Voltage | Min Voltage | Max Voltage | Static (A) | Dynamic (A) | Total (A) | Powerup (A) |
|---|---|---|---|---|---|---|---|
| System Auxiliary | | | | | | | |
| VCCAUX | 1.800 | 1.746 | 1.854 | 0.016 | 0.118 | 0.134 | |
| VCCAUX_IO | 1.800 | 1.746 | 1.854 | 0.011 | 0.162 | 0.173 | |
| VCCAUX_IO_HP | 1.800 | 1.746 | 1.854 | 0.011 | 0.000 | 0.011 | |
| System Core | | | | | | | |
| VCCINT_IO | 0.850 | 0.825 | 0.875 | 0.013 | 0.216 | 0.229 | |
| Programmable Logic Core | | | | | | | |
| VCCINT | 0.850 | 0.825 | 0.875 | 0.035 | 2.043 | 2.079 | |
| VCCBRAM | 0.850 | 0.825 | 0.875 | 0.001 | 0.000 | 0.001 | 0.065 |
| Programmable Logic IO | | | | | | | |
| VCCO 1.5V | 1.500 | 1.455 | 1.545 | 0.000 | 0.000 | 0.000 | |
| VCCO 1.35V | 1.350 | 1.310 | 1.391 | 0.000 | 0.000 | 0.000 | |
| VCCO 1.2V | 1.200 | 1.164 | 1.236 | 0.000 | 0.166 | 0.166 | |
| VCCO 1.0V | 1.000 | 0.970 | 1.030 | 0.000 | 0.000 | 0.000 | |
| VCCO 3.3V | 3.300 | 3.201 | 3.399 | 0.000 | 0.000 | 0.000 | |
| VCCO 2.5V | 2.500 | 2.425 | 2.575 | 0.000 | 0.000 | 0.000 | |
| VCCO 1.8V | 1.800 | 1.746 | 1.854 | 0.000 | 0.022 | 0.022 | |
| Other | | | | | | | |
| VCCADC | 1.800 | 1.746 | 1.854 | 0.008 | 0.000 | 0.008 | |

# START PROTOTYPING WITH ULTASCALE+ BOARDS TODAY

## Avnet AUBoard 15P Development Kit

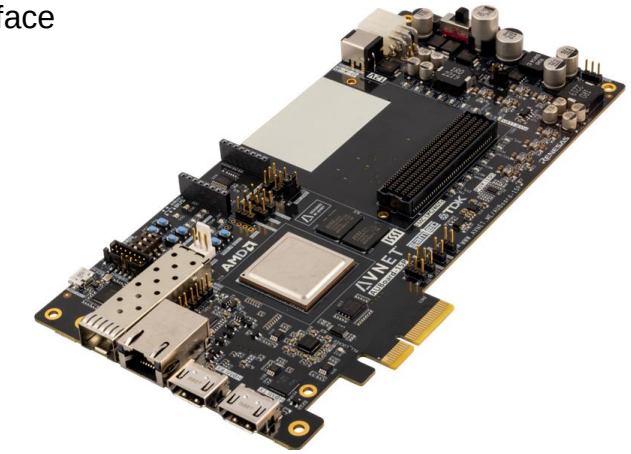
Featuring the AMD Artix™ UltraScale+™ **AU15P** device

### Feature List

- Targets XCAU15P-2FFVB676E device
- 170K logic cells, 10/100/1000 Ethernet, as well as 2 GB DDR4 RAM
- GPIO switches and LEDs
- Click I/O expansion
- 64 MB QSPI flash
- FMC LPC with 4 transceivers
- HDMI™ 2.0 Rx & Tx, SFP+ 10 GbE interface
- PCIe® Gen4 x4 card edge interface

### Target Applications

- Embedded vision
- Wired communications
- Industrial networking



Product Page

**$699**

## Avnet ZUBoard 1CG MPSoC Development Kit

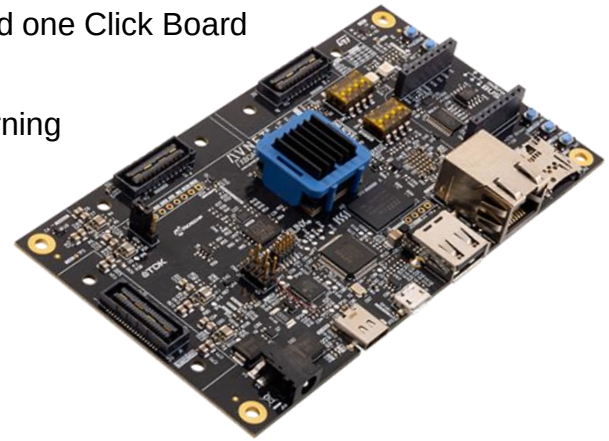
Featuring the AMD Zynq™ UltraScale+ **ZU1CG** device

### Feature List

- Targets XCZU1CG-1SBVA484E device
- Dual-core Arm® Cortex®-A53 MPCore and Dual-core Arm Cortex-R5F MPCore
- 81.9K logic cells, USB 2.0 Host, 10/100/1000 Ethernet, as well as cache and on-chip memory
- 1 GB of LPDDR4 with nonvolatile boot options in the 256 Mb QSPI flash or a microSD card slot
- A microUSB port provides onboard JTAG/UART access
- Three high-speed expansion ports and one Click Board

### Target Applications

- Artificial intelligence and Machine learning
- Embedded processing
- Robotics



Product Page

**$159**

Prices as of October, 2024 and are subject to change.

# NEXT STEPS

## Check the AMD Webpages for More Information

- Visit the AMD Spartan UltraScale+ FPGA webpage: https://www.amd.com/spartan-ultrascale-plus.html
- Learn how AMD stacks on top of the competition: https://www.amd.com/en/products/adaptive-socs-and-fpgas/cost-optimized-portfolio/scale-above-the-rest.html

## Engage in our AMD Spartan™ UltraScale+™ EA Program

- Set up NDA agreement to receive our roadmap updates
- Talk to your FAE about AMD Spartan™ UltraScale+™ FPGA Designs

## Experiment with Cost-Optimized Evaluation Kits

- Avnet ZUBoard 1CG: www.avnet.me/zuboard-1cg
- Avnet AUBoard 15P: www.avnet.me/auboard-15p

# AMD SPARTAN™ ULTRASCALE+™ FPGA

## High I/O, Low Power & State-of-the-Art Security Features

- Industry's highest I/O to logic cell ratio ≤28nm, enabling cost reduction for I/O-intensive applications
- Up to 30% power reduction[1] with 16 nm FinFET & power efficiency via hardened DDR and PCIe®
- Most security features in AMD Cost-Optimized Portfolio, NIST approved Post-Quantum Cryptography

## Accelerate Time to Market with Proven Design Tools

- Tools leadership since 2012 with AMD Vivado™ Design Suite
- One tool covering simulation to verification for entire FPGA portfolio[2]

## Design Once with a Trusted Supplier

- Nearly 40 years in the FPGA market & billions of devices shipped
- >15 years product lifecycle and in-field upgradeability for maximum design longevity


**Available H1'25**

See Endnotes SUS-001, SUS-002, SUS-003, SUS-011
[1]AMD Projection
[2]Starting at 28 nm


AMD

# ENDNOTES

1. Based on AMD internal analysis December 2023, comparing the total I/O to logic cell ratios in the AMD product data sheets for AMD Spartan™ UltraScale+™ FPGAs to previous generations of AMD Cost-Optimized FPGAs. (SUS-01)
2. Based on AMD internal analysis in December 2023, using the product data sheets to compare the number of security features in Spartan UltraScale+ FPGAs to previous generation AMD Cost-Optimized FPGAs. (SUS-02)
3. Projection is based on AMD labs internal analysis in January 2024, using Total Power calculation (Static plus Dynamic power) based on the difference in logic cell count of an AMD Artix™ UltraScale+ AU7P FPGA, to estimate the power of a 16 nm AMD Spartan UltraScale+ SU35P FPGA versus a 28 nm AMD Artix 7 7A35T FPGA, using Xilinx Power Estimator (XPE) tool version 2023.1.2. Actual Total Power will vary when final products are released in market, based on configuration, design, usage, and other factors. (SUS-03)
4. Projection is based on AMD labs internal analysis in January 2024, using nine different designs on two devices Artix UltraScale+ AU10P FPGA as a scale to Spartan UltraScale+ FPGA versus a 28 nm Artix 7 7A100T FPGA that were run at different clocks for $F_{max}$ calculation. The constraints were set so that the device runs at its max performance. Performance results may vary based on configuration, design, usage, and other factors. (SUS-04)
5. Based on AMD internal analysis of the product datasheets for a 16 nm AMD Spartan UltraScale+ SU35P FPGA versus a 28 nm Artix 7 7A35T. Actual I/O performance will vary based on configuration, design, usage, and other factors. (SUS-05)
6. Projection is based on AMD internal analysis, as of January 2024, using a Total Power calculation (Static plus Dynamic power) based on the logic scale count of an Artix UltraScale AU7P FPGA to estimate the total power of Spartan UltraScale+ SU200P FPGA versus Artix 7 7A200T FPGA, using Xilinx Power Estimator (XPE) tool version 2023.1.2. Actual Total power interfacing may vary when products are released in market based on configuration, design, usages, and other factors. (SUS-06)

# ENDNOTES

7 AMD Spartan™ UltraScale+™ FPGA SU200P FPGA memory controller bandwidth based on the data sheet against 28 nm AMD Artix™ 7 7A200T FPGA. (SUS-07)

8 Spartan UltraScale+ FPGA SU200P PCIe® bandwidth based on the data sheet against 28nm Artix 7 7A200T FPGA. (SUS-08)

9 Based on data sheet comparison of the AMD Spartan UltraScale+ SU10P FPGA to the Spartan 7 7S50 FPGA and calculating cost savings per I/O based on AMD list prices as of February 2024, for user designs requiring at least 200 GPIO. Prices subject to change, results may vary. (SUS-09)

10 Based on data sheet comparison of the Spartan UltraScale+ SU55P FPGA versus the Artix 7 7A100T FPGA, calculating a reduction in programmable logic requirements of the Spartan UltraScale+ SU55P FPGA and the resulting cost savings using AMD list prices as of February 2024. Prices are subject to change, results may vary. (SUS-10)

11 Based on product datasheets for AMD Spartan UltraScale+ FPGAs versus Efinix, Intel, Lattice, and Microchip, as of February 2024, comparing the total I/O to logic cell ratios of comparable 28 nm and lower node size FPGAs. (SUS-11)

12 Projection is based on AMD labs internal analysis in March 2024, using total power calculation (static plus dynamic power) based on the difference in logic cell count of an AMD Artix UltraScale+ AU7P FPGA, to estimate the power of a 16nm AMD Spartan™ UltraScale+™ SU35P FPGA versus a 45nm AMD Spartan 6 6SLX45 FPGA, using Xilinx Power Estimator (XPE) tool version 2023.1.2. Actual Total power will vary when final products are released in market, based on configuration, usage, and other factors. (SUS-12)

13 Projection is based on AMD labs internal analysis in January 2024, using 9 different designs on two devices Artix UltraScale+ AU10P FPGA as a scale to Spartan UltraScale+ FPGA versus a 28nm Artix 7 7A100T FPGA. that were run at different clocks for fmax calculation. The constraints were set so that the device runs at its max performance. Performance results may vary based on configuration, usage, and other factors. (SUS-13)

# DISCLAIMER AND ATTRIBUTIONS

## DISCLAIMER

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# Appendix: Product Table

# AMD Spartan™ UltraScale+™ FPGA Product Table

| | Device Name | | SU10P | SU25P | SU35P | SU50P | SU55P | SU65P | SU100P | SU150P | SU200P |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Logic | System Logic Cells (K) | | 11 | 22 | 36 | 52 | 52 | 65 | 100 | 137 | 218 |
| | CLB Flip-Flops (K) | | 10 | 20 | 32 | 48 | 48 | 60 | 92 | 126 | 200 |
| | CLB LUTs (K) | | 5 | 10 | 16 | 24 | 24 | 30 | 46 | 63 | 100 |
| Memory | Max. Distributed RAM (Mb) | | 0.07 | 0.14 | 0.23 | 0.41 | 0.41 | 0.51 | 0.79 | 1.25 | 1.99 |
| | Total Block RAM (Mb) | | 1.7 | 1.7 | 1.7 | 2.5 | 2.5 | 3.8 | 5.1 | 5.9 | 6.8 |
| | 36K Block RAM Blocks | | 48 | 48 | 48 | 72 | 72 | 108 | 144 | 168 | 192 |
| | Total UltraRAM (Mb) | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 4.5 | 18.0 |
| | 288K UltraRAM Blocks | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 16 | 64 |
| | Integrated Memory Controller | | 0 | 0 | 0 | 0 | 2 | 2 | 2 | 2 | 2 |
| Clocking | Clock Mgmt Tiles (CMTs) | | 2 | 2 | 2 | 2 | 4 | 5 | 5 | 6 | 6 |
| Integrated IP | DSP Slices | | 24 | 36 | 48 | 96 | 96 | 144 | 144 | 384 | 384 |
| | PCIE4CE Blocks | | 0 | 0 | 0 | 0 | 0 | 1x Gen4x4 | 1x Gen4x4 | 1x Gen4x8 or 2x Gen4x4 | 1x Gen4x8 or 2x Gen4x4 |
| I/O | Max. Single-Ended HD I/O | | 252 | 252 | 252 | 336 | 168 | 294 | 294 | 336 | 336 |
| | Max. Single-Ended HP I/O | | 52 | 52 | 52 | 52 | 52 | 52 | 52 | 104 | 104 |
| | Max. Single-Ended XP5IO | | 0 | 0 | 0 | 0 | 132 | 132 | 132 | 132 | 132 |
| | GTH Transceivers (16.3 Gb/s) | | 0 | 0 | 0 | 0 | 0 | 4 | 4 | 8 | 8 |
| Security | Platform Management Controller | | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Speed Grades | Extended | | -1, -2 | | | | | | | | |
| | Industrial | | -1, -2, -1L | | | | | | | | |
| Package | Dimensions (mm) | Ball Pitch (mm) | HD I/O, HP I/O, XP5IO, GTH | | | | | | | | |
| CMVA361 | 10x10 | 0.5 | 168, 52, 0, 0 | 168, 52, 0, 0 | 168, 52, 0, 0 | | | | | | |
| CMVA529 | 12x12 | 0.5 | 252, 52, 0, 0 | 252, 52, 0, 0 | 252, 52, 0, 0 | 280, 52, 0, 0 | | | | | |
| CMVB529 | 12x12 | 0.5 | | | | | 100, 52, 132, 0 | 100, 52, 132, 4 | 100, 52, 132, 4 | | |
| SBVC529 | 19x19 | 0.8 | | | | | 120, 52, 132, 0 | 120, 52, 132, 0 | 120, 52, 132, 0 | | |
| SBVB625 | 21x21 | 0.8 | 252, 52, 0, 0 | 252, 52, 0, 0 | 252, 52, 0, 0 | 336, 52, 0, 0 | | | | | |
| SBVF784 | 23x23 | 0.8 | | | | | 168, 52, 132, 0 | 224, 52, 132, 4 | 224, 52, 132, 4 | 224, 52, 132, 4 | 224, 52, 132, 4 |
| SBVG784 | 23x23 | 0.8 | | | | | | 120, 52, 132, 4 | 120, 52, 132, 4 | 120, 104, 132, 8 | 120, 104, 132, 8 |
| SBVA1024 | 27x27 | 0.8 | | | | | | 294, 52, 132, 4 | 294, 52, 132, 4 | 294, 104, 132, 8 | 294, 104, 132, 8 |
| FSVG1156 | 35x35 | 1.0 | | | | | | 294, 52, 132, 4 | 294, 52, 132, 4 | 336, 104, 132, 8 | 336, 104, 132, 8 |