AMD Vitis™ Tool: AI Engine Rapid Prototyping

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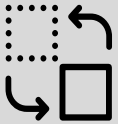
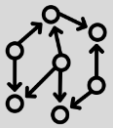
AI Engine Rapid Prototyping Introduction

AI Engine Rapid Prototyping → **Methodology for AI Engine System Validation**

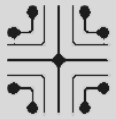


Early estimation of system resources

Early throughput and latency validation



Exploring buffer sizing, placement, routing solutions



Identifying stream contention & routing challenges up front

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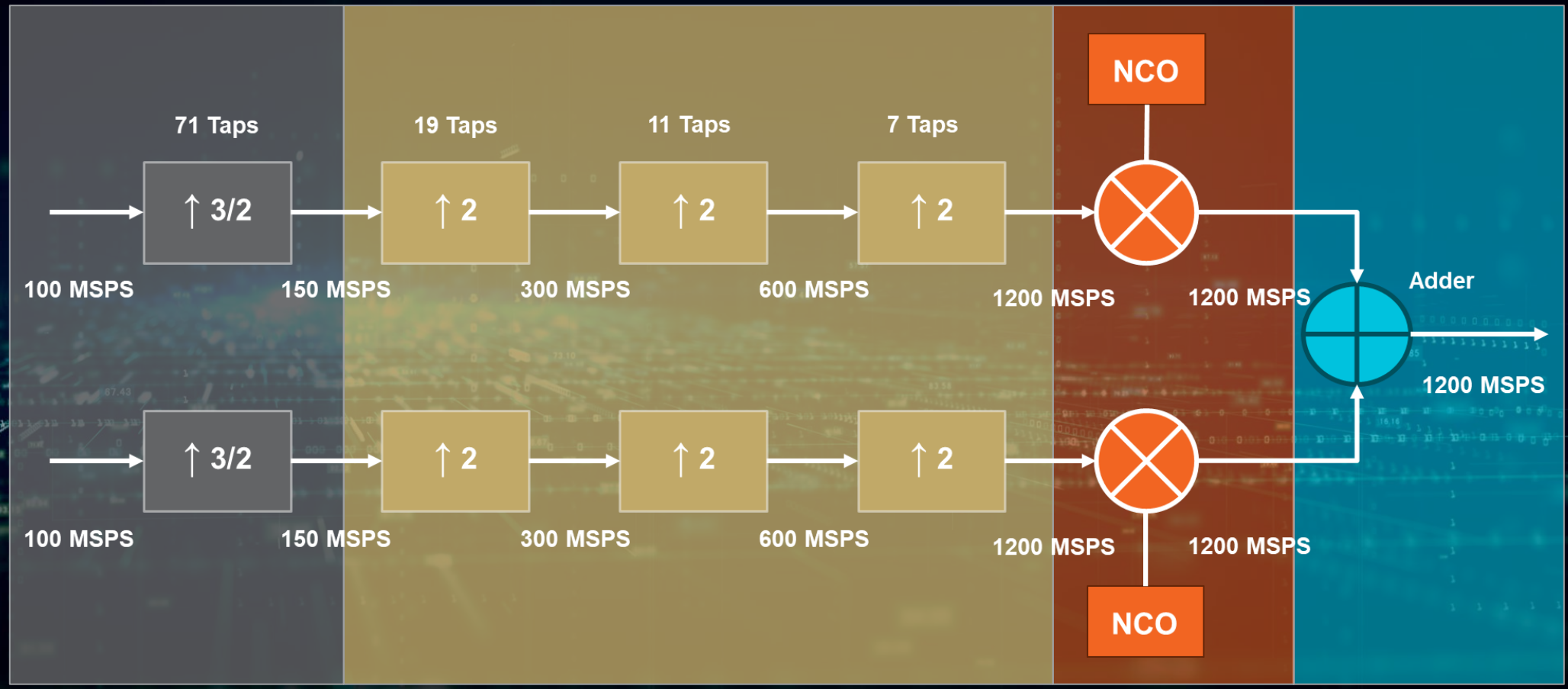
Example Design – Digital Up Conversion (DUC) Chain



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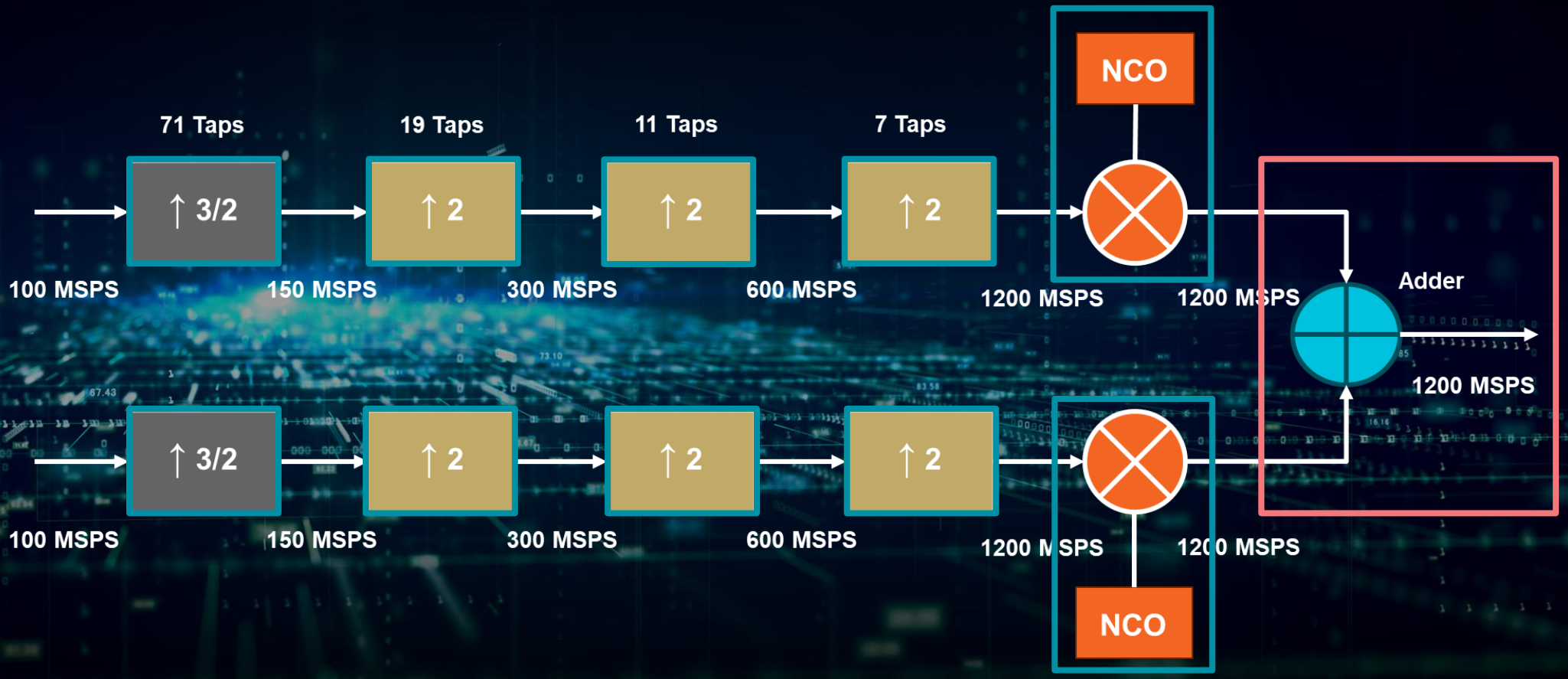
Example Design – Digital Up Conversion (DUC) Chain



Library Function Kernel Custom Coded Kernel

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System Requirements

DATA type: cint16

Sampling rate (Fs): 1200 MSPS

Adder for digital-up conversion

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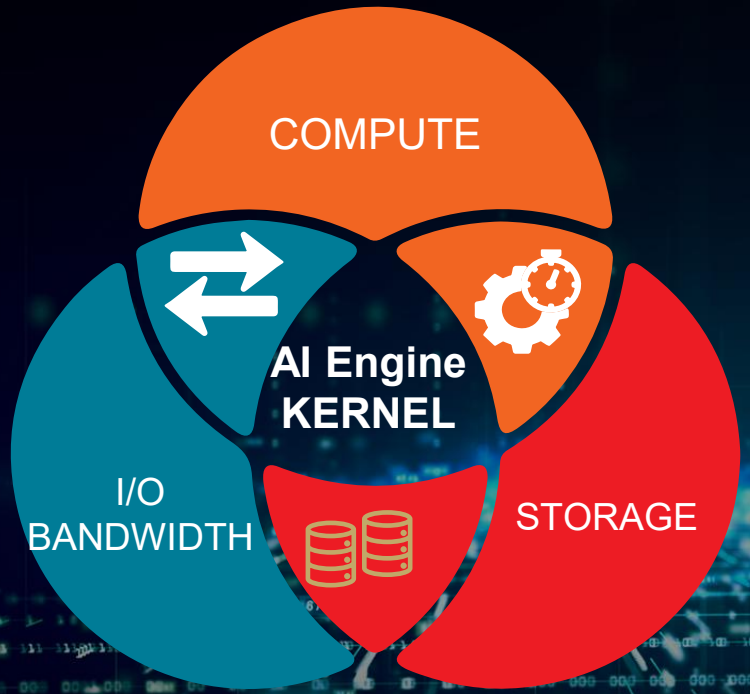
System Mapping



Understanding the number of AI Engine tiles/processors required based on:

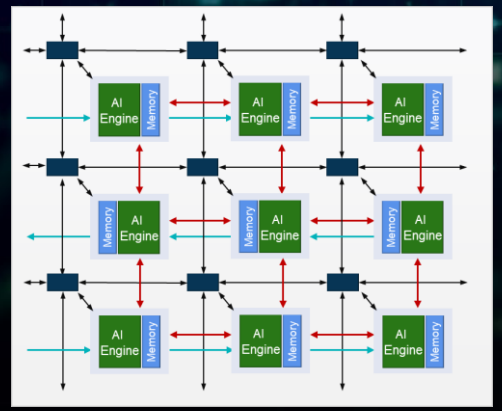
- Data types
- Sampling rate
- Algorithm

Memory requirements such as local memory and non-neighboring tile memory

- Buffer size
- Data types
- RTPs
- Stack size
- DMA FIFOs
- Memory tile (AIE-ML)

Understanding the number of ports required for the design

- Number of PLIO ports
- PL clock
- Buffer/stream interface



AI Engine system mapping helps to achieve your design goal

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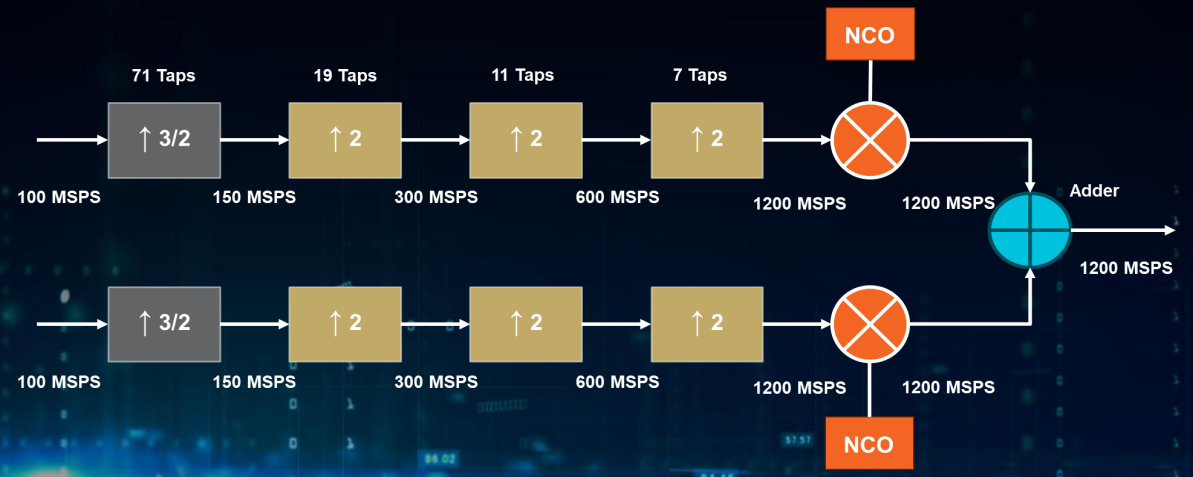
System Mapping



Design Needs

- 1200 MSPS sampling rate, < 500 ns latency
- Implement an “adder block” using 1 tile (while the Resampler, HB1, HB2, HB3, and mixer each in one tile
- Adder inputs two <cint16>, output one <cint16>

System Partitioning Analysis

- 1 MAC/cycle → need a single tile
- 3 KB @ 1200 MSPS
- Use input/output buffer
- **What do we do next?**

Sampling Rate (MSPS)	# I/O Buffers	Adder Data
1200	2 input 1 output	3 KB*

Storage - data type: cint16 (4 bytes)
Total bytes = 768*4 = 3072 bytes

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AI Engine Rapid Prototyping

- Build empty kernel wrappers
- Build the graph and compile
- Simulating and analyzing for an early estimation

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Vitis™ Unified IDE AI Engine Rapid Prototyping Feature

Tool part of the Vitis Unified IDE in 2024.2 to help quickly generate data flow models

Generated model built with kernel for which the ports can be parametrized

Model includes the final multi-core graph topology with full buffering & stream details and all LUT storages

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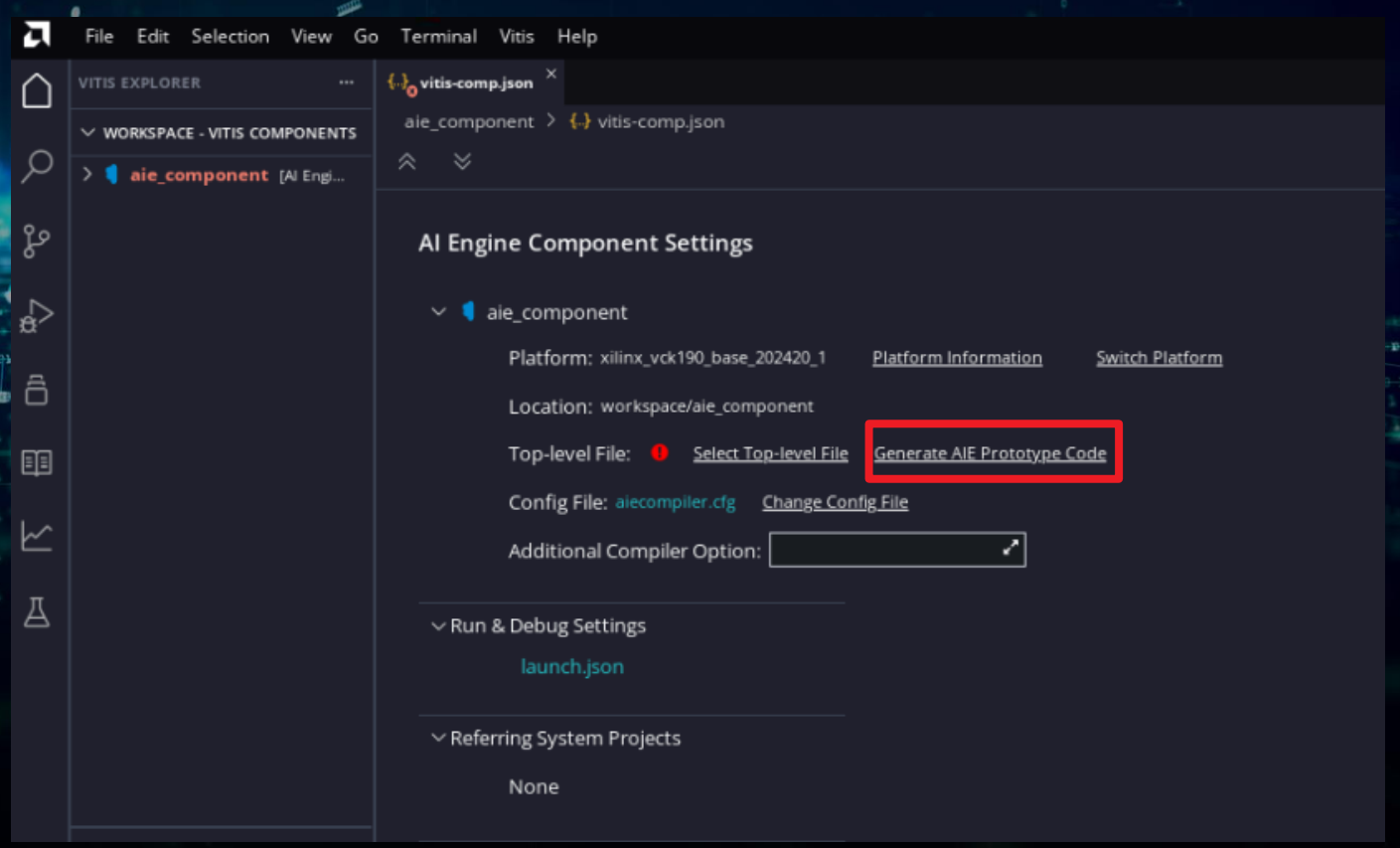
Rapid Prototyping of AI Engine Designs: Methodology (1)

1

Create an empty AI Engine component and select “Generate AIE Prototype Code”



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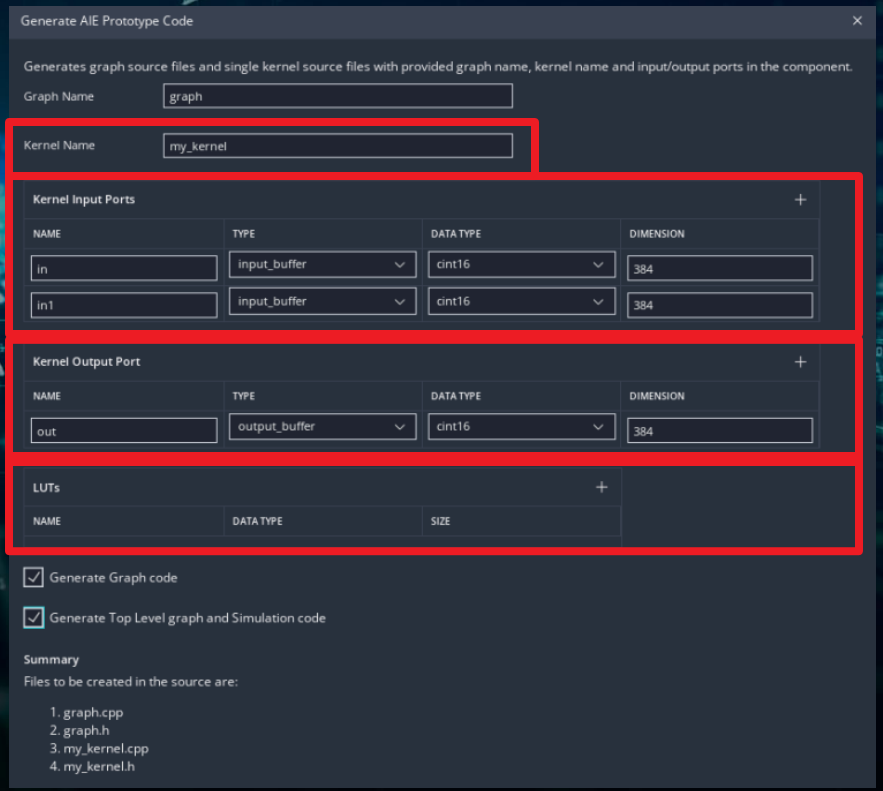
Rapid Prototyping of AI Engine Designs: Methodology (2)

2

Set the parameters of the kernel



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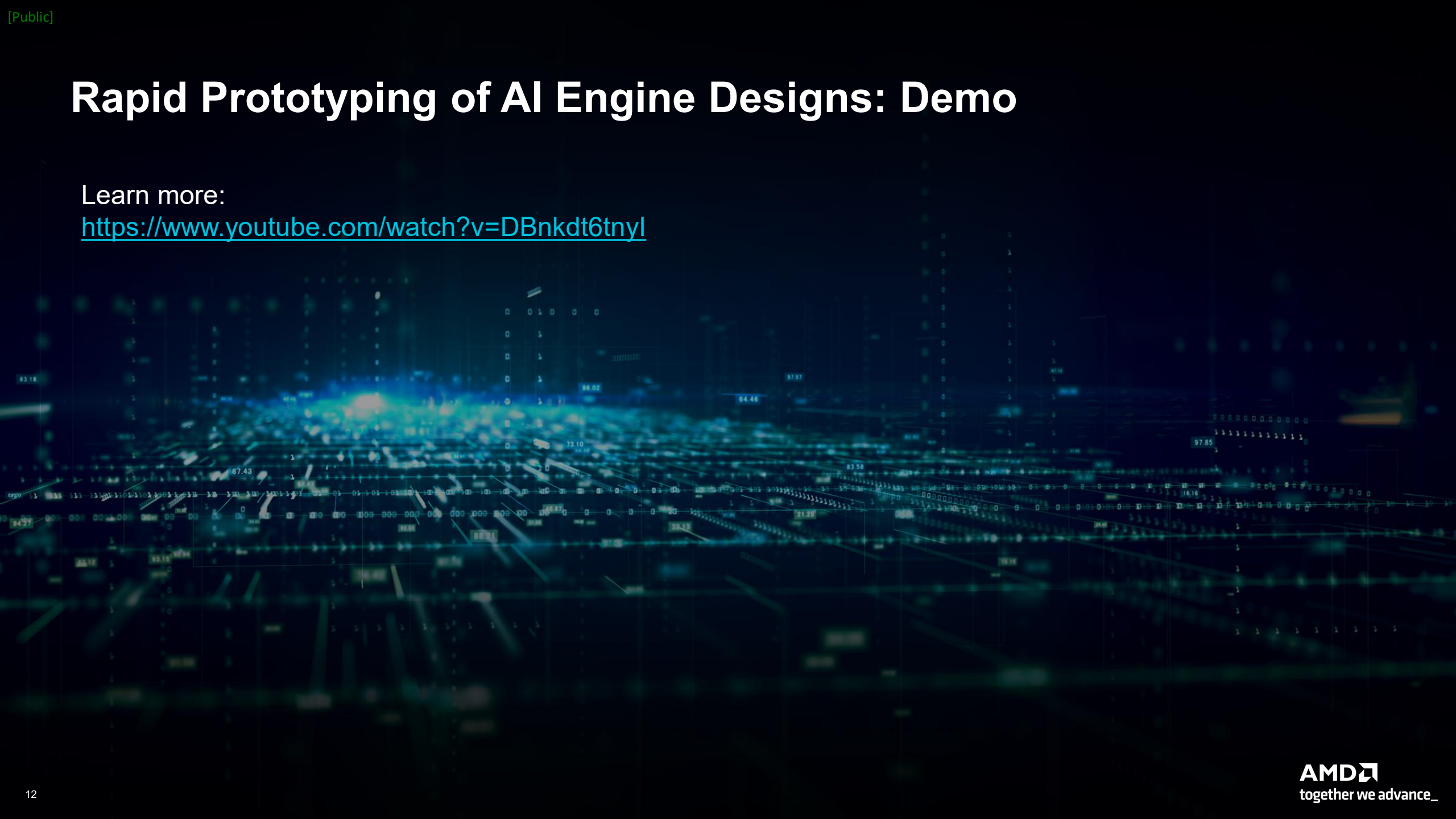
Rapid Prototyping of AI Engine Designs: Demo

Learn more:
https://www.youtube.com/watch?v=DBnkdt6tnyI



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