Newtouch Delivers 4th Gen Large-Scale Prototyping System with AMD FPGA

Newtouch's PHINEDesign Platform Uses AMD Virtex™ UltraScale+™ FPGA to Deliver Highest Logic Density for Device Prototyping and Simulation

AT A GLANCE:

Newtouch Electronics (Shanghai) Co., Ltd. was established in 2004 as one of the first generation of enterprises using FPGA chips in the world. It now has more than 10 years of hardware IC and FPGA design experience. In 2014, Newtouch launched its own FPGA prototype platform, PHINEDesign, which has continued to evolve over three generations of innovation.

Industry: Test & Measurement
Head Office: Beijing, China
Established: 2004
Website: http://www.newtouch-elec.com

Image1. NE-VU19P-LSI Prototype Verification Platform

SUMMARY:

In recent years, China's domestic chip market has developed rapidly, and demand for verification, simulation, and testing in the chip design process has also increased sharply. Newtouch Electronics was looking to update its PHINEDesign FPGA prototyping platform with the latest FPGA technology available. The company's two most-recent platform generations were built on AMD's Virtex-7 2000T FPGA and Virtex UltraScale VU440 FPGA devices, respectively.

When AMD extended its world largest-capacity FPGA record with the launch of its Virtex UltraScale+ VU19P FPGA in August 2019, Newtouch jumped on the opportunity to incorporate this technology into its 4th generation PHINEDesign platform - NE-VU19P-LSI. The result is improved verification efficiency, shorter verification cycles, and faster customer time-to-market.

CHALLENGE:

Since 2014, Newtouch has been providing high-quality FPGA prototyping platforms, named PHINEDesign, that are all based on AMD's most-advanced FPGA technologies. The company's two most-recent platform generations were built on AMD's Virtex-7 2000T and Virtex UltraScale VU440 FPGA devices, respectively.

Demand for verification, simulation, and testing in the chip design process has increased sharply in China in recent years, so Newtouch turned to AMD technology for its next-generation, high-volume PHINEDesign platform.

SOLUTION:

In August 2019, AMD extended its own world largest-capacity FPGA record with the Virtex UltraScale+ VU19P FPGA. With 35 billion transistors, the VU19P provides the highest logic density and I/O count on a single device ever built, enabling emulation and prototyping of tomorrow's most advanced ASIC and SoC technologies. It is also ideal for test, measurement, compute, networking, aerospace and defense-related applications.

One of AMD's earliest primary Alliance Member partners, Newtouch was able to leverage the early access program for Virtex UltraScale+ VU19P FPGA, and actively invested in R&D and design of its fourth-generation prototype verification platform. At the end of 2020, Newtouch had publicly launched its fourth-generation PHINEDesign—NE-VU19P-LSI platform.

"As an early user of the first two generations of 'world's largest capacity' FPGAs from AMD, Newtouch had a deeper understanding of VU19P's world-record performance and value," said by Jiajun Lu, general manager of Newtouch. "We are very excited to be able to use this revolutionary product to upgrade our verification platform to the top level in the industry, and provide strong support for the explosive growth of 5G, medical, consumer electronics, and other major trends related to IC design."

The VU19P sets a new standard in FPGAs, featuring nine million system logic cells, up to 1.5 terabits per-second of DDR4 memory bandwidth, up to 4.5 terabits per-second of transceiver bandwidth, and more than 2,000 user I/Os. It is 1.6X larger than its predecessor, the 20 nm Virtex UltraScale 440 FPGA, and fully meets Newtouch's urgent desire for a large-capacity FPGA to upgrade its existing platform.

The new NE-VU19P-LSI platform's features include:

- More than 1,800 I/Os are connected through the FMC standard connector, which are compatible with AMD and other major manufacturers' standard daughter cards. That provides users with a wealth of expansion interface options. Meanwhile, Newtouch also equipped various FMC daughter cards specifically for prototype verification.
- 48 high-speed GTY transceivers, up to 25Gbps. It can be extended through FMC or SLIMSAS. The performance of high-speed SerDes is guaranteed, and the interface form is more convenient for cascading expansion of multiple systems without causing pin redundancy.
- FMC I/O with adjustable voltage can be adapted to various external interface debugging.
- Scalable multi-channel DDR4/DDR3 and other memory cards. The rate can reach FPGA nominal 2,400Mbps.
- Abundant global clock and reset resources can support various frequency application scenarios. It can meet the verification requirements of multiple clock domains, and it can also meet the requirements of the synchronous clock when multiple FPGAs are connected.
- Flexible system configuration software, providing intuitive and convenient interface operation.
- Provides simultaneous command-line execution mode.

RESULT:

Newtouch's fourth-generation PHINEDesign NE-VU19P-LSI platform has improved verification efficiency of up to 30% for some ASIC prototypes or large-scale SoC developments. For customers who need larger scale verification, the new platform can save almost 50% of the workload on resource partitioning, which significantly shortens the verification cycle, and accelerates the customers' time-to-market.

ADDITIONAL RESOURCES:

Learn More About AMD's Virtex UltraScale VU19P FPGA

PID 1870060