NYCU MODERNIZES IC DESIGN EDUCATION WITH AMD EPYC™ SERVER CPUs

CASE STUDY

NYCU scaled its IC design training to support 500 concurrent users by deploying a secure private cloud powered by 4th Gen AMD EPYC™ Server CPUs

As semiconductor manufacturing moves to more advanced process technologies, the compute and simulation demands of IC design and Electronic Design Automation (EDA) workloads continue to rise. Yet many university teaching environments have remained focused on legacy planar nodes, creating a disconnect between academia and industry. With support from Taiwan's Ministry of Education Talent Cultivation Project for Advanced IC Design, National Yang Ming Chiao Tung University (NYCU) deployed a secure private cloud environment powered by 4th Gen AMD EPYC™ Server CPUs to bring advanced process IC design workflows into the classroom and research lab.

> **"NYCU needed an isolated, self-managed infrastructure that could provide both the performance and security required for industry-relevant IC design education."**

According to Professor Ming-Dou Ker, Associate Dean of the College of Electrical and Computer Engineering at NYCU, the university's previous course environments relied on standard PCs for remote access. Under heavy workloads such as large-scale Monte Carlo analysis and auto placement and routing (APR), performance became a bottleneck. Post-layout simulations could take up to a week per run, slowing down iterative design and validation and limiting the effectiveness of instruction.

As FinFET-based design was introduced into coursework, the challenge extended beyond compute performance. Advanced-node process parameters, design rules, and PDK data require strict protection, making public cloud deployment less viable. NYCU needed an isolated, self-managed infrastructure that could provide both the performance and security required for industry-relevant IC design education.

BUILDING A SECURE, SCALABLE PRIVATE CLOUD FOR IC DESIGN TRAINING

To address these requirements, NYCU implemented an HPC-based private cloud architecture using 4th Gen AMD EPYC™ Server CPUs as the compute foundation and virtualization for unified resource management. The design gives the university a flexible environment that can dynamically allocate computing resources based on course requirements while isolating workloads across different classes and users.

Dr. Lin-Hong Lai, who led the system planning, explained that virtualization replaced the previous model in which hundreds of students shared a single server. With the new architecture, resources can be allocated more efficiently, and issues affecting one node are less likely to disrupt other workloads.

INDUSTRY

Higher education and semiconductor talent development

CHALLENGES

Modernizing IC design education infrastructure, handling compute-intensive EDA workloads, and maintaining strict security for advanced-node design environments

SOLUTION

Deploying an on-premises private cloud using 4th Gen AMD EPYC™ Server processors for scalable, isolated resource allocation

RESULTS

Support for 18 courses and approximately 500 concurrent users, reduced lag and crashes, faster simulation workflows, and expanded access to advanced process IC design training

AMD TECHNOLOGY AT A GLANCE

4th Gen AMD EPYC™ Server CPUs

The team also developed an in-house account management system to digitize account application, activation, and password reset processes, helping reduce administrative overhead.

> **"The platform now supports 18 courses and approximately 500 concurrent users."**

NYCU has deployed 10 servers equipped with 4th Gen AMD EPYC™ Server CPUs, with up to 192 cores per server. The platform now supports 18 courses and approximately 500 concurrent users. By leveraging the high core density and performance of AMD EPYC™ Server CPUs, the university has significantly reduced lag and crashes in its teaching environment, enabling students to complete simulations more smoothly and with less waiting.

With the new infrastructure in place, NYCU has started extending advanced IC design training—previously concentrated at the graduate level—into undergraduate curricula. Through industry-supported virtual process platforms and the university's HPC environment, students can now gain earlier exposure to FinFET-based circuit design, simulation, and layout training beginning in their junior year.

These courses are significantly more demanding than traditional IC design classes. Students must learn design concepts, industry-grade EDA tools, workflows, and extensive parameter settings at the same time. In one undergraduate Analog IC Design Lab course, seven graduate teaching assistants support more than 100 students, illustrating both the complexity of the curriculum and the importance of a stable, high-performance computing environment.

EXPANDING ACCESS TO ADVANCED PROCESS DESIGN EDUCATION

On the research side, NYCU is advancing 7nm chip design projects with support from the Taiwan Semiconductor Research Institute (TSRI). Professor Ker noted that advanced-node design involves far more than tape-out, requiring students to understand extensive design rules and verification processes. Through Taiwan's semiconductor talent development initiative, graduate students can also apply for free 16nm multi-project wafer runs through TSRI, extending hands-on access to real FinFET process training.

"Within a unified AMD EPYC™ Solutions, we can dynamically allocate resources to support high-concurrency teaching workloads while also meeting the strong single-thread performance demands of research. This provides us a more flexible and scalable platform for balancing both education and research on the same infrastructure," says Dr. Lin-Hong Lai, Project Lead for System Planning.

NYCU's decision to continue building on AMD EPYC™ Server CPUs was informed by prior validation of EDA tool compatibility and platform stability.

> **"Within a unified AMD EPYC™ Solutions, we can dynamically allocate resources to support high-concurrency teaching workloads while also meeting the strong single-thread performance demands of research. This provides us a more flexible and scalable platform for balancing both education and research on the same infrastructure."**

Dr. Lin-Hong Lai, Project Lead for System Planning

According to Dr. Lai, that experience gave the university confidence to expand from pilot deployment to a broader infrastructure supported by the Semiconductor Talent Development Program. As a result, AMD EPYC™ Server CPUs have become more than a hardware choice—they are now a core part of the environment supporting both teaching and system reliability.

- High core-count nodes for handling large-scale concurrent teaching workloads
- High-frequency nodes optimized for single-thread performance, tailored to research applications

ALIGNING ACADEMIC TRAINING WITH REAL-WORLD SEMICONDUCTOR WORKFLOWS

Under this AMD CPU-based architecture, NYCU uses a dual-track configuration to support both teaching and research requirements:

- Bigstack virtualization dynamically allocates resources across these nodes, enabling NYCU to serve high-concurrency classroom usage while also supporting advanced research workloads that depend on strong single-thread performance. This approach also reflects the broader industry environment, as many semiconductor manufacturers and IC design companies in Taiwan already run EDA workloads on AMD CPU-based platforms. By learning on a similar architecture, students can transition more quickly into production semiconductor development environments.

As IC design education shifted to FinFET-based workflows, NYCU modernized its IC design environment with AMD EPYC™ Server CPUs to better prepare tomorrow's semiconductor engineers.

Looking ahead, NYCU is preparing a third-phase expansion that will add server nodes with higher single-core performance and GPU nodes for AI-accelerated simulations and more demanding graduate-level IC design workloads. As graduate enrollment and research intensity continue to grow, the university expects demand for computing resources to increase further.

> **"Adopting the AMD platform is not merely about delivering compute capacity—it is about building a sustainable foundation for education that supports teaching, advances research, and helps bridge academic training with real-world semiconductor industry needs."**
>
> Professor Ming-Dou Ker, Associate Dean of the College of Electrical and Computer Engineering at NYCU

For NYCU, infrastructure investment is ultimately about developing the next generation of semiconductor talent. By building a secure, high-performance computing environment centered on AMD EPYC™ Server CPUs, the university can support large-scale teaching, advanced research, and stronger alignment with real semiconductor industry requirements. The result is a more sustainable education platform that helps students gain practical experience with advanced IC design workflows before entering the workforce.

"Adopting the AMD platform is not merely about delivering compute capacity—it is about building a sustainable foundation for education that supports teaching, advances research, and helps bridge academic training with real-world semiconductor industry needs," says Professor Ming-Dou Ker, Associate Dean of the College of Electrical and Computer Engineering at NYCU.

With AMD EPYC™ Server CPUs at the foundation of its private cloud environment, NYCU is helping close the gap between academic IC design education and the performance, security, and workflow expectations of modern semiconductor development.

Professor Ming-Dou Ker helped design NYCU's flexible computing infrastructure that balances high-concurrency teaching with advanced semiconductor research.

WANT TO LEARN HOW AMD EPYC SERVER CPUs MIGHT WORK FOR YOU?
Sign up to receive our data center content:
amd.com/epycsignup

ABOUT National Yang Ming Chiao Tung University (NYCU)

National Yang Ming Chiao Tung University (NYCU) was founded on the idea that people work across the disciplines to solve real-world problems, from information and communications technology to biomedical research. It also requires contributing to fields located at the intersection of these research areas, as well as training students so that the next generation will not be as constrained by disciplinary boundaries as the previous one. NYCU continues to be guided by the idea that we can achieve something much greater together than we can individually. For more information visit www.nycu.edu.tw.

ABOUT AMD

For more than 50 years AMD has driven innovation in high-performance computing, graphics, and visualization technologies. Billions of people, leading Fortune 500 businesses, and cutting-edge scientific research institutions around the world rely on AMD technology daily to improve how they live, work and play. AMD employees are focused on building leadership high-performance and adaptive products that push the boundaries of what is possible. For more information about how AMD is enabling today and inspiring tomorrow, visit the AMD (NASDAQ: AMD) website, blog, LinkedIn, and X pages.