SIEMENS' VELOCE proFPGA CS FOR SOFTWARE PROTOTYPING - ENABLED BY AMD VERSAL™ PREMIUM ADAPTIVE SoC

CUSTOMER

SIEMENS

INDUSTRY

IP and Chip Development and Verification

CHALLENGES

RTL design verification typically starts with a software simulator. At some point though, the simulator doesn't run fast enough to find more bugs in a reasonable amount of time. That's when customers switch to a Hardware Assisted Verification (HAV) Solution, often initially on an emulator, then, once the RTL design is stable, to an FPGA-based prototype.

SOLUTION

The Veloce proFPGA prototyping solution offers state-of-the-art modularity, scalability, flexibility, and portability to serve the verification requirements of today's hardware and software engineers. The new Veloce proFPGA CS prototyping solution, enabled by the AMD Versal™ Premium VP1902 adaptive SoC, is easy to deploy, empowering design teams to quickly perform pre-silicon validation of ICs and software.

RESULTS

Siemens determined that the Versal Premium VP1902 adaptive SoC offered the best solution for its requirements and design goals, considering the capabilities, the performance provided and availability of the device.

AMD TECHNOLOGY AT A GLANCE

AMD Versal Premium VP1902 adaptive SoC

Enables fast performance prototyping for data centers, lab, and portable/mobile environments

Siemens' Veloce™ proFPGA CS is a prototyping system optimized for software validation and hardware/software system integration. It's an FPGA-based tool at the logical functional verification level.

The software verification process tests and validates the functionality of a designed integrated circuit (IC) by simulating its behavior under different input conditions, to ensure it will perform as intended. This is a highly flexible and affordable platform, supporting virtually every design size from single FPGA to multi-FPGA, multi-blade configurations for even the largest designs. Engineers need to verify the logic functionality of an SoC and they do this by running software workloads, often with an operating system on it, in a cycle-accurate environment.

RTL design emulation and large-scale FPGA-based prototyping are enabling tools for SoC, software, and system verification and validation. Emulation, with its ease of compiling RTL into an executable model and its full-signal observability, is an indispensable tool for RTL design and verification. FPGA-based large-scale prototyping that achieves greater execution speed in exchange for more limited flexibility is vital for software teams that must validate code against the RTL design. Together they are an incredible force for full-system verification/validation.

CHALLENGE

The size and complexity of chip designs is driven today by artificial intelligence—in training and executing generative AI models, powering smart vehicles, and general-intelligence research. Leading-edge IC processes and multi-die modules and chiplets promote this increase in chip size. For chip vendors, the product is the chip. If the chip conforms to its data sheet, it is correct. For a system house, the product is the chip on its board, running its entire software stack from drivers and operating systems up through applications. It is the integrated system that they must test, not just modules of the RTL. As a result, the scale of IC designs has increased enormously, driven by a leap in demands of a few key applications: data center CPUs and GPUs, mobile platforms, and artificial-intelligence (AI) accelerators. In that latter case, exploding training demands for generative AI models and the beginnings of research into general AI shows an insatiable appetite for hardware.

"An SoC verification and validation project typically starts with verification of the RTL design for the hardware portion of it," said Juergen Jaeger, director of prototyping product strategy at Siemens. "In many cases, engineers do a software simulation for the very early RTL design including all the various system components that come together. At some point, the simulator doesn't run fast enough, and customers switch to an emulator. This allows them to validate the RTL design at a much higher performance level than simulation does. Then, at some point, the RTL design is stable enough that it doesn't change daily, and you want to start running software workloads on it. At that point, customers often switch

SOLUTION

to an FPGA-based prototype platform. It enables even higher performance than emulation does. This is also the point where you see the more software workloads brought up; firmware, operating system and sometimes application software."

Siemens started collaborating with AMD early on, by getting the specs of the AMD Versal Premium VP1902 device in hand so hardware and software development of the new proFPGA CS platform could begin. Next was getting mechanical samples, so the Siemens team could fine-tune its manufacturing process. The AMD Versal Premium VP1902 is a massive device with thousands of pins underneath. Soon after, the teams started collaborating on the software side, specifically on the interface between the Siemens compilation and synthesis tool, and the AMD Vivado™ stack, used for place and route. The third area of cooperation was on the debug side, where the AMD Versal Premium VP1902 adaptive SoC offers a) up to 2X the capacity of previous generation AMD Virtex™ Ultrascale+™ VU19P FPGA, in terms of the number of system logic cells[1], and b) up to 2X aggregate I/O bandwidth compared to the prior generation Virtex Ultrascale + VU19P FPGA[2].

The Veloce proFPGA CS Software Prototyping Platform is a high performing and fully configurable system where designers can validate hardware/software integration with massive software workloads prior to silicon availability. It is architected to offer state-of-the-art modularity, scalability, flexibility, and portability to serve the verification requirements of today's hardware and software engineers. "This FPGA prototyping solution, enabled by the AMD Versal Premium VP1902 adaptive SoC, is easy to deploy, empowering design teams to quickly perform pre-silicon validation of ICs and software," Jaeger said.

The Versal Premium VP1902 adaptive SoC offers the highest logic capacity, interconnect, and external memory bandwidth available in the Versal portfolio[3]. With more than 18.5 million logic cells, over 2,000 I/Os, and up to 160 high-speed transceivers capable of operating up to 112 Gbps, the Versal Premium VP1902 device is designed for applications that stretch the boundaries of engineering. Built on the proven Versal architecture, the VP1902 not only delivers leadership logic resources but also integrates Arm® scalar processors, hardened IP for PCIe® Gen5, Ethernet, and memory interfacing, all tied together by the Versal programmable network on chip (NoC) for simplified data movement across the massive device.

"The Veloce proFPGA CS system can be used in a data center or in a lab or benchtop environment where it can be connected to external interfaces like PCIe and to peripheral devices," Jaeger explained. "The software contents in today's products are growing exponentially, and verifying software early, also called "shift left," is the key to product success and time to market."

The Veloce proFPGA CS performance, at-speed interfaces, and scalability enable software teams to validate and debug software well before silicon availability. The system can scale from a single FPGA, or a single blade on the desk to multi-blade rack mount configurations for multi-user environments. Users have the flexibility of defining the number of FPGAs, the interconnects, and the at-speed protocol interfaces, that best match the verification and performance needs of the project.

"The Veloce software removes the cumbersome and manual tasks of modifying the design to become FPGA friendly," Jaeger added. "FPGA-based large-scale prototyping, that achieves greater execution speed in exchange for more limited observability, is vital for software teams that must validate code against the RTL design."

The Veloce proFPGA CS system is designed for performance and to take full advantage of the latest FPGA device technology, delivered by the AMD Versal Premium VP1902 adaptive SoC. The Veloce proFPGA CS implementation, debug, and runtime software maximizes the performance and productivity of a multi-FPGA design implementation, in fully automatic or user-guided modes. The system is cost-effective with its modular and scalable architecture. Starting with a single FPGA system on the desktop, or the new interconnectable multi-FPGA blade system, it's possible to efficiently expand to a multi-user prototyping farm with hundreds of blades. With the flexibility offered by the accessibility to all I/Os of the Versal Premium VP1902 adaptive SoC, the user can configure the prototype with a comprehensive suite of hardware interfaces, memories, speed-bridges and interconnect cables to mimic the real system.

RESULT

Siemens investigated alternatives and determined that the Versal Premium VP1902 adaptive SoC offered the best solution for its requirements and design goals, considering the capabilities, and the timing and availability of the device.

"AI plays an important role in the Siemens software flow," said Romain Petit, product manager for proFPGA CS at Siemens. "With it, the system maps a random RTL design into a large FPGA, like the Versal Premium VP1902 adaptive SoC, or multiples instances of this device. This requires various strategies depending on the target SoC design, and how fast it should run. The AMD Vivado design tool creates a new chip model based on place-and-route inputs. AI is then used to improve the quality of the result as well as the reliability and dependability of the compiles."

ABOUT SIEMENS DIGITAL INDUSTRIES SOFTWARE

Siemens Digital Industries Software is a division of Siemens that focuses on providing software solutions to help businesses across various industries achieve digital transformation. Their offerings include: a) Product Lifecycle Management (PLM): Tools like Teamcenter and NX help manage the entire lifecycle of a product, b) Manufacturing Operations Management (MOM): Solutions that enhance manufacturing efficiency and flexibility, c) Digital Twin Technology: Creating digital replicas of physical assets to optimize performance and maintenance, d) Smart Manufacturing: Integrating digital tools to improve production processes and supply chain management

ABOUT AMD VERSAL PREMIUM VP1902 ADAPTIVE SoC

The Versal Premium VP1902 adaptive SoC is the first emulation-class device to feature a scalar processing subsystem on-chip, which enables a wide range of control and stimulus generation use modes for SW/HW firmware development and system bring-up. It provides an extensive debug and IP ecosystem for traditional, desktop, and IP prototyping, and enables scalability with extremely high capacity and connectivity, enhancing rout ability and low latency, and speeding up design iteration. For more information, please visit https://www.amd.com/en/products/adaptive-socs-and-fpgas/versal/premium-series/vp1902.html

ABOUT AMD

For more than 50 years, AMD has driven innovation in high-performance computing, graphics, and visualization technologies. Billions of people, leading Fortune 500 businesses, and cutting-edge scientific research institutions around the world rely on AMD technology daily to improve how they live, work, and play. AMD employees are focused on building leadership, high-performance, and adaptive products that push the boundaries of what is possible. For more information about how AMD is enabling today and inspiring tomorrow, visit the AMD (NASDAQ: AMD) website, blog, LinkedIn, and Twitter pages.

Performance and cost-savings claims are provided by Siemens and have not been independently verified by AMD. Performance and cost benefits are impacted by a variety of variables. Results herein are specific to Siemens and may not be typical GD-181.

1.- VER-001: Based on AMD internal analysis in May 2023, comparing the number of system logic cells of the Versal Premium VP1902 device versus the Virtex Ultrascale+ VU19P device
2.- VER-003: Based on AMD Labs testing using the Versal Premium VP1902 VSVA6865 package to simulate the XPIO data rate performance of an AMD Versal Premium VP1902 device versus the published data rate of an AMD Virtex Ultrascale+ VU19P FPGA. Actual results will vary.
3.- Product selection guide can be found here: Versal™ Premium Series Product Selection Guide (XMP463) • Viewer • AMD Technical Information Portal