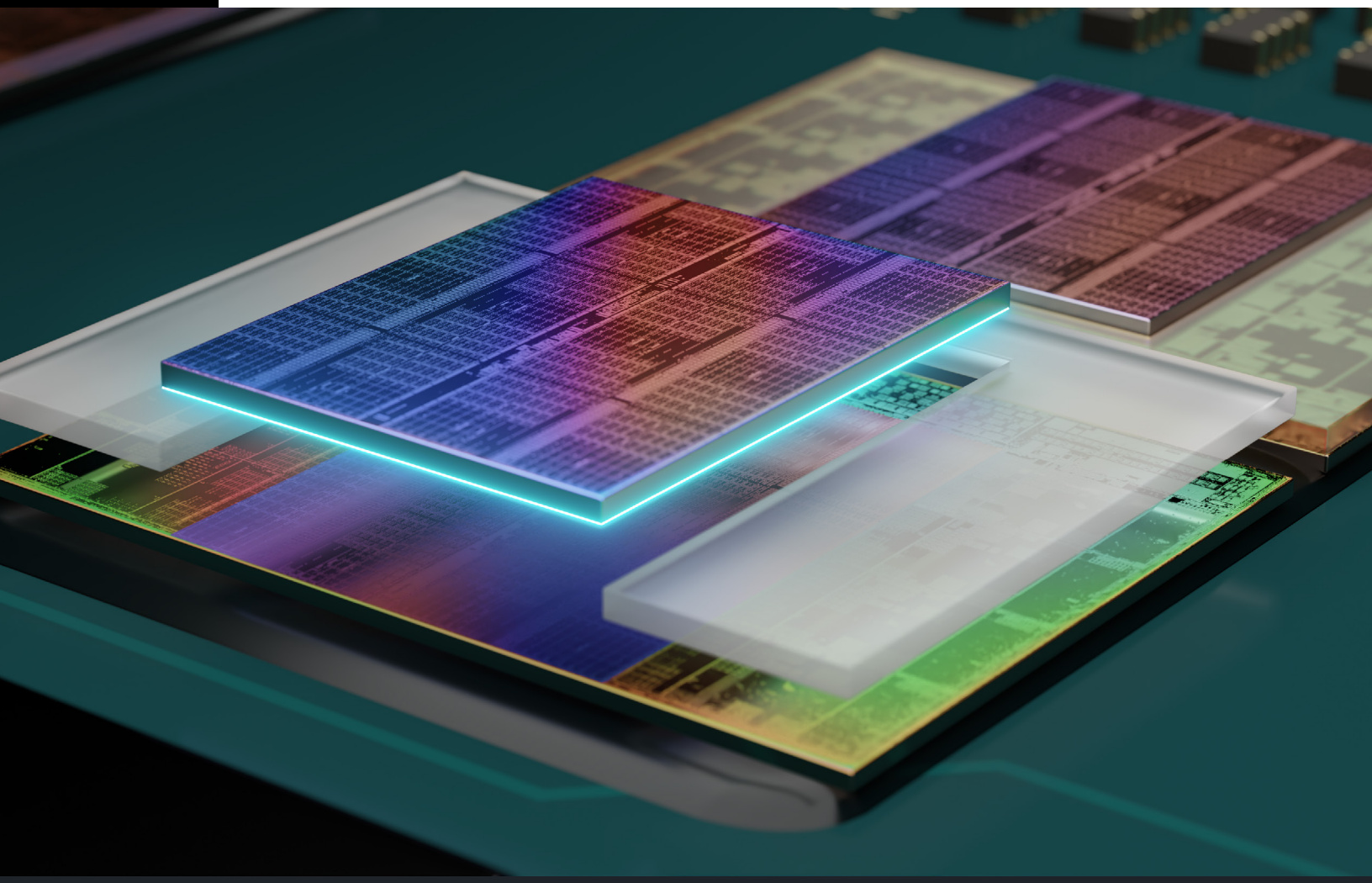

NOTHING STACKS UP TO EPYC™

ELEVATING DATA CENTER COMPUTING
WITH AMD 3D V-CACHE

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High-performance computing (HPC) applications are increasingly powering our lives and work. This means that the demand for even more processing capability is on the rise. Traditional approaches to meet this imperative include increasing die sizes and/or shrinking logic circuits. These approaches, however, have their limits. Today, Moore's Law, which dictates that the number of transistors in a dense integrated circuit will double every two years, is slowing down just as the demand for more powerful processers is surging. The future of computing therefore relies on advanced packaging innovations that will enable the continued scaling of processor performance to meet the intense computing demands of HPC applications. AMD is answering the challenge with its new 3D chiplet technology.

MULTI-CHIP MODULE ARCHITECTURE

Chiplets replace monolithic SoCs with multiple simpler building blocks that are typically less expensive to manufacture. These simpler building blocks can then be mixed and matched to suit a variety of needs. The added complexity of assembling multiple blocks into a single system is more than offset by the corresponding design flexibility.

The 2nd Gen AMD EPYC™ processors released in 2019 introduced the world's first multi-chip module (MCM) architecture. This MCM architecture boosted performance by including different processor nodes for the CPU and I/O in the same package. The 3rd Gen AMD EPYC™ processors released in early 2021 leverage this same architecture to drive even higher performance.

3RD GEN AMD EPYC™ WITH AMD 3D V-CACHE

3X MORE
L3 cache, from 256MB to 768MB[1]

UP TO 66% MORE
simulation jobs per day[2]

200X MORE
interconnect density than 2D chiplets[3]

15X MORE
density than traditional 3D stacking solutions[3]

INTRODUCING AMD 3D V-CACHE

Traditional "2D" MCM designs add performance and flexibility; however there comes a point at which adding chiplets creates a larger SoC with more distance between components, which increases latency. The need to deliver world-record data center CPU performance requires AMD to look up—literally.

This is where 3D V-Cache comes in. It's the first x86 CPU technology with true 3D die stacking. AMD and TSMC have been collaborating to leverage TSMC 3D Fabric technology to develop the highly differentiated 3rd Gen AMD EPYC™ processors with AMD 3D V-Cache, formerly code named "Milan-X."

Developed for breakthrough performance on targeted critical product design and technical computing workloads, these processors will be game changers for electronic design automation (EDA), computational fluid dynamics (CFD), and finite element analysis (FEA). In these processors, stacking chiplets deliver TRIPLE the L3 cache of other 3rd Gen AMD EPYC™ processors, from 256MB to 768MB.[1] It also locates logic units and corresponding memory on top of each other instead of spreading them out, yielding significantly lower latency. Tripling the L3 cache enables these processors to deliver up to 66% more EDA RTL simulation jobs per day for technical computing applications compared to 3rd Gen AMD EPYC™ processors with the same number of cores but no 3D V-Cache.[2]

3rd Gen AMD EPYC™ processors with AMD 3D V-Cache achieve true 3D chiplet stacking using the industry's first copper-to-copper hybrid bonds plus a through-silicon vias (TSVs) approach that provides up to 200 times the interconnect density versus 2D chiplets and approximately 15 times the density versus traditional 3D stacking solutions using solder bumps.[3] The unique bump-less design also consumes less energy than existing 3D approaches.[4]

With components placed in a 3D stack for minimum latency, increased bandwidth thanks to the tripled L3 cache, and the resultant thermal efficiencies, 3rd Gen AMD EPYC™ processors with AMD 3D V-Cache deliver breakthrough performance, especially for product and engineering design, one of the most compute intensive workloads. AMD 3D V-Cache will allow teams to accelerate simulation runs and design iterations, as well as increase design fidelity, all of which frees up design teams to work faster and deliver better quality products to their customers.

The innovative design of 3rd Gen AMD EPYC processors with AMD 3D V-Cache continues AMD's legacy of innovation and market leadership by elevating data center CPU performance to handle even the most demanding technical computing workloads.

LEARN MORE ABOUT AMD EPYC™ PROCESSORS

[1] EPYC™ 7003 Processors with 3D V-Cache have 768MB of L3 Cache, while EPYC 7003 processors without 3D V-Cache have 256MB. MLNX-12
[2] EDA RTL Simulation comparison based on AMD internal testing completed on 9/20/2021 measuring the average time to complete a test case simulation. comparing: 1x 16C EPYC™ 7373X with AMD 3D V-Cache Technology versus 1x 16C AMD EPYC™ 73F3 on the same AMD "Daytona" reference platform. Results may vary based on factors including silicon version, hardware and software configuration and driver versions. MLNX-001A
[3] Lisa Su Keynote, Computex 2021. https://www.amd.com/en/press-releases/2021-05-31-amd-showcases-industry-leading-innovation-across-the-high-performance
[4] Lisa Su Keynote, Computex 2021. https://www.amd.com/en/press-releases/2021-05-31-amd-showcases-industry-leading-innovation-across-the-high-performance