



Family 15h Models 00h-0Fh AMD Opteron™ Processor Product Data Sheet

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Revision History

Date	Revision	Description
October 2012	3.01	Second Public Release. <ul style="list-style-type: none">• Updated APML features.• Added AM3r2 package information.
November 2011	3.00	Initial Public Release.

1 Features

The following is a list of features and capabilities of the Family 15h Models 00h-0Fh AMD Opteron™ processor.

- **Compatible with Existing 32-Bit and 64-Bit Code Base**
 - Including support for SSE, SSE2, SSE3, SSE4a, SSE4.1, SSE4.2, SSSE3, ABM, AVX, AES, XSAVE/XRSTOR, PCLMULQDQ, FMA4, XOP, MMX™, and legacy x86 instructions
 - Runs existing operating systems and drivers
 - Local APIC on the chip
 - Light Weight Process (LWP) support
- **AMD64 Technology**
 - AMD64 technology instruction-set extensions
 - 64-bit integer registers, 48-bit addresses
 - Sixteen 64-bit integer registers
 - Sixteen 128-bit SSE/SSE2/SSE3/SSE4a registers
- **Family 15h Architecture**
 - FPU shared between the two cores of a Compute Unit (CU)
 - Support for up to 8 cores per node
- **Machine-Check Architecture**
 - Includes hardware scrubbing of L3 ECC-protected arrays
- **Cache Structures**
 - **16-Kbyte 4-Way Associative, Write-through ECC-Protected L1 Data Cache per Core**
 - Two 64-bit operations per cycle, 3-cycle latency
 - **64-Kbyte 2-Way Associative Parity-Protected L1 Instruction Cache Shared between Both Cores of a CU**
 - With advanced branch prediction
 - **2048-Kbyte 16-Way Associative ECC-Protected L2 Cache Shared between Both Cores of a CU**
 - Exclusive cache architecture storage in addition to L1 caches
 - **8192-Kbyte (8-Mbyte) Maximum 64-way Associative Cache Shared between All Cores on a Node**
 - Shared cache architecture storage in addition to exclusive L1 and L2 caches
- **Flexible Floating-Point Unit**
 - 256-bit shared or two dedicated 128-bit floating-point units (FPU)
 - Shared between the two cores of a CU
- **Management and Virtualization Features**
 - Advanced Platform Management Link (APML)
 - SMBus v2.0-compatible interface
 - Remote-Management Interface (SB-RMI)
 - SB-RMI is not supported in AM3r2 packages.
 - AMD Virtualization™ (AMD-V™) technology
 - SVM pause count capability
 - SVM disable and lock
 - Rapid virtualization indexing (nested paging)
 - Improved world-switch speed

• Power Management

- Multiple low-power states
- Advanced Power Management
- AMD Turbo CORE technology with per core power gating
- CPU PowerCap
- System Management Mode (SMM)
- Hardware Thermal Control (HTC)
- ACPI-compliant, including support for processor performance states
- Supported power states: C0, C1, C1E, C6, CC6, S0, S3, S4, and S5
- Effective frequency interface

• Electrical Interfaces

- DDR3 SDRAM: Compliant with JEDEC DDR3 1.5-V, LV-DDR3 1.35V and 1.25V SDRAM specifications
- Refer to the *AMD Family 15h Models 00-0Fh Processor Electrical Data Sheet*, order# 47079, for electrical details of AMD Family 15h processors.

• HyperTransport™ Technology

- HyperTransport™ 3 technology supported
- Link Speed PowerCap
- Link Width PowerCap
- Maximum four (4) links on G34 package, three (3) links on C32 package, and one (1) link on AM3r2 package, 16-bits in each direction, supporting up to 2000 MT/s (4.0 GB/s) in each direction in HyperTransport Generation 1.0 mode and up to 6400 MT/s (12.8 GB/s) in each direction in HyperTransport Generation 3.0 mode

• Integrated Memory Controller

- AMD Memory Controller PowerCap
- Low-latency, high-bandwidth
- DRAM Prefetcher:
 - Adaptive prefetching support
 - 32-entry DRAM prefetch table
 - Differentiate between core prefetch requests and core demand requests
- ECC checking with double-bit detect and single-bit correct
- 144-bit DDR3 SDRAM controller operating at frequencies up to 1866 MT/s (933 MHz)
- Package AM3r2
 - Supports up to four (4) unbuffered DIMMs
- Package C32
 - Supports up to four (4) unbuffered DIMMs
 - Supports up to six (6) registered DIMMs
 - Supports up to six (6) load-reduced DIMMs
- Package G34
 - Supports up to eight (8) unbuffered DIMMs
 - Supports up to twelve (12) registered DIMMs
 - Supports up to twelve (12) load-reduced DIMMs

• Available Packages

- Compliant with RoHS (EU Directive 2002/95/EC) with lead used only in small amounts in specifically exempted applications
- AM3r2 package
 - Refer to the *AM3r2 Processor Functional Data Sheet*, order# 47707, for functional and mechanical details of the AM3r2 package processor.
 - 940-pin lidded micro PGA package
 - 1.27-mm pin pitch
 - 31-row x 31-col pin array
 - C4 die attach
- C32 package
 - Refer to the *Socket C32 Processor Functional Data Sheet*, order# 47390, for functional and mechanical details of the socket C32 package processor.
 - 1207-land lidded LGA package
 - 1.10-mm land pitch
 - 35-row x 35-col land array
 - C4 die attach
- G34r1 package
 - Refer to the *Socket G34 Processor Functional Data Sheet*, order# 45937, for functional and mechanical details of the socket G34 package processor.
 - 1944-land lidded LGA package
 - 1.00-mm land pitch
 - 57-row x 40-col land array
 - C4 die attach

2 Compatible Socket Infrastructures

Refer to the AMD *Infrastructure Roadmap*, order# 41842, for information on platform-feature implications of package and socket-infrastructure combinations. Family 15h Models 00h-0Fh AMD Opteron™ processors support the following socket infrastructures:

- **AM3r2 Socket Infrastructure**
 - Compatible with AM3 and AM3r2 package processors
 - Refer to the *AM3r2 Processor Functional Data Sheet*, order# 47707, for functional and mechanical details of the AM3r2 socket infrastructure.
- **Socket C32 Socket Infrastructure**
 - Compatible with socket C32 package processors
 - Refer to the *Socket C32 Processor Functional Data Sheet*, order# 47390, for functional and mechanical details of the socket C32 package.
- **Socket G34 Socket Infrastructure**
 - Compatible with socket G34 package processors
 - Refer to the *Socket G34 Processor Functional Data Sheet*, order# 45937, for functional and mechanical details of the socket G34 package.